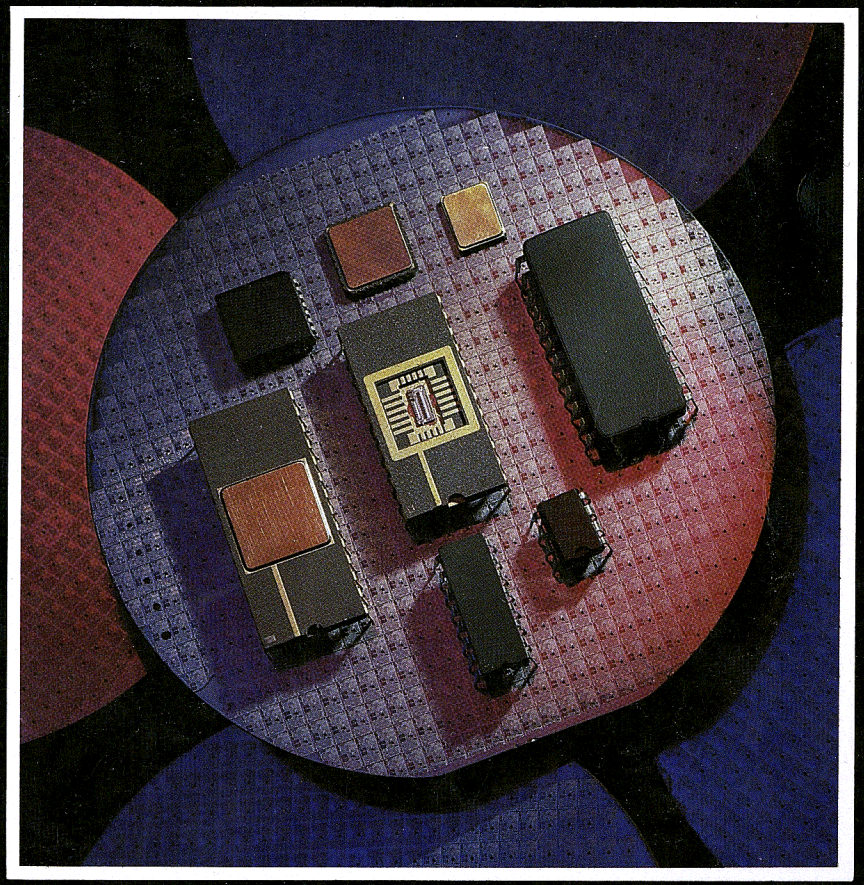
ANALOG
PRODUCT DATA BOOK
INDUSTRIAL/COMMERCIAL



HARRIS

Volume 6
$5.00

Harris Semiconductor
Sector Capabilities

Harris Semiconductor, one of the top ten U.S. merchant semiconductor suppliers, is a sector of Harris Corporation — a producer of advanced information processing, communication and microelectronic products for the worldwide information technology market.

Harris Semiconductor is organized to address the standard products, custom products, and gallium arsenide semiconductor markets.

SEMICONDUCTOR PRODUCTS DIVISION:

Harris Semiconductor offers a wide selection of standard analog and digital circuits through its Semiconductor Products Division including those designed to operate in very severe environments.

Analog Products

Harris is a major force in analog integrated circuitry, offering a broad line of products including: analog-to-digital converters, digital-to-analog converters, sample-and-hold circuits, multiplexers, switches, operational amplifiers, telecommunications, speech processing products and active filters (See complete analog product listing, page 1-1.)

Digital Products

Harris is a pioneer in developing and producing digital CMOS products including: CMOS, RAMs, CMOS PROMs, CMOS microprocessors, CMOS peripherals, CMOS data communications products, and a full line of 80C286 and 80C86/88 microprocessors and peripherals. Semicustom solutions are accomplished using a combination of fully characterized cells, macros, complex megacells and compilable functions. (See complete digital product listing, page 12-2.)

CUSTOM INTEGRATED CIRCUITS DIVISION (CICD)

CICD is dedicated to the development and production of custom/semi-custom and specialized integrated circuits for use in such areas as tactical/strategic radiation environments and secure communications. CICD employs high performance CMOS and bipolar technologies to meet the needs of high-end major military and hi-reliability programs.

CICD is oriented to engineering and manufacturing to specific customer requirements. The division also has its own dedicated manufacturing operation and engineering, product assurance, and program manager representation to insure close customer interaction and tight control of the design and quality aspects of individual programs. (See complete CICD product listing, page 12-3.)

MICROWAVE SEMICONDUCTOR OPERATIONS

Harris Microwave Semiconductor Operations develops and manufactures gallium arsenide field effect transistors (GaAs FETs), digital integrated circuits and monolithic microwave integrated circuits. Custom design and fabrication services are available whereby customers can design or specify specialized digital, MMIC or FET devices for manufacture at HMS. (See complete Microwave product listing, page 12-5.)

Harris Linear, Data Acquisition and Telecom Products

Harris Semiconductor's spectrum of analog products meet many specialized requirements ranging from precision to low power to high speed performance. Capitalizing on advanced linear processing technologies developed over the past 19 years, Harris Semiconductor offers analog products of high quality and unmatched performance.

This data book describes Harris Semiconductor's industrial line of Linear, Data Acquisition, and Telecommunication products. In addition, it includes a complete set of data sheets for product specifications; a section of application notes with design details for specific applications of Harris products; and a description of the Harris quality and high reliability program.

If you need more information on these and other Harris products, please contact the nearest Harris sales office listed in the back of this data book, or return the reply card attached inside back cover.

ANALOG

1988 Data Book

ANALOG

General Information

1

ALPHA NUMERIC PRODUCT INDEX

ALPHA NUMERIC PRODUCT INDEX (Continued) **PAGE**

Analog Product Listing

Analog Product Listing (Continued)

Analog Product Listing (Continued)

Analog Product Listing (Continued)

Switches (Continued)

Sample and Hold Amplifiers

Telecommunication Circuits

Ordering Information

Harris products are designated by a "Harris Product Code." The codes always begin with the letter "H", and the numbers which identify specific devices are separated by hyphens. An example of a product code is shown below. When ordering, please refer to products by their full code identification.

HARRIS PRODUCT CODE EXAMPLE

H I 7 — 5147 — 5

PREFIX:
H (HARRIS)

FAMILY:
A : Analog
C : Communications
D : Digital
F : Filters
I : Interface
M : Memory
V : Analog High Voltage

PACKAGE:
1 : Dual-In-Line Ceramic
2 : Metal Can
3 : Dual-In-Line Plastic
4 : Ceramic Leadless Chip Carriers (LCC)
4P : Plastic Leaded Chip Carriers (PLCC)
7 : Mini-DIP, Ceramic
0 : Chip Form

PART NUMBER

TEMPERATURE:
2 : -55°C to +125°C
4 : -25°C to +85°C
5 : 0°C to +75°C
6 : 100% +25°C Probe (Dice Only)
7 : Dash-7 High Reliability Commercial Product 0°C to +75°C, Includes 96 hour Burn-In
8 : Dash-8 Program, Hi-Rel Processing with Burn-In, -55°C to +125°C
/883 : Full Compliance to MIL-STD-883

Special High Temperature Testing Available on Certain Product Types. Consult Factory for Availability.

COMMERCIAL AND INDUSTRIAL PRODUCTS

Harris Semiconductor offers a variety of product grades to satisfy your system requirements. These grades are differentiated in four areas:

1) Operating Temperature Range

2) Electrical Performance

3) Package Type

4) Additional Screening Tests

Parts are marked with appropriate prefix and suffix designations, as illustrated in the Product Code Example. The information contained in this data book is intended to describe the expected product performance under the specified operating conditions for each temperature and performance grade.

Device testing sufficient to assure conformance is performed to provide the highest quality in the most cost-effective manner. These products are available worldwide from authorized distributors.

SPECIAL ORDERS

For those customers wishing additional screening (burn-in, etc.), Harris offers the DASH 7 screening program (described in Section 9). If additional electrical parameter guarantees for reliability screening are absolutely required, a Request For Quotation and Source Control Drawing should be submitted through the local Harris Sales Office or Sales Representative. Harris reserves the right to decline to quote on, or to request modification to, special screening requirements.

Harris application engineers may be consulted for information concerning the suitability of a product for a given application.

MILITARY PRODUCTS

Harris offers a full line of products that are processed in full conformance to the provisions of military standards, including MIL-STD-883C for Class B parts. The requirements for these products are controlled in one of two ways:

1. Government standards (such as JAN Slash Sheets, Standard Military Drawings (SMDs), or BS9000;
2. Harris Standards.

The Harris Standard Military Products Program is based on our experience in the JAN program. JAN certification is maintained on our production and Product Assurance operations and forms the basis of our MIL-STD-883 conformance program. These areas are regularly audited by Harris and by the U.S. government to assure compliance.

Selected products have been qualified to the MIL-M-38510 requirements and are listed on the QPL. There are also a number of Harris parts which are specified by SMDs. In addition, Harris offers many products as fully conformant to MIL-STD-883 via an internal standards program.

The information in this data book is intended to describe the expected part behavior under certain operating conditions. The product descriptions, particularly in the area of electrical performance, do not precisely reflect those of our JAN qualified, SMD, BS9000, or MIL-STD-883 compliant products and are not necessarily test requirements for Harris military standard compliant products.

The actual product test requirements for JAN and SMD parts are described in the appropriate MIL-M-38510 slash sheet or SMD. In addition, Harris issues product data sheets for MIL-STD-883 compliant parts which describe actual test requirements. These compliant products are identified by a "/883" suffix on the part number (e.g., HX1-XXXX/883). Please contact the factory or your local Harris Sales Office or Representative for details.

IC Handling Procedures

Harris Analog IC processes are designed to produce the most rugged products on the market. However, no semiconductor is immune from damage resulting from the sudden application of many thousands of volts of static electricity. While the phenomenon of catastrophic failure of devices containing MOS transistors or capacitors is well known, even bipolar circuits can be damaged by static discharge, with altered electrical properties and diminished reliability. None of the common IC internal protection networks operate quickly enough to positively prevent damage.

It is suggested that all semiconductors be handled, tested, and installed using standard "MOS handling techniques" of proper grounding of personnel and equipment. Parts and subassemblies should not be in contact with untreated plastic bags or wrapping material. High impedance IC inputs wired to a P.C. connector should have a path to ground on the card.

HANDLING RULES

Since the introduction of integrated circuits with MOS structures and high quality junctions, a safe and effective means of handling these devices has been of primary importance. One method employed to protect gate oxide structures is to incorporate input protection diodes directly on the monolithic chip. However, there is no completely foolproof system of chip input protection in existence in the industry. In addition, most compensation networks in linear circuits are located at high impedance nodes, where protection networks would disturb normal circuit operation. If static discharge occurs at sufficient magnitude (2kV or more), some damage or degradation will usually occur. It has been found that handling equipment and personnel can generate static potentials in excess of 10kV in a low humidity environment. Thus it becomes necessary for additional measures to be implemented to eliminate or reduce static charge. It is evident, therefore, that proper handling procedures or rules should be adopted.

Elimination or reduction of static charge can be accomplished as follows:

- Use conductive work stations. Conductive plastic* mats on work benches and floor, connected to ground through a 1MΩ resistor, help eliminate static build-up and discharge. Do not use metallic surfaces.
- Ground all handling equipment.
- Ground all handling personnel with a conductive bracelet through 1MΩ to ground (the 1MΩ resistor will prevent electroshock injury to personnel). Transient product personnel should wear grounding heel straps.
- Smocks, clothing, and especially shoes of certain insulating materials (notably nylon) should not be worn in areas where devices are handled. These materials, highly dielectric in nature, will hold, or aid in the generation of a static charge. Where they cannot be eliminated, natural materials such as cotton should be used to minimize charge generation capacity. Conductive smocks are also available as an alternative.
- Control relative humidity to as high a level as practical. 50% is generally considered sufficient. (Operations should cease if R.H. falls below 25%).
- Ionized air blowers reduce charge build-up in areas where grounding is not possible or practical.
- Devices should be in conductive carriers during all phases of transport. Leads may be shorted by tubular metallic carriers, conductive foam, or foil.
- In automated handling equipment, the belts, chutes, or other surfaces should be of conducting non-metal material. If this is not possible, ionized air blowers or ionizing bars may be a good alternative.

* Supplier 3M Company
"Static Control Table Mat 8210/8210R"
"Static Control Floor Mat 8200/8200R"

Harris Analog IC Technologies

JUNCTION ISOLATION (JI)

Although it is the most common integrated circuit process, Harris offers only a limited number of products, such as the HA-4741, using JI technology. Latchup and other problems have made the Harris Dielectric Isolation (DI) process, described below, more reliable.

Bipolar ICs using the JI process generally begin with a p-type wafer into which a buried layer pattern can be first diffused. Next the n-type epitaxial layer is grown, and p-type isolation walls are diffused around each area to be electrically isolated from the other circuitry. These isolation walls must be diffused deeply into the wafer in order to contact the original p-substrate. In operation, the p-substrate and isolation walls are connected to the most negative circuit potential, so that each active area is surrounded on the sides and bottom by a reverse biased junction through which negligible current flows (Figure 1).

To complete the IC, base and emitter diffusions are performed, the wafer is coated with aluminum, and the conductor pattern is etched.

DIELECTRIC ISOLATION (DI)

Harris has developed a different process which has many advantages over JI for fabricating high performance analog ICs. With Dielectric Isolation (DI), each active area is surrounded on the sides and bottom by an insulating layer of silicon dioxide and embedded in polycrystalline silicon for mechanical strength.

For bipolar ICs, the process begins with a wafer of n-type silicon. The side of the wafer which will eventually be the bottom is deeply etched to form the sidewall pattern. Silicon dioxide and polycrystalline silicon are grown to fill the etched "moats." The opposite side of the wafer is then polished until the insulating sidewalls appear at the wafer surface (Figure 2). Conventional diffusion and metallization processes follow to complete the IC.

ICs fabricated under the DI process are superior in the following ways.

1. Almost all op amp designs require at least one PNP transistor in the signal path. Typical JI op amps must use a lateral PNP with its inherent very low frequency response, thus limiting typical compensated bandwidth to 1MHz.

   The DI process makes it practical to build a vertical PNP, allowing compensated op amp bandwidths of 12MHz, or higher (Figure 3). Also, transistor collector to substrate capacitance is 2/3 less using DI, further enhancing high frequency performance.

2. Other devices, such as optimally specified MOS or JFET transistors may be fabricated on the same chip. Isolated diffused and thin film resistors are also practical.

3. The isolation removes the possibility of parasitic SCRs which might create latchup under certain sequences of power and signal application.

4. Leakage currents to the substrate under high temperature conditions are greatly reduced. Although the circuits described in this data book were not specifically designed for operating temperatures greater than +125°C, many have shown superior performance. For ICs requiring the ultimate in radiation resistance, Harris Semiconductor Custom Integrated Circuits Division should be consulted.

DIELECTRIC ISOLATED CMOS

JI processed CMOS analog ICs, which are generally used in conjunction with several power supplies, are particularly prone to parasitic SCR latchup failures as well as failures due to input voltage spikes. The DI CMOS process (described in detail in Harris Application Note 521) has proven to be the best solution.

Since analog multiplexers are often used at the input of a data acquisition system, particular attention must be paid to the possibility of damaging input overvoltage conditions. Harris has provided an effective answer in the HI-546 through HI-549 multiplexers with built-in overvoltage protection.

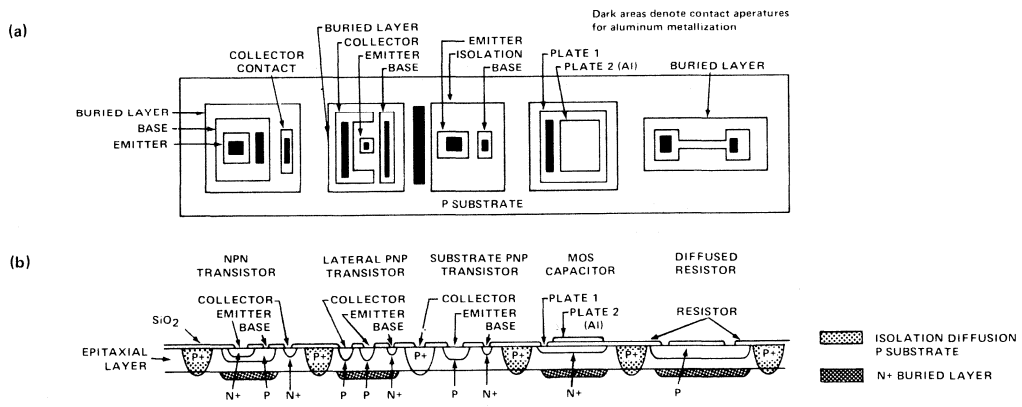


FIGURE 1. STRUCTURES OF VARIOUS COMPONENTS FORMED IN THE JUNCTION-ISOLATION PROCESS. (a) TOPOLOGICAL VIEW. (b) CROSS-SECTIONAL VIEW.

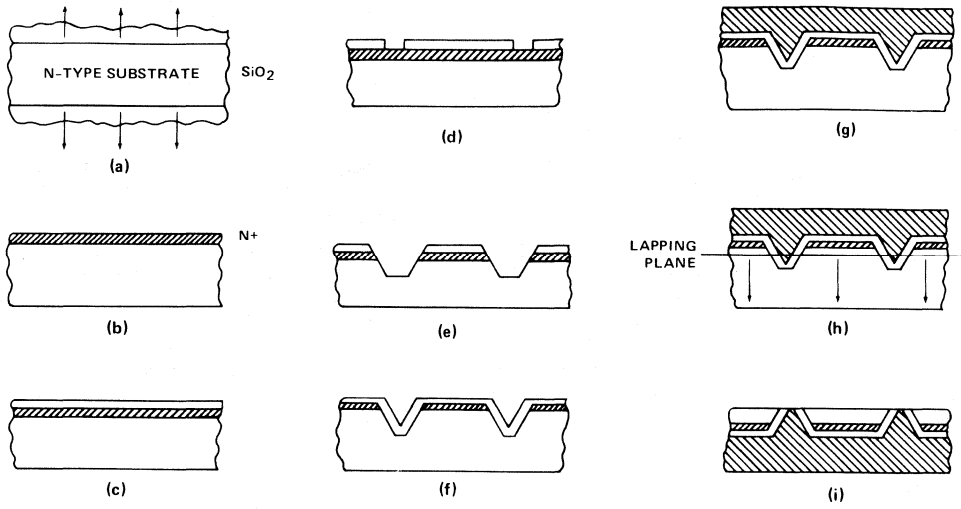


FIGURE 2. PROCESS STEPS FOR DIELECTRIC ISOLATION. (a) SURFACE PREPARATION, (b) N-BURIED LAYER DIFFUSION, (c) MASKING OXIDE, (d) ISOLATION PATTERN, (e) SILICON ETCH, (f) DIELECTRIC OXIDE, (g) POLYCRYSTALLINE DEPOSITION, (h) BACKLAP AND POLISH, (i) FINISHED SLICE.

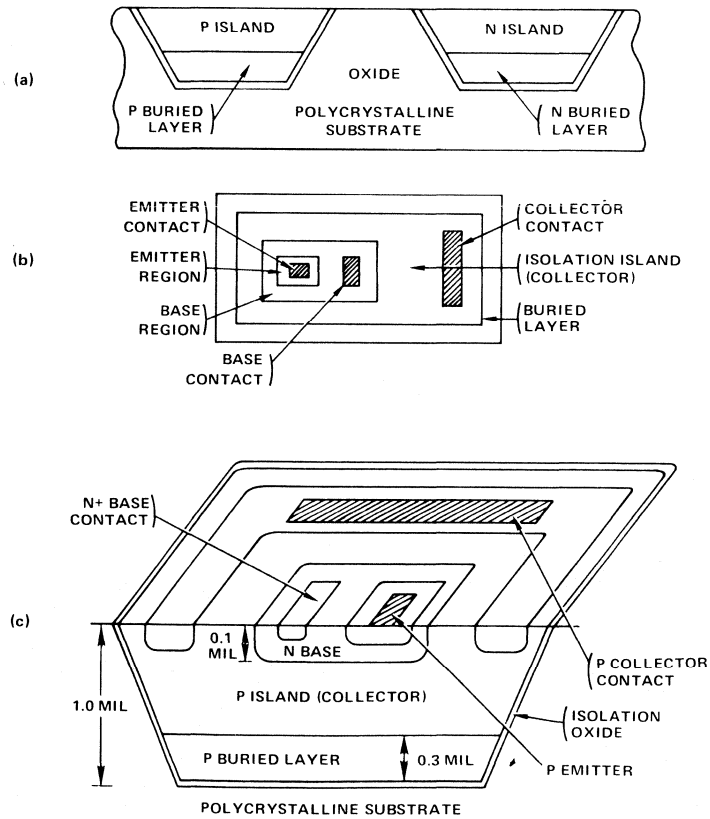


FIGURE 3. THE HIGH-FREQUENCY PROCESS. (a) CROSS-SECTIONAL VIEW OF P AND N ISLANDS FOR PNP AND NPN TRANSISTORS. (b) TOPOLOGICAL VIEW SHOWING RELATIVE PLACEMENT OF TRANSISTOR REGIONS. (c) CROSS-SECTIONAL VIEW OF HIGH- FREQUENCY PNP DEVICE FORMATION IN THE D.I. PROCESS.

Competitive Cross Reference Chart

Manufacturer	Part Number	Harris Pin-for-Pin Replacement	Harris Closest Replacement	Harris Advantages
AMD	AM118		HA-2510	Unity gain stable
	AM1408		HI-5618-5	Faster, application resistors
	AM1508		HI-5618-2	Faster, application resistors
	AM318		HA-2515	Unity gain stable
	AM6012		HI-562A	Faster, application resistors, int. linearity
			HI-5660	Int. linearity, application resistors
	AM6420		HA-5320	
			HA-5330	
	LF198		HA-2420	Improved performance
	LF398		HA-2425	Improved performance
	SSS1408		HI-5618-5	Faster, application resistors
	SSS1508		HI-5618-2	Faster, application resistors
ANALOG DEV	52		HA-5180	Monolithic
	AD1408		HI-5618-5	Faster, application resistors
	AD1508		HI-5618-2	Faster, application resistors
	AD380,AD382		HA-2542	Monolithic
	AD381		HA-2541	Monolithic
	AD389		HA-5320	Faster, monolithic
	AD507	HA-2620		Identical
	AD509	HA-2520	HA-2529	Identical
	AD515		HA-5180	Monolithic
	AD518	HA-2510		
	AD542L		HA-5170	Better AC
	AD545		HA-5180	Monolithic
	AD547J		HA-5170	Better AC
	AD562		HI-562A	Faster
			HI-5660	Faster
	AD563		HI-565A	Faster
	AD565	HI-565A		Faster
	AD565A	HI-565A		
	AD566		HI-5660	
			HI-562	
	AD566A		HI-5660	
			HI-562A	
	AD574A	HI-574A,HI-674A		Digital timing, 674A is 2.3 times faster
	AD582		HA-2425	Acquisition time
	AD583K	HA-2425-5		Identical
	AD585		HA-5320/HA-5330	Faster, better accuracy
	AD667		HI-5811	
	AD7501		HI-508	DI process
	AD7502	HI-1828A		DI process
	AD7503	HI-1818A		DI process
	AD7506	HI-506		DI process
	AD7507	HI-507		DI process
	AD7511		HI-201	
	AD7512		HI-5043	
	ADADC80		HI-574A	Power, smaller pkg.
			HI-674A	Faster, power, smaller pkg.
	ADADC84/85		HI-674A	Power, smaller pkg.
	ADDAC 08		HI-5618	Faster, application resistors
	DAC 80	HI-5680,HI-5690		5690 is 2.67 times faster
	DAC 85	HI-5685,HI-5695		5695 is 2.67 times faster
	DAC 87	HI-5687,HI-5697		5697 is 2.67 times faster
	ADG200		HI-200	
	ADLH0032		HA-5190,HA-2542	Monolithic
	H0S050		HA-2542	Monolithic
	H0S100		HA-5033	Monolithic
ANALOGIC	MN4708		HI-508	
			HI-1818A	
	MP1812A		HI-5680V	Faster, monolithic, power, smaller pkg.
	MP250M		HA-2420/25	Faster, monolithic, smaller
	MP260		HA-2420/25	Monolithic, smaller pkg.
	MP261		HA-2420	Monolithic, smaller pkg.
	MP270/271		HA-5320	Monolithic, smaller pkg.
BECKMAN	7556		HI-574A	Faster, smaller pkg.
	7580	HI-5690	HI-5680	Faster, monolithic
BURR-BROWN	3500		HA-2600	Better AC
	3503	HA-2505		Identical
	3506	HA-2605		Identical
	3507	HA-2525	HA-2529	Identical
	3508	HA-2625		Identical

Competitive Cross Reference Chart (Continued)

Manufacturer	Part Number	Harris Pin-for-Pin Replacement	Harris Closest Replacement	Harris Advantages
BURR-BROWN (cont.)	3521		HA-5170	Better AC
	3523		HA-5180	Better AC
	3527		HA-5180	Better AC and DC
	3528		HA-5180	Better AC
	3550		HA-2541	Monolithic
	3553		HA-5033	Monolithic
	'3554		HA-2542	Monolithic
	ADC80		HI-574A	Smaller pkg., power
			HI-674A	Faster, smaller pkg., power
	ADC84/85		HI-674A	Smaller pkg., power
	DAC70		HI-DAC16	Faster, monolithic
	DAC700/701		HI-DAC16	
	DAC702/703		HI-DAC16	
	DAC71/72		HI-DAC16	Monolithic, "I" output
	DAC80	HI-5680,HI-5690		Faster, monolithic, power
	DAC800	HI-5680,HI-5690		5690 is 3.33 times faster, lower power
	DAC811	HI-5811		
	DAC85	HI-5685,HI-5695		Faster, monolithic, power
	DAC850	HI-5685,HI-5695		5695 is 3.33 times faster, lower power
	DAC851	HI-5687,HI-5697		5697 is 3.33 times faster, lower power
	DAC87	HI-5687,HI-5697		Faster, monolithic, power
	MPC16S	HI-546-5		Identical
	MPC4D	HI-549-5		Identical
	MPC800KG	HI-516-5		Identical
	MPC801KG	HI-518-5		Identical
	MPC801SG	HI-518-2		Identical
	MPC8D	HI-547-5		Identical
	MPC8S	HI-548-5		Identical
	OPA103		HA-5180	Better AC
	OPA104		HA-5180	
	OPA11		HA-2600	
	OPA21		HA-5141,HA-5151	
	OPA27		HA-5127	
	OPA37		HA-5137,HA-5147	
	OPA600		HA-2542	
	OPA633		HA-5033	
	SCH298AM		HA-2425	Improved performance
	SCH80/85		HA-2425	Faster, monolithic, power
	SHC85ET		HA-2420	Faster, monolithic, power
	SHM60		HA-5320	Monolithic, smaller pkg.
	ADC574A	HI-574A		Identical
	ADC674A	HI-674A		Identical
	SHC5320	HA-5320		Identical
DATA DEVICE CORP.	ADH051		HA-5330	Monolithic, smaller pkg., power
	ADH8585		HI-674A	Smaller pkg., power
	DDC5200		HI-574A	Faster
	DDC5210/11		HI-674A	
	DDC5212/16		HI-674A	
	DDCADC85		HI-674A	Smaller pkg., power
	DDCDAC85	HI-5680,HI-5690		Faster, smaller pkg., power
	DDCDAC85LD	HI-5685,HI-5695		Monolithic, power
	DDCDAC87	HI-5687,HI-5697		Monolithic, power, 5697 is 3.33 times faster
	DGL13		HA-5320	Monolithic, smaller pkg., power
	THC4460		HA-5320	Monolithic, smaller pkg.
DATEL	ADC52XX		HI-674A	Lower power
	ADC574A	HI-574A,HI-674A		Identical, 674 is 1.67 times faster
	ADC8412		HI-674A	Smaller pkg. power
	ADC85C12		HI-674A	Smaller pkg., power
	ADC8712		HI-674A	Smaller pkg., power
	ADCHX12B		HI-574A	Smaller pkg., power
			HI-674A	Faster, smaller pkg., power
	ADCL12B2		HI-574A	Smaller pkg.
			HI-674A	Faster, smaller pkg.
	ADCM12B2		HI-674A	Smaller pkg.
	ADCMA12B2A		HI-574A	Faster, smaller pkg.
	ADCMA12B2B		HI574A	Smaller pkg.
			HI-674A	Faster, smaller pkg.
	AM450	HA-2505		
	AM452	HA-2525	HA-2529	
	AM460	HA-2605		
	AM462	HA-2625		
	AM464	HA-2645		
	DAC08B		HI-5618	Faster, application resistors
	DAC562	HI-562A		Identical

Competitive Cross Reference Chart (Continued)

Manufacturer	Part Number	Harris Pin-for-Pin Replacement	Harris Closest Replacement	Harris Advantages
DATEL (cont.)	DAC71/72		HI-DAC16	Monolithic
	DAC85	HI-5685,HI-5695		Faster, monolithic, power
	DAC85C	HI-5680,HI-5690		Monolithic, power, 5690 is 2 times faster
	DAC87	HI-5687,HI-5697		Faster, monolithic, power
	DACHP16B		HI-DAC16	Monolithic
	DACHR16B		HI-DAC16	Monolithic, smaller pkg.
	DACHZ12B	HI-5690/95/97	HI-5680/85/87	Faster, monolithic
	DACIC10B		HI-5610	Faster, application resistors
	DACIC8B		HI-5618	Faster, application resistors
	MV1606	HI-506		Identical
	MV808	HI-1818A		Identical
	MVD409	HI-1828A		Identical
	MVD807	HI-507		Identical
	MX1606	HI-546		Identical
	MX1616	HI-516		Identical
	MX808	HI-548		Identical
	MX818	HI-518		Identical
	MXD409	HI-549		Identical
	MXD807	HI-547		Identical
	SHM1C-1	HA-2425		Identical
	SHM1C-1M	HA-2420		Identical
	SHM20	HA-5320		Identical
	SHM6M		HA-5320	Monolithic, smaller pkg.
			HA-5330	Faster, monolithic, smaller pkg.
	SHM9M		HA-2420	Faster, monolithic, smaller pkg.
	SHMLM-2		HA-2420	Faster
ELANTEC	EHA2500	HA-2500		
	EHA2502	HA-2502		
	EHA2505	HA-2505		
	EHA2510	HA-2510		
	EHA2512	HA-2512		
	EHA2515	HA-2515		
	EHA2520	HA-2520		
	EHA2522	HA-2522		
	EHA2525	HA-2525		
	EHA2600	HA-2600		
	EHA2602	HA-2602		
	EHA2605	HA-2605		
	EHA2620	HA-2620		
	EHA2622	HA-2622		
	EHA2625	HA-2625		
	ELH0002		HA-5002-2	Monolithic
	ELH0002C		HA-5002-5	Monolithic
	ELH0033		HA-5033-2	Monolithic
	ELH0033C		HA-5033-5	Monolithic
	ELH0041		HA-2542-2	Monolithic
	ELH0041C		HA-2542-5	Monolithic
EXAR	XR4212		HA-4741	
	XR3417			Lower power
	XR3418		HC-55536 or	Fewer external components
	XR3517		HC-55564	Military pkg.
	XR3518			
FAIRCHILD	μA0801/02		HI-5618	Faster, application resistors
	μA1458		HA-5102	Better AC, lower noise
	μA1558		HA-5102	Better AC, lower noise
	μA198		HA-2420	Improved performance
	μA398		HA-2425	Improved performance
	μA565	HI-565A		
	μA702		HA-2620	
	μA709		HA-2620	
	μA714		HA-5135	Better DC
	μA715		HA-2520,HA-2529	Better AC
	μA727		HA-5135	Better DC
	μA740		HA-5170	Better AC
	μA741		HA-2600	Better AC
FAIRCHILD	μA747		HA-5102	Lower noise
	μA748		HA-2600	Better AC
	μA776		HA-2720	Better AC, lower noise
HITACHI	HA17408		HI-5618	Faster, application resistors

Competitive Cross Reference Chart (Continued)

Manufacturer	Part Number	Harris Pin-for-Pin Replacement	Harris Closest Replacement	Harris Advantages
HYBRID SYSTEM	ADC550		HI-574A	Faster, smaller pkg., power
	ADC581		HI-574A	
			HI-674A	Faster
	DAC3281-16		HI-DAC16	Monolithic, smaller pkg.
	DAC335-12		HI-5687V	Faster, monolithic
	DAC346C-12		HI-5680V	Faster, monolithic
	DAC347LP-12		HI-5687V	Faster, monolithic
	DAC372		HI-5680	Monolithic
	DAC3721-8		HI-5618	Faster, monolithic
	DAC395-8		HI-5618	Monolithic, smaller pkg.
	HS346		HA-5320	Faster, monolithic
	HS5200		HI-674A	
	HS574	HI-574A,HI-674A		Digital timing, 674 is 2 times faster
	HS730		HA-5320	Monolithic, smaller pkg.
			HA-5330	Faster, monolithic, smaller pkg.
	HSDAC80	HI-5680,HI-5690		Faster, monolithic, power, 5690 is 5.56 times faster
	HSDAC87	HI-5687,HI-5697		Faster, monolithic, power
	MUX201	HI-1818A		Lower power, smaller pkg.
	SH725		HA-2420	Faster, monolithic, smaller pkg.
INTECH	1048BIN-P		HI-574A	Smaller pkg., power
			HI-674A	Faster, smaller pkg., power
	416 BIN		HI-DAC16	Smaller pkg.
	A3103		HI-674A	Smaller pkg., power
	A3155		HI-574A	Smaller pkg., power
			HI-674A	Faster, smaller pkg., power
	A880/880-2		HA-5320	Faster, monolithic, power
	A881		HA-5320	Monolithic, smaller pkg., power
	A882/884		HA-2420/25	Faster, monolithic, power
	ADC111		HI-574A	Smaller pkg., power
			HI-674A	Faster, smaller pkg., power
	ADC2812		HI-547A	Smaller pkg., power
			HI-674A	Faster, smaller pkg., power
	ASH240/250		HA-2420/25	Monolithic, smaller pkg., power
	ASH271		HA-5320	Monolithic, smaller pkg., power
	CYAAD12QM		HI-574A	Smaller pkg., power
			HI-674A	Faster, smaller pkg., power
INTEL	D2912	HC-5512		Lower power, lower noise
	D2912A	HC-5512		Lower power, lower noise
		HC-5512A/12D		Lower power, lower noise
	SBC 86/05	HB0-986C05		CMOS micro components. Lower
	NMOS			power 16K static RAM w/full mercury back-up
INTERSIL	DG200	HI-200		Dielectric Isolation
	DG201	HI-201		Dielectric Isolation
	ICL7541			Identical
	ICL7611		HA-5141	Lower noise
	ICL7615		HA-5141	Better AC, lower noise
	ICL7621		HA-5142	Better AC, lower noise
	ICL7642		HA-5144	Better AC, lower noise
	ICL8017		HA-2520,HA-2529	
	ICL8021		HA-5141	Better AC
	ICL8075			
	ICL8211			
	IH201	HI-201		More stable over temp.
	IH5040	HI-5040		More stable over temp.
	IH5041	HI-5041		More stable over temp.
	IH5042	HI-5042		More stable over temp.
	IH5043	HI-5043		More stable over temp.
	IH5044	HI-5044		More stable over temp.
	IH5045	HI-5045		More stable over temp.
	IH5046	HI-5046		More stable over temp.
	IH5047	HI-5047		More stable over temp.
	IH5048	HI-5048		More stable over temp.
	IH5049	HI-5049		More stable over temp.
	IH5050	HI-5050		More stable over temp.
	IH5051	HI-5051		More stable over temp.
	IH5108	HI-548		Signal range, same pinout
	IH5110/11		HA-2420/25	
	IH5112/13		HA-2420/25	
	IH5114/15		HA-2420/25	
	IH5200	HI-200		Constant Ron
	IH5201	HI-201		Constant Ron
	IH5208	HI-509A		Vin range, same pinout
	IH6108	HI-508		Ron, DI, same pinout

Competitive Cross Reference Chart (Continued)

Manufacturer	Part Number	Harris Pin-for-Pin Replacement	Harris Closest Replacement	Harris Advantages
INTERSIL (cont.)	IH6116	HI-506		Ron, DI, same pinout
	IH6208	HI-509		Ron, DI, same pinout
	IH6216	HI-507		Ron, DI, same pinout
	LM4250		HA-2720	Better AC, lower noise
INTRONICS	A-560		HA-2525,HA-2529	
	A-561		HA-2625	
MAXIM	MAX400M		HA-5127-2	
	MAX400C		HA-5127-5	
	MAX460M		HA-5033-2	Lower noise, DI
	MAX460C		HA-5033-5	Lower noise, DI
	BB3553		HA-5033	Monolithic, DI
	BB3554		HA-2542	Monolithic, DI
	LH0033		HA-5033	Monolithic
	OP07		HA-5130	Better AC - DI
	DG201A	HI-201		Dielectric Isolation
	DG211		HI-201	Full Temperature Range Specified
	DG300A	HI-300		Dielectric Isolation
	DG301A	HI-301		Dielectric Isolation
	DG302A	HI-302		Dielectric Isolation
	DG303A	HI-303		Dielectric Isolation
	DG304A	HI-304		Dielectric Isolation
	DG305A	HI-305		Dielectric Isolation
	DG306A	HI-306		Dielectric Isolation
	DG307A	HI-307		Dielectric Isolation
	DG381A	HI-381		Dielectric Isolation
	DG384A	HI-384		Dielectric Isolation
	DG387A	HI-387		Dielectric Isolation
	DG390	HI-390		Dielectric Isolation
	IH5040	HI-5040		Dielectric Isolation
	IH5041	HI-5041		Dielectric Isolation
	IH5042	HI-5042		Dielectric Isolation
	IH5043	HI-5043		Dielectric Isolation
	IH5044	HI-5044		Dielectric Isolation
	IH5045	HI-5045		Dielectric Isolation
	IH5046	HI-5046		Dielectric Isolation
	IH5047	HI-5047		Dielectric Isolation
	IH5048	HI-5048		Dielectric Isolation
	IH5049	HI-5049		Dielectric Isolation
	IH5050	HI-5050		Dielectric Isolation
	IH5051	HI-5051		Dielectric Isolation
	MAX358/359	HI-508A/509A		Wider input range, constant Ron, same pinout
MICRO NETWORKS	ADC80		HI-574A	Smaller pkg., power
			HI-674A	Faster, smaller pkg., power
	DAC80	HI-5680,HI-5690		Monolithic, power, 5690 is 5.56 times faster
	DAC85	HI-5685,HI-5695		Monolithic, power, 5695 is 5.56 times faster
	DAC87	HI-5687,HI-5697		Monolithic, power, 5697 is 5.56 times faster
	MN-ADC84/85/87		HI-674A	Smaller pkg., power
	MN3009		HI-5618	Monolithic
	MN3014		HI-5618	Monolithic
	MN3348		HI-5680V/87V	Faster, monolithic, power
	MN3349		HI-5685V/87V	Faster, monolithic
	MN343/344		HA-2420	Faster, monolithic
	MN346/347		HA-5320	Faster, monolithic
	MN370/371		HI-5687V	Monolithic
	MN373	HA-5320		
	MN375		HA-5330	Monolithic, lower power
	MN5200		HI-574A	Faster
	MN5210		HI-674A	Two chip design
	MN565A	HI-565A		
	MN574A	HI-574A,HI-674A		674A is 2.3 times faster
MICRO POWER SYSTEMS	MP200DI	HI-200		Constant Ron
	MP201DI	HI-201		Constant Ron
	MP5527		HA-5127	
	MP5537		HA-5137	
	MP562	HI-562A		Faster
	MP574	HI-574A,HI-674A		Digital timing, 674A is 2 times faster
	MP7501	HI-508		
	MP7503	HI-1818A		
	MP7502	HI-1828A		
	MP7506	HI-506		DI processing
	MP7507	HI-507		DI processing
	MP7508DI	HI-508		
	MP7509DI	HI-509		

Competitive Cross Reference Chart (Continued)

Manufacturer	Part Number	Harris Pin-for-Pin Replacement	Harris Closest Replacement	Harris Advantages
MITEL	MT8912	HC-5512		Lower noise, lower cross talk
MOSTEK	MK5912	HC-5512		Lower noise and power
MOTOROLA	LF155		HA-5170	Better DC
	LF155A		HA-5170	Better DC
	LF156		HA-5170	Better DC
	LF156A		HA-5170	Better DC
	LF157		HA-5160	Better DC
	LF157A		HA-5160	Better DC
	LF355		HA-5170	Better DC
	LF355A		HA-5170	Better DC
	LF356		HA-5170	Better DC
	LF356A		HA-5170	Better DC
	LF357		HA-5160	Better DC
	LF357A		HA-5160	Better DC
	MC1408		HI-5618-5	Faster, application resistors
	MC1430		HA-2600	Better AC
	MC1431		HA-2600	Better AC
	MC1436		HA-2640	Better AC and DC
	MC1458		HA-5102	Better AC, lower noise
	MC1508		HI-5618-2	Faster, application resistors
	MC1558		HA-5102	Better AC, lower noise
	MC1748		HA-2600	Better AC and DC
	MC1776		HA-5141	Better AC, lower noise
	MC34002		HA-5102	Better AC
	MC34004		HA-5104	Better AC
	MC3403		HA-4741	Better AC
	AD562A	HI-562A		
	MC3412	HI-565A		
	MC3417		HC-55564 or	Lower power, few external components, military pkg.
	MC3418		HC-55536	
	MC3517			
	MC3518			
	MC3419		HC-5502A	Better longitudinal balance, transhybrid loss. Fewer external components
			HC-5504	Better longitudinal balance, transhybrid loss Fewer external components
	MC35002		HA-5102	Better AC
	MC35004		HA-5104	Better AC
	MC4741	HA-4741		Better AC
NATIONAL SEMICONDUCTOR	ADC1080/1280		HI-574A	Smaller pkg., lower power
			HI-674A	Faster, smaller pkg. power
	ADC1210/11		HI-574A	Faster, complete A/D
	BLC 86/05	HBO-986C05		CMOS micro components, lower power 16K static ram w/full mercury back-up
	DAC0800/0102		HI-5618	Faster, application resistors
	DAC0806/07/08		HI-5618	Faster, application resistors
	DAC1200/01		HI-5685V/87V	Faster, lower power
	DAC1265	HI-565A		
	DAC1266	HI-5660		
	DAC1280	HI-5680,HI-5690		Monolithic, performance, 5690 is 4.44 times faster
	DAC1285	HI-5685/87 HI-5695/97		Monolithic, performance, 5695/97 is 4.44 times faster
	LF0023/43		HA-2420	Monolithic, performance
	LF0053		HA-2420/25	Monolithic
			HA-5320	Faster, monolithic
	LF11201	HI-201		
	LF11508	HI-508-2		Faster, Ron, power
	LF11509	HI-509-2		Faster, Ron, power
	LF13201	HI-201		CMOS Dielectric Isolation
	LF13508	HI-508-5		Faster, Ron, power
	LF13509	HI-509-5		Faster, Ron, power
	LF147		HA-5104	
	LF151		HA-5170	
	LF153		HA-5102	
	LF155		HA-5170	Better DC
	LF155A		HA-5170	Better DC
	LF156		HA-5170	Better DC
	LF156A		HA-5170	Better DC
	LF157		HA-5170	Better DC
	LF157A		HA-5160	Better DC
	LF198		HA-2420	Improved performance
	LF247			
	LF253			

Competitive Cross Reference Chart (Continued)

Manufacturer	Part Number	Harris Pin-for-Pin Replacement	Harris Closest Replacement	Harris Advantages
NATIONAL SEMICONDUCTOR (cont.)	LF347			
	LF353			
	LF355		HA-5170	Better DC
	LF355A		HA-5170	Better DC
	LF356		HA-5170	Better DC
	LF356A		HA-5170	Better DC
	LF357		HA-5160	Better DC
	LF357A		HA-5160	Better DC
	LF398		HA-2425	Improved performance
	LF412		HA-5102	
	LF412A		HA-5102	
	LF441		HA-5141	Lower noise
	LF442		HA-5142	
	LF444		HA-5144	
	LH0002		HA-5002	Monolithic, better AC and DC
	LH0003		HA-2520,HA-2529	Monolithic
	LH0004		HA-2640	Monolithic
	LH0005		HA-2620	Monolithic
	LH0022		HA-5180	Monolithic, better AC and DC
	LH0032		HA-2542	Monolithic
	LH0033		HA-5033	Monolithic, better DC
	LH0042		HA-5180	Monolithic, better AC and DC
	LH0052		HA-5180	Monolithic, better AC
	LH0062		HA-5160	Monolithic, better AC
	LM108		HA-5135	Better DC and AC
	LM108A		HA-5135	Better DC and AC
	LM118		HA-2510	Unity gain stable
	LM124		HA-4741	Better AC
	LM143		HA-2640	Higher supply voltage
	LM144		HA-2640	
	LM146		HA-2740	Better AC
	LM148		HA-4741	Better AC
	LM208		HA-5135	Better DC and AC
	LM208A		HA-5135	Better DC and AC
	LM308		HA-5135	Better DC and AC
	LM308A		HA-5135	Better DC and AC
	LM308A		HA-5135	Better DC and AC
	LM318		HA-2510	Unity gain stable
	LM324		HA-4741	Better AC
	LM343		HA-2640	Higher supply voltage
	LM344		HA-2640	
	LM348		HA-4741	Better AC
	LM4250		HA-5141	Lower noise
	TP3040	HC-5512		Identical
	TP3040A	HC-5512A		Identical
		HC-5512D		Military spec
PMI	PM-155		HA-5180	
	PM-156		HA-5170	
	PM-157		HA-5160	
	OP-15		HA-5170	
	OP-16		HA-5160	
	OP-17		HA-5160	
	OP-42		HA-5160	
	OP-43		HA-5170	
	OP-77		HA-5177	
	OP-227		HA-5102	
	OP-400		HA-5134	
	OP-470		HA-5104	
PRECISION MONOLITHICS	DAC-08		HI-5618	Faster, application resistors
	DAC-1408		HI-5618-5	Faster, application resistors
	DAC-1508		HI-5618-2	Faster, application resistors
	DAC-312		HI-562A	Int. linearity, application resistors
	DMX-88	HI-508		V_{IN} range, lower power
	GAP01		HA-2400	4 channels
	MUX-08	HA-508		I_N range, lower power
	MUX-16	HI-506		V_{IN} range, lower power
	MUX-24	HI-509		V_{IN} range, lower power
	MUX-28	HI-507		V_{IN} range, lower power
	MUX-88	HI-508		V_{IN} range, lower power
	OP01		HA-2500	Better AC
	OP05		HA-5135	Better AC and DC
	OP11		HA-4741	
	OP20		HA-5141	Better AC
	OP220		HA-5142	Better AC

Competitive Cross Reference Chart (Continued)

Manufacturer	Part Number	Harris Pin-for-Pin Replacement	Harris Closest Replacement	Harris Advantages
PRECISION MONOLITHICS (cont.)	OP27		HA-5127	
	OP37		HA-5137,HA-5147	HA-5147 Superior performance
	OP420		HA-5144	Better AC
	PM-562		HI-562A	Faster
	SMP-10/11	HA-2425		Lower power
			HA-5320	Faster, improved accuracy
	SMP-81		HA-2420/25	Lower power
			HA-5320	Faster, improved accuracy
	SSS1458		HA-5102	Better AC, lower noise
	SS1558		HA-5102	Better AC, lower noise
RAYTHEON	LF155		HA-5170	Better DC
	LF155A		HA-5170	Better DC
	LF156		HA-5170	Better DC
	LF156A		HA-5170	Better DC
	LF157		HA-5160	Better DC
	LF157A		HA-5160	Better DC
	LF355		HA-5170	Better DC
	LF355A		HA-5170	Better DC
	LF356		HA-5170	Better DC
	LF356A		HA-5170	Better DC
	LF357		HA-5160	Better DC
	LF357A		HA-5160	Better DC
	LM108		HA-5135	Better AC and DC
	LM108A		HA-5135	Better AC and DC
	LM118		HA-2510	Unity gain stable
	LM124		HA-4741,HA-5154	Better AC
	LM148		HA-4741,HA-5154	Better AC
	LM208		HA-5135	Better AC and DC
	LM208A		HA-5135	Better AC and DC
	LM308		HA-5135	Better AC and DC
	LM308A		HA-5135	Better AC and DC
	LM318		HA-2515	Unity gain stable
	LM324		HA-4741,HA-5154	Better AC
	LM348		HA-4741,HA-5154	Better AC
	RC1556		HA-2605	Better AC and DC
	RC4131		HA-2605	Better AC
	RC4136		HA-4741	
	RC4531		HA-2505	Dielectric Isolation
	RC4741	HA-4741		Better AC
	RM1556		HA-2600	Better AC and DC
	RM4131		HA-2600	Better AC
	RM4136		HA-4741,HA-5154	
	RM4156		HA-4741,HA-5154	
	RM4531		HA-2500	Dielectric Isolation, Better AC
	RM4741	HA-4741		Better AC
RCA	CA3020			
	CA3100		HA-2620	
	CA6078		HA-5141	
	CD4016		HI-201	Better AC and DC
SIGNETICS	AM6012		HI-562A	Int. linearity, application resistors
			HI-5660	Int. linearity, application resistors
	DAC08		HI-5618	Faster, application resistors
	LF198		HA-2420	Improved performance
	LF398		HA-2425	Improved performance
	MC1408		HI-5618-5	Faster, application resistors
	MC1508		HI-5618-2	Faster, application resistors
	NE531		HA-2515	
	NE5532		HA-5102	Lower noise
	NE5533		HA-5112	Lower noise
	NE5534		HA-5135	
	NE5537		HA-2425-5	Lower power
			HA-5320-5	Faster
	NE5539		HA-2539	Better AC
	SE531		HA-2510	
	SE5532		HA-5102	Lower noise
	SE5533		HA-5112	Lower noise
	SE5534		HA-5135	
	SE5539		HA-2539	Better AC
SILICON-GENERAL	SG741		HA-2500	
SILICONIX	DG181		HI-381	Dielectric Isolation

Competitive Cross Reference Chart (Continued)

Manufacturer	Part Number	Harris Pin-for-Pin Replacement	Harris Closest Replacement	Harris Advantages
SILICONIX (cont.)	DG182		HI-381	Dielectric Isolation
	DG184		HI-384	Dielectric Isolation
	DG185		HI-384	Dielectric Isolation
	DG187		HI-387	Dielectric Isolation
	DG188		HI-387	Dielectric Isolation
	DG190		HI-390	Dielectric Isolation
	DG191		HI-390	Dielectric Isolation
	DG200A	HI-200		Dielectric Isolation
	DG201A	HI-201		Dielectric Isolation
	DG211		HI-201	Full temp range specified
	DG271		HI-201HS	Faster
	DG300A	Hi-300		Dielectric Isolation
	DG301A	HI-301		Dielectric Isolation
	DG302A	HI-302		Dielectric Isolation
	DG303A	HI-303		Dielectric Isolation
	DG304A	HI-304		Dielectric Isolation
	DG305A	HI-305		Dielectric Isolation
	DG306A	HI-306		Dielectric Isolation
	DG307A	HI-307		Dielectric Isolation
	DG381A	HI-381		Dielectric Isolation
	DG384A	HI-384		Dielectric Isolation
	DG387A	HI-387		Dielectric Isolation
	DG390A	HI-390		Dielectric Isolation
	DG5040	HI-5040		Dielectric Isolation
	DG5041	HI-5041		Dielectric Isolation
	DG5042	HI-5042		Dielectric Isolation
	DG5043	HI-5043		Dielectric Isolation
	DG5044	HI-5044		Dielectric Isolation
	DG5045	HI-5045		Dielectric Isolation
	DG506A	HI-506		Lower power, DI processing
	DG506AA	HI-506-2		Lower power, DI processing
	DG507A	HI-507		Lower power, DI processing
	DG507AA	HI-507-2		Lower power, DI processing
	DG508A	HI-508		Lower power, DI processing
	DG508AA	HI-508-2		Lower power, DI processing
	DG509A	HI-509		Lower power, DI processing
	DG509AA	HI-509-2		Lower power, DI processing
	SD5200		HI-201HS	Dielectric Isolation
SOLITRON	CM4016A		HI-201	Better AC and DC
	UC4000		HA-2600	
	UC4002		HA-2605	
SPRAGUE	ULN2139		HA-2600	
	ULN2151		HA-2600	
	ULN2156		HA-2600	
	ULN2157		HA-2650	
	ULN2158		HA-2650	
	ULN2171		HA-2600	
	ULN2172		HA-2620	
	ULN2173		HA-2600	
	ULN2174		HA-2620	
	ULN2175		HA-2600	
	ULN2176		HA-2600	
TELEDYNE PHILBRICK	1321	HA-2620		Identical
	1322	HA-2620		Identical
	1332	HA-2645		Identical
	1339		HA-2625	
	1341	HA-2540		Identical
	1342	HA-2539		Identical
	1343	HA-5190		Identical
	1344	HA-5160		Identical
	1345	HA-5162		Identical
	1346	HA-5180		Identical
	1347	HA-5180A		Identical
	1437		HA-2541	Monolithic
	1438		HA-2541	Monolithic
	1460		HA-2542	Monolithic
	1466		HA-2542	Monolithic
	4058		HI-5680	Monolithic
	4058-83		HI-5687	Monolithic
	4068A	HI-562A		Identical
	4084	HI-5618		Identical
	4088	HI-DAC16		Identical

Competitive Cross Reference Chart (Continued)

Manufacturer	Part Number	Harris Pin-for-Pin Replacement	Harris Closest Replacement	Harris Advantages
TELEDYNE PHILBRICK (cont.)	4189			
	4551	HI-547		Identical
	4552	HI-546		Identical
	4553	HI-549		Identical
	4554	HI-548		Identical
	4853		HA-5320	Monolithic, smaller pkg.
	4854		HA-2420	Faster, monolithic, smaller pkg.
	4856	HA-2420/25		Identical
	4857		HA-5320	Monolithic, smaller pkg., power
	4866	HA-5320		Identical
	DAC80I/V	HI-5680I/V		Identical
	TP5210		HI-674A	
	TP565A	HI-565A		Identical
	TP574A	HI-574A,HI-674A		Identical, 674A is 1.67 times faster
	TPADC85/87			
TEXAS INSTRUMENTS	MC1458		HA-5102	Lower noise
	MC1558		HA-5102	Lower noise
	TCM2912A	HC-5512		Lower noise, lower cross talk, lower power
	TCM4212+		HC-5502A or	Fewer external components
	TCM4201+		HC-5504	
	TCM4208= 3 chip set			
	TL022		HA-5142	Better DC
	TL044		HA-5144	Better DC
	TL061		HA-5141,HA-5151	Better DC, lower noise
	TL062		HA-5142,HA-5152	MIL range available
	TL064		HA-5144,HA-5154	MIL range available
	TL072		HA-5102	MIL range available
	TL074		HA-5104	MIL range available
	TL082		HA-5102	MIL range available
	TL084		HA-5104	MIL range available
TRANSITRON	TOA7709	HA-2600		
	TOA8709	HA-2605		

High Temperature Electronics

To serve the growing need for electronics that will operate in severe high temperature environments, Harris offers integrated circuits that have been characterized over elevated temperatures and that have electrical characteristics guaranteed at 200°C. Typical applications include:

- Well Logging
- Industrial Process Control
- Engine Control and Testing
- High Temperature Data Acquisition Systems

All parts offered in the -1 series have had their electrical performance parameters characterized up to 250°C.

Production flow of -1 parts includes 160 hours burn-in and final electrical test at 200°C. Devices available now:

- HA-2600-1 ..... Operational Amplifier
- HA-2620-1 ..... Operational Amplifier
- HI-200-1 ..... Analog Switch
- HI-201-1 ..... Analog Switch

Consult factory for price and availability information.

Packaging Techniques

Harris Semiconductor offers Leadless Chip Carriers (LCC) as a packaging option on various Analog integrated circuits. An LCC is a square or rectangular package for an Integrated Circuit (IC) that is manufactured in the same manner as a conventional side-braze dual-in-line package (DIP). The LCC is comprised of the cavity and seal ring section of a standard DIP and offers the user a means of achieving high density system configurations while retaining the reliability benefits of hermetic IC Packaging. Figure 1 provides a comparison of the construction of an LCC and a conventional side-braze DIP.

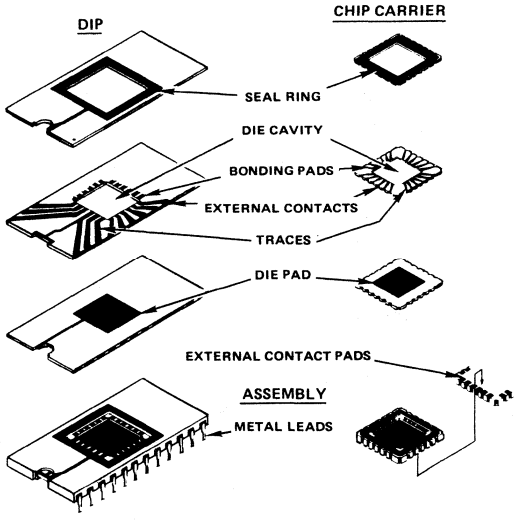


FIGURE 1. EXPLODED VIEW OF CHIP CARRIER AND DIP

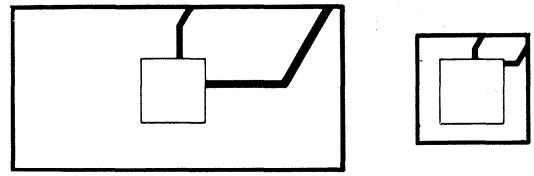
The LCC's two principle advantages over conventional side-braze DIPs are packaging density and electrical performance. Packaging density is the number one advantage to an LCC over a side-braze DIP. The size of a DIP is governed primarily by the number of leads required and not by the size of the IC. As pin count increases, more and more of the DIP package is used only to provide an electrical trace path to the external leads. The size of an LCC is dependent on the size of the die not on the number of leads. As pin count increases, overall size increases but at a much slower rate. Table 1 provides a comparison between the areas of 18, 28 and 48 lead LCCs to 18, 28 and 48 lead side-braze DIPs.

TABLE 1.

LEAD COUNT	LCC AREA	DIP AREA	DIP AREA vs. LCC AREA
18	0.10	0.22	220%
28	0.20	0.84	420%
48	0.31	1.68	542%

(All Units in Square Inches)

The chart indicates a 220% improvement in packaging area for the 18 lead LCC, and 542% improvement for the 48 lead LCC. Obviously, sizeable savings in circuit board area can be achieved with this packaging option. The second major advantage of the LCC is in electrical performance. The package size and geometry also dictates trace length and uniformity. Figure 2 provides a comparison between the trace lengths for various LCCs and side-braze DIPs. As pin count goes up, trace lengths get longer, adding resistance and capacitance unequally around the package. As ICs get faster and more complex these factors start to become a limiting factor on performance. LCCs minimize this effect by maintaining, as close as possible, uniform trace length so that the package is a significantly smaller determinant of system performance.



LEAD COUNT	LONGEST TRACE DIP / LONGEST TRACE LCC	LONGEST TRACE SHORTEST TRACE	
		LCC	DIP
18	2:1	1.5:1	6:1
24	4:1	1.5:1	3:1
40	5:1	1.5:1	6:1
54	6:1	1.5:1	7:1

FIGURE 2. ELECTRICAL PERFORMANCE (RESISTANCE AND SPEED)

Packaging Techniques (Continued)

The LCC also offers environmental advantages over "chip-and-wire" manufacturing techniques used in high density hybrid circuits. An IC can be fully tested, burned-in and processed in an LCC, thereby guaranteeing its performance.

The IC is further protected by a small hermetic package in which internal vapor content can be carefully controlled during production.

Harris Semiconductor Leadless Chip Carriers in both Ceramic and Epoxy provide reliable, high density, high performance packaging options for today's systems.

Those products available in LCC form are shown in the Standard Products Packaging Availability Guide at the beginning of each section. Consult the factory or your Harris sales representative for pricing and availability.

Chip Information

Harris Standard Flows

Harris Semiconductor offers three standard integrated circuit dice product flows which cover the application environments our customers experience. These flows range from low cost commercial dice to military temperature range dice with sample electrical performance data. All of these product grades have one thing in common. They result from meticulous attention to quality, staring with design decisions made during product development and ending with the labeling of shipping containers for delivery to our customers.

Most of the dice offered by Harris are available in the three standard grades. Consult the dice data sheets or contact your Harris representative to determine which grades are available for a particular circuit. The standard flows offered are:

DASH 6 - Commercial Grade Dice

DASH 6 dice are 100% probe tested at +25°C to assure the maximum/mimimum DC characteristics listed in the DASH 6 dice data sheet. DASH 6 dice are intended for use in non-military applications. DASH 6 dice are 100% visually inspected to Harris Semiconductor's commercial grade criteria.

DASH 3 - Military Grade Dice

DASH 3 dice are 100% probe tested at +25°C to assure the maximum/minimum DC characteristics listed in the DASH 3 dice data sheet. DASH 3 dice are intended for use in military applications. DASH 3 dice are 100% visually inspected to Harris Semiconductor's MIL-STD-883, Method 2010, Condition B (Class B) criteria.

To assure that the electrical specifications will be met, a sample of the DASH 3 dice are pulled. The dice are assembled into standard packages and tested at +25°C, -55°C and +125°C to an LTPD of 15/1. The dice and test data are supplied to the customer. DASH 3 dice are 100% visually inspected to Harris Semiconductor's MIL-STD-883, Method 2010, Condition B (Class B) criteria.

Mechanical Information

Dimensions:

All dimensions given in the die layout section of the dice data sheets are nominal with a tolerance of ± 0.003 inches (± 0.08mm) Die thicknesses are 0.018 inches ± 0.003 inches (0.46mm ± 0.08mm).

Bonding Pads:

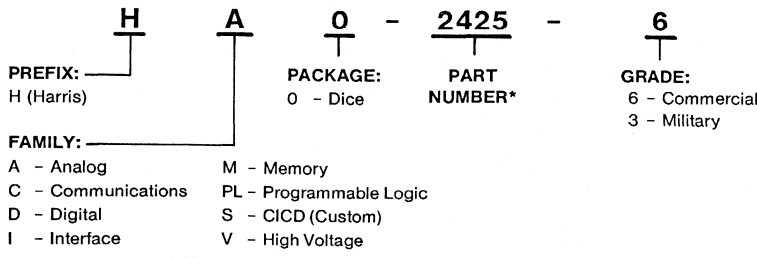
Minimum bonding pad size is 0.004 x 0.004 inches (0.10mm x 0.10mm).

Dice are placed in conductive waffle carriers, sealed in an antistatic bag, and packaged in a suitable shipping container. The dice data sheets for each product will specify the number of dice which will be packed in each individual tray.

Ordering Information

Harris products are designated by Product Code. Harris Semiconductor Analog dice products will always begin with H. When ordering, please refer to products by the full code. Other Harris dice products may be specified by industry standard part numbers. Specific device numbers will always be isolated by hyphens.

Harris Part Number Example



* Alpha suffix parts are defined in individual data sheets.

ANALOG

Operational Amplifiers and Comparators

2

ABSOLUTE MAXIMUM RATINGS

As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Specifications" are the only conditions recommended for satisfactory operation.

Ordering Information

HARRIS PRODUCT CODE EXAMPLE

H A 7 — 5147 — 5

PREFIX:
H (HARRIS)

FAMILY:
A : Analog
C : Communications
D : Digital
F : Filters
I : Interface
M : Memory
V : Analog High Voltage

PACKAGE:
1 : Dual-In-Line Ceramic
2 : Metal Can
3 : Dual-In-Line Plastic
7 : Mini-DIP, Ceramic
0 : Chip Form

PART NUMBER

TEMPERATURE:
2 : -55°C to +125°C
4 : -25°C to +85°C
5 : 0°C to +75°C
7 : Dash-7 High Reliability Commercial Product 0°C to +75°C, includes 96 hour Burn-In.

These products are available fully screened to Mil-Std-883C. Contact a Harris Sales Office for a copy of the /883 data sheet.

Standard Products Packaging Availability†

PACKAGE	PLASTIC DIP 3-	CERAMIC DIP 1-				CERAMIC MINI-DIP 7-				METAL CAN 2-			
TEMPERATURE	**-5**	**-2**	**-4**	**-5**	**-7**	**-2**	**-4**	**-5**	**-7**	**-2**	**-4**	**-5**	**-7**
DEVICE NUMBER													
HA-2400		C1											
HA-2404			C1										
HA-2405				C1	C1								
HA-2406	O			C1									
HA-2500						A				W			
HA-2502						A				W			
HA-2505	M							A	A			W	W
HA-2510						A				W			
HA-2512						A				W			
HA-2515	M							A	A			W	W
HA-2520						A				W			
HA-2522						A				W			
HA-2525	M							A	A			W	M
HA-2529	M					A		A	A	W		W	W
HA-2539	N	B1	B1	B1	B1								
HA-2540	N	B1	B1	B1	B1								
HA-2541				B1						Y		Y	Y
HA-2542	N	B1		B1						Y		Y	Y
HA-2544	M					A		A	A	W		W	W
HA-2600						A				W			
HA-2602						A				W			
HA-2605	M							A	A			W	W

† Letter codes in this chart indicate available packages as shown in Packaging Section 11.

Standard Products Packaging Availability (Continued)

PACKAGE	PLASTIC DIP 3-	CERAMIC DIP 1-				CERAMIC MINI-DIP 7-				METAL CAN 2-			
TEMPERATURE	-5	-2	-4	-5	-7	-2	-4	-5	-7	-2	-4	-5	-7
DEVICE NUMBER													
HA-2620						A				W			
HA-2622						A				W			
HA-2625	M			A	A			A	A			W	W
HA-2640						A				W			
HA-2645								A	A			W	W
HA-2650		B1				A				W			
HA-2655			B1	B1				A				W	
HA-2720						A				W			
HA-2725								A				W	
HA-4741	N	B1		B1									
HA-4900		C1											
HA-4902		C1											
HA-4905				C1	C1								
HA-5002						A		A	A	W		W	W
HA-5033	M									Y		Y	Y
HA-5101	M					A		A	A	W		W	W
HA-5102	M					A		A	A	W		W	W
HA-5104	N	B1		B1	B1								
HA-5111	M					A		A	A	W		W	W
HA-5112	M	B1		B1	B1	A		A	A	W		W	W
HA-5114	N	B1		B1	B1								
HA-5127						A		A	A	W		W	W
HA-5130						A		A	A	W		W	W
HA-5134		B1		B1	B1								
HA-5135						A		A	A	W		W	W
HA-5137						A		A	A	W		W	W
HA-5141	M					A		A	A	W		W	W
HA-5142	M					A		A	A	W		W	W
HA-5144	N	B1		B1	B1								
HA-5147						A		A	A	W		W	W
HA-5151	M					A		A	A	W		W	W
HA-5152	M					A		A	A	W		W	W
HA-5154	N	B1		B1	B1								
HA-5160										W		W	W
HA-5162												W	W
HA-5170						A	A	A	A	W	W	W	W
HA-5177						A	A	A	A	W	W	W	W
HA-5180						A	A	A	A	W	W	W	W
HA-5190		B1								Y			
HA-5195				B1	B1							Y	Y

Selection Guide

OPERATIONAL AMPLIFIERS: HIGH SLEW-RATE

PART NUMBER	TEMPERATURE RANGE			SLEW RATE (V/μs)	BANDWIDTH PRODUCT (MHz)	FULL POWER BANDWIDTH (MHz)	BIAS CURRENT (nA)	OPEN LOOP GAIN (V/mV)	MINIMUM GAIN STABLE	COMMENTS	PAGE
	-55°C TO +125°C	0°C TO +75°C	-40°C TO +85°C								
HA-5112	X	X		20	60	0.3	130	250	10	Low Noise	2-133
HA-5114	X	X		20	60	0.3	130	250	10	Low Noise	2-133
HA-5137	X	X		20	63	0.3	10	1500	5	Low Noise	2-163
HA-2400	X			30	40	0.5	50	150	10	Addressable	2-9
HA-2404			X	30	40	0.5	50	150	10	Addressable	2-9
HA-2405		X		30	40	0.5	50	150	10	Addressable	2-9
HA-2406		X		30	40	0.5	50	150	10	Addressable	2-13
HA-5147	X	X		35	120	0.5	10	1800	10	Low Noise	2-176
HA-2620	X			35	100	0.6	1	150	5		2-77
HA-2622	X			35	100	0.6	5	150	5		2-77
HA-2625		X		35	100	0.6	5	150	5		2-77
HA-5111	X	X		50	100	0.7	150	250	10	Low Noise	2-123
HA-2512	X			60	12	1.0	125	15	Unity		2-21
HA-2515	X			60	12	1.0	125	15	Unity		2-21
HA-2510	X			65	12	1.0	100	15	Unity		2-21
HA-5162	X	X		70	100	1.0	0.02	100	10	JFET	2-190
HA-5160	X	X		120	100	1.9	0.02	150	10	JFET	2-190
HA-2520	X			120	20	2.0	100	15	3		2-25
HA-2522	X			120	20	2.0	125	15	3		2-25
HA-2525		X		120	20	2.0	125	15	3		2-25
HA-2529	X	X		150	20	2.6	100	15	3	Power Output	2-30
HA-2544	X	X		150	50	4.2	9000	6	Unity	Video Amp	2-63
HA-5190	X			200	150	6.5	5000	30	5		2-211
HA-5195		X		200	150	6.5	5000	30	5		2-211
HA-2541	X	X		300	40	4.7	6000	10	Unity		2-48
HA-2542	X	X		350	60	5.5	6000	10	2	Power Output	2-55
HA-2540	X	X	X	400	400	6.0	5000	15	10		2-42
HA-2539	X	X	X	600	600	9.5	5000	15	10		2-36

Selection Guide (Continued)

OPERATIONAL AMPLIFIERS: WIDE BANDWIDTH

PART NUMBER	TEMPERATURE RANGE -55°C TO +125°C	TEMPERATURE RANGE 0°C TO +75°C	TEMPERATURE RANGE -40°C TO +85°C	GAIN BANDWIDTH PRODUCT (MHz)	FULL POWER BANDWIDTH (MHz)	SLEW RATE (V/μs)	BIAS CURRENT (nA)	OPEN LOOP GAIN (V/mV)	MINIMUM GAIN STABLE	COMMENTS	PAGE
SINGLE											
HA-2510	X			12	1.0	65	100	15	Unity		2-21
HA-2512	X			12	1.0	60	125	15	Unity		2-21
HA-2515		X		12	1.0	60	125	15	Unity		2-21
HA-2600	X			12	0.075	7	1	150	Unity		2-72
HA-2602	X			12	0.075	7	15	150	Unity		2-72
HA-2605		X		12	0.075	7	5	150	Unity		2-72
HA-2520	X			20	2.0	120	100	15	3		2-25
HA-2522	X			20	1.9	120	125	15	3		2-25
HA-2525		X		20	1.9	120	125	15	3		2-25
HA-2529	X	X		20	2.6	150	100	15	3	Power Output	2-30
HA-2541	X	X		40	4.7	300	6000	10	Unity		2-48
HA-2544	X	X		50	4.2	150	9000	6	15	Video Amp	2-63
HA-2542	X	X		70	5.5	350	6000	10	2	Power Output	2-55
HA-5137	X	X		63	0.3	17	8	1800	5	Low Noise	2-163
HA-5147	X	X		100	0.5	35	8	1800	10	Low Noise	2-176
HA-5111	X	X		100	0.7	50	150	250	10	Low Noise	2-123
HA-2620	X			100	0.6	35	1	150	5		2-77
HA-2622	X			100	0.6	35	5	150	5		2-77
HA-2625		X		100	0.6	35	5	150	5		2-77
HA-5160	X	X		100	1.9	120	0.02	150	10	JFET	2-190
HA-5162	X	X		100	1.1	70	0.02	100	10	JFET	2-190
HA-5190	X			150	6.5	200	5000	30	5		2-211
HA-5195		X		150	6.5	200	5000	30	5		2-211
HA-2540	X	X	X	400	6.0	400	5000	30	10		2-42
HA-2539	X	X	X	600	9.5	600	5000	30	10		2-36
DUAL											
HA-5112	X	X		60	0.3	20	130	250	10	Low Noise	2-133
QUAD											
HA-2400	X			40	0.5	30	50	150	10	Addressable	2-9
HA-2404			X	40	0.5	30	50	150	10	Addressable	2-9
HA-2405		X		40	0.5	30	50	150	10	Addressable	2-9
HA-2406		X		40	0.5	30	50	150	10	Addressable	2-13
HA-5114	X	X		60	0.3	20	130	250	10	Low Noise	2-133

Selection Guide (Continued)

OPERATIONAL AMPLIFIERS: PRECISION

PART NUMBER	TEMPERATURE RANGE -55°C TO +125°C	TEMPERATURE RANGE 0°C TO +75°C	TEMPERATURE RANGE -40°C TO +85°C	OFFSET VOLTAGE (μV)	OFFSET VOLTAGE DRIFT (μV/°C)	BIAS CURRENT (nA)	OPEN LOOP GAIN (V/mV)	NOISE CURRENT (pA/√Hz)	NOISE VOLTAGE (nV/√Hz)	CMRR (dB)	PSRR (dB)	SUPPLY CURRENT (mA)	COMMENTS	P
SINGLE														
HA-5180	X	X	X	100	5	0.00003	1000	0.01	70	110	105	0.8	JFET	2
HA-5170	X	X	X	100	2	0.02	600	0.01	10	100	105	1.9	JFET	2
HA-5130	X	X		10	0.4	1	1400	0.14	15	120	130	1.3		2
HA-5177	X	X		10	0.2	1.2	1380	0.12	9	140	120	1.7		2
HA-5127	X	X		10	0.2	10	1500	0.60	3	120	120	3		2
HA-5137	X	X		10	0.2	10	1500	0.60	3	120	120	3	High Speed	2
HA-5147	X	X		10	0.2	10	1800	0.60	3	120	120	3	High Speed	2
QUAD														
HA-5134	X	X		50	2.5	2	1000	0.60	7	120	120	5	Quad	2

OPERATIONAL AMPLIFIERS: LOW POWER

PART NUMBER	TEMPERATURE RANGE -55°C TO +125°C	TEMPERATURE RANGE 0°C TO +75°C	TEMPERATURE RANGE -40°C TO +85°C	SUPPLY CURRENT (μA)	SUPPLY RANGE (V)	SLEW RATE (V/μs) AT INDICATED SUPPLY CURRENT	GAIN BANDWIDTH PRODUCT (kHz) AT INDICATED SUPPLY CURRENT	OUTPUT SWING (V) ±15V POWER SUPPLIES	OFFSET VOLTAGE (mV)	COMMENTS	P
SINGLE											
HA-5141	X	X		50	+2/+40	1	400	0/+3 (+5V_S)	0.7		2-
HA-5151	X	X		200	+2/+40	4	1300	±10	2	Lower Noise	2-
DUAL											
HA-5142	X	X		50	+2/+40	1	400	0/+3 (+5V_S)	0.7		2-
HA-5152	X	X		200	+2/+40	4	1300	±10	2	Lower Noise	2-
QUAD											
HA-5144	X	X		50	+2/+40	1	400	0/+3 (+5V_S)	0.7		2-
HA-5154	X	X		200	+2/+40	4	1300	±10	2	Lower Noise	2-

OPERATIONAL AMPLIFIERS: GENERAL PURPOSE

PART NUMBER	TEMPERATURE RANGE -55°C TO +125°C	TEMPERATURE RANGE 0°C TO +75°C	TEMPERATURE RANGE -40°C TO +85°C	GAIN BANDWIDTH PRODUCT (MHz)	SLEW RATE (V/μs)	OFFSET VOLTAGE (mV)	BIAS CURRENT (nA)	NOISE VOLTAGE (nV/√Hz)	OPEN LOOP GAIN (V/mV)	COMMON MODE RANGE (V) +15V POWER SUPPLIES	SUPPLY CURRENT (mA)	COMMENTS	P
SINGLE													
HA-2600	X			12	7	0.5	1	16	150	±11	3		2-
HA-2602	X			12	7	3	15	16	150	±11	3		2-
HA-2605		X		12	7	3	5	16	150	±11	3		2-
HA-5101	X	X		8	10	0.5	130	4.3	250	±12	5	Low Noise	2-
HA-5111	X	X		100	50	0.5	130	4.3	250	±12	5	Low Noise	2-
DUAL													
HA-5102	X	X		8	3	0.5	130	4.3	250	±12	5	Low Noise	2-
HA-5112	X	X		60	20	0.5	130	4.3	250	±12	5	Low Noise	2-
QUAD													
HA-2400	X			40	30	4	50	20	150	±9	4.8	Addressable	2-
HA-2404			X	40	30	4	50	20	150	±9	4.8	Addressable	2-
HA-2405		X		40	30	4	50	20	150	±9	4.8	Addressable	2-
HA-2406		X		40	30	4	50	20	150	±9	4.8	Addressable	2-
HA-5104	X	X		8	3	0.5	130	4.3	250	±12	6.5	Low Noise	2-
HA-5114	X	X		60	20	0.5	130	4.3	250	±12	6.5	Low Noise	2-

Selection Guide (Continued)

OPERATIONAL AMPLIFIERS: HIGH VOLTAGE

PART NUMBER	FEATURES		APPLICATIONS	PAGE
HA-2640 HA-2645	• Slew Rate: • Bandwidth: • Input Offset Voltage: • Offset Current: • Output Voltage Swing: • Input Voltage Range: • Supply Range: • Output Overload Protection	1V/µs 4MHz 4mV 5nA ±35V ±35V ±10V to ±40V	• Industrial Control Systems • Power Supplies • High Voltage Regulators • Resolver Excitation • Signal Conditioning	2-82

OPERATIONAL AMPLIFIERS: ADDRESSABLE

PART NUMBER	FEATURES		APPLICATIONS	PAGE
HA-2400 HA-2404 HA-2405	• Four Channels Addressable • High Slew Rate • Wide Gain Bandwidth Product:	 30V/µs 40MHz	• Signal Selection/Multiplexing • Variable gain stages • Oscillators	2-9
HA-2406	• High Gain: • TTL Compatible	150kV/V	• Filters • Comparators • Integrators	2-13

CURRENT BUFFERS/DRIVERS

PART NUMBER	FEATURES		APPLICATIONS	PAGE
HA-5033	• Differential Phase Error: • Differential Gain Error: • High Slew Rate: • Wide Power Bandwidth: • Fast Rise Time: • Wide Power Supply Range:	0.1° 0.1% 1300V/µs 80MHz 3ns ±5/±16V	• Video Buffers • HF Buffers • Op Amp Isolation Buffers • High Speed Line Drivers • Impedance Matching	2-114
HA-5002	• High Slew Rate • High Output Current • Low Quiescent Current	1300V/µs 200mA 9mA	• Precision Buffers • Op Amp Isolation Buffers • High Speed Line Drivers	2-107
HA-2542	• $A_V \geq -1, +2$ Stable with No Compensation • High Output Current: • Wide Power Bandwidth: • High Slew Rate:	 100mA 5.5MHz 350V/µs	• Video Cable Drivers • Pulse Amplifiers • Wideband Signal Conditioners	2-55

COMPARATORS

PART NUMBER	FEATURES		APPLICATIONS	PAGE
HA-4900 HA-4902 HA-4905	• Fast Response Time: • Low Offset Voltage: • Low Offset Current: • Single or Dual Supply • Analog and logic supplies separated for easier interface and noise immunity	130ns 2mV 10nA	• Threshold Detectors • Zero Crossing Detectors • Window Detectors • Interface • Oscillators	2-100

Operational Amplifiers Glossary

AVERAGE INPUT OFFSET CURRENT DRIFT - The average change in offset current between room (+25°C) and high temperature (+125°C, +85°C or +75°C) or between room temperature and low temperature (0°C, -25°C or -55°C) divided by the temperature difference.

AVERAGE OFFSET VOLTAGE DRIFT - The average change in offset voltage between room (+25°C) and high temperature (+125°C, +85°C or +75°C) or between room temperature and low temperature (0°C, -25°C or -55°C) divided by the temperature difference.

CHANNEL SEPARATION - The ratio of the output of a driven amplifier to the output (referred to input) of an adjacent undriven amplifier.

COMMON MODE INPUT VOLTAGE (V_{IC}) - The average of the voltages present at the differential input terminals.

COMMON MODE INPUT VOLTAGE RANGE (V_{ICR}) - The range of voltage that if exceeded at either input terminal will cause the amplifier to cease operating properly.

COMMON MODE REJECTION RATIO (CMRR) - The ratio of change in input offset voltage to change in input common-mode voltage, expressed in dB.

$$CMRR = 20 \times \log_{10}\left(\frac{VIO}{VCM}\right)$$

COMMON MODE RESITANCE (r_{ic}) - The ratio of change in input common-mode voltage to the resulting change in input current.

DIFFERENTIAL INPUT RESISTANCE (r_{id}) - The ratio of change in input differential voltage (small-signal, assumes amplifier operating linearly) to the resulting change in differential input current.

FULL POWER BANDWIDTH (FPBW) - The maximum frequency at which a full scale undistorted (THD $\leq$ 1%) sine wave can be obtained at the output of the amplifier.

GAIN BANDWIDTH (GBW) - The open-loop gain of an op amp (in V/V) at a mid-band, linear-region frequency (usually between 1KHz and 10KHz) times that frequency (in Hz). GBW = $[A_{VOL}] \bullet f$

INPUT BIAS CURRENT (I_{BIAS}) - The average of the currents flowing into or out of the input terminals when the output is at zero volts.

INPUT CAPACITANCE (C_{IN}) - The equivalent capacitance seen looking into either input terminal.

INPUT NOISE CURRENT (i_n) - The input noise current that would reproduce the noise seen at the output if all amplifier noise sources were set to zero and the source impedances were large compared to the optimum source impedance.

INPUT OFFSET CURRENT (I_{OS}) - The difference in the currents flowing into the two input terminals when the output is at zero volts.

INPUT OFFSET VOLTAGE (V_{OS}) - The differential D.C. voltage required to zero the output voltage with no input signal or load. Input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT NOISE VOLTAGE (e_n) - The input noise voltage that would reproduce the noise seen at the output if all the amplifier noise sources and source resistances were set to zero.

LARGE SIGNAL VOLTAGE GAIN (A_V) - The ratio of the peak to peak output voltage swing (over a specified range) to the change in input voltage required to drive the output.

OUTPUT CURRENT (I_{OUT}) - The output current available from the amplifier at some specified output voltage.

OUTPUT RESISTANCE (RO) - The ratio of the change in output voltage to the change in output current.

OUTPUT SHORT CIRCUIT CURRENT (I_{SC}) - The output current available from the amplifier with the output shorted to ground (or other specified potential).

OUTPUT VOLTAGE SWING (V_{OUT}) - The maximum output voltage swing, referred to ground, that can be obtained under specified loading conditions.

OVERSHOOT - Peak excursion above final value of an output step response.

POWER SUPPLY REJECTION RATIO (PSRR) - The ratio of the change in input offset voltage to the change in power supply voltage producing it.

RISE TIME (t_r) - The time required for an output voltage step to change from 10% to 90% of its final value, when the input is subjected to a small-signal voltage pulse.

SETTLING TIME ($t_{set.}$) - The time required, after application of a step input signal, for the output voltage to settle and remain within a specified error band around the final value.

SLEW RATE (SR) - The rate of change of the output under large-signal conditions. Slew rate may be specified separately for both positive and negative going changes.

SUPPLY CURRENT (I_S) - The current required from the power supply to operate the amplifier with no load and the output at zero volts.

SUPPLY VOLTAGE RANGE - The range of power supply voltage over which the amplifier may be safely operated.

UNITY GAIN BANDWIDTH - The frequency range from D.C. to that frequency where the amplifiers open loop gain is unity.

HA-2400/04/05

PRAM Four Channel Programmable Amplifier

Features

- Programmability
- High Rate Slew 30V/μs
- Wide Gain Bandwidth 40MHz
- High Gain 150kV/V
- Low Offset Current 5nA
- High Input Impedance 30MΩ
- Single Capacitor Compensation
- DTL/TTL Compatible Inputs

Applications

- Thousands of Applications; Program:
  - Signal Selection/Multiplexing
  - Operational Amplifier Gain
  - Oscillator Frequency
  - Filter Characteristics
  - Add-Subtract Functions
  - Integrator Characteristics
  - Comparator Levels
- For Further Design Ideas, See App. Note 514.

Description

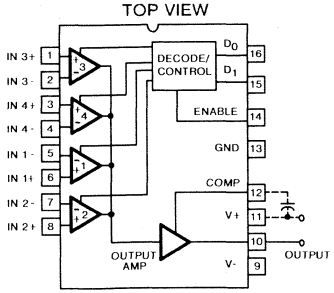
HA-2400/04/05 comprise a series of four-channel programmable amplifiers providing a level of versatility unsurpassed by any other monolithic operational amplifier. Versatility is achieved by employing four input amplifier channels, any one (or none) of which may be electronically selected and connected to a single output stage through DTL/TTL compatible address inputs. The device formed by the output and the selected pair of inputs is an op amp which delivers excellent slew rate, gain bandwidth and power bandwidth performance. Other advantageous features for these dielectrically isolated amplifiers include high voltage gain and input impedance coupled with low input offset voltage and offset current. External compensation is not required on this device at closed loop gains greater than 10.

Each channel of the HA-2400/04/05 can be controlled and operated with suitable feedback networks in any of the standard op amp configurations. This specialization makes these amplifiers excellent components for multiplexing signal selection, and mathematical function designs. With 30V/μs slew rate, 40MHz gain bandwidth, and 30M ohms input impedance these devices are ideal building blocks for signal generators, active filters, and data acquisition designs. Programmability coupled with 2mV typical offset voltage and 5nA offset current makes these amplifiers outstanding components for signal conditioning circuits.

HA-2400/04/05 are available in a 16 pin Dual-In-Line package. HA-2400 is specified from -55°C to +125°C. HA-2404 is specified over the -25°C to +85°C range, while HA-2405 operates from 0°C to +75°C.

Pinout

HA1-2400 (CERAMIC DIP)
TOP VIEW



TRUTH TABLE

D_1	D_0	EN	SELECTED CHANNEL
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4
X	X	L	NONE

Schematic

HA-2400

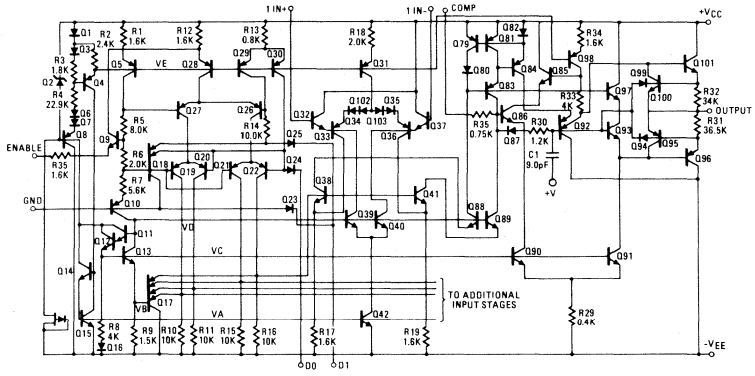


Diagram Includes: One Input Stage, Decode Control, Bias Network, and Output Stage.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings

Voltage between V+ and V- Terminals 45.0V
Differential Input Voltage ..... $\pm V_{SUPPLY}$
Digital Input Voltage ..... -0.76V to +10.0V
Output Current ..... Short Circuit Protected ($I_{SC} < \pm 33mA$)
Internal Power Dissipation (Note 13) 300mW

Operating Temperature Ranges

HA-2400 ..... $-55^oC \leq T_A \leq +125^oC$
HA-2404 ..... $-25^oC \leq T_A \leq +85^oC$
HA-2405 ..... $0^oC \leq T_A \leq +75^oC$
Storage Temperature Range ..... $-65^oC \leq T_A \leq +150^oC$

Electrical Specifications

Test Conditions: $V_{SUPPLY} = \pm 15.0V$ Unless Otherwise Specified.
Digital Inputs: $V_{IL} = +0.5V$, $V_{IH} = +2.4$. Limits apply to each of the four channels, when addressed.

PARAMETER	TEMP	HA-2400/04 LIMITS			HA-2405 LIMITS			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Offset Voltage	+25°C	-	4	9	-	4	9	mV
	Full	-	-	11	-	-	11	mV
Bias Current (Note 12)	+25°C	-	50	200	-	50	250	nA
	Full	-	-	400	-	-	500	nA
Offset Current (Note 12)	+25°C	-	5	50	-	5	50	nA
	Full	-	-	100	-	-	100	nA
Input Resistance (Note 12)	+25°C	-	30	-	-	30	-	MΩ
Common Mode Range	Full	±9.0	-	-	±9.0	-	-	V
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Notes 1, 5)	+25°C	50k	150k	-	50k	150k	-	V/V
	Full	25K	-	-	25K	-	-	V/V
Common Mode Rejection Ratio (Note 2)	Full	80	100	-	74	100	-	dB
Gain Bandwidth (Notes 3,14)	+25°C	20	40	-	20	40	-	MHz
(Notes 4,14)	+25°C	4	8	-	4	8	-	MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 1)	Full	±10.0	±12.0	-	±10.0	±12.0	-	V
Output Current	+25°C	10	20	-	10	20	-	mA
Full Power Bandwidth (Notes 3,5,15)	+25°C	200	500	-	200	500	-	kHz
(Notes 4,5,15)	+25°C	100	200	-	100	200	-	kHz
TRANSIENT RESPONSE								
Rise Time (Notes 4,6)	+25°C	-	20	45	-	20	50	ns
Overshoot (Notes 4,6)	+25°C	-	25	40	-	25	40	%
Slew Rate (Notes 3,7)	+25°C	20	30	-	20	30	-	V/μs
(Notes 4,7,14)	+25°C	6	8	-	6	8	-	V/μs
Settling Time (Notes 4,7,8,14)	+25°C	-	1.5	2.5	-	1.5	2.5	μs
CHANNEL SELECT CHARACTERISTICS								
Digital Input Current ($V_{IN} = 0V$)	Full	-	1	1.5	-	1	1.5	mA
Digital Input Current ($V_{IN} = +5.0V$)	Full	-	5	-	-	5	-	nA
Output Delay (Notes 9,14)	+25°C	-	100	250	-	100	250	ns
Crosstalk (Note 10)	+25°C	-80	-110	-	-74	-110	-	dB
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C	-	4.8	6.0	-	4.8	6.0	mA
Power Supply Rejection Ratio (Note 11)	Full	74	90	-	74	90	-	dB

NOTES:

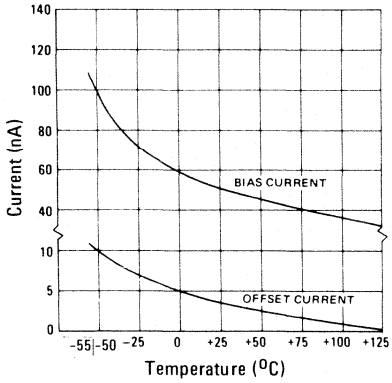
1. $R_L = 2k\Omega$
2. $V_{CM} = \pm 5VDC$
3. $A_V = +10$, $C_{COMP} = 0$, $R_L = 2k\Omega$, $C_L = 50pF$.
4. $A_V = +1$, $C_{COMP} = 15pF$, $R_L = 2k\Omega$, $C_L = 50pF$.
5. $V_{OUT} = 20V$ peak to peak.
6. $V_{OUT} = 200mV$ peak.
7. $V_{OUT} = 10.0V$ peak to peak.
8. To 0.1% of final value.
9. To 10% of final value; output then slews at normal rate to final value.
10. Unselected input to output; $V_{IN} = \pm 10V$ D.C.
11. $V_{SUPPLY} = \pm 10V$ D.C. to $\pm 20V$ D.C.
12. Unselected channels have approximately the same input parameters.
13. Derate by 4.3mW/°C above 105°C.
14. Guaranteed by design.
15. Full Power Bandwidth based on slew rate measurement using:

$$FPBW = \frac{S.R.}{2\pi\ Vpeak}$$

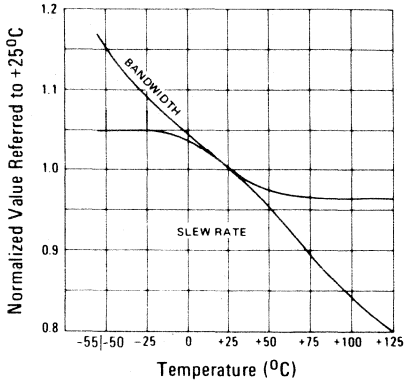
Typical Performance Curves

V+ = +15V D.C., V- = -15V D.C., T_A = +25°C, Unless Otherwise Specified.

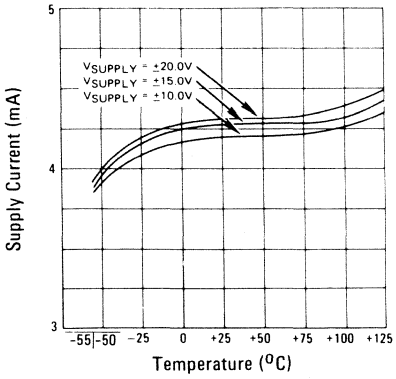
INPUT BIAS CURRENT AND OFFSET CURRENT AS A FUNCTION OF TEMPERATURE



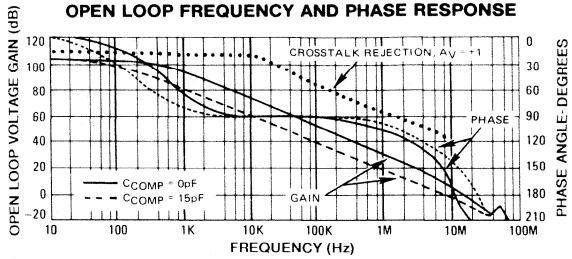
NORMALIZED A.C. PARAMETERS vs. TEMPERATURE



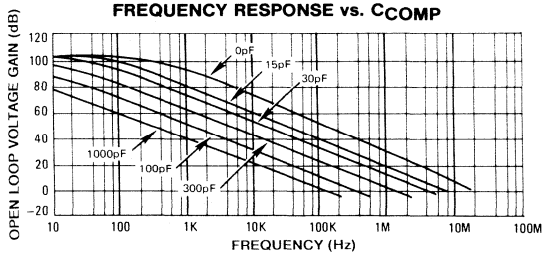
POWER SUPPIY CURRENT DRAIN AS A FUNCTION OF TEMPERATURE



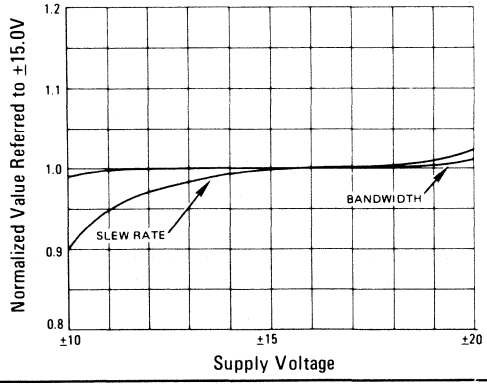
OPEN LOOP FREQUENCY AND PHASE RESPONSE



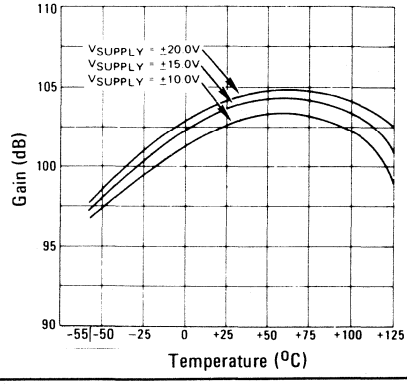
FREQUENCY RESPONSE vs. C_{COMP}



NORMALIZED A.C. PARAMETERS vs. SUPPLY VOLTAGE

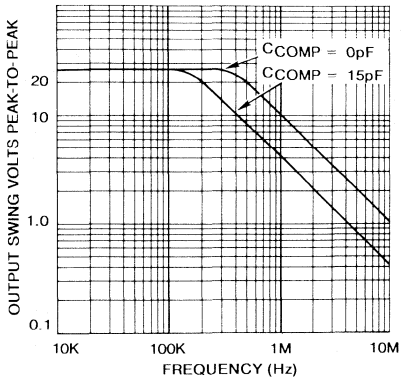


OPEN LOOP VOLTAGE GAIN vs. TEMPERATURE

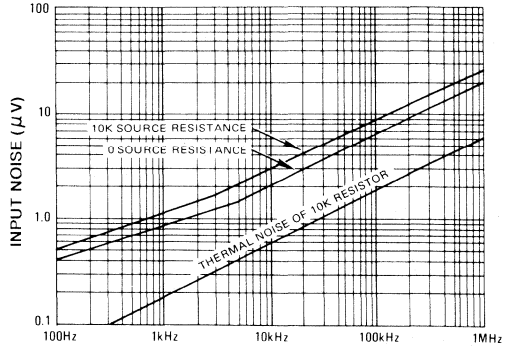


Typical Performance Curves (Continued)

OUTPUT VOLTAGE SWING vs. FREQUENCY

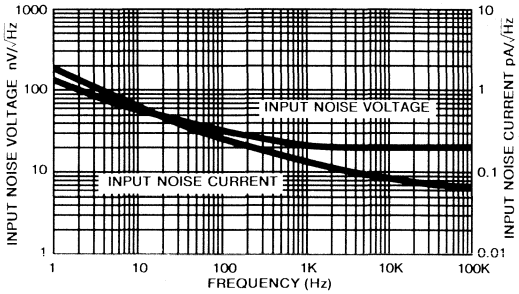


EQUIVALENT INPUT NOISE vs. BANDWIDTH

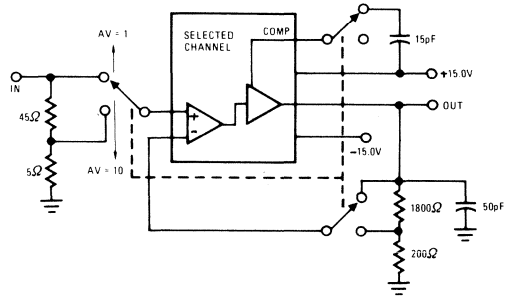


UPPER 3dB FREQUENCY
LOWER 3dB FREQUENCY-10Hz
BROADBAND NOISE CHARACTERISTICS

INPUT NOISE vs. FREQUENCY

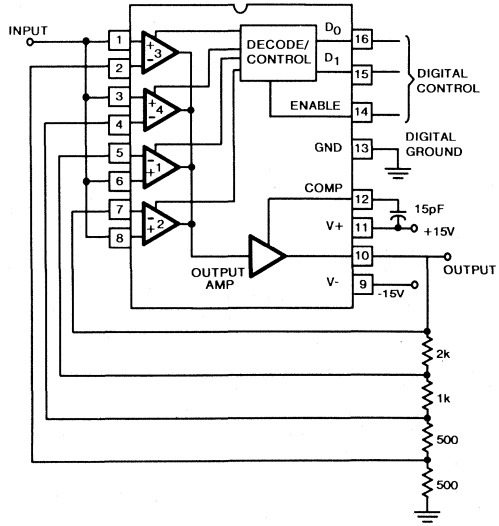


SLEW RATE AND TRANSIENT RESPONSE

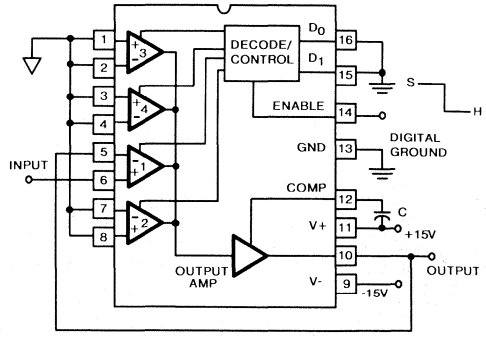


Typical Applications

HA-2400
AMPLIFIER, NON-INVERTING PROGRAMMABLE GAIN



HA-2400
SAMPLE AND HOLD



Sample Charging Rate = $\frac{I_1}{C}$ V/Sec.

Hold Drift Rate = $\frac{I_2}{C}$ V/Sec.

Switch Pedestal Error = $\frac{Q}{C}$ Volts

$I_1 \approx 150 \times 10^{-6}$A
$I_2 \approx 200 \times 10^{-9}$A @ +25°C
$\approx 600 \times 10^{-9}$A @ -55°C
100×10^{-9}A @ +125°C
$Q \approx 2 \times 10^{-12}$ Coul.

For More Examples, See Harris Application Note 514

HA-2406

Digitally Selectable Four Channel Operational Amplifier

Features

- TTL Compatible Inputs
- Single Capacitor Compensation
- Low Crosstalk ..... -110dB
- High Slew Rate 20V/μs
- Low Offset Current 5nA
- Offset Voltage 7mV
- High Gain-Bandwidth 30MHz
- High Input Impedance 30MΩ

Applications

- Digital Control Of:
  - Analog Signal Multiplexing
  - Op Amp Gains
  - Oscillator Frequencies
  - Filter Characteristics
  - Comparator Levels
- For Further Design Ideas See App. Note 514

Description

The HA-2406 is a monolithic device consisting of four op amp input stages that can be individually connected to one output stage by decoding two TTL lines into four channel select signals. In addition to allowing each channel to be addressed, an enable control disconnects all input stages from the output stage when asserted low.

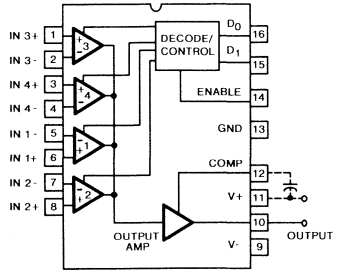
Each input-output combination of the HA-2406 is designed to be a 20V/μs, 30MHz gain-bandwidth amplifier that is stable at a gain of ten but by connecting one external 15pF capacitor all amplifiers are compensated for unity gain operation. The compensation pin may also be used to limit the output swing to TTL levels through suitable clamping diodes and divider networks (see Application Note 514).

Dielectric isolation and short-circuit protected output stages contribute to the quality and durability of the HA-2406 When used as a simple amplifier, its dynamic performance is very good and when its added versatility is considered, the HA-2406 is unmatched in the analog world. It can replace a number of individual components in analog signal conditioning circuits for digital signal processing systems. Its advantages include saving board space and reducing power supply requirements.

The HA-2406 is available in a 16 pin dual-in-line package and is guaranteed for operation over the full commercial temperature range (0°C to +75°C).

Pinout

HA3-2406-5
HA1-2406-5
TOP VIEW



TRUTH TABLE

D1	D0	EN	SELECTED CHANNEL
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4
X	X	L	NONE

Schematic

HA-2406

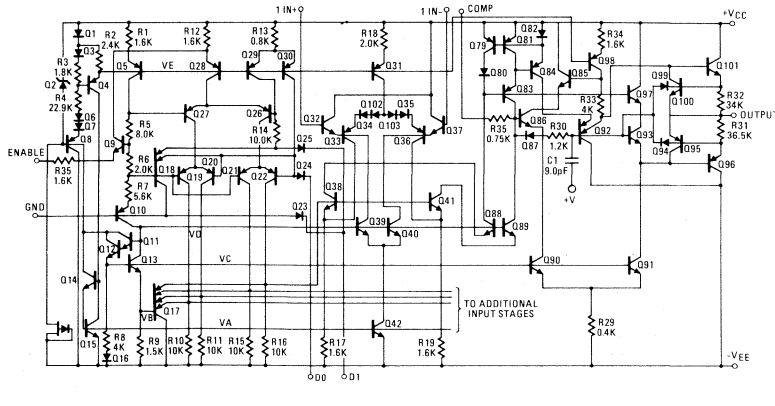


Diagram Includes: One Input Stage, Decode Control, Bias Network, and Output Stage.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 45.0V
Differential Input Voltage ..... $\pm V_{Supply}$
Digital Input Voltage ..... -0.76V to +10.0V
Output Current ..... Short Circuit Protected ($I_{SC} \leq \pm 33mA$)
Internal Power Dissipation 300mW
Operating Temperature Range ..... $0^oC \leq T_A \leq +75^oC$
Storage Temperature Range ..... $-65^oC \leq T_A \leq +150^oC$

Electrical Specifications

Test Conditions: $V_{Supply} = \pm 15.0V$ Unless Otherwise Specified. Digital Inputs: $V_{IL} = +0.5V$, $V_{IH} = +2.4V$. Limits apply to each of the four channels, when addressed.

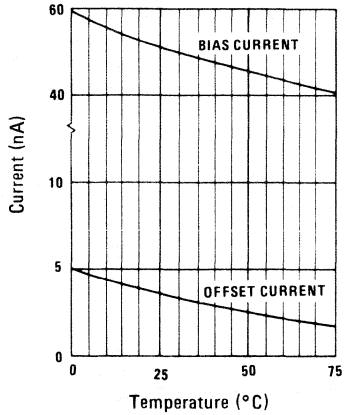
PARAMETER	TEMP	HA-2406 LIMITS MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS					
Offset Voltage	+25°C		7	10	mV
	Full			12	mV
Bias Current (Note 12)	+25°C		50	250	nA
	Full			500	nA
Offset Current (Note 12)	+25°C		5	50	nA
	Full			100	nA
Input Resistance (Note 12)	+25°C		30		MΩ
Common Mode Range	Full	±9.0			V
TRANSFER CHARACTERISTICS					
Large Signal Voltage Gain (Notes 1, 5)	+25°C	40K	150K		V/V
	Full	20K			V/V
Common Mode Rejection Ratio (Note 2)	Full	74	80		dB
Gain Bandwidth (Note 3, 15)	+25°C	15	30		MHz
Gain Bandwidth (Note 4, 15)	+25°C	3	6		MHz
OUTPUT CHARACTERISTICS					
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		V
Output Current (Note 13)	+25°C	10	15		mA
Full Power Bandwidth (Notes 3, 5, 14, 15)	+25°C	240	320		kHz
Full Power Bandwidth (Notes 4, 5, 14)	+25°C	64	95		kHz
TRANSIENT RESPONSE					
Rise Time (Notes 4, 6)	+25°C		30	100	ns
Overshoot (Notes 4, 6)	+25°C		25	40	%
Slew Rate (Notes 3, 7, 15)	+25°C	15	20		V/μs
Slew Rate (Notes 4, 7)	+25°C	4	6		V/μs
Settling Time (Notes 4, 7, 8, 15)	+25°C		2.0	3.5	μs
CHANNEL SELECT CHARACTERISTICS					
Digital Input Current ($V_{IN} = 0V$)	Full		1	1.5	mA
Digital Input Current ($V_{IN} = +5.0V$)	Full		15		nA
Output Delay (Note 9, 15)	+25°C		150	300	ns
Crosstalk (Note 10)	+25°C	-74	-110		dB
POWER SUPPLY CHARACTERISTICS					
Supply Current	+25°C		4.8	7.0	mA
Power Supply Rejection Ratio (Note 11)	Full	74	90		dB

NOTES:
1. $R_L = 2k\Omega$
2. $V_{CM} = \pm 5VDC$
3. $A_V = +10$, $C_{COMP} = 0$, $R_L = 2k\Omega$, $C_L = 50pF$.
4. $A_V = +1$, $C_{COMP} = 15pF$, $R_L = 2k\Omega$, $C_L = 50pF$.
5. $V_{OUT} = 20V$ peak to peak.
6. $V_{OUT} = 200mV$ peak.
7. $V_{OUT} = 10.0V$ peak to peak.
8. To 0.1% of final value.
9. To 10% of final value; output then slews at normal rate to final value.
10. Unselected input to output; $V_{IN} = \pm 10V$ D.C.
11. $V_{SUPPLY} = \pm 10V$ D.C. to $\pm 20V$ D.C.
12. Unselected channels have approximately the same input parameters.
13. $V_{OUT} = \pm 10V$.
14. Full Power Bandwidth based on slew rate measurement using:
$$FPBW = \frac{S.R.}{2\pi \, Vpeak}$$
15. Sample Tested.

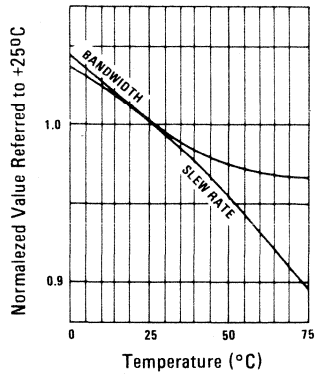
Typical Performance Curves

V+ = +15V D.C., V- = -15V D.C., T_A = +25°C, Unless Otherwise Specified.

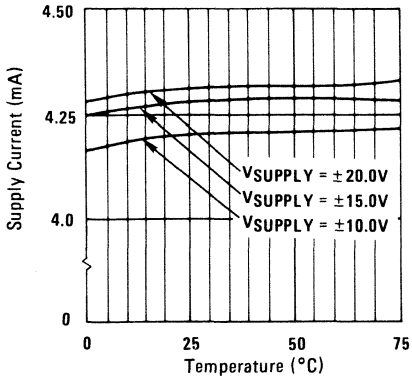
INPUT BIAS CURRENT AND OFFSET CURRENT AS A FUNCTION OF TEMPERATURE



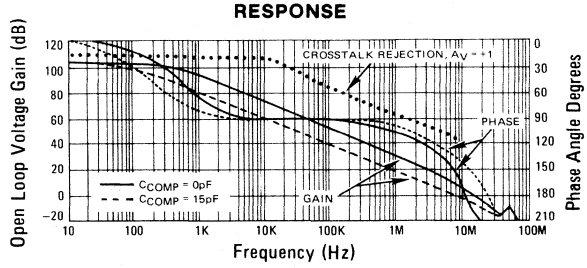
NORMALIZED A. C. PARAMETERS VS. TEMPERATURE



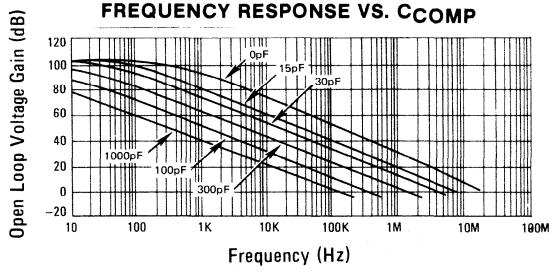
POWER SUPPLY CURRENT DRAIN AS A FUNCTION OF TEMPERATURE



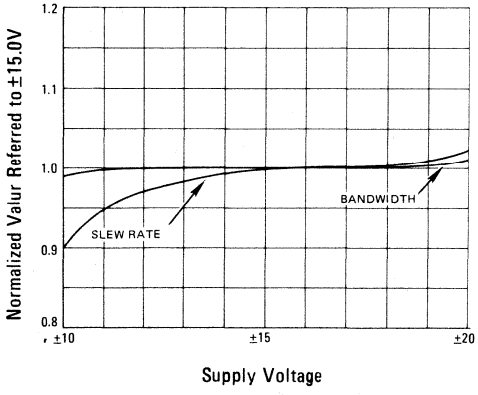
OPEN LOOP FREQUENCY AND PHASE RESPONSE



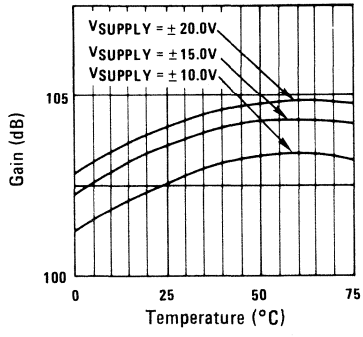
FREQUENCY RESPONSE VS. C_{COMP}



NORMALIZED A. C. PARAMETERS VS. SUPPLY VOLTAGE

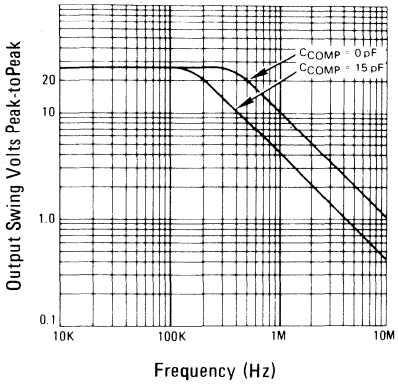


OPEN LOOP VOLTAGE GAIN VS. TEMPERATURE

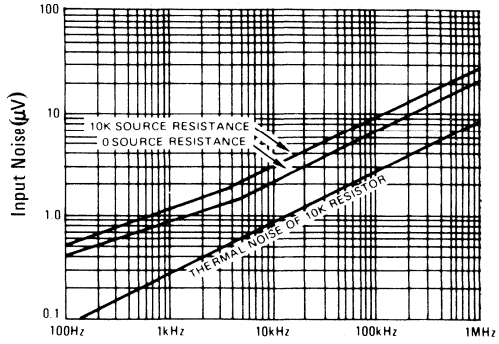


Typical Performance Curves (Continued)

OUTPUT VOLTAGE SWING VS. FREQUENCY

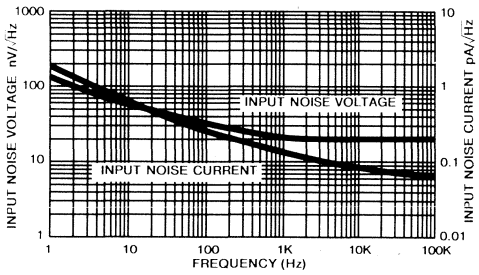


EQUIVALENT INPUT NOISE VS. BANDWIDTH

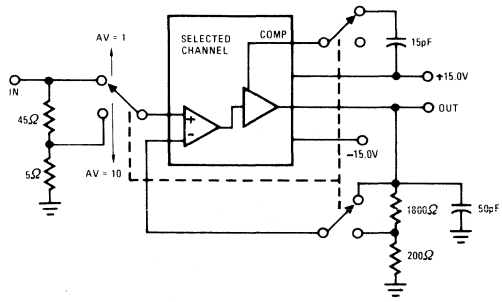


Upper 3dB Frequency
Lower 3dB Frequency - 10Hz
Broadband Noise Characteristics

INPUT NOISE VS. FREQUENCY

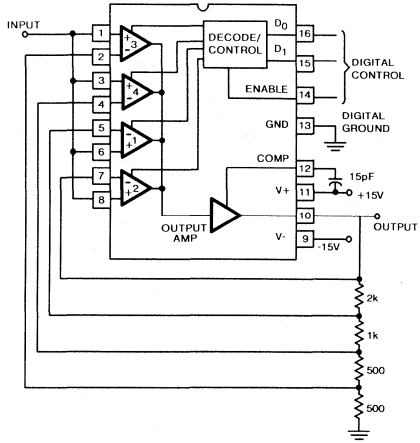


SLEW RATE AND TRANSIENT RESPONSE

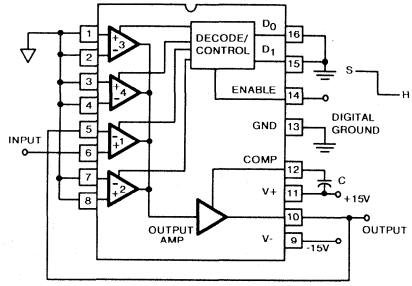


Typical Applications

HA-2406
AMPLIFIER, NON-INVERTING PROGRAMMABLE GAIN



HA-2406
SAMPLE AND HOLD



Sample charging rate = $\frac{I_1}{C}$ V/sec.

Hold drift rate = $\frac{I_2}{C}$ V/sec.

Switch pedestal error = $\frac{Q}{C}$ Volts

$I_1 \approx 150 \times 10^{-6}$ A

$I_2 \approx 200 \times 10^{-9}$ A at +25°C
$\approx 600 \times 10^{-9}$ A at -55°C
$\approx 100 \times 10^{-9}$ A at +125°C

$Q \approx 2 \times 10^{-12}$ Coul.

For more examples, see Harris Application Note 514.

HA-2500/02/05

Precision High Slew Rate Operational Amplifiers

Features

- High Slew Rate 30V/μs
- Fast Settling 330ns
- Wide Power Bandwidth 500KHz
- High Gain Bandwidth 12MHz
- High Input Impedance 50MΩ
- Low Offset Current 10nA
- Internally Compensated For Unity Gain Stability

Applications

- Data Acquisition Systems
- R.F. Amplifiers
- Video Amplifiers
- Signal Generators
- Pulse Amplification

Description

HA-2500/2502/2505 comprises a series of monolithic operational amplifiers whose designs are optimized to deliver excellent slew rate, bandwidth, and settling time specifications. The outstanding dynamic features of this internally compensated device are complemented with low offset voltage and offset current.

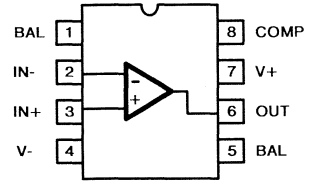
These dielectrically isolated amplifiers are ideally suited for applications such as data acquisition, R.F., video, and pulse conditioning circuits. Slew rates of $\pm$25V/μs and 330ns (0.1%) settling time make these devices excellent components in fast, accurate data acquisition and pulse amplification designs. 12MHz small signal bandwidth and 500kHz power bandwidth make these devices well suited to R.F. and video applications. With 2mV typical offset voltage plus offset trim capability and 10nA offset current, HA-2500/2502/2505 are particularly useful components in signal conditioning designs.

The gain and offset voltage figures of the HA-2500 series are optimized by internal component value changes while the similar design of the HA-2510 series is maximized for slew rate.

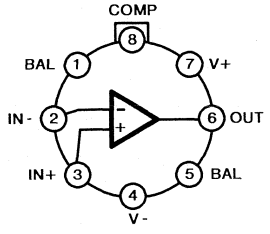
The HA-2500 and HA-2502 have guaranteed operation from -55°C to +125°C and are available in hermetic metal can and ceramic miniDIP packages. Both are offered as a /883 military grade part with the HA-2502 also available in LCC package. The HA-2505 has guaranteed operation from 0°C to +75°C and is available in plastic and ceramic miniDIP and metal can packages. Mil-Std-883 product and data sheets are available upon request.

Pinouts

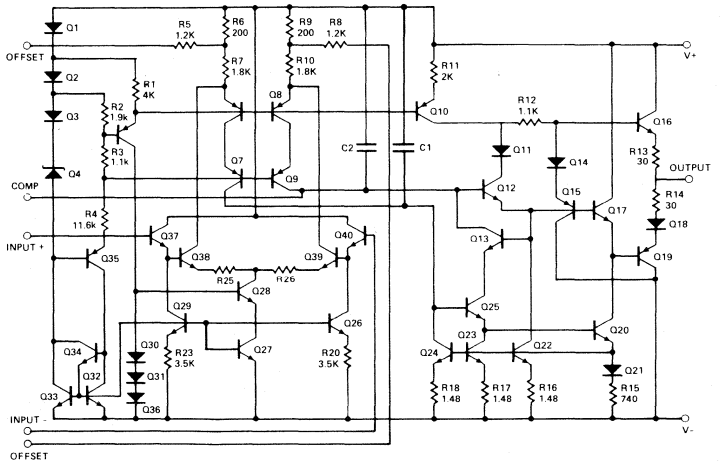
HA7-2500/02/02 (CERAMIC MINI-DIP)
HA3-2505 (PLASTIC MINI-DIP)
TOP VIEW



HA2-2500/02/05 (TO-99 METAL CAN)
TOP VIEW



Schematic



CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

Absolute Maximum Ratings (Note 6)

Voltage Between V+ and V- Terminals 40.0V
Differential Input Voltage ..... ±15.0V
Peak Output Current 50mA
Internal Power Dissipation 300mW
Lead Solder Temperature (10 Seconds) ..... +275°C

Operating Temperature Range
HA-2510/2512 ..... $-55^{\circ}C \leq T_A \leq +125^{\circ}C$
HA-2515 ..... $0^{\circ}C \leq T_A \leq +75^{\circ}C$
Storage Temperature Range ..... $-65^{\circ}C \leq T_A \leq +150^{\circ}C$
Maximum Junction Temperature ..... +175°C

Electrical Specifications V+ =+15V D.C., V- = -15V D.C.

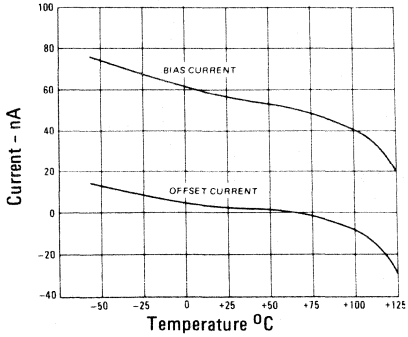
PARAMETER	TEMP.	HA-2500 -55°C to +125°C			HA-2502 -55°C to +125°C			HA-2505 0°C to +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS											
Offset Voltage	+25°C		2	5		4	8		4	8	mV
	Full			8			10			10	mV
Offset Voltage Average Drift	Full		20			20			20		µV/°C
Bias Current	+25°C		100	200		125	250		125	250	nA
	Full			400			500			500	nA
Offset Current	+25°C		10	25		20	50		20	50	nA
	Full			50			100			100	nA
Input Resistance (Note 10)	+25°C	25	50		20	50		20	50		MΩ
Common Mode Range	Full	±10.0			±10.0			±10.0			V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Note 1, 4)	+25°C	20K	30K		15K	25K		15K	25K		V/V
	Full	15K			10K			10K			V/V
Common Mode Rejection Ratio (Note 2)	Full	80	90		74	90		74	90		dB
Gain Bandwidth Product (Note 3)	+25°C		12			12			12		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
Output Current (Note 4)	+25°C	±10	±20		±10	±20		±10	±20		mA
Full Power Bandwidth (Notes 4,11)	+25°C	350	500		300	500		300	500		KHz
TRANSIENT RESPONSE											
Rise Time (Notes 1, 5, 7 & 8)	+25°C		25	50		25	50		25	50	ns
Overshoot (Notes 1, 5, 7 & 8)	+25°C		25	40		25	50		25	50	%
Slew Rate (Notes 1, 5, 8 & 12)	+25°C	±25	±30		±20	±30		±20	±30		V/µs
Settling Time to 0.1% (Notes 1, 5, 8 & 12)	+25°C		0.33			0.33			0.33		µs
POWER SUPPLY CHARACTERISTICS											
Supply Current	+25°C		4	6		4	6		4	6	mA
Power Supply Rejection Ratio (Note 9)	Full	80	90		74	90		74	90		dB

NOTES:
1. $R_L = 2K\Omega$
2. $V_{CM} = \pm 10V$
3. $A_V > 10$
4. $V_O = \pm 10.0V$
5. $C_L = 50pF$
6. Absolute Maximum Ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired.
7. $V_O = \pm 200mV$
8. See Transient Response Test Circuits and Waveforms.
9. $\Delta V = \pm 5.0V$
10. This parameter value is based on design calculations.
11. Full Power Bandwidth guaranteed based on slew rate measurement using: $FPBW = S.R./2\pi V_{peak}$.
12. $V_{OUT} = \pm 5V$.

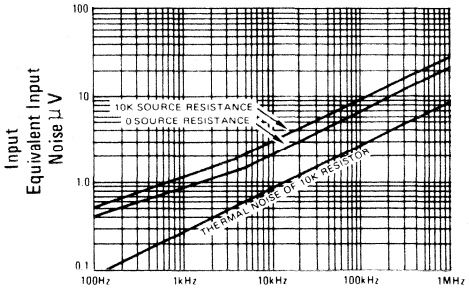
Performance Curves

$V+ = +15VDC$, $V- = -15VDC$, $T_A = +25^oC$, Unless Otherwise Stated

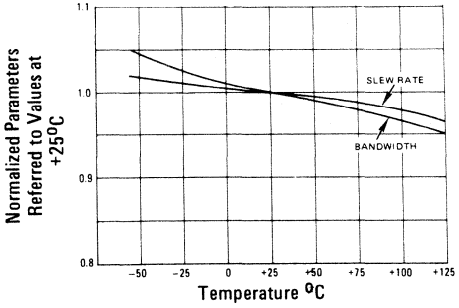
INPUT BIAS AND OFFSET CURRENT vs TEMPERATURE



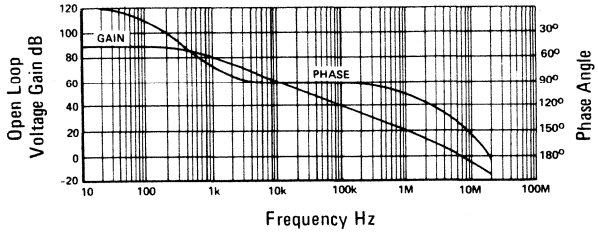
EQUIVALENT INPUT NOISE vs BANDWIDTH



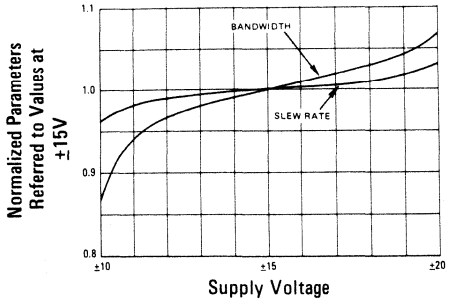
NORMALIZED AC PARAMETERS vs TEMPERATURE



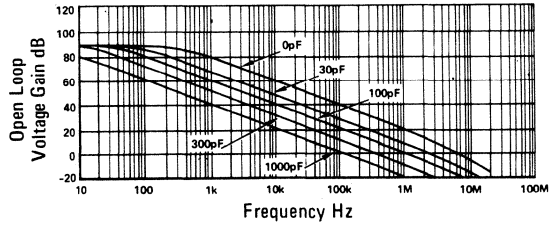
OPEN-LOOP FREQUENCY AND PHASE RESPONSE



NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE AT +25°C

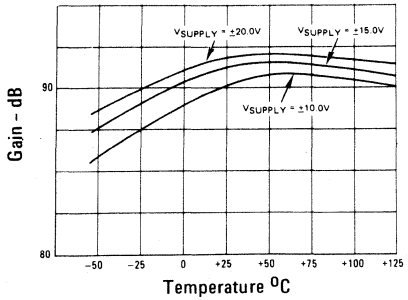


OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMPENSATION PIN TO GROUND

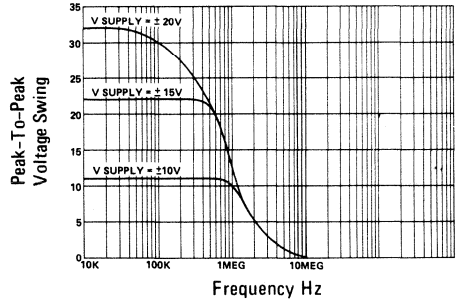


NOTE: External compensation components are not required for stability, but may be added to reduce bandwidth if desired.

OPEN LOOP VOLTAGE GAIN vs TEMPERATURE

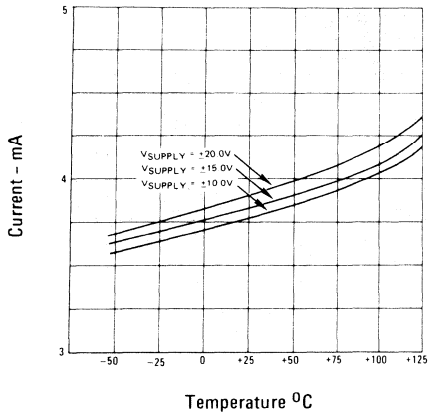


OUTPUT VOLTAGE SWING vs FREQUENCY AT +25°C

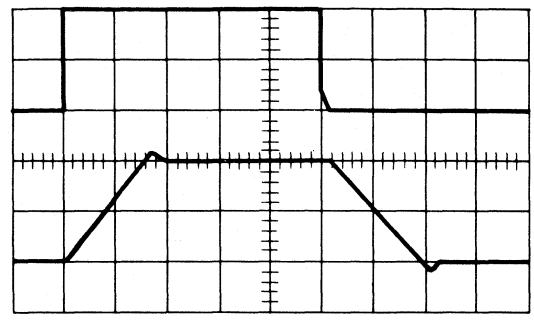


Typical Performance Curves (Continued)

POWER SUPPLY CURRENT vs TEMPERATURE



VOLTAGE FOLLOWER PULSE RESPONSE

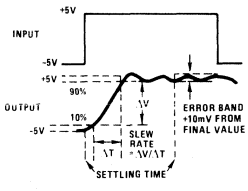


R_L = 2KΩ, C_L = 50pF
Upper Trace: Input
Lower Trace: Output

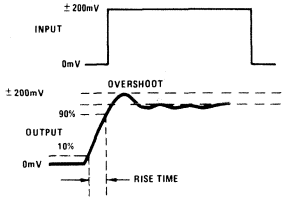
Vertical = 5V/Div.
Horizontal = 200ns/Div.
T_A = +25°C, V_S = ±15.0V

Test Circuits

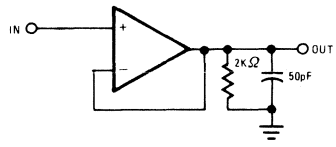
SLEW RATE AND SETTLING TIME



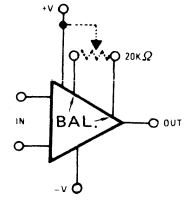
TRANSIENT RESPONSE



SLEW RATE AND TRANSIENT RESPONSE



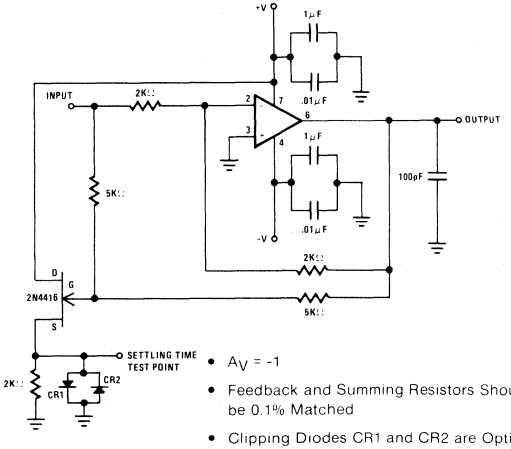
SUGGESTED VOS ADJUSTMENT



NOTE: Measurement on both positive and negative transitions from 0V to +200mV and 0V to -200mV at the output.

Tested Offset Adjustment Range is $|V_{OS} + 1mV|$ minimum referred to output. Typical ranges is ±8mV with R_T = 20kΩ.

Settling Time Circuit



- A_V = -1
- Feedback and Summing Resistors Should be 0.1% Matched
- Clipping Diodes CR1 and CR2 are Optional. HP5082-2810 Recommended

Die Characteristics

Transistor Count 40
Die Dimensions ..... 57 x 65 x 19 mils
Substrate Potential ..... Unbiased
Process ..... Bipolar-DI

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
HA2- Metal Can (-2, -5, -7)	202	56
HA2- Metal Can (-8, /883)	168	52
HA3- Plastic Mini-DIP (-5)	84	34
HA4- Ceramic LCC (/883)	97	35
HA7- Ceramic Mini-DIP (-8, /883)	138	63
HA7- Ceramic Mini-DIP (-2, -5, -7)	204	112

HA-2510/12/15

High Slew Rate Operational Amplifiers

Features

- High Slew Rate 60V/μs
- Fast Settling 250ns
- Wide Power Bandwidth 1,000KHz
- High Gain Bandwidth 12MHz
- High Input Impedance 100MΩ
- Low Offset Current 10nA
- Internally Compensated For Unity Gain Stability

Applications

- Data Acquisition Systems
- R.F. Amplifiers
- Video Amplifiers
- Signal Generators
- Pulse Amplification

Description

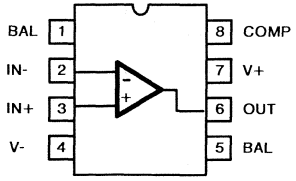
HA-2510/2512/2515 are a series of high performance operational amplifiers which set the standards for maximum slew rate, highest accuracy and widest bandwidths for internally compensated monolithic devices. In addition to excellent dynamic characteristics, these dielectrically isolated amplifiers also offer low offset current and high input impedance.

The ±60V/μs slew rate and 250ns (0.1%) settling time of these amplifiers is ideally suited for high speed D/A, A/D, and pulse amplification designs. HA-2510/2512/2515's superior 12MHz gain bandwidth and 1000kHz power-bandwidth is extremely useful in R.F. and video applications. For accurate signal conditioning these amplifiers also provide 10nA offset current, coupled with 100MΩ input impedance, and offset trim capability.

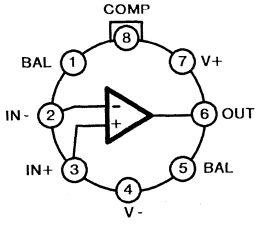
The HA-2510 and HA-2512 have guaranteed operation from -55°C to +125°C and are available in metal can and ceramic miniDIP packages. Both are offered as a /883 military grade part with the HA-2512 also available in LCC package. The HA-2515 has guaranteed operation from 0°C to +75°C and is available in plastic and ceramic miniDIP and metal can packages. Mil-Std-883 product and data sheets are available upon request.

Pinouts

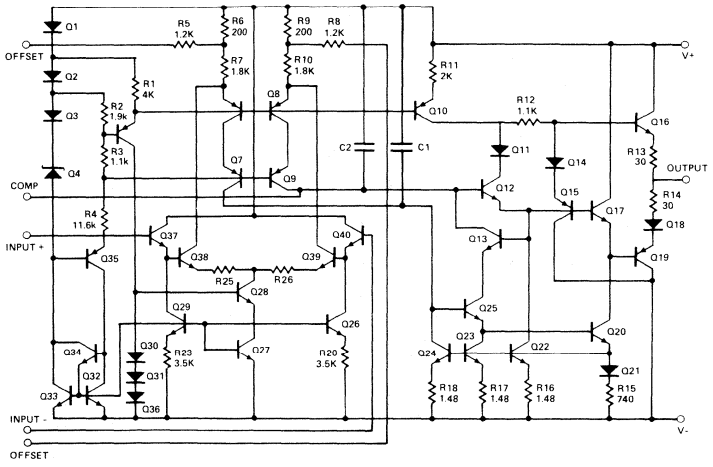
HA7-2510/12/15 (CERAMIC MINI-DIP)
HA3-2515 (PLASTIC MINI-DIP)
TOP VIEW



HA2-2510/12/15 (TO-99 METAL CAN)
TOP VIEW



Schematic



CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

Absolute Maximum Ratings (Note 6)

Voltage Between V+ and V- Terminals 40.0V
Differential Input Voltage ..... ±15.0V
Peak Output Current 50mA
Internal Power Dissipation 300mW
Lead Solder Temperature (10 Seconds) ..... +275°C

Operating Temperature Range
HA-2510/2512 ..... $-55°C \leq T_A \leq +125°C$
HA-2515 ..... $0°C \leq T_A \leq +75°C$
Storage Temperature Range ..... $-65°C \leq T_A \leq +150°C$
Maximum Junction Temperature ..... +175°C

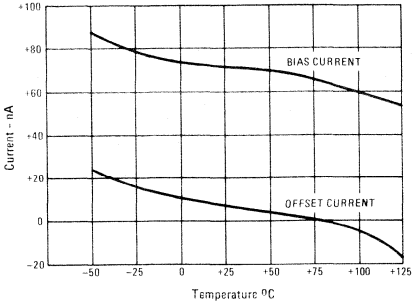
Electrical Specifications V+ =+15V D.C., V- = -15V D.C.

PARAMETER	TEMP.	HA-2510 -55°C to +125°C			HA-2512 -55°C to +125°C			HA-2515 0°C to +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS											
Offset Voltage	+25°C		4	8		5	10		5	10	mV
	Full			11			14			14	mV
Offset Voltage Average Drift	Full		20			25			30		µV/°C
Bias Current	+25°C		100	200		125	250		125	250	nA
	Full			400			500			500	nA
Offset Current	+25°C		10	25		20	50		20	50	nA
	Full			50			100			100	nA
Input Resistance (Note 10)	+25°C	50	100		40	100		40	100		MΩ
Common Mode Range	Full	±10.0			±10.0			±10.0			V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Note 1, 4)	+25°C	10K	15K		7.5K	15K		7.5K	15K		V/V
	Full	7.5K			5K			5K			V/V
Common Mode Rejection Ratio (Note 2)	Full	80	90		74	90		74	90		dB
Gain Bandwidth Product (Note 3)	+25°C		12			12			12		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
Output Current (Note 4)	+25°C	±10	±20		±10	±20		±10	±20		mA
Full Power Bandwidth (Note 4, 11)	+25°C	750	1000		600	1000		600	1000		kHz
TRANSIENT RESPONSE											
Rise Time (Notes 1, 5, 7 & 8)	+25°C		25	50		25	50		25	50	ns
Overshoot (Notes 1, 5, 7 & 8)	+25°C		25	40		25	50		25	50	%
Slew Rate (Notes 1, 5, 8 & 12)	+25°C	±50	±65		±40	±60		±40	±60		V/µs
Settling Time (Notes 1, 5, 8 & 12)	+25°C		0.25			0.25			0.25		µs
POWER SUPPLY CHARACTERISTICS											
Supply Current	+25°C		4	6		4	6		4	6	mA
Power Supply Rejection Ratio	Full	80	90		74	90		74	90		dB

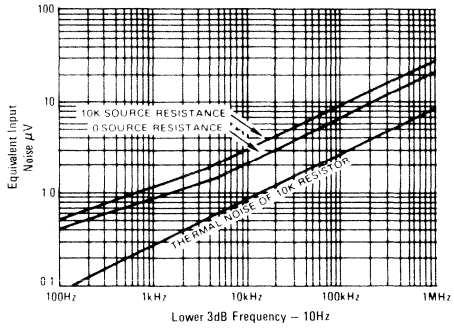
NOTES:
1. $R_L = 2K\Omega$
2. $V_{CM} = \pm 10V$
3. $A_V > 10$
4. $V_O = \pm 10.0V$
5. $C_L = 50pF$
6. Absolute Maximum Ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired.
7. $V_O = \pm 200mV$
8. See Transient Response Test Circuits and Waveforms.
9. $\Delta V = \pm 5.0V$
10. This parameter value is based on design calculations.
11. Full Power Bandwidth guaranteed based on slew rate measurement using: $FPBW = S.R./2\pi V_{peak}$.
12. $V_{OUT} = \pm 5V$.

$V_S = \pm 15V$ D.C., $T_A = +25^oC$ Unless Otherwise Stated

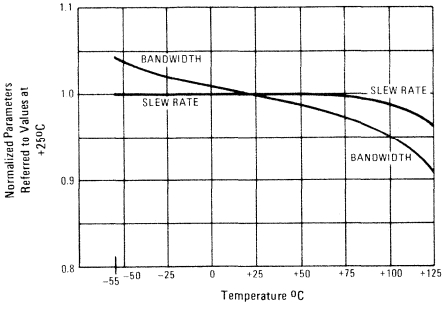
INPUT BIAS AND OFFSET CURRENT vs. TEMPERATURE



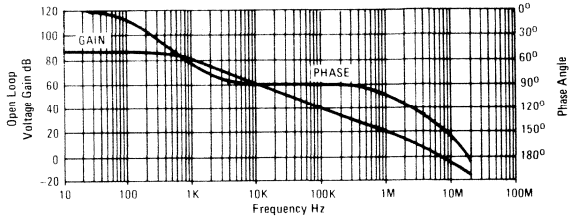
EQUIVALENT INPUT NOISE vs. BANDWIDTH



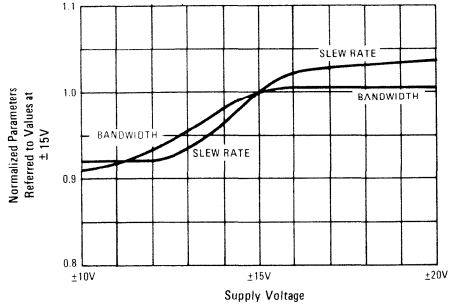
NORMALIZED AC PARAMETERS vs. TEMPERATURE



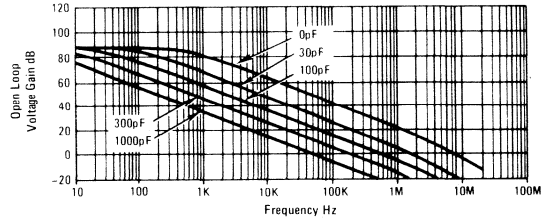
OPEN LOOP FREQUENCY AND PHASE RESPONSE



NORMALIZED AC PARAMETERS vs. SUPPLY VOLTAGE

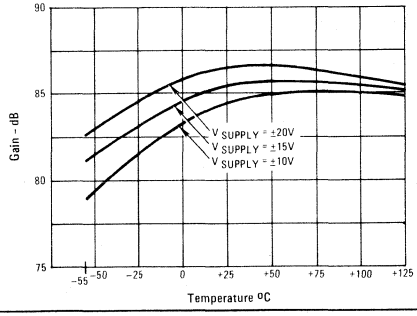


OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMPENSATION PIN TO GROUND

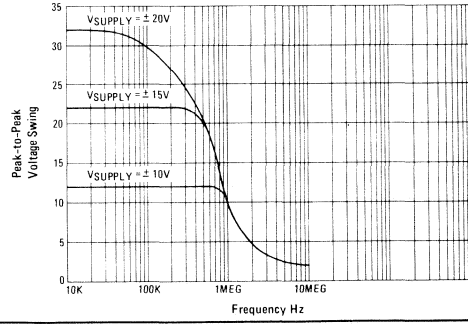


NOTE: External compensation components are not required for stability, but may be added to reduce bandwidth if desired.

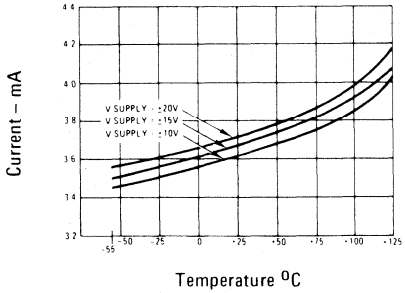
OPEN LOOP VOLTAGE GAIN vs. TEMPERATURE



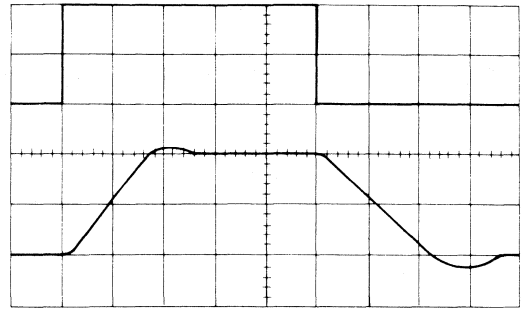
OUTPUT VOLTAGE SWING vs. FREQUENCY AT +25°C



POWER SUPPLY CURRENT VS TEMPERATURE



VOLTAGE FOLLOWER PULSE RESPONSE

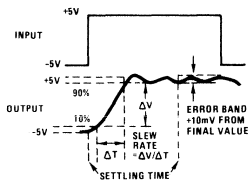


R_L = 2KΩ, C_L = 50pF
Upper Trace: Input
Lower Trace: Output

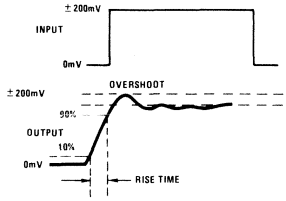
Vertical = 5V/Div.
Horizontal = 100ns/Div.
T_A = +25°C, V_S = ±15.0V

Test Circuits

SLEW RATE AND SETTLING TIME

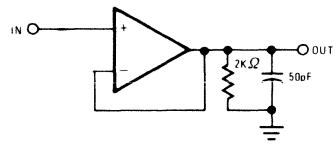


TRANSIENT RESPONSE

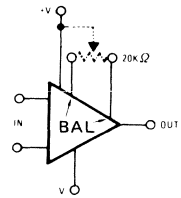


NOTE: Measurement on both positive and negative transitions from 0V to +200mV and 0V to -200mV at the output.

SLEW RATE AND TRANSIENT RESPONSE

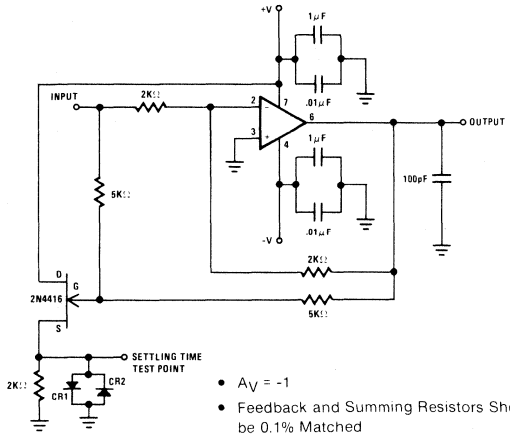


SUGGESTED VOS ADJUSTMENT



Tested Offset Adjustment Range is $|V_{OS} \pm 1mV|$ minimum referred to output. Typical ranges is ±8mV with R_T = 20kΩ.

Settling Time Circuit



- A_V = -1
- Feedback and Summing Resistors Should be 0.1% Matched
- Clipping Diodes CR1 and CR2 are Optional. HP5082-2810 Recommended

Die Characteristics

Transistor Count 40
Die Dimensions ..... 57 x 65 x 19 mils
Substrate Potential ..... Unbiased
Process ..... Bipolar-DI

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
HA2- Metal Can (-2, -5, -7)	202	56
HA2- Metal Can (-8, /883)	168	52
HA3- Plastic Mini-DIP (-5)	84	34
HA4- Ceramic LCC (/883)	97	35
HA7- Ceramic Mini-DIP (-8, /883)	138	63
HA7- Ceramic Mini-DIP (-2, -5, -7)	204	112

HA-2520/22/25

Uncompensated High Slew Rate Operational Amplifiers

Features

- High Slew Rate 120V/μs
- Fast Settling 200ns
- Wide Power Bandwidth 2,000kHz
- High Gain Bandwidth ($A_V \geq 3$) 20MHz
- High Input Impedance 100MΩ
- Low Offset Current 10nA

Applications

- Data Acquisition Systems
- R.F. Amplifiers
- Video Amplifiers
- Signal Generators
- Pulse Amplification

Description

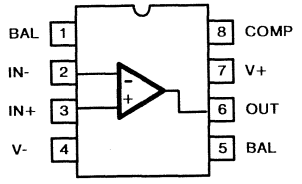
HA-2520/2522/2525 comprise a series of monolithic operational amplifiers delivering an unsurpassed combination of specifications for slew rate, bandwidth and settling time. These dielectrically isolated amplifiers are controlled at close loop gains greater than 3 without external compensation. In addition, these high performance components also provide low offset current and high input impedance.

120V/μs slew rate and 200ns (0.2%) settling time of these amplifiers make them ideal components for pulse amplification and data acquisition designs. These devices are valuable components for R.F. and video circuitry requiring up to 20MHz gain bandwidth and 2MHz power bandwidth. For accurate signal conditioning designs the HA-2520/2522/2525's superior dynamic specifications are complimented by 10nA offset current, 200MΩ input impedance and offset trim capability.

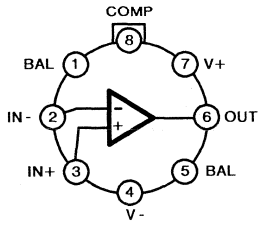
The HA-2520 and HA-2522 have guaranteed operation from -55°C to +125°C and are available in metal can and ceramic miniDIP packages. Both are offered in /883 grade with the HA-2522 also available in LCC package. The HA-2525 has guaranteed operation from 0°C to +75°C and is available in plastic and ceramic miniDIP and metal can packages. Mil-Std-883 product and data sheets are available upon request.

Pinouts

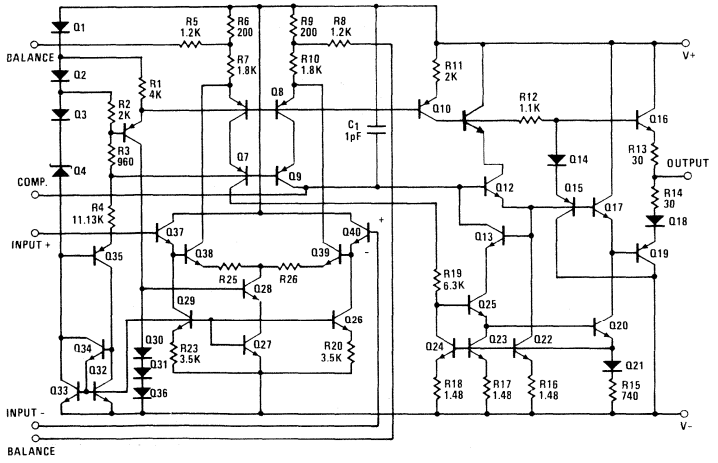
HA7-2520/22/25 (CERAMIC MINI-DIP)
HA3-2525 (PLASTIC MINI-DIP)
TOP VIEW



HA2-2520/22/25 (TO-99 METAL CAN)
TOP VIEW



Schematic



CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

Absolute Maximum Ratings (Note 13)

Voltage Between V+ and V- Terminals 40.0V
Differential Input Voltage ..... ±15.0V
Peak Output Current 50mA
Internal Power Dissipation 300mW
Lead Solder Temperature (10 Seconds) ..... +275°C

Operating Temperature Range
HA-2520/2522 ..... $-55°C \leq T_A \leq +125°C$
HA-2525 ..... $0°C \leq T_A \leq +75°C$
Storage Temperature Range ..... $-65°C \leq T_A \leq +150°C$
Maximum Junction Temperature ..... +175°C

Electrical Specifications

V+ =+15V D.C., V- = -15V D.C.

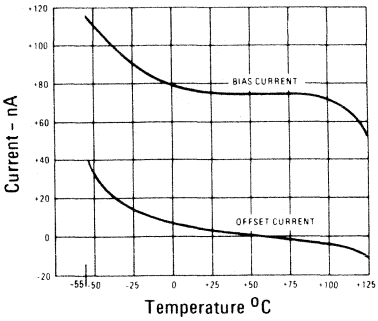
PARAMETER	TEMP	HA-2520 -55°C to +125°C			HA-2522 -55°C to +125°C			HA-2525 0°C to +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS											
Offset Voltage	+25°C		4	8		5	10		5	10	mV
	Full			11			14			14	mV
Offset Voltage Average Drift	Full		20			25			30		µV/°C
Bias Current	+25°C		100	200		125	250		125	250	nA
	Full			400			500			500	nA
Offset Current	+25°C		10	25		20	50		20	50	nA
	Full			50			100			100	nA
Input Resistance (Note 9)	+25°C	50	100		40	100		40	100		MΩ
Common Mode Range	Full	± 10.0			± 10.0			± 10.0			V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Note 1, 4)	+25°C	10K	15K		7.5K	15K		7.5K	15K		V/V
	Full	7.5K			5K			5K			V/V
Common Mode Rejection Ratio (Note 2)	Full	80	90		74	90		74	90		dB
Gain Bandwidth Product (Notes 3, 12)	+25°C	10	20		10	20		10	20		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	± 10.0	± 12.0		± 10.0	± 12.0		± 10.0	± 12.0		V
Output Current (Note 4)	+25°C	± 10	± 20		± 10	± 20		± 10	± 20		mA
Full Power Bandwidth (Notes 4, 10)	+25°C	1500	2000		1200	1600		1200	1600		kHz
TRANSIENT RESPONSE (A_V = +3)											
Rise Time (Notes 1, 5, 6 & 8)	+25°C		25	50		25	50		25	50	ns
Overshoot (Notes 1, 5, 6 & 8)	+25°C		25	40		25	50		25	50	%
Slew Rate (Notes 1, 5, 8 & 11)	+25°C	± 100	± 120		± 80	± 120		± 80	± 120		V/µs
Settling Time (Notes 1, 5, 8 &11)	+25°C		0.20			0.20			0.20		µs
POWER SUPPLY CHARACTERISTICS											
Supply Current	+25°C		4	6		4	6		4	6	mA
Power Supply Rejection Ratio (Note 7)	Full	80	90		74	90		74	90		dB

NOTES:

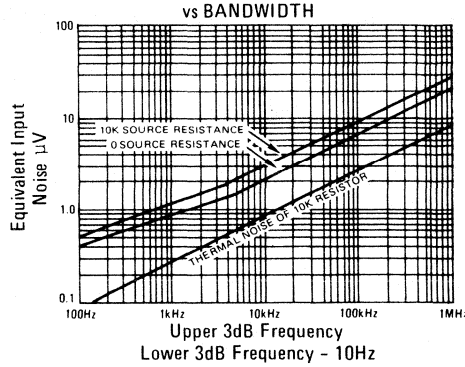
1. $R_L = 2k\Omega$
2. $V_{CM} = \pm 10V$
3. $A_V > 10$
4. $V_O = \pm 10.0V$
5. $C_L = 50pF$
6. $V_O = \pm 200mV$
7. $\Delta V = \pm 5.0V$
8. See Transient Response Test Circuits and Waveforms.
9. This parameter value is based on design calculations.
10. Full Power Bandwidth guaranteed based on slew rate measurement using: $FPBW = S.R./2\pi V_{peak}$.
11. $V_{OUT} = \pm 5V$
12. Guaranteed by design.
13. Absolute Maximum Ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.

$V_S = \pm 15V$ D.C., $T_A = +25^oC$ Unless Otherwise Stated

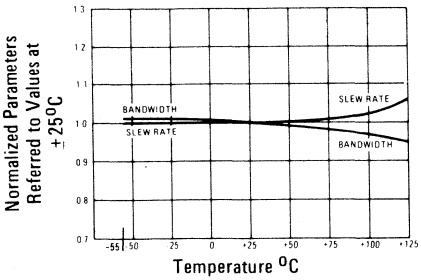
INPUT BIAS AND OFFSET CURRENT vs TEMPERATURE



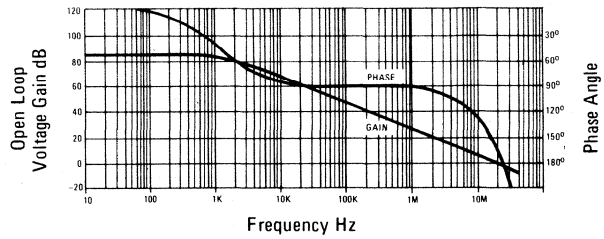
EQUIVALENT INPUT NOISE vs BANDWIDTH



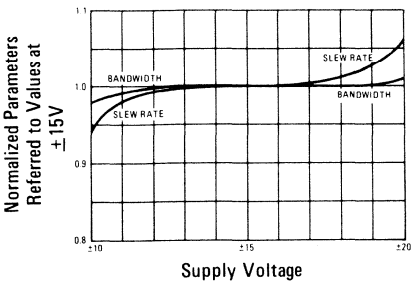
NORMALIZED AC PARAMETERS vs TEMPERATURE



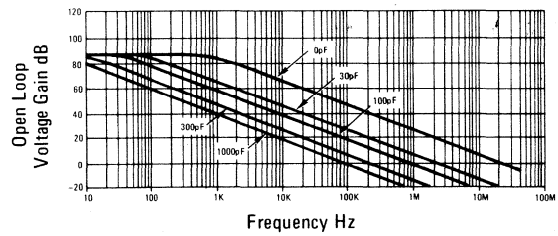
OPEN-LOOP FREQUENCY AND PHASE RESPONSE



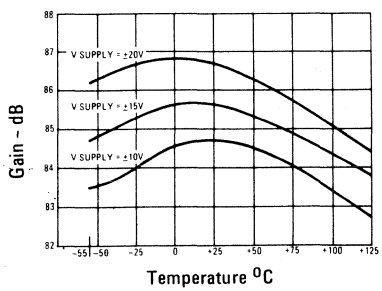
NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE AT +25°C



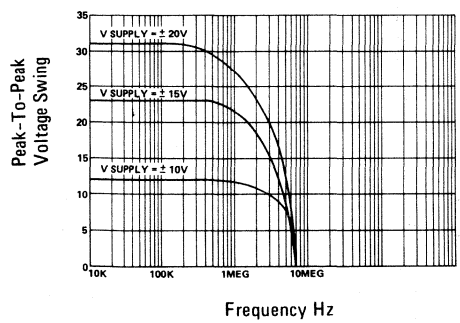
OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM BANDWIDTH CONTROL PIN TO GROUND



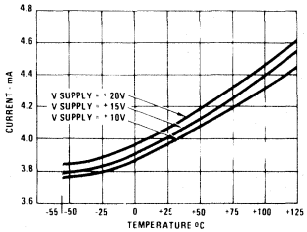
OPEN LOOP VOLTAGE GAIN vs TEMPERATURE



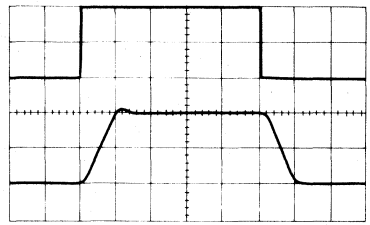
OUTPUT VOLTAGE SWING vs FREQUENCY AT +25°C



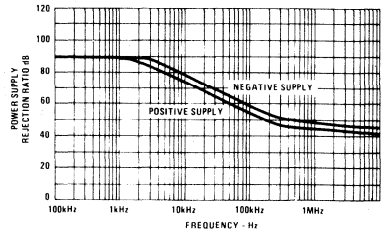
POWER SUPPLY CURRENT VS TEMPERATURE



VOLTAGE FOLLOWER PULSE RESPONSE



POWER SUPPLY REJECTION RATIO VS FREQUENCY

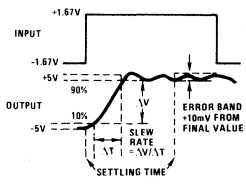


R_L = 2KΩ, C_L = 50pF
Upper Trace: Input; 1.67V/Div.
Lower Trace: Output; 5V/Div.

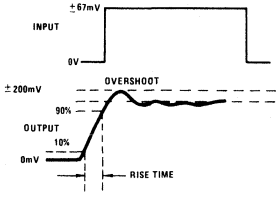
Horizontal = 100ns/Div.
T_A = +25°C, V_S = ±15V

Test Circuits

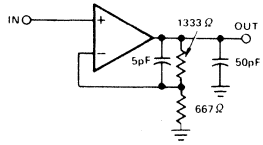
SLEW RATE AND SETTLING TIME



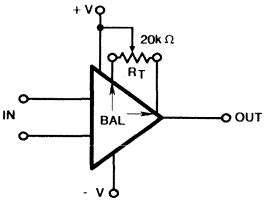
TRANSIENT RESPONSE



SLEW RATE AND TRANSIENT RESPONSE



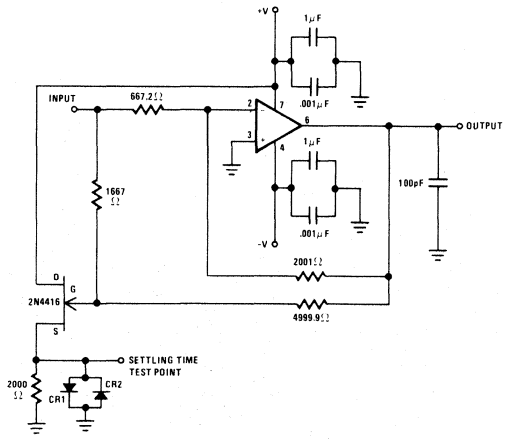
SUGGESTED VOS ADJUSTMENT



NOTE: Measurement on both positive and negative transitions from 0V to +200mV and 0V to -200mV at the output.

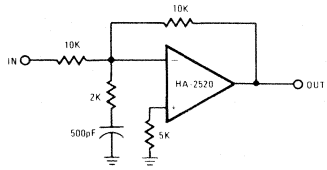
Tested Offset Adjustment Range is $|V_{OS}$ +1mV| minimum referred to output. Typical range is +20mV to -18mV with R_T = 20kΩ.

Settling Time Circuit



- A_V = -3
- Feedback and Summing Resistor Ratios Should be 0.1% matched.
- Clipping Diodes CR1 and CR2 are Optional. HP5082-2810 Recommended.

Typical Application

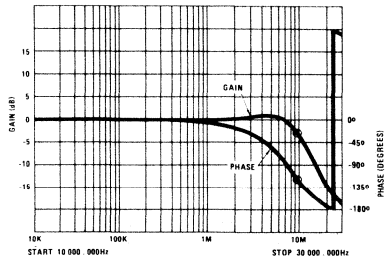


NOTE: Compensation Circuit for $A_V = -1$
Slew Rate ≈120V/μs
Bandwidth ≈ 10MHz
Settling Time (0.1%) ≈ 500ns

Capacitance at pin 8 must be minimized for maximum bandwidth.

Tested and functional with supply voltages from ±4V to ±15V.

FREQUENCY RESPONSE FOR INVERTING UNITY GAIN CIRCUIT



Die Characteristics

Transistor Count 40
Die Dimensions ..... 50 x 65 x 19 mils
Substrate Potential ..... Unbiased
Process ..... Bipolar-DI

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
HA2- Metal Can (-2, -5, -7)	206	56
HA2- Metal Can (-8, /883)	168	52
HA3- Plastic Mini-DIP (-5)	90	39
HA4- Ceramic LCC (/883)	99	37
HA7- Ceramic Mini-DIP (-8, /883)	140	65
HA7- Ceramic Mini-DIP (-2, -5, -7)	204	112

HARRIS

HA-2529

Uncompensated, High Slew Rate High Output Current, Operational Amplifier

Features

- High Slew Rate 150V/μs
- Fast Settling 200ns
- Wide Power Bandwidth 2MHz
- Wide Gain Bandwidth ($A_V \geq 3$) 20MHz
- High Input Impedance 130MΩ
- Low Offset Current 200nA
- High Output Current ..... ±30mA

Applications

- Data Acquisition Systems
- R.F. Amplifiers
- Video Amplifiers
- Signal Generators
- Pulse Amplification

Description

The HA-2529 is a monolithic operational amplifier which typifies excellence of design. With a design based on years of experience coupled with the reliable dielectric isolation process, these amplifiers provide an outstanding combination of DC and AC parameters at closed loop gains greater than 3.

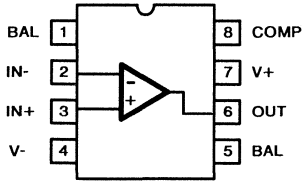
The HA-2529 offers 150V/μs slew rate and fast settling time (200ns), while consuming a mere 6mA of quiesent current, making these amplifiers ideal components for video circuitry and data acquisition designs. With 20MHz gain-bandwidth combined with 7.5kV/V open loop gain, the HA-2529 is an ideal component for demanding signal conditioning designs.These devices provide ±30mA output current drive with an output voltage swing of ±10V making then suited for pulse amplifier and R.F. amplifier components.

The HA-2529 will upgrade output current, slew rate, offset voltage drift and offset current drift in systems presently using the HA-2520/22/25 or EHA-2520/22/25.

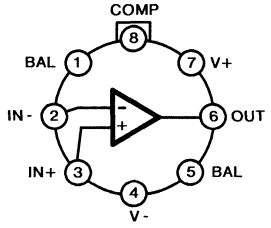
The HA-2529-2 has guaranteed operation over the military temperature range (-55°C to +125°C) and the HA-2529-5 has guaranteed operation over the commercial temperature range (0°C to +75°C). MIL-STD-883 product and data sheets are available upon request.

Pinouts

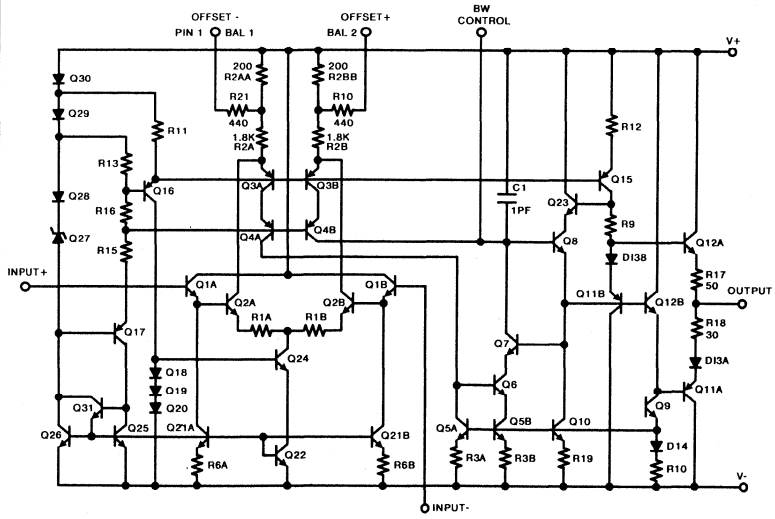
HA7-2529 (CERAMIC MINI-DIP)
HA3-2529 (PLASTIC MINI-DIP)
TOP VIEW



HA2-2529 (TO-99 METAL CAN)
TOP VIEW



Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Terminals 40.0V
Differential Input Voltage..... ±15V
Output Current ..... 90mA (Peak)
Internal Power Dissipation (Note 10) 300mW
Maximum Junction Temperature..... +175°C

Operating Temperature Ranges

HA-2529-2.....$-55°C \leq T_A \leq +125°C$
HA-2529-5..... $0°C \leq T_A \leq +75°C$
Storage Temperature Range .....$-65°C \leq T_A \leq +150°C$

Electrical Specifications

$V_S = \pm 15V$, $C_L = 50pF$, $R_L = 2k\Omega$, Unless Otherwise Specified.

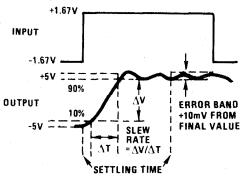
PARAMETER	TEMP	HA-2529-2 -55°C to +125°C			HA-2529-5 0°C to +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Offset Voltage (Note 8)	+25°C	-	2	5	-	2	10	mV
	Full	-	-	8	-	-	14	mV
Average Offset Voltage Drift (Note 8, 11)	Full	-	10	-	-	10	-	µV/°C
Bias Current (Note 8)	+25°C	-	50	200	-	50	250	nA
	Full	-	80	400	-	80	400	nA
Average Bias Current Drift (Note 8)	Full	-	0.2	-	-	0.2	-	nA/°C
Offset Current (Note 8)	+25°C	-	5	25	-	5	50	nA
	Full	-	10	50	-	10	100	nA
Average Offset Current Drift	Full	-	0.02	-	-	0.02	-	nA/°C
Common Mode Range	Full	±10	±13	-	±10	±13	-	V
Differential Input Resistance (Note 11)	+25°C	50	130	-	50	130	-	MΩ
Differential Input Capacitance (Note 11)	+25°C	-	3	-	-	3	-	pF
Input Noise Voltage (f = 1kHz)	+25°C	-	20	-	-	20	-	$nV/\sqrt{Hz}$
Input Noise Current (f = 1kHz)	+25°C	-	1.8	-	-	1.8	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 3)	+25°C	10	18	-	7.5	18	-	kV/V
	Full	7.5	15	-	5	15	-	kV/V
Common Mode Rejection Ratio (Note 5)	Full	80	100	-	74	100	-	dB
Gain-Bandwidth Product (Note 2)	+25°C	-	20	-	-	20	-	MHz
Minimum Stable Gain	+25°C	3	-	-	3	-	-	V/V
OUTPUT CHARACTERISTICS								
Output Voltage Swing	Full	±10	±12	-	±10	±12	-	V
Full Power Bandwidth (Notes 3 & 6)	+25°C	2.1	2.6	-	2.1	2.6	-	MHz
Output Current (Note 8)	+25°C	30	35	-	30	35	-	mA
	Full	25	30	-	25	30	-	mA
Output Resistance (Open Loop)	+25°C	-	30	-	-	30	-	Ω
TRANSIENT RESPONSE ($A_V = +3$)								
Rise Time (Note 2, 7)	+25°C	-	20	45	-	20	50	ns
Overshoot (Note 2, 7)	+25°C	-	10	30	-	10	30	%
Slew Rate (Note 3, 7)	+25°C	135	150	-	135	150	-	V/µs
Settling Time (Note 4, 7)	+25°C	-	200	-	-	200	-	ns
POWER SUPPLY CHARACTERISTICS								
Supply Current	Full	-	4.5	6	-	4.5	6	mA
Power Supply Rejection Ratio (Note 12)	Full	80	90	-	74	90	-	dB

NOTE:

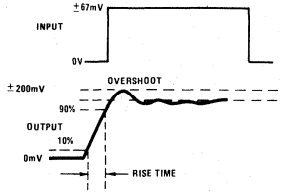
1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. $V_{OUT} = \pm 200mV$, $A_V \geq 3$.
3. $V_{OUT} = \pm 10V$.
4. Settling Time is specified to 0.1% of final value for a 10V output step and $A_V = -1$.
5. $\Delta V_{CM} = \pm 10V$.
6. Full Power Bandwidth is guaranteed by equation: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$
7. See Transient Response and Settling Time Test Circuits.
8. Refer to typical performance curve in data sheet.
9. $V_{OUT} = \pm 5V$.
10. Refer to package thermal constants in Die Information section.
11. Parameter is guaranteed by design and characterization data.
12. $\Delta V_S = \pm 10V$ to $\pm 20V$.

Test Circuits

SLEW RATE AND SETTLING TIME WAVEFORM

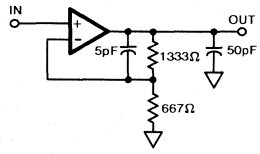


TRANSIENT RESPONSE WAVEFORM

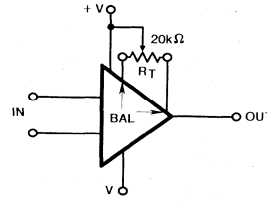


NOTE: Measured on both positive and negative transitions from 0 to +200mV and 0 to -200mV.

SLEW RATE AND TRANSIENT RESPONSE TEST CIRCUIT



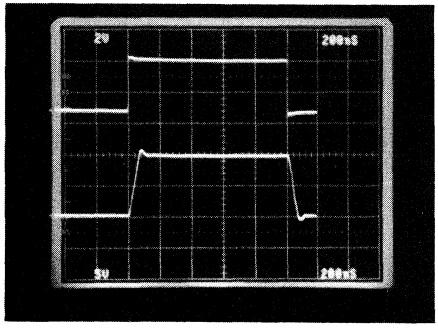
SUGGESTED V_{OS} ADJUSTMENT



Tested Offset Adjustment is $|V_{OS} + 1mV|$ minimum referred to output. Typical range is +28mV to -18mV with $R_T = 20k\Omega$.

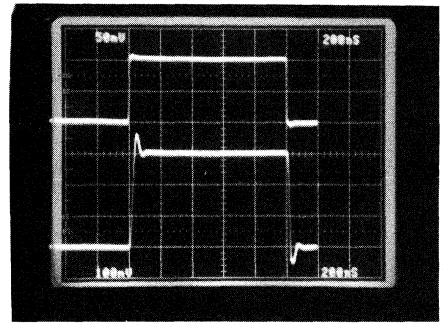
LARGE SIGNAL RESPONSE

Vertical Scale: (200ns/Div.)
Horizontal Scale: (2V/Div. Input)
(5V/Div. Output)

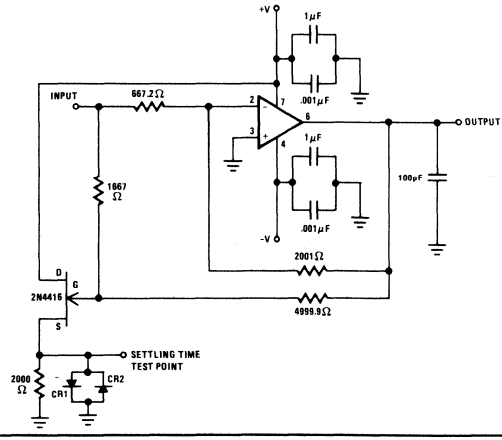


SMALL SIGNAL RESPONSE

Vertical Scale: (200ns/Div.)
Horizontal Scale : (50mV/Div. Input)
(100mV/Div. Output)



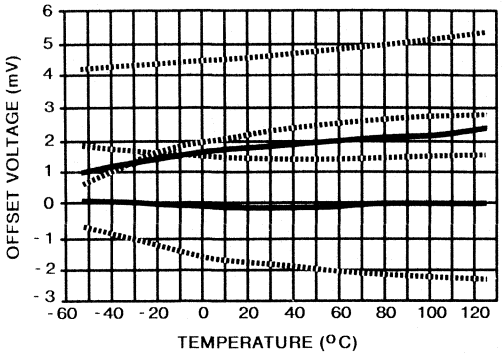
Settling Time Circuit



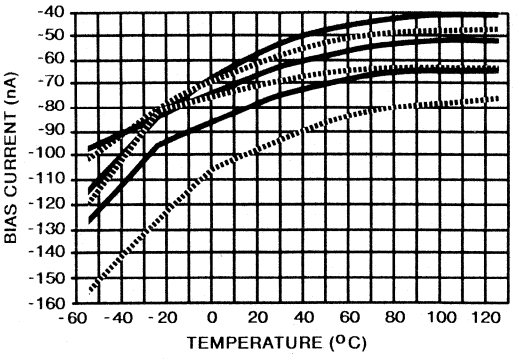
- $A_V = -3$
- Feedback and summing resistor ratios should be 0.1% matched.
- Clipping diodes CR1 and CR2 are optional. HP5082-2810 recommended.

Typical Performance Curves

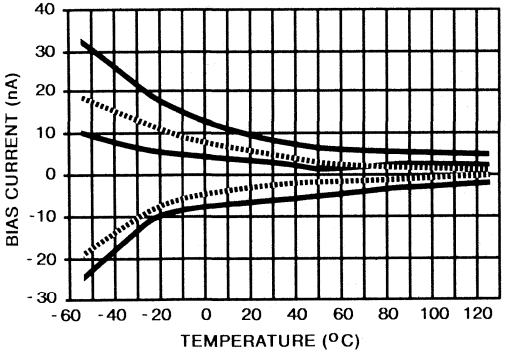
OFFSET VOLTAGE vs. TEMPERATURE
6 Typical Units From 3 Lots @ $V_S = \pm 15V$



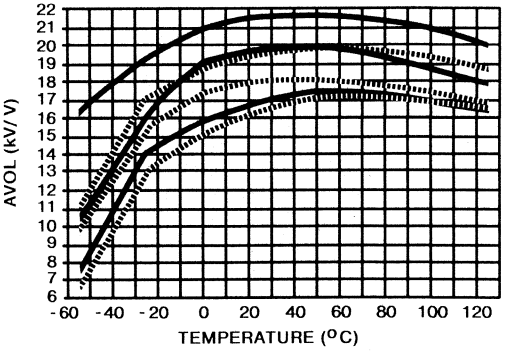
BIAS CURRENT vs. TEMPERATURE
6 Typical Units From 3 Lots @ $V_S = \pm 15V$



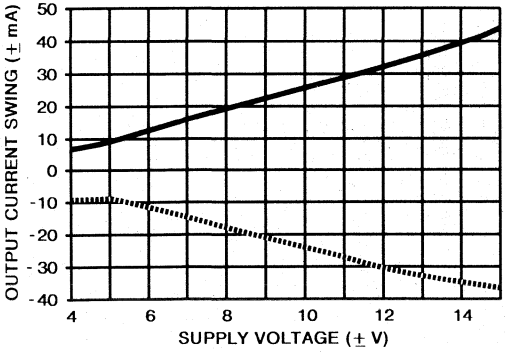
OFFSET CURRENT vs. TEMPERATURE
5 Typical Units From 3 Lots @ $V_S = \pm 15V$



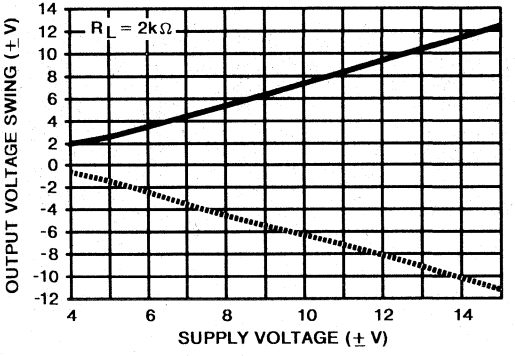
OPEN LOOP GAIN vs. TEMPERATURE
6 Typical Units From 3 Lots @ $V_S = \pm 15V$



OUTPUT CURRENT vs. SUPPLY VOLTAGE

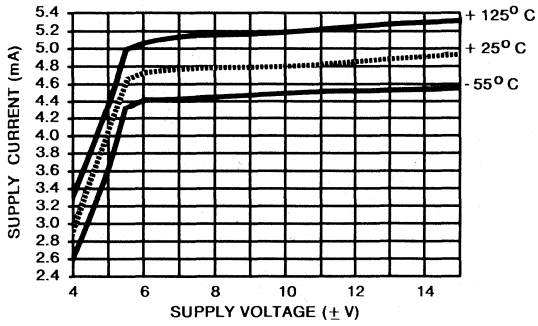


OUTPUT VOLTAGE SWING vs. SUPPLY VOLTAGE

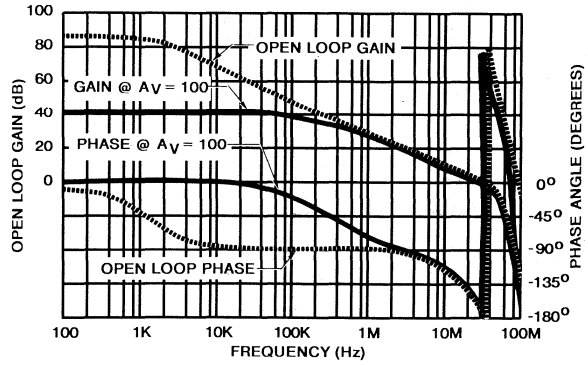


Typical Performance Curves (Continued)

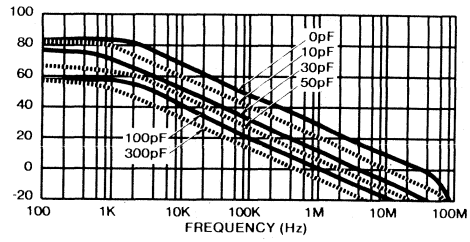
SUPPLY CURRENT vs. SUPPLY VOLTAGE
Over Full Temperature



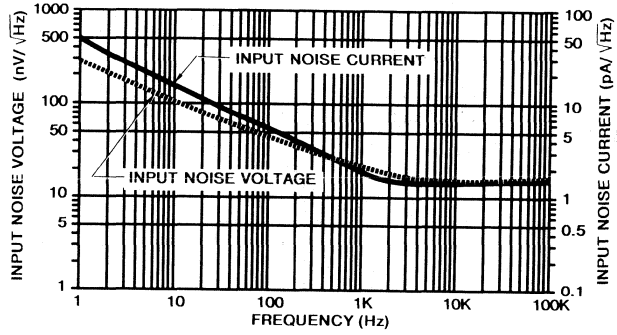
FREQUENCY RESPONSE AT VARIOUS GAINS



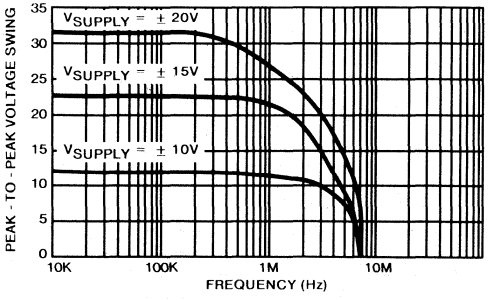
OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM BANDWIDTH CONTROL PIN TO GROUND



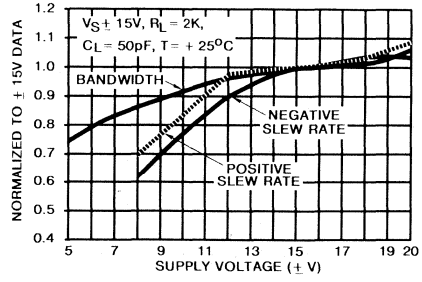
INPUT NOISE CHARACTERISTICS



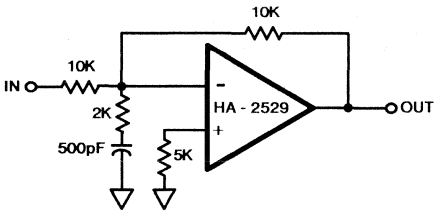
OUTPUT VOLTAGE SWING vs. FREQUENCY



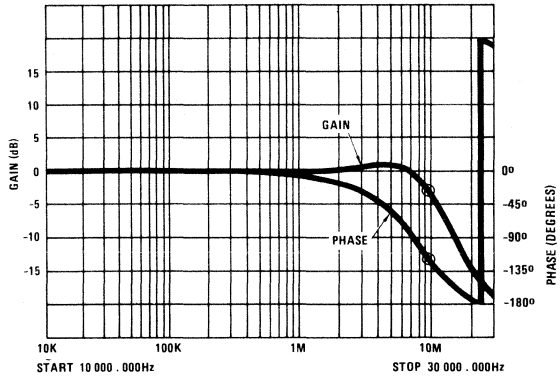
NORMALIZED A.C. PARAMETERS vs. SUPPLY VOLTAGE



Typical Applications



FREQUENCY RESPONSE FOR INVERTING UNITY GAIN CIRCUIT



NOTE: Compensation Circuit for $A_V = -1$
Slew Rate $\approx$ 120V/µs
Bandwidth $\approx$ 10MHz
Settling Time (0.1%) $\approx$ 500ns
Capacitance at pin 8 must be minimized for maximum bandwidth.
Tested and functional with supply voltages from ±4V to ±15V.

Die Characteristics

Transistor Count 40
Die Dimensions ..... 1660µm x 1300µm x 485µm (65 mils x 51 mils x 19 mils)
Substrate Potential ..... V-
Process ..... Bipolar-DI

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
HA2-Metal Can (-2, -5, -7)	206	56
HA2-Metal Can (-8, /883)	168	52
HA3-Plastic Mini-DIP (-5)	90	39
HA4-Ceramic LCC (/883)	99	37
HA7-Ceramic Mini-DIP (-8, /883)	140	65
HA7-Ceramic Mini-DIP (-2, -5, -7)	204	112

HARRIS

HA-2539

Very High Slew Rate Wideband Operational Amplifier

Features

- Very High Slew Rate 600V/μs
- Open Loop Gain 30kV/V
- Wide Gain-Bandwidth ($A_V \geq 10$) 600MHz
- Power Bandwidth 9.5MHz
- Low Offset Voltage 8mV
- Input Voltage Noise ..... 6nV/$\sqrt{Hz}$
- Output Voltage Swing ..... $\pm$10V
- Monolithic Bipolar Dielectric Isolation Construction

Applications

- Pulse and Video Amplifiers
- Wideband Amplifiers
- High Speed Sample-Hold Circuits
- RF Oscillators

Description

The Harris HA-2539 represents the ultimate in high slew rate, wideband, monolithic operational amplifiers. It has been designed and constructed with the Harris High Frequency Bipolar Dielectric Isolation process and features dynamic parameters never before available from a truly differential device.

With a 600V/μs slew rate and a 600MHz gain bandwidth product, the HA-2539 is ideally suited for use in video and RF amplifier designs, in closed loop gains of 10 or greater. Full $\pm$10V swing coupled with outstanding A.C. parameters and complemented by high open loop gain makes the devices useful in high speed data acquisition systems.

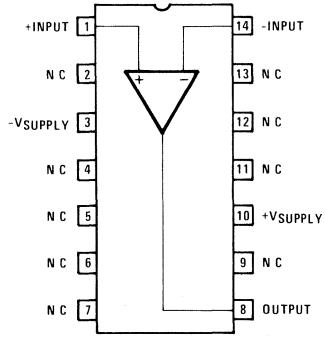
The HA-2539 is available in 14 pin ceramic and plastic DIP. The HA-2539-2 operates over -55°C to +125°C temperature range while the HA-2539-5 and HA-2539C-5 operates over the 0°C to +75°C range.

For further design assistance please refer to Application Note 541 (Using The HA-2539 Very High Slew Rate Wideband Operational Amplifiers) and Application Note 556 (Thermal Safe-Operating-Areas For High Current Operational Amplifiers).

For military grade product information, the HA-2539/883 data sheet is available upon request.

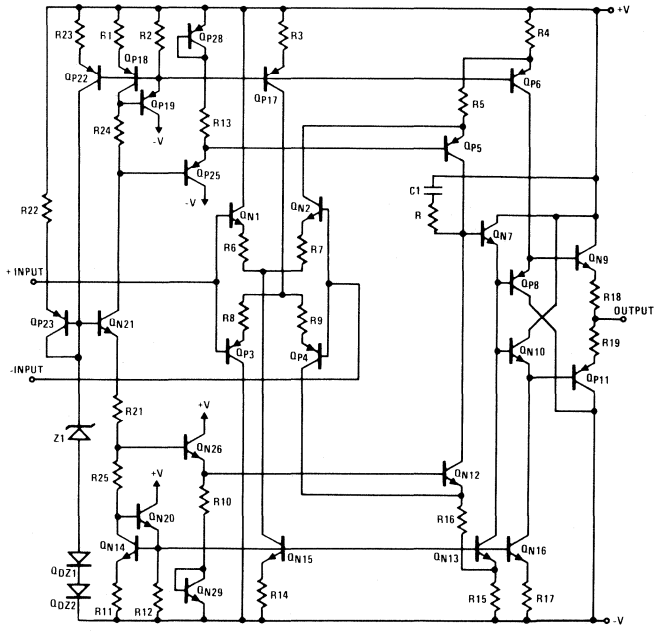
Pinout

HA1-2539/2539C (CERAMIC DIP)
HA3-2539/2539C (PLASTIC DIP)
TOP VIEW



(N C) No Connection pins may be tied to a ground plane for better isolation and heat dissipation.

Schematic



CAUTION: These devices are sensitive to electostatic discharge. Proper IC handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Terminals 35V
Differential Voltage ..... ±6V
Peak Output Current 50mA
Continuous Output Current ..... $33mA_{rms}$
Internal Quiescent Power Dissipation (Note 2) .... 870mW (Ceramic DIP)

Operating Temperature Range

HA-2539-2 ..... $-55^oC \leq T_A \leq +125^oC$
HA-2539/2539C-5 ..... $0^oC \leq T_A \leq +75^oC$
Storage Temperature Range ..... $-65^oC \leq T_A \leq +150^oC$
Maximum Junction Temperature ..... $+175^oC$

Electrical Specifications

$V_{SUPPLY} = \pm 15V$, $R_L = 1k\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified.

PARAMETER	TEMP	HA-2539-2 -55°C to +125°C			HA-2539-5 0°C to +75°C			HA-2539C-5 0°C to +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS											
Offset Voltage	+25°C	—	8	10	—	8	15	—	8	15	mV
	Full	—	13	15	—	13	20	—	13	20	mV
Average Offset Voltage Drift	Full	—	20	—	—	20	—	—	20	—	µV/°C
Bias Current	+25°C	—	5	20	—	5	20	—	5	20	µA
	Full	—	—	25	—	—	25	—	—	25	µA
Offset Current	+25°C	—	1	6	—	1	6	—	1	6	µA
	Full	—	—	8	—	—	8	—	—	8	µA
Input Resistance	+25°C	—	10	—	—	10	—	—	10	—	kΩ
Input Capacitance	+25°C	—	1	—	—	1	—	—	1	—	pF
Common Mode Range	Full	±10	—	—	±10	—	—	±10	—	—	V
Input Current Noise (f = 1KHz, $R_{SOURCE} = 0\Omega$)	+25°C	—	6	—	—	6	—	—	6	—	$pA/\sqrt{Hz}$
Input Voltage Noise (f = 1KHz, $R_{SOURCES} = 0\Omega$)	+25°C	—	6	—	—	6	—	—	6	—	$nV/\sqrt{Hz}$
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Note 3)	+25°C	10K	15K	—	10K	15K	—	7K	10K	—	V/V
	Full	5K	—	—	5K	—	—	5K	—	—	V/V
Common-Mode Rejection Ratio (Note 4)	Full	60	72	—	60	72	—	60	72	—	dB
Minimum Stable Gain	+25°C	10	—	—	10	—	—	10	—	—	V/V
Gain Bandwidth Product (Notes 5 & 6)	+25°C	—	600	—	—	600	—	—	600	—	MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 3, 10)	Full	±10	—	—	±10	—	—	±10	—	—	V
Output Current (Note 3)	+25°C	±10	±20	—	±10	±20	—	±10	±20	—	mA
Output Resistance	+25°C	—	30	—	—	30	—	—	30	—	Ω
Full Power Bandwidth (Notes 3 & 7)	+25°C	8.7	9.5	—	8.7	9.5	—	8.7	9.5	—	MHz
TRANSIENT RESPONSE (Note 8)											
Rise Time	+25°C	—	7	—	—	7	—	—	7	—	ns
Overshoot	+25°C	—	15	—	—	15	—	—	15	—	%
Slew Rate	+25°C	550	600	—	550	600	—	550	600	—	V/µs
Settling Time: 10V Step to 0.1%	+25°C	—	180	—	—	180	—	—	200	—	ns
POWER REQUIREMENTS											
Supply Current	Full	—	20	25	—	20	25	—	20	25	mA
Power Supply Rejection Ratio (Note 9)	Full	60	70	—	60	70	—	60	70	—	dB

NOTES:

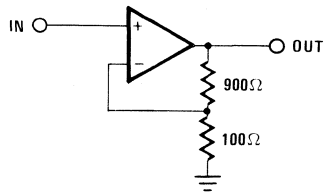
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

2. This value assumes a no load condition: Maximum power dissipation with load conditions must be designed to maintain the maximum junction temperature below +175°C. By using Application Note 556 on Safe Operating Area equations, along with the packaging thermal resistances listed in the die information section, proper load conditions can be determined. Heat sinking is recommended above +75°C with suggested models:
   Thermalloy #6007 (θ_{SA} = 40°C/W) or AAVID #5602B (θ_{SA} = 16°C/W).

3. R_L = 1kΩ, V_O = ±10V
4. VCM = ±10V
5. V_O = 90mV
6. A_V = 10.
7. Full Power Bandwidth guaranteed based on slew rate measurement using FPBW = $\frac{\text{Slew Rate}}{2\pi V_{PEAK}}$
8. Refer to Test Circuits section of data sheet.
9. V_{SUPPLY} = ±5VDC to ±15VDC
10. Guaranteed range for output voltage is ±10V. Functional operation outside of this range is not guaranteed.

Test Circuits

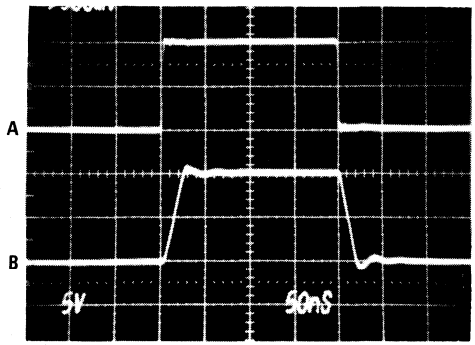
TEST CIRCUIT



V_S = ±15V
A_V = +10
$C_L \leq$ 10pF

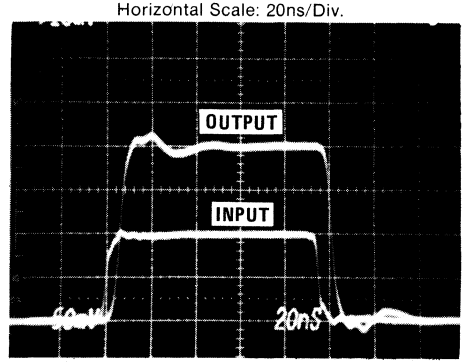
LARGE SIGNAL RESPONSE

Vertical Scale: A = 0.5V/Div., B = 5.0V/Div.
Horizontal Scale: Time: 50ns/Div.

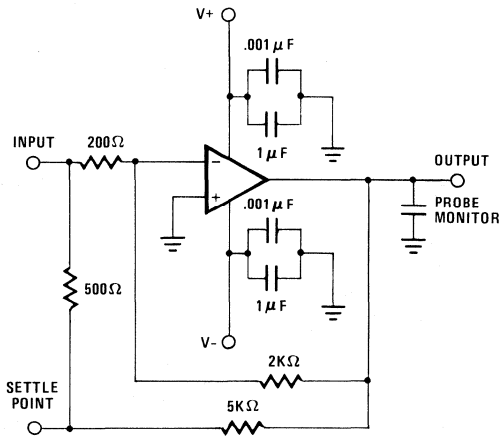


SMALL SIGNAL RESPONSE

Vertical Scale: Input = 10mV/Div., Output = 50mV/Div.
Horizontal Scale: 20ns/Div.



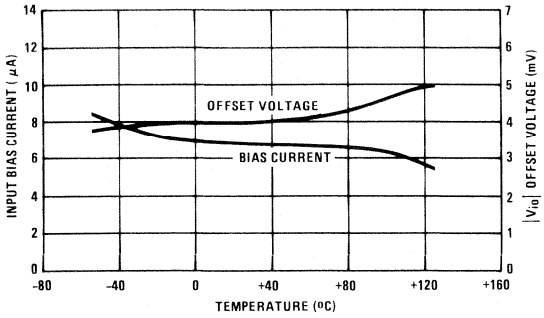
SETTLING TIME TEST CIRCUIT



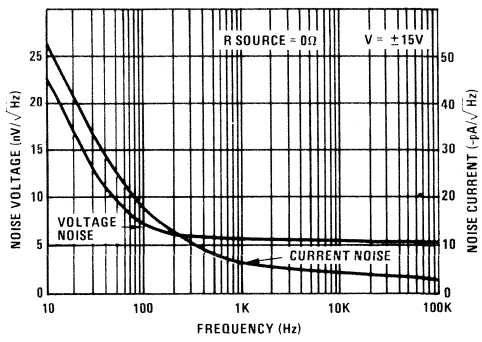
- A_V = -10
- Load Capacitance should be less than 10pF.
- It is recommended that resistors be carbon composition and that feedback and summing network ratios be matched to 0.1%.
- SETTLE POINT (Summing Node) capacitance should be less than 10pF. For optimum settling time results, it is recommended that the test circuit be constructed directly onto the device pins. A Tektronix 568 Sampling Oscilloscope with S-3A sampling heads is recommended as a settle point monitor.

Typical Performance Curves

INPUT OFFSET VOLTAGE AND BIAS CURRENT vs. TEMPERATURE

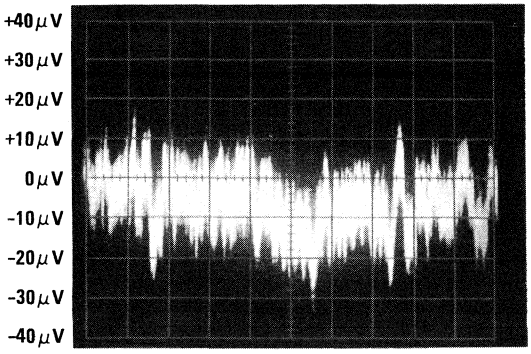


INPUT NOISE VOLTAGE AND NOISE CURRENT vs. FREQUENCY

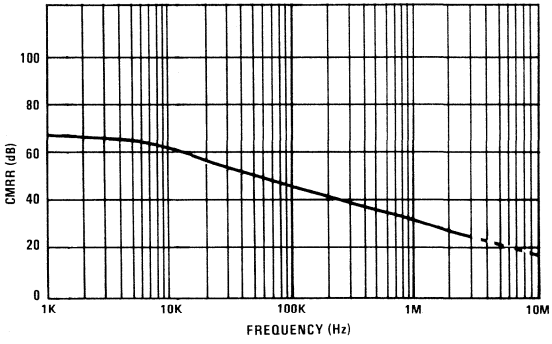


BROADBAND NOISE (0.1Hz to 1MHz)

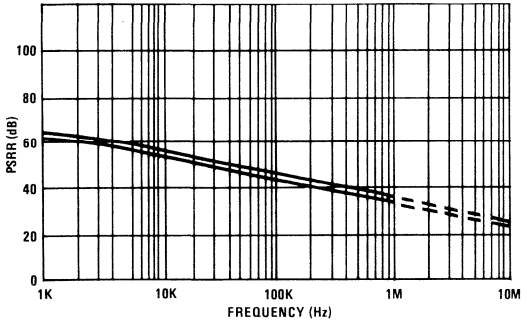
Vertical Scale: 10μV/Div.
Horizontal Scale: 50ms/Div.



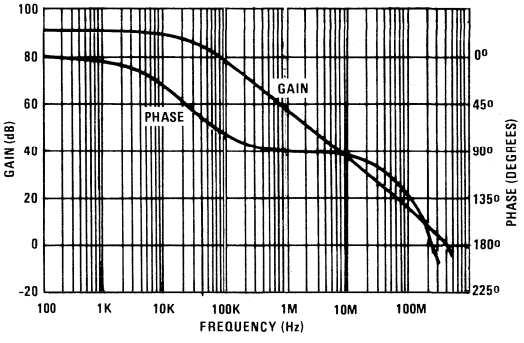
COMMON MODE REJECTION RATIO vs. FREQUENCY



POWER SUPPLY REJECTION RATIO vs. FREQUENCY

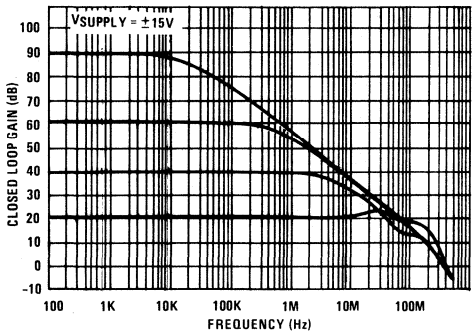


OPEN LOOP GAIN/PHASE vs. FREQUENCY HA-2539

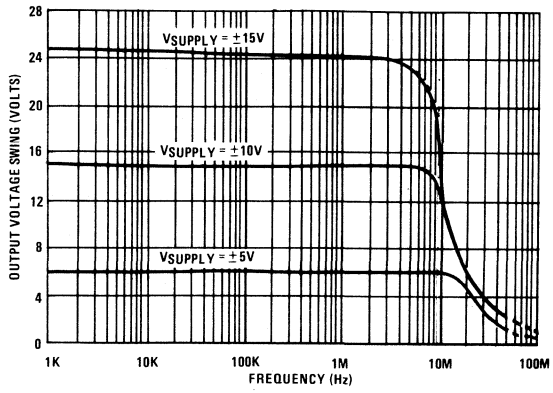


Typical Performance Curves (Continued)

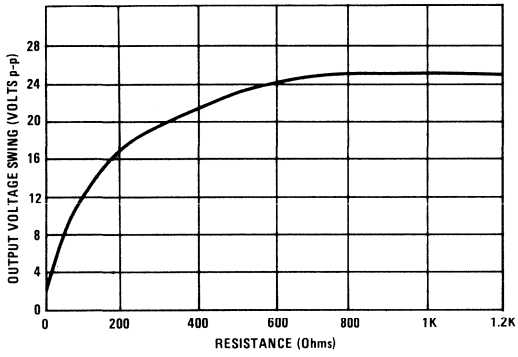
CLOSED LOOP FREQUENCY RESPONSE FOR VARIOUS CLOSED LOOP GAINS



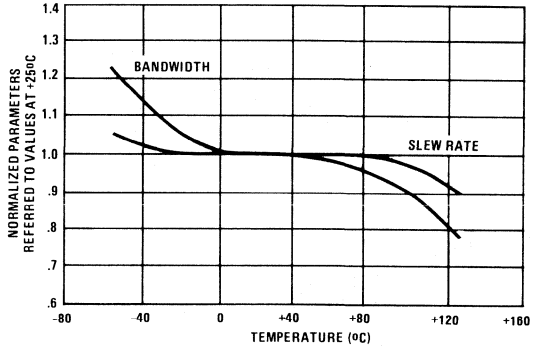
OUTPUT VOLTAGE SWING vs. FREQUENCY



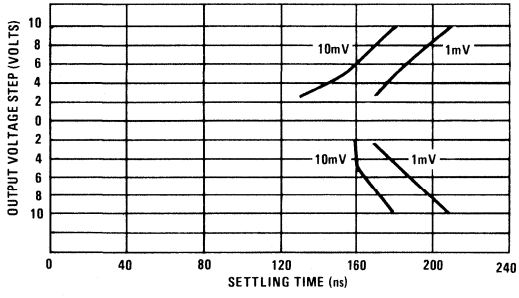
OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE



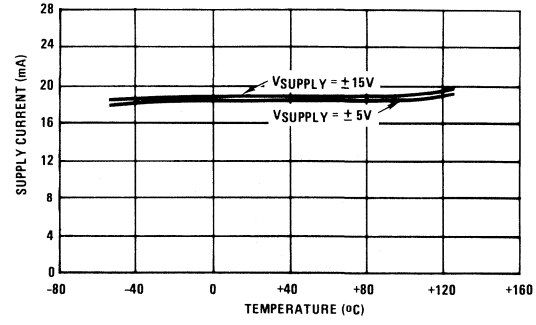
NORMALIZED AC PARAMETERS vs. TEMPERATURE



SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES

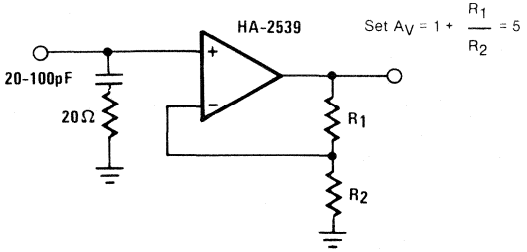


POWER SUPPLY CURRENT vs. TEMPERATURE AND SUPPLY VOLTAGE

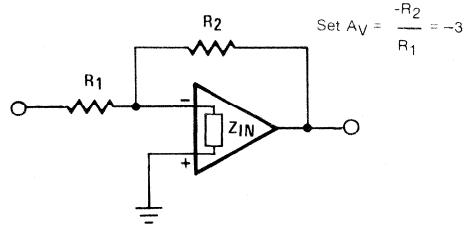


Applications

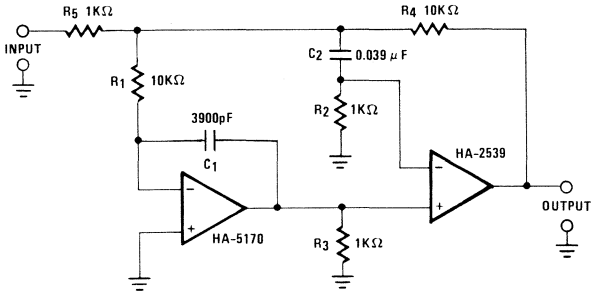
FREQUENCY COMPENSATION
COMPENSATION BY OVERDAMPING



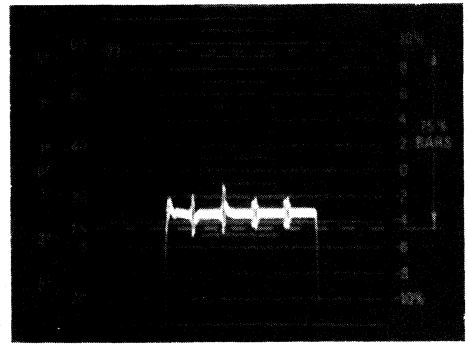
STABILIZATION USING Z_{IN}



REDUCING DC ERRORS
COMPOSITE AMPLIFIER



DIFFERENTIAL GAIN ERROR (3%)
HA-2539 20dB VIDEO GAIN BLOCK



NOTE: No connect pins (NC) on the HA-2539 should be tied to a ground plane.
Refer to Figure 4 in Application Note 541 for detailed Application suggestions.

Die Characteristics

Transistor Count 30
Die Dimensions ..... 75 x 61 x 19 mils
(1910μm x 1550μm x 483μm)
Substrate Potential (Powered Up)* ..... V-
Process ..... High Frequency Bipolar-DI
Passivation ..... Nitride

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
HA1-2539/2539C Ceramic DIP	104	48
HA3-2539/2539C Plastic DIP	95	46

*The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.

HARRIS

HA-2540

Wideband, Fast Settling Operational Amplifier

Features

- Very High Slew Rate 400V/μs
- Fast Settling Time 200ns
- Wide Gain-Bandwidth (Av $\geq$ 10) 400MHz
- Power Bandwidth 6MHz
- Low Offset Voltage 8mV
- Input Voltage Noise ..... 6nV/$\sqrt{Hz}$
- Output Voltage Swing ..... $\pm$10V
- Monolithic Bipolar Construction

Applications

- Pulse and Video Amplifiers
- Wideband Amplifiers
- High Speed Sample-Hold Circuits
- Fast, Precise D/A Converters

Description

The Harris HA-2540 is a wideband, very high slew rate, monolithic operational amplifier featuring superior speed and bandwidth characteristics. Bipolar construction coupled with dielectric isolation allows this truly differential device to deliver outstanding performance in circuits where closed loop gain is 10 or greater. Additionally, the HA-2540 has a drive capability of $\pm$10V into a 1KΩ load. Other desirable characteristics include low input voltage noise, low offset voltage, and fast settling time.

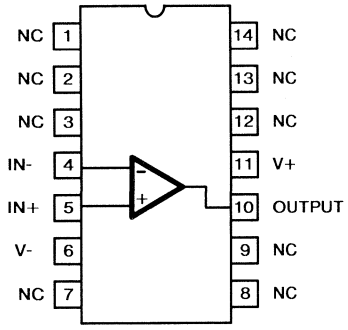
A 400/μs slew rate ensures high performance in video and pulse amplification circuits, while the 400MHz gain-bandwidth-product is ideally suited for wideband signal amplification. A settling time of 200ns also makes the HA-2540 an excellent selection for high speed Data Acquisition Systems.

The HA-2540-2 is specified over the -55°C to +125°C range while the HA-2540-5 and HA-2540C-5 is specified from 0°C to +75°C. The HA-2540 and HA-2540C are available in the 14 pin Ceramic and Epoxy DIP packages.

Refer to Application Note 541 and Application Note 556 for more information on High Speed Op-Amp applications. MIL-STD-883 data sheet is available on request.

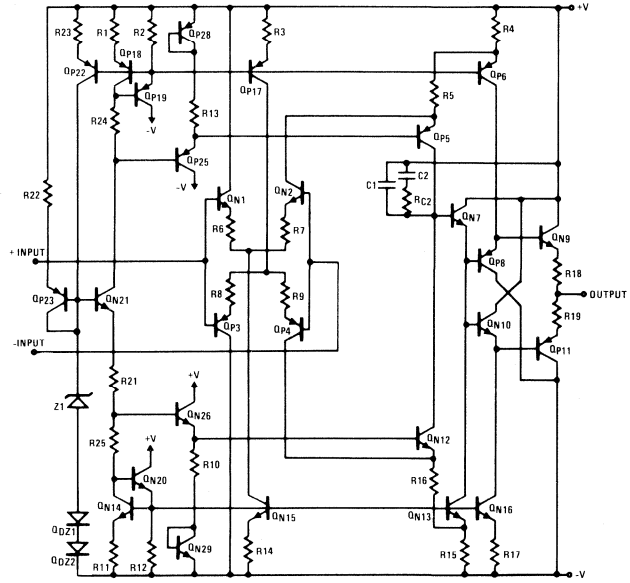
Pinout

HA1-2540/2540C (CERAMIC DIP)
HA3-2540/2540C (PLASTIC DIP)
TOP VIEW



NC - No Connection. These pins may be tied to a ground plane for added isolation and heat dissipation

Schematic



CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Terminals 35V
Differential Voltage ..... ±6V
Output Current ..... 33mArms (Continuous), 50mA (Peak)
Internal Power Dissipation (Note 2) ..... 870mW (Cerdip)

Operating Temperature Ranges

HA-2540-2 ..... $-55^oC \leq T_A \leq +125^oC$
HA-2540/2540C-5 ..... $0^oC \leq T_A \leq +75^oC$
Storage Temperature Range ..... $-65^oC \leq T_A \leq +150^oC$
Junction Temperature ..... $+175^oC$

Electrical Specifications

$V_{SUPPLY} = \pm 15V$, $R_L = 1k\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified.

PARAMETER	TEMP	HA-2540-2 -55°C to +125°C			HA-2540-5 0°C to +75°C			HA-2540C-5 0°C to +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS											
Offset Voltage	+25°C	—	8	10	—	8	15	—	8	15	mV
	Full	—	13	15	—	13	20	—	13	20	mV
Average Offset Voltage Drift	Full	—	20	—	—	20	—	—	20	—	µV/°C
Bias Current	+25°C	—	5	20	—	5	20	—	5	20	µA
	Full	—	—	25	—	—	25	—	—	25	µA
Offset Current	+25°C	—	1	6	—	1	6	—	1	6	µA
	Full	—	—	8	—	—	8	—	—	8	µA
Input Resistance	+25°C	—	10	—	—	10	—	—	10	—	kΩ
Input Capacitance	+25°C	—	1	—	—	1	—	—	1	—	pF
Common Mode Range	Full	±10	—	—	±10	—	—	±10	—	—	V
Input Noise Current (f = 1kHz, $R_{SOURCE} = 0\Omega$)	+25°C	—	6	—	—	6	—	—	6	—	$pA/\sqrt{Hz}$
Input Noise Voltage (f = 1kHz, $R_{SOURCES} = 0\Omega$)	+25°C	—	6	—	—	6	—	—	6	—	$nV/\sqrt{Hz}$
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain	+25°C	10K	15K	—	10K	15K	—	7K	10K	—	V/V
(Note 3)	Full	5K	—	—	5K	—	—	5K	—	—	V/V
Common-Mode Rejection Ratio (Note 4)	Full	60	72	—	60	72	—	60	72	—	dB
Minimum Stable Gain	+25°C	10	—	—	10	—	—	10	—	—	V/V
Gain-Bandwidth-Product (Notes 5 & 6)	+25°C	—	400	—	—	400	—	—	400	—	MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 3, 10)	Full	±10	—	—	±10	—	—	±10	—	—	V
Output Current (Note 3)	+25°C	±10	±20	—	±10	±20	—	±10	±20	—	mA
Output Resistance	+25°C	—	30	—	—	30	—	—	30	—	Ω
Full Power Bandwidth (Notes 3 & 7)	+25°C	5.5	6	—	5.5	6	—	5.5	6	—	MHz
TRANSIENT RESPONSE (Note 8)											
Rise Time	+25°C	—	14	—	—	14	—	—	14	—	ns
Overshoot	+25°C	—	5	—	—	5	—	—	5	—	%
Slew Rate	+25°C	350	400	—	350	400	—	350	400	—	V/µs
Settling Time: 10V Step to 0.1%	+25°C	—	140	—	—	140	—	—	140	—	ns
POWER REQUIREMENTS											
Supply Current	Full	—	20	25	—	20	25	—	20	25	mA
Power Supply Rejection Ratio (Note 9)	Full	60	70	—	60	70	—	60	70	—	dB

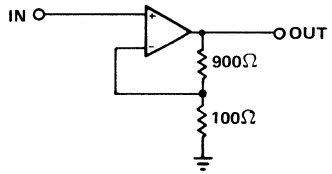
NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. This value assumes a no load condition. Maximum power dissipation with load conditions must be designed to maintain the maximum junction temperature below +175°C. By using Application Note 556 on Safe Operating Area Equations, along with the packaging thermal resistances listed in the Die Information section, proper load conditions can be determined. Heat sinking is recommended above +75°C with suggested models:

   Thermalloy #6007 ($\theta_{SA} \cong 40^{o}C/W$) or AAVID #5602B ($\theta_{SA} \cong 16^{o}C/W$).
3. $R_L = 1k\Omega$, $V_O = \pm 10V$.
4. $V_{CM} = \pm 10V$.
5. $V_O = 90mV$.
6. $A_V = 10V$.
7. Full power bandwidth guaranteed based on slew rate measurement using: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$
8. Refer to Test Circuits section of the data sheet.
9. $V_{SUPPLY} = \pm 5VDC$ to $\pm 15VDC$.
10. Guaranteed range for output voltage is $\pm 10V$. Functional operation outside of this range is not guaranteed.

Test Circuits

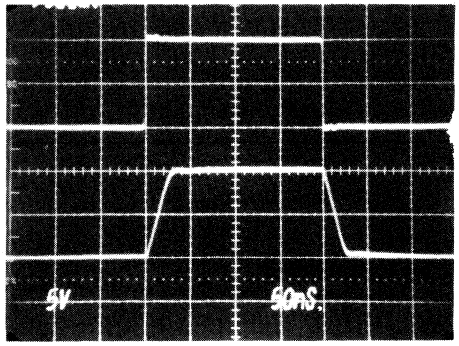
LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT



$A_V = +10$
$C_L \leq 10pF$

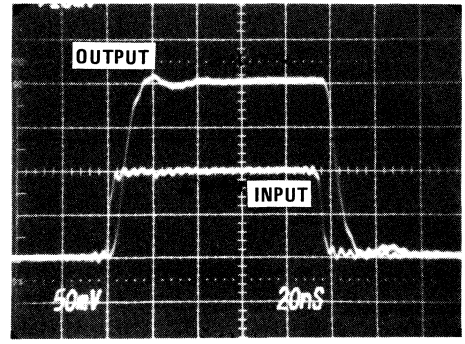
LARGE SIGNAL RESPONSE

Vertical Scale: (Volts: A = 0.5V/Div., B = 5.0V/Div.)
Horizontal Scale: (Time: 50ns/Div.)



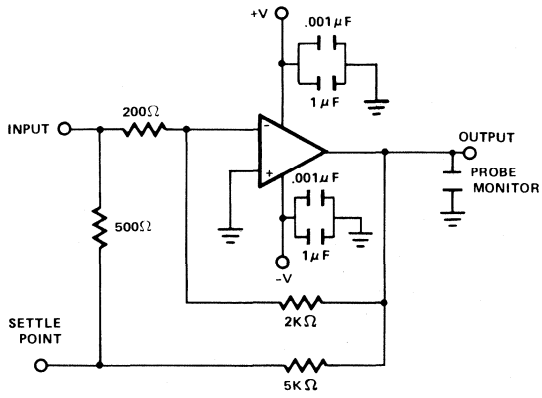
SMALL SIGNAL RESPONSE

Vertical Scale: Input = 10mV/Div.; Output = 50mV/Div.
Horizontal Scale: 20ns/Div.



TURN-ON TIME DELAY TYPICALLY 4ns.

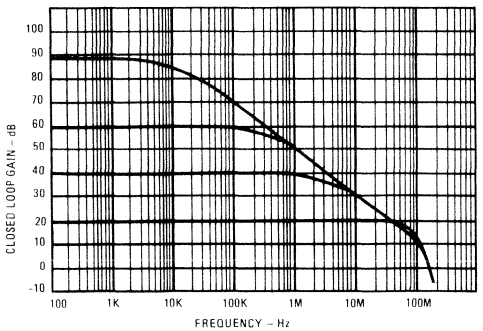
SETTLING TIME TEST CIRCUIT



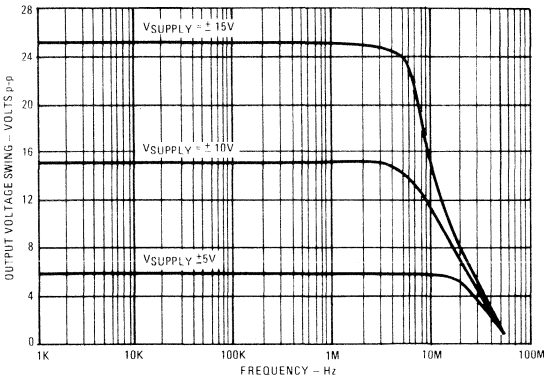
- $A_V = -10$.
- Load Capacitance should be less than 10pF. Turn on time delay typically 4ns.
- It is recommended that resistors be carbon composition and that feedback and summing network ratios be matched to 0.1%.
- SETTLE POINT (Summing Node) capacitance should be less than 10pF. For optimum settling time results, it is recommened that the test circuit be constructed directly onto the device pins. A Tektronix 568 Sampling Oscilloscope with S-3A sampling heads is recommended as a settle point monitor.

Performance Curves

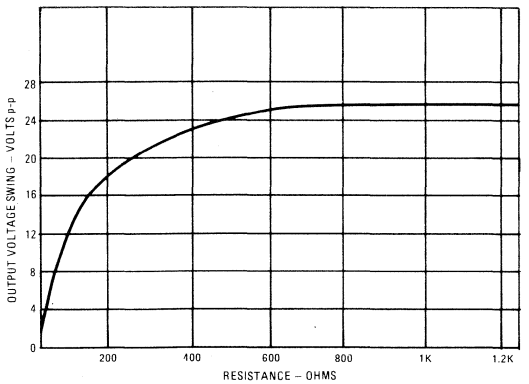
CLOSED LOOP FREQUENCY RESPONSE



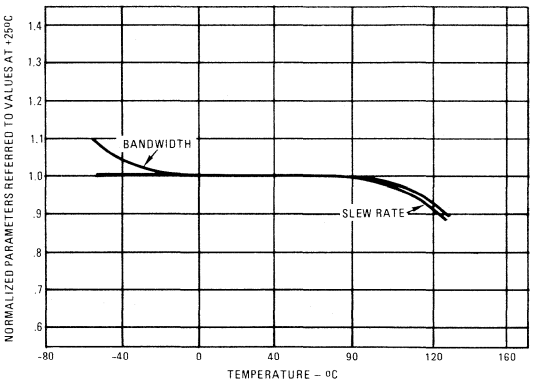
OUTPUT VOLTAGE SWING vs. FREQUENCY



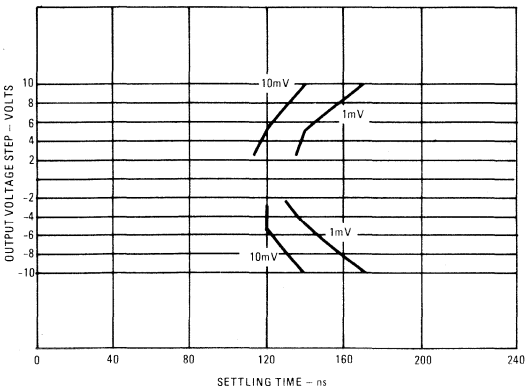
OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE



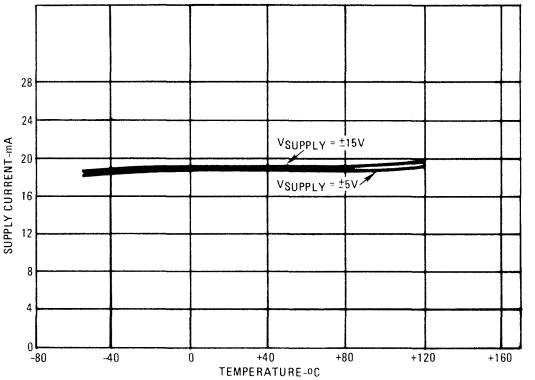
NORMALIZED AC PARAMETERS vs. TEMPERATURE



SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES

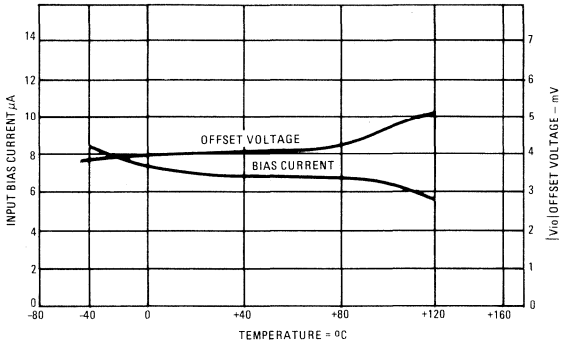


POWER SUPPLY CURRENT vs. TEMPERATURE AND SUPPLY VOLTAGE

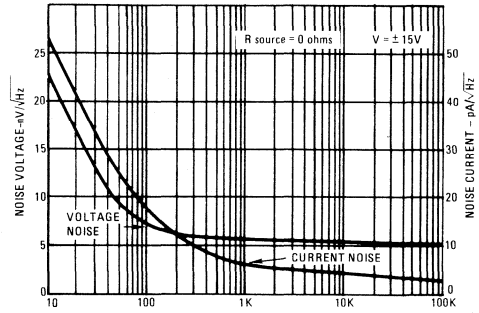


Performance Curves

INPUT OFFSET VOLTAGE AND BIAS CURRENT vs. TEMPERATURE

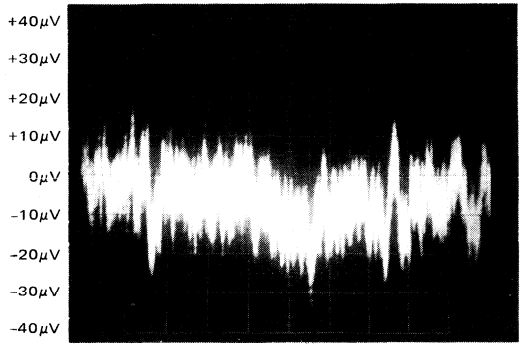


INPUT NOISE VOLTAGE AND NOISE CURRENT vs. FREQUENCY

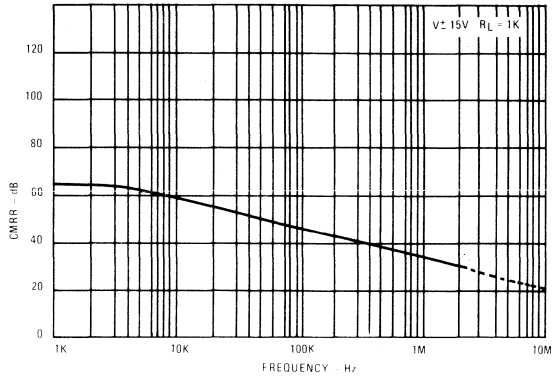


BROADBAND NOISE (0.1HZ to 1MHz)

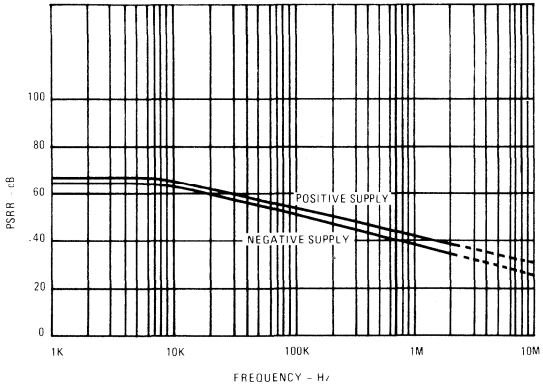
Vertical Scale: 10μV/Div.
Horizontal Scale: 50ms/Div.



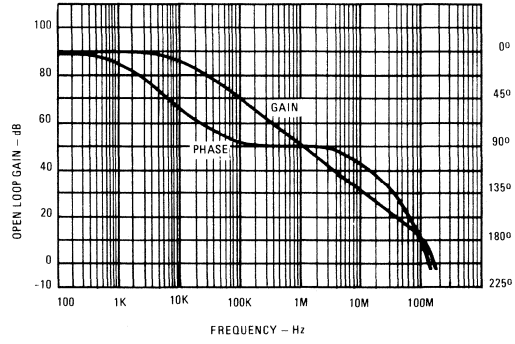
COMMON MODE REJECTION RATIO vs. FREQUENCY



POWER SUPPLY REJECTION RATIO vs. FREQUENCY



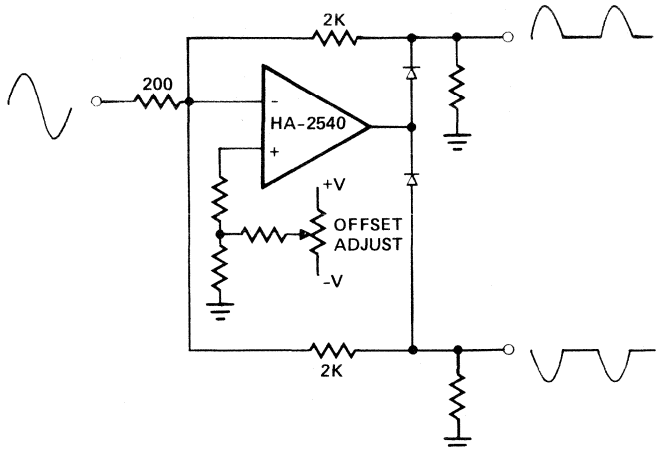
OPEN LOOP GAIN/PHASE vs. FREQUENCY HA-2540



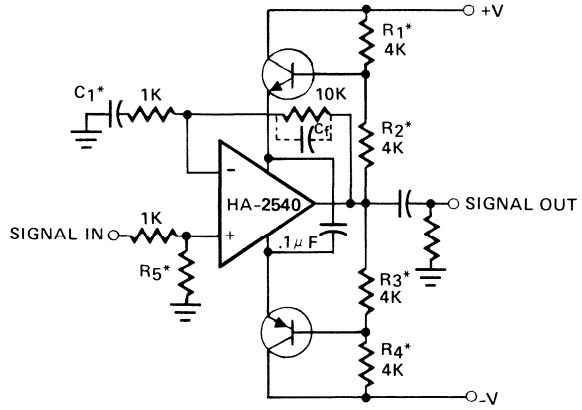
Applications

WIDEBAND SIGNAL SPLITTER

With one HA-2540 and two low capacitance switching diodes, signals exceeding 10MHz can be seperated. This circuit is most useful for full wave rectification, AM detectors or sync generation.



BOOTSTRAPPING FOR MORE OUTPUT CURRENT AND VOLTAGE SWING



NOTES:
1. Used for experimental purposes. $C_f \approx 3pF$.
2. C_1 is optional (0.001μF → 0.01μF ceramic)
3. R_S is optional and can be utilized to reduce input signal amplitude and/or balance input conditions. R_S = 500Ω to 1kΩ.

Refer to Application Note 541 For Further Applications Information.

Die Characteristics

Transistor Count 30
Die Dimensions ..... 75 x 61 x 19 mils (1910μm x 1550μm x 483μm)
Substrate Potential (Powered Up)* ..... V-
Process ..... High Frequency Bipolar-DI
Passivation ..... Nitride

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
HA1-2540/2540C Ceramic DIP	104	48
HA3-2540/2540C Plastic DIP	95	46

*The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.

HARRIS

HA-2541

Wideband, Fast Settling, Unity Gain Stable, Operational Amplifier

Features

- Unity Gain Bandwidth 40MHz
- High Slew Rate 250V/μs
- Low Offset Voltage 0.8mV
- Fast Settling Time (0.1%) 90ns
- Power Bandwidth 4MHz
- Output Voltage Swing (Min) ..... $\pm$10V
- Unity Gain Stability
- Monolithic Bipolar Dielectric Isolation Construction

Applications

- Pulse and Video Amplifiers
- Wideband Amplifiers
- High Speed Sample-Hold Circuits
- Fast, Precise D/A Converters
- High Speed A/D Input Buffer

Description

The HA-2541 is the first unity gain stable monolithic operational amplifier to achieve 40MHz unity gain bandwidth. A major addition to the Harris series of high speed, wideband op amps, the HA-2541 is designed for video and pulse applications requiring stable amplifier response at low closed loop gains.

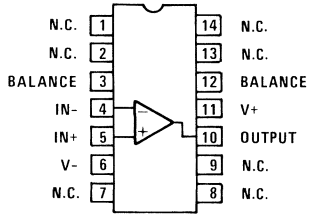
The uniqueness of the HA-2541 is that its slew rate and bandwidth characteristics are specified at unity gain. Historically, high slew rate, wide bandwidth and unity gain stability have been incompatible features for a monolithic operational amplifier. But features such as 250V/μs slew rate and 40MHz unity gain bandwidth clearly show that this is not the case for the HA-2541. These features, along with 90ns settling time to 0.1%, make this product an excellent choice for high speed data acquisition systems.

Packaged in a metal can (TO-8) or 14 pin ceramic DIP, the HA-2541 is pin compatible with the HA-2540 and HA-5190 op amps. The HA-2541-2 is specified over the temperature range of -55°C to +125°C. The HA-2541-5 is specified over the temperature range of 0°C to +75°C. For the military grade product, refer to the HA-2541 military data sheet.

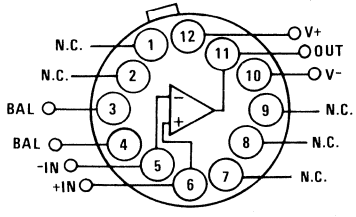
For further application suggestions on the HA-2541, please refer to Applicaton Note 550 (Using the HA-2541), and Application Note 556 (Thermal Safe-Operating-Areas For High Current Operational Amplifiers). Also see 'Applications' in this data sheet.

Pinouts

HA1-2541 (CERAMIC DIP)
TOP VIEW

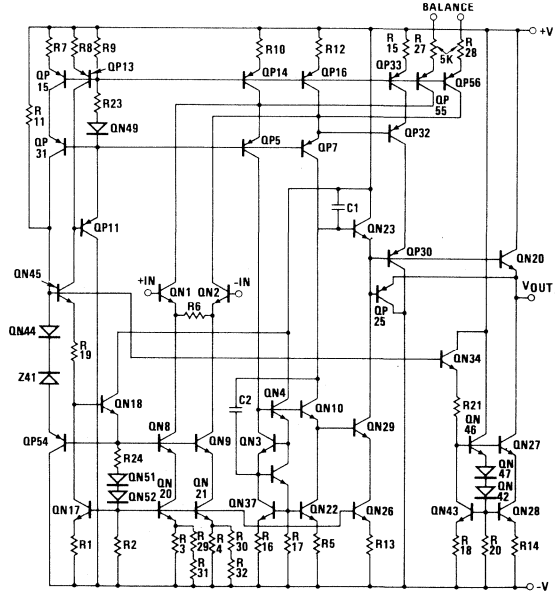


HA2-2541 (TO-8 METAL CAN)
TOP VIEW



V_{CASE} = V-

Schematic



CAUTION: Electronic devices are sensitive to electrostic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- 35V
Differential Input Voltage ..... ±6V
Peak Output Current 50mA
Continuous Output Current 28mArms

Operating Temperature Range:

HA-2541-2 ..... $-55^oC \leq T_A \leq +125^oC$
HA-2541-5 ..... $0^oC \leq T_A \leq +75^oC$
Storage Temperature Range ..... $-65^oC \leq T_A \leq +150^oC$
Maximum Junction Temperature (Note 11) ..... $+175^oC$

Electrical Specifications V_{SUPPLY} = ±15 Volts; R_L = 2kΩ, $C_L \leq$ 10pF, Unless Otherwise Specified

PARAMETER	TEMP	HA-2541-2 -55°C to +125°C			HA-2541-5 0°C to +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		0.8	2		1	2	mV
	Full			6			6	mV
Average Offset Voltage Drift	Full		9			9		µV/°C
Bias Current	+25°C		11	25		11	25	µA
	Full			30			30	µA
Average Bias Current Drift	Full		85			85		nA/°C
Offset Current	+25°C		1	7		1	7	µA
	Full			9			9	µA
Input Resistance	+25°C		100			100		kΩ
Input Capacitance	+25°C		1			1		pF
Common Mode Range	Full	±10	±11		±10	±11		V
Input Noise Voltage (f = 1kHz, R_g = 0Ω)	+25°C		10			10		$nV/\sqrt{Hz}$
Input Noise Current (f = 1kHz, R_g = 0Ω)	+25°C		4			4		$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 3)	+25°C	10k	16k		10k	16k		V/V
	Full	5k			5k			V/V
Common-Mode Rejection Ratio (Note 5)	Full	70	90		70	90		dB
Minimum Stable Gain	+25°C	1			1			V/V
Unity Gain-Bandwidth (Note 6)	+25°C		40			40		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 4)	Full	±10	±11		±10	±11		V
Output Current (Note 4)	+25°C	±10	±15		±10	±15		mA
Output Resistance	+25°C		2			2		Ω
Full Power Bandwidth (Note 3 & 7)	+25°C	3	4		3	4		MHz
Differential Gain (Note 2)	+25°C		0.1			0.1		%
Differential Phase (Note 2)	+25°C		0.2			0.2		Degree
Harmonic Distortion (Note 10)	+25°C		<0.01			<0.01		%
TRANSIENT RESPONSE (Note 8)								
Rise Time	+25°C		4			4		ns
Overshoot	+25°C		40			40		%
Slew Rate	+25°C	200	250		200	250		V/µs
Settling Time:								
10V Step to 0.1%	+25°C		90			90		ns
10V Step to 0.01%	+25°C		175			175		ns
POWER REQUIREMENTS								
Supply Current	+25°C		29			29		mA
	Full			40			40	mA
Power Supply Rejection Ratio (Note 9)	Full	70	80		70	78		dB

NOTES:

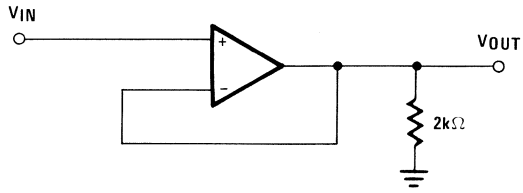
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Differential Gain and Phase are measured with a 1 Volt differential voltage at 5MHz.
3. $V_O = \pm 10V$
4. $R_L = 1k\Omega$
5. $V_{CM} = \pm 10V$
6. $V_O = 90mV$.
7. Full Power Bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$
8. Refer to Test Circuits section of this data sheet.
9. $V_{SUPPLY} = \pm 5VDC$ to $\pm 15VDC$
10. $V_{IN} = 1V_{RMS}$; f = 10kHz; $A_V = 10$
11. This value assumes a no load condition: Maximum power dissipation with load conditions must be designed to maintain the maximum junction temperature below $+175^oC$. By using Application Note 556 on Safe Operating Area equations, along with the packaging thermal resistances listed in the Die Characteristics section, proper load conditions can be determined. Heat sinking is recommended above $+75^oC$ with suggested models:

    14 Lead Ceramic DIP:
    Thermalloy #6007 or AAVID #5602B ($\theta_{sa} = 16^oC/W$).

    12 Lead Metal Can (TO-8):
    Thermalloy #2240A ($\theta_{sa} = 27^oC/W$) or #2268B ($\theta_{sa} = 24^oC/W$)

Test Circuits

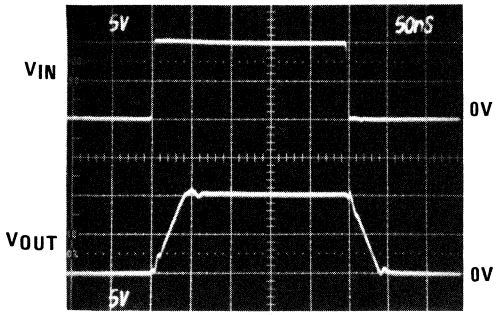
TEST CIRCUIT



$V_S = \pm 15V$
$A_V = +1$
$C_L \leq 10pF$

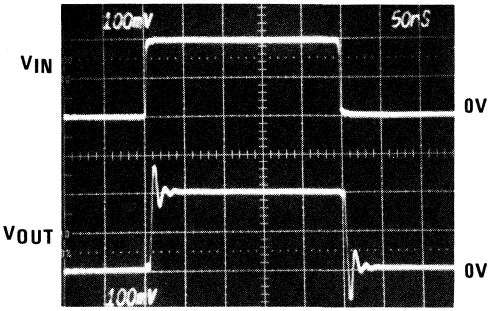
LARGE SIGNAL RESPONSE

Vertical Scale (Volts: 5V/Div.)
Horizontal Scale (Time: 50ns/Div.)



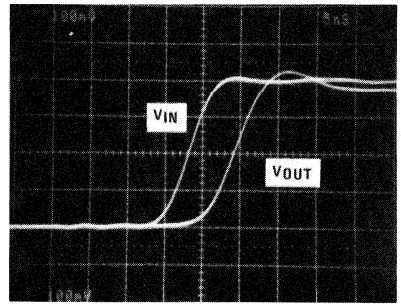
SMALL SIGNAL RESPONSE

Vertical Scale (Volts: 100mV/Div.)
Horizontal Scale (Time: 50ns/Div.)



PROPAGATION DELAY

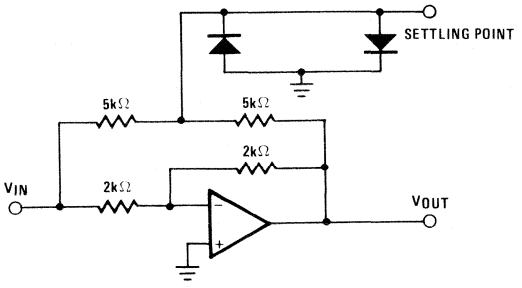
Vertical Scale (Volts: 100mV/Div.)
Horizontal Scale (Time: 5ns/Div.)



$V_S = \pm 15V$, $R_L = 1k\Omega$
$T = +25^oC$
Propagation delay variance is negligible over full temperature range.

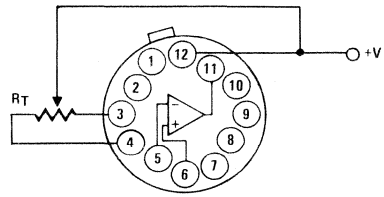
Test Circuits (Continued)

SETTLING TIME TEST CIRCUIT



- $A_V = -1$
- Feedback and Summing Resistors Must Be Matched (0.1%)
- HP5082-2810 Clipping Diodes Recommended
- Tektronix P6201 FET Probe Used At Settling Point.

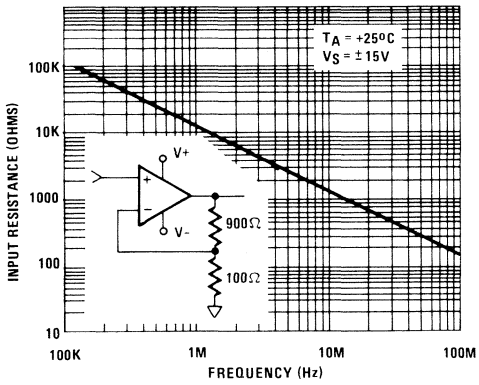
Suggested Offset Voltage Adjustment



Tested Offset Adjustment Range is $| V_{OS} \pm 1mV |$ minimum referred to output. Typical range is ±15mV with $R_T = 5k\Omega$.

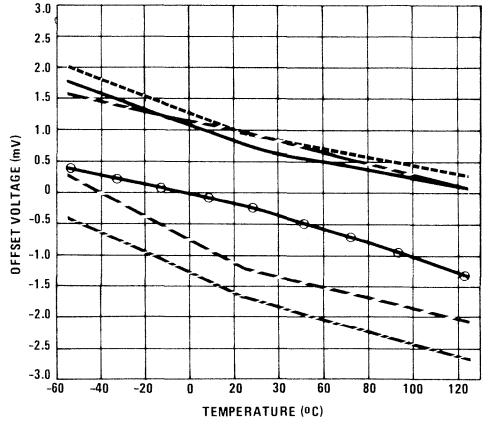
Typical Performance Curves

INPUT RESISTANCE vs. FREQUENCY



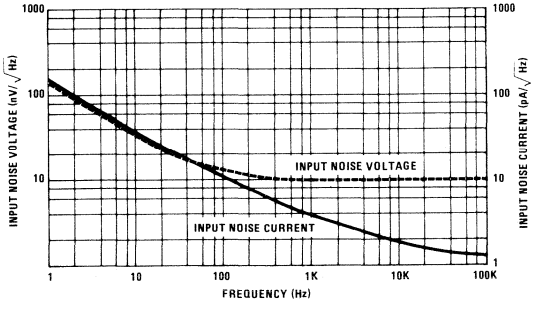
OFFSET VOLTAGE DRIFT WITH TEMPERATURE

Of 6 Representative Units



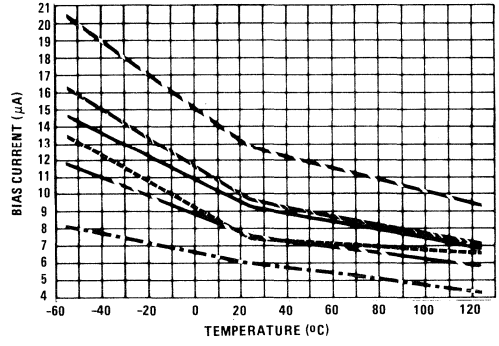
NOISE DENSITY vs. FREQUENCY

$T_A = +25°C$



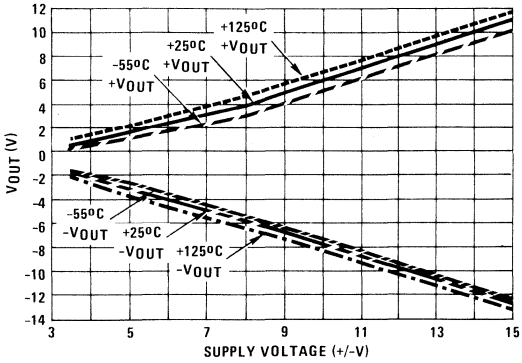
BIAS CURRENT DRIFT WITH TEMPERATURE

Of 6 Representative Units

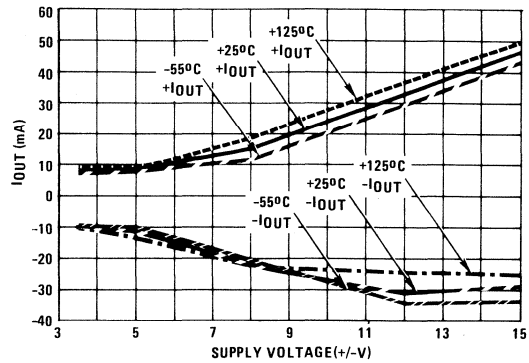


Typical Performance Curves (Continued)

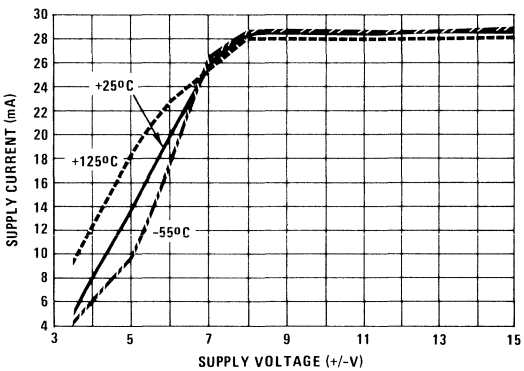
OUTPUT VOLTAGE SWING vs. SUPPLY VOLTAGE
At Various Temperatures



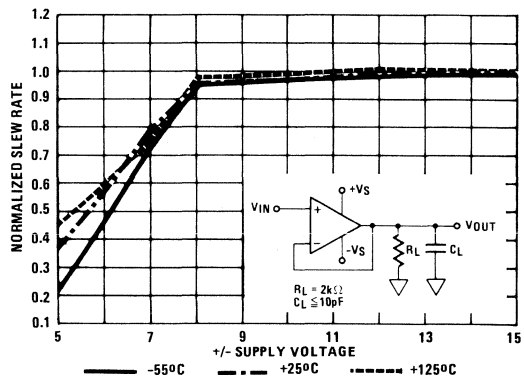
OUTPUT CURRENT vs. SUPPLY VOLTAGE
At Various Temperatures



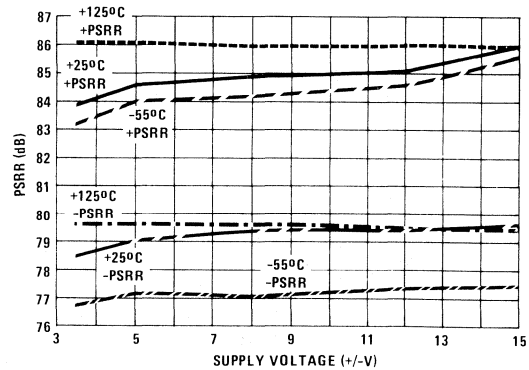
SUPPLY CURRENT vs. SUPPLY VOLTAGE
At Various Temperatures



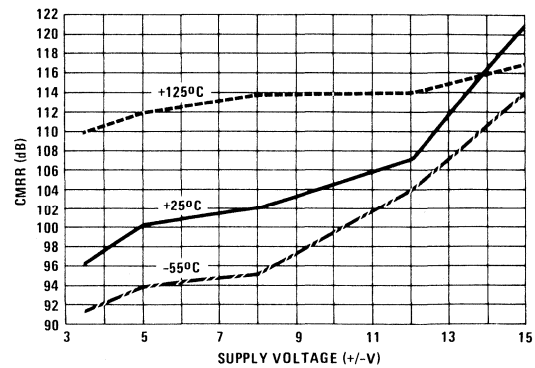
SLEW RATE vs. SUPPLY VOLTAGE
Normalized With V_S = ±15V at +25°C



PSRR vs. SUPPLY VOLTAGE
Average Of 3 Lots At Various Temperatures

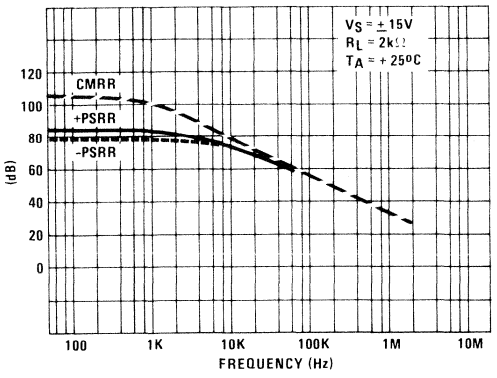


CMRR vs. SUPPLY VOLTAGE
Average of 3 Lots At Various Temperatures

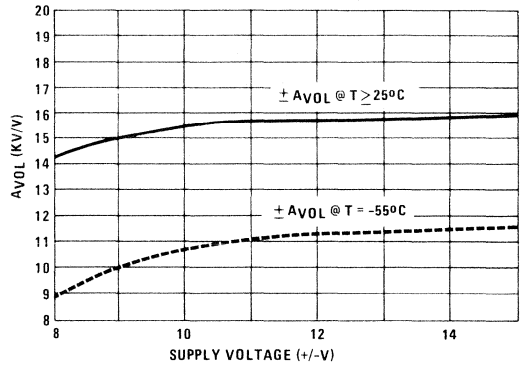


Typical Performance Curves (Continued)

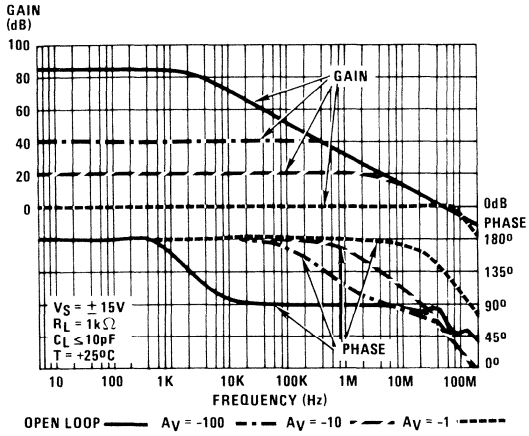
REJECTION RATIOS vs. FREQUENCY



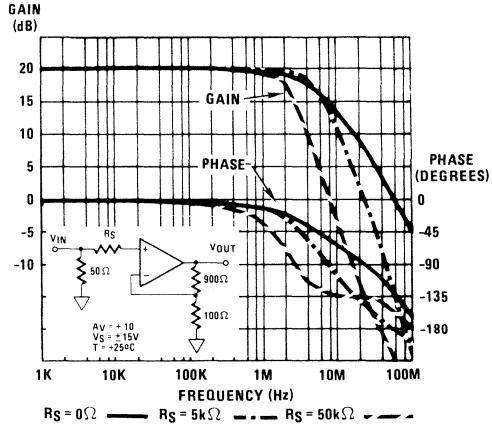
+/- OPEN LOOP GAIN vs. SUPPLY VOLTAGE
Average of 3 Lots Over Temperature



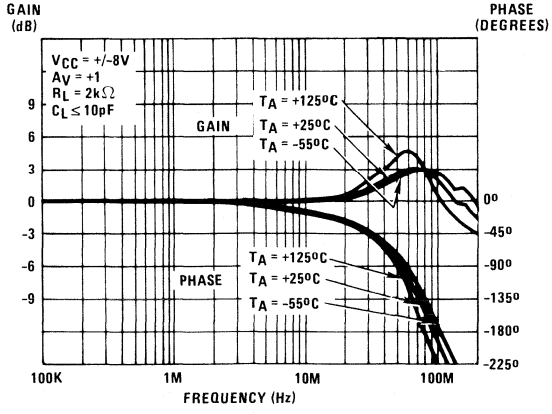
GAIN AND PHASE FREQUENCY RESPONSE
$V_S = \pm 15V$, $R_L = 1k$, $C_L \leq 10pF$, $T_A = +25^oC$



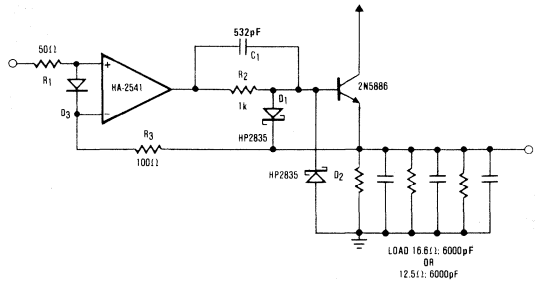
SMALL SIGNAL BANDWIDTH vs. SOURCE RESISTANCE
$V_S = \pm 15V$, $R_L = 1k\Omega$



CLOSE LOOP FREQUENCY RESPONSE vs. TEMPERATURE



Applications (Also See Application Note 550)



APPLICATION 1. DRIVING POWER TRANSISTORS TO GAIN ADDITIONAL CURRENT BOOSTING

APPLICATION 1

High power amplifiers and buffers are in use in a wide variety of applications. Many times the "high power" capability is needed to drive large capacitive loads as well as low value resistive loads. In both cases the final driver stage is usually a power transistor of some type, but because of their inherently low gain, several stages of pre-drivers are often required. The HA-2541, with its 10mA output rating, is powerful enough to drive a power transistor without additional stages of current amplification. This capability is well demonstrated with the high power buffer circuit in Application 1.

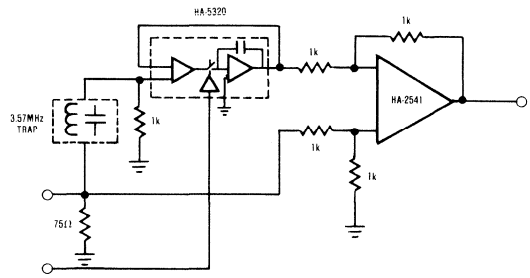
The HA-2541 acts as the pre-driver to the output power transistor. Together, they form a unity gain buffer with the ability to drive three 50 ohm coaxial cables in parallel, each with a capacitance of 2000pF. The total combined load is 16.6 ohms and 6000pF capacitance.

APPLICATION 2

Video

One of the primary uses of the HA-2541 is in the area of video applications. These applications include signal construction, synchronization addition and removal, as well as signal modification. A wide bandwidth device such as the HA-2541 is well suited for use in this class of amplifier. This, however, is a more involved group of applications than ordinary amplifier applications since video signals contain precise DC levels which must be retained.

The addition of a clamping circuit restores D.C. levels at the output of an amplifier stage. The circuit shown in Application 2 utilizes the HA-5320 sample and hold amplifier as the D.C. clamp. Also shown is a 3.57MHz trap in series, which will block the color burst portion of the video signal and allow the D.C. level to be amplified and restored.



APPLICATION 2. VIDEO D.C. RESTORER

Die Characteristics

Transistor Count 41
Die Dimensions ..... 89 x 79 x 19 mils
(2250μm x 1990μm x 485μm)
Substrate Potential (Powered Up)* ..... V–
Process: ..... High Frequency Bipolar
Dielectric Isolation
Passivation ..... Silox

Thermal Constants (^{o}C/W)	θja	θjc
Ceramic DIP	91	35
Metal Can	66	30

*The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.

HA-2542

Wideband, High Slew Rate, High Output Current Operational Amplifier

Features

- Stable at Gains of 2 or Greater
- Gain Bandwidth.....70MHz
- High Slew Rate (Min.).....300V/μs
- High Output Current (Min.).....100mA
- Power Bandwidth (Typ.).....5.5MHz
- Output Voltage Swing (Min.)..... $\pm$10V
- Monolithic Bipolar Dielectric Isolation Construction

Applications

- Pulse and Video Amplifiers
- Wideband Amplifiers
- Coaxial Cable Drivers
- Fast Sample-Hold Circuits
- High Frequency Signal Conditioning Circuits

Description

The HA-2542 is a wideband, high slew rate, monolithic operational amplifier featuring an outstanding combination of speed, bandwidth, and output drive capability.

Utilizing the advantages of the Harris D. I. technology this amplifier offers 350V/μs slew rate, 70MHz gain bandwidth, and $\pm$100mA output current. Application of this device is further enhanced through stable operation down to closed loop gains of 2.

For additional flexibility, offset null and frequency compensation controls are included in the HA-2542 pinout.

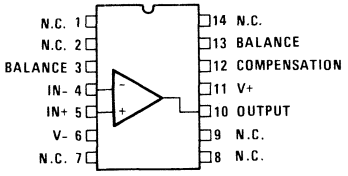
The capabilities of the HA-2542 are ideally suited for high speed coaxial cable driver circuits where low gain and high output drive requirements are necessary. With 5.5MHz full power bandwidth, this amplifier is most suitable for high frequency signal conditioning circuits and pulse video amplifiers. Other applications utilizing the HA-2542 advantages include wideband amplifiers and fast sample-hold circuits.

The HA-2542 is available in ceramic or plastic 14 lead DIP packages, or a 12 lead metal can (TO-8) which is pin compatible with the HA-2541, HA-5190, LH0032 and HOS-050C. The HA-2542-2 is specified over the -55°C to +125°C temperature range and is also offered as a military part. The HA-2542-5 is specified over the commercial temperature range of 0°C to 75°C.

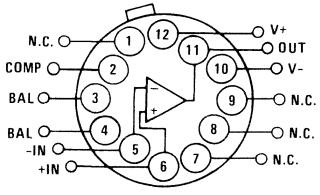
For more information on the HA-2542, please refer to Application Note 552 (Using The HA-2542), or Application Note 556 (Thermal Safe-Operating-Areas For High Current Op Amps).

Pinouts

HA1-2542 (CERAMIC DIP)
HA3-2542 (PLASTIC DIP)
TOP VIEW

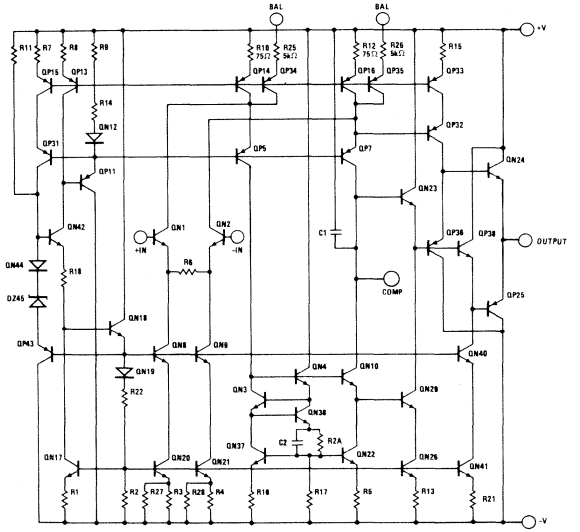


HA2-2542 (TO-8 METAL CAN)
TOP VIEW



V_{CASE} = V-

Schematic



CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

Voltage between V+ and V- Terminals 35V
Differential Input Voltage ..... ±6V
Output Current ..... 125mA (Peak)
107mA rms (Continuous)

Operating Temperature Range:

HA-2542-2 ..... $-55^oC \leq T_A \leq +125^oC$
HA-2542-5 ..... $0^oC \leq T_A \leq +75^oC$
Storage Temperature Range ..... $-65^oC \leq T_A \leq +150^oC$
Maximum Junction Temperature (Note 11) ..... $+175^oC$

Electrical Specifications $V_{SUPPLY} = \pm 15$ Volts; $R_L = 1k\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified.

PARAMETER	TEMP	HA-2542-2 -55°C to +125°C MIN	TYP	MAX	HA-2542-5 0°C to +75°C MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		5	10		5	10	mV
	Full		8	20		8	20	mV
Average Offset Voltage Drift	Full		14			14		µV/°C
Bias Current	+25°C		15	35		15	35	µA
	Full		26	50		26	50	µA
Average Bias Current Drift	Full		66			45		nA/°C
Offset Current	+25°C		1	7		1	7	µA
	Full			9			9	µA
Input Resistance	+25°C		100			100		kΩ
Input Capacitance	+25°C		1			1		pF
Common Mode Range	Full	±10			±10			V
Input Noise Voltage (0.1Hz to 100Hz)	+25°C		2.2			2.2		μV_{p-p}
Input Noise Voltage Density (fo = 1kHz, R_g = 0Ω)	+25°C		10			10		$nV/\sqrt{Hz}$
Input Noise Current Density (fo = 1kHz, R_g = 0Ω)	+25°C		3			3		$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 3)	+25°C	10k	30k		10k	30k		V/V
	Full	5k	15k		5k	20k		V/V
Common-Mode Rejection Ratio (Note 4)	Full	70	100		70	100		dB
Minimum Stable Gain	+25°C	2			2			V/V
Gain-Bandwidth-Product (Note 5)	+25°C		70			70		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 3)	Full	±10	±11		±10	±11		V
Output Current (Note 6)	+25°C	100			100			mA
Output Resistance	+25°C		5			5		Ω
Full Power Bandwidth (Note 3 & 7)	+25°C	4.7	5.5		4.7	5.5		MHz
Differential Gain (Note 2)	+25°C		0.1			0.1		%
Differential Phase (Note 2)	+25°C		0.2			0.2		Degrees
Harmonic Distortion (Note 10)	+25°C		<0.04			<0.04		%
TRANSIENT RESPONSE (Note 8)								
Rise Time	+25°C		4			4		ns
Overshoot	+25°C		25			25		%
Slew Rate	+25°C	300	350		300	350		V/µs
Settling Time:								
10V Step to 0.1%	+25°C		100			100		ns
10V Step to 0.01%	+25°C		200			200		ns
POWER REQUIREMENTS								
Supply Current	+25°C		30			30		mA
	Full		31	34.5		31	40	mA
Power Supply Rejection Ratio (Note 9)	Full	70	79		70	79		dB

NOTES:

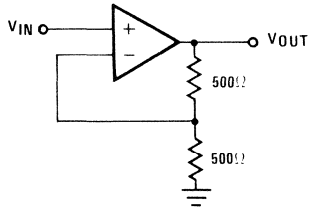
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Differential gain and phase are measured at 5MHz with a 1 Volt differential input voltage.
3. $R_L = 1k\Omega$, $V_O = \pm 10V$
4. $V_{CM} = \pm 10V$
5. $A_{VCL} = 100$
6. $R_L = 50\Omega$, $V_O = \pm 5V$
7. Full Power Bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$
8. Refer to Test Circuits section of this data sheet.
9. $V_{SUPPLY} = \pm 5VDC$ to $\pm 15VDC$
10. $V_{IN} = 1V_{RMS}$; f = 10kHz; $A_V = 10$.
11. This value assumes a no load condition: Maximum power dissipation with load conditions must be designed to maintain the maximum junction temperature below $+175^oC$. By using Application Note 556 on Safe Operating Area equations, along with the packaging thermal resistances listed in the Die Characteristics section, proper load conditions can be determined. Heat sinking is recommended above $+75^oC$ with suggested models.

    14 Lead Ceramic DIP:
    Thermalloy #6007 or AAVID #5602B ($\theta_{sa} = 16^oC/W$).

    12 Lead Metal Can (TO-8):
    Thermalloy #2240A ($\theta_{sa} = 27^oC/W$) or #2268B ($\theta_{sa} = 24^oC/W$)

Test Circuits

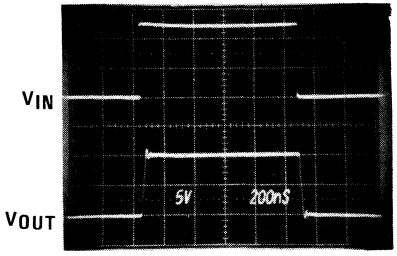
TEST CIRCUIT



$V_S = \pm 15V$
$A_V = +2$
$C_L \leq 10pF$

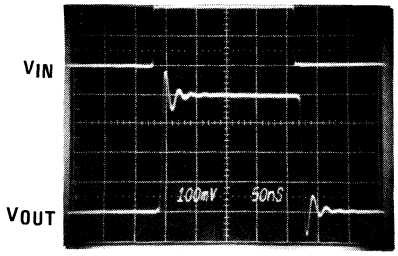
LARGE SIGNAL RESPONSE

Vertical Scale (Volts: V_{IN} = 2.0V/Div., V_{OUT} = 5.0V/Div.)
Horizontal Scale (Time: 200ns/Div.)



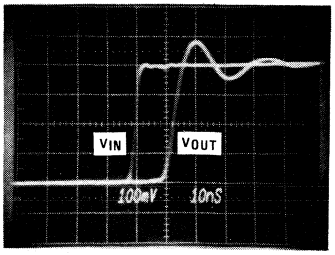
SMALL SIGNAL RESPONSE

Vertical Scale (Volts: 100mV/Div.)
Horizontal Scale (Time: 50ns/Div.)



TIME DELAY

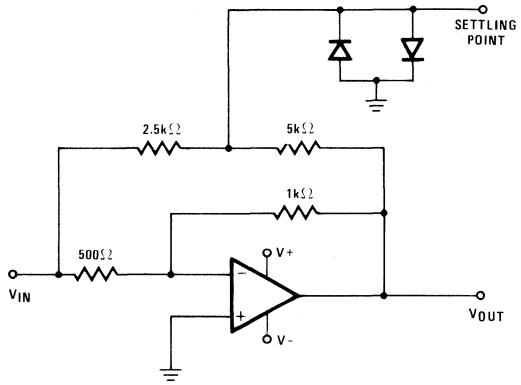
Vertical Scale (Volts: 100mV/Div.)
Horizontal Scale (Time: 10ns/Div.)



$V_S = \pm 15V$, $R_L = 1k\Omega$
$T = +25^oC$
Propagation delay variance is negligible over full temperature range.

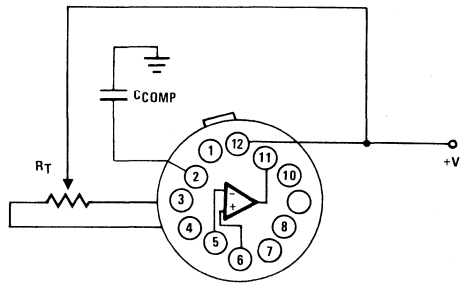
Test Circuits (Continued)

SETTLING TIME TEST CIRCUIT



- A_V = -2
- Feedback and summing resistors must be matched (0.1%)
- HP5082-2810 clipping diodes recommended
- Tektronix P6201 FET probe used at settling point
- For 0.01% settliing time, heat sinking is suggested to reduce thermal effects and an analog ground plane with supply decoupling is suggested to minimize ground loop errors.

SUGGESTED OFFSET VOLTAGE ADJUSTMENT

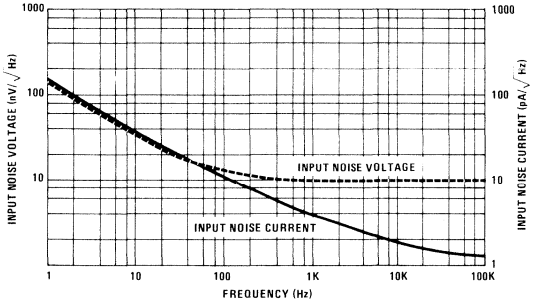


Suggested compensation scheme 5-20pF

Tested Offset Adjustment Range is $|V_{OS} \pm 1mV|$ minimum referred to output. Typical range is +20mV with R_T = 5kΩ.

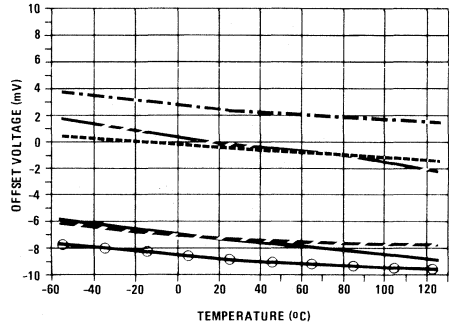
Typical Performance Curves

INPUT NOISE VOLTAGE AND INPUT NOISE CURRENT vs. FREQUENCY

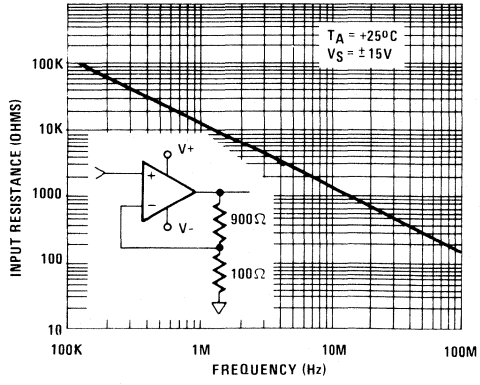


OFFSET VOLTAGE DRIFT WITH TEMPERATURE

Of Six Representative Units, V_S = +/−12V

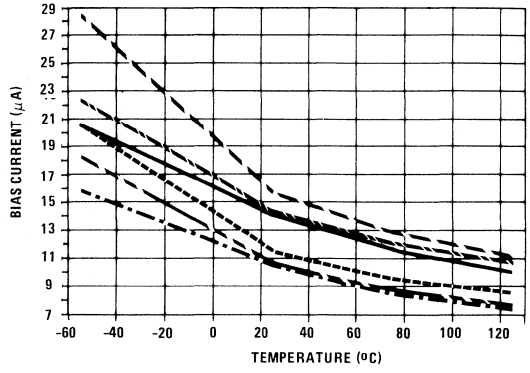


INPUT RESISTANCE vs. FREQUENCY



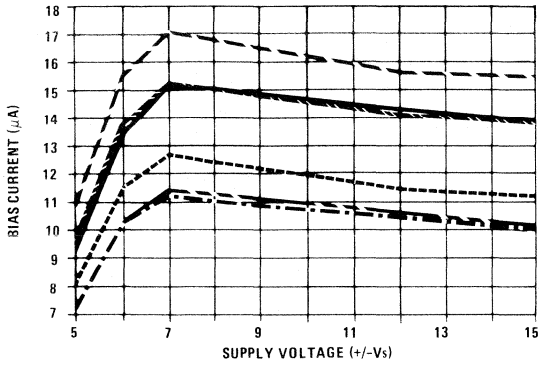
BIAS CURRENT DRIFT WITH TEMPERATURE

Of Six Representative Units, V_S = +/−12V

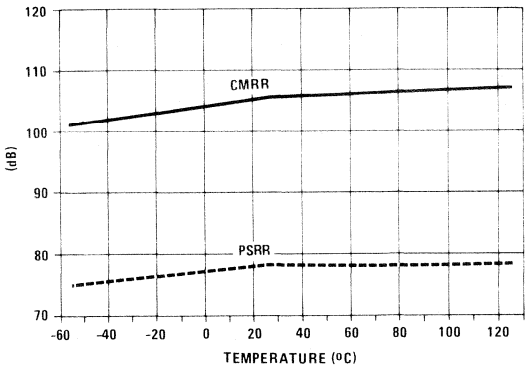


Typical Performance Curves (Continued)

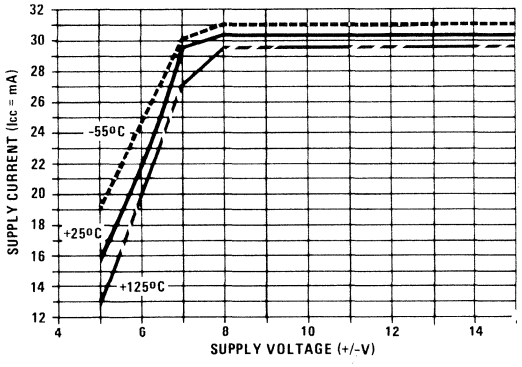
BIAS CURRENT vs. POWER SUPPLY
Six Units At Various Supplies At +25°C



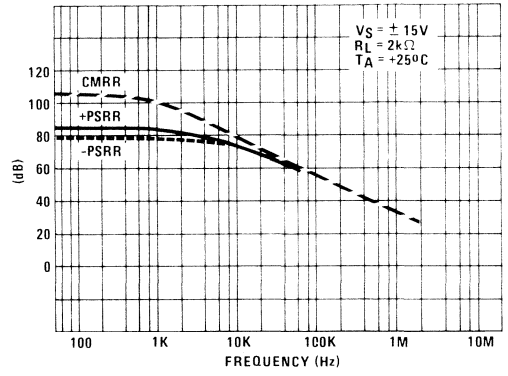
PSRR AND CMRR vs. TEMPERATURE
$V_S = \pm 15V$



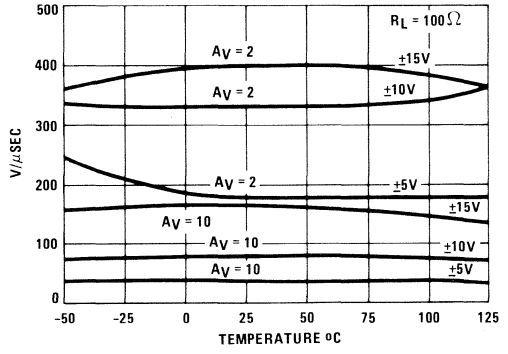
SUPPLY CURRENT vs. SUPPLY VOLTAGE
At Various Temperatures



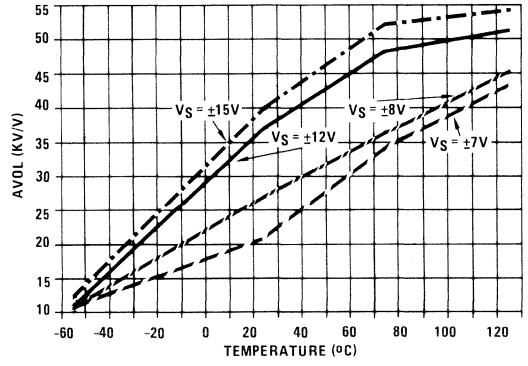
PSRR AND CMRR vs. FREQUENCY



SLEW RATE vs. TEMPERATURE
At Various Supply Voltages With $R_{Load} = 100\Omega$

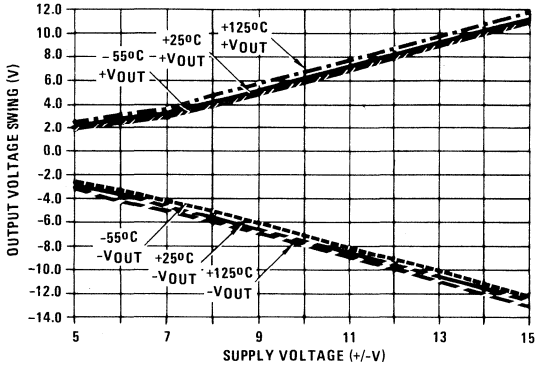


OPEN LOOP GAIN vs. TEMPERATURE
At Various Supply Voltages

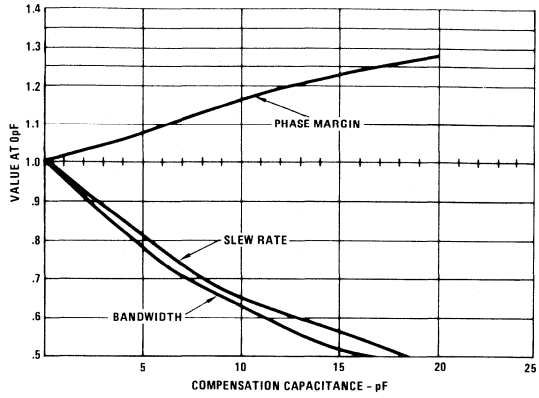


Typical Performance Curves (Continued)

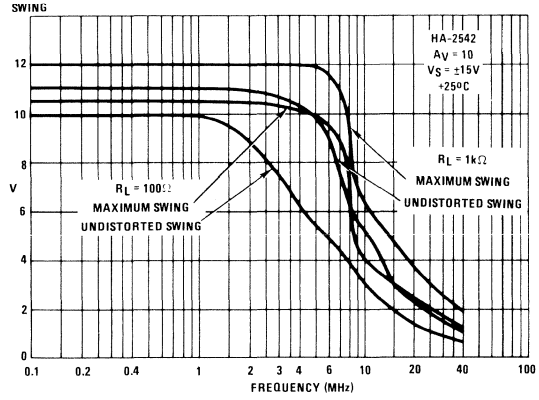
OUTPUT VOLTAGE SWING vs. SUPPLY VOLTAGE
At Various Temperatures



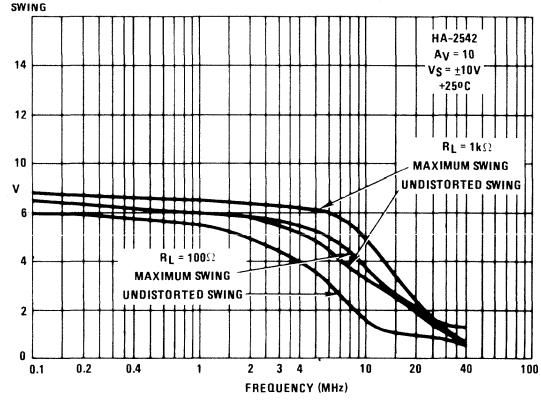
NORMALIZED AC PARAMETERS vs. COMPENSATION CAPACITANCE



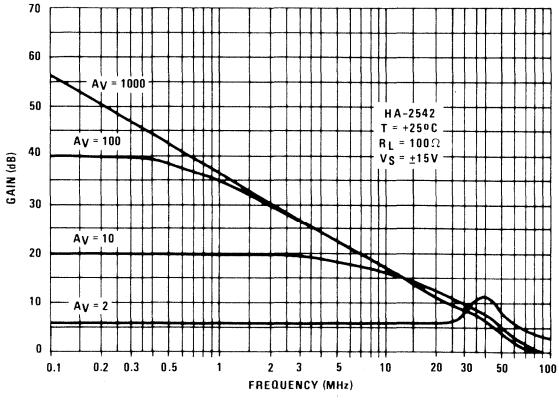
OUTPUT VOLTAGE SWING vs. FREQUENCY
$V_S = \pm 15V$



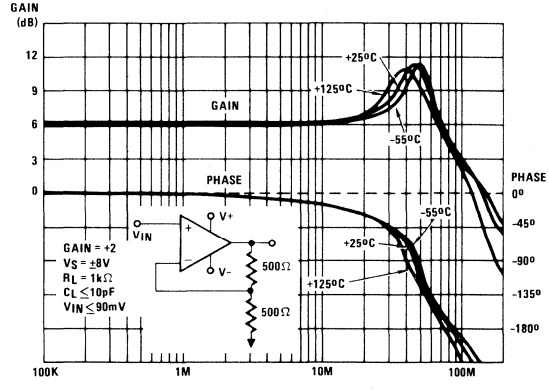
OUTPUT VOLTAGE SWING vs. FREQUENCY
$V_S = \pm 10V$



FREQUENCY RESPONSE CURVES



HA-2542 CLOSED LOOP GAIN vs. TEMPERATURE



Die Characteristics

Transistor Count 43
Die Dimensions ..... 72 x 105 x 19 mils (1820µm x 2670µm x 485µm)
Substrate Potential* ..... V-
Process ..... High Frequency Bipolar-DI
Passivation ..... Nitride

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
HA1-2542 Ceramic DIP	86.6	32.5
HA3-2542 Plastic DIP	78.8	30.6
HA2-2542 Metal Can	58	29

*The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.

Typical Applications (Refer to Application Note 552 for Further Information)

The Harris HA-2542 is a state of the art monolithic device which also approaches the "ALL-IN-ONE" amplifier concept. This device features an outstanding set of AC parameters augmented by excellent output drive capability providing for suitable application in both high speed and high output drive circuits.

Primarily intended to be used in balanced 50Ω and 75Ω coaxial cable systems as a driver, the HA-2542 could also be used as a power booster in audio systems as well as a power amp in power supply circuits. This device would also be suitable as a small DC motor driver.

The applications shown on the following page demonstrate the HA-2542 at gains of +100 and +2 and as a video cable driver for small signals.

Prototyping Guidelines

For best overall performance in any application, it is recommended that high frequency layout techniques be used. This should include: 1) mounting the device through a ground plane: 2) connecting unused pins (N.C.) to the ground plane: 3) mounting feedback components on Teflon standoffs and/or locating these components as close to the device as possible; 4) placing power supply decoupling capacitors from device supply pins to ground.

As a result of speed and bandwidth optimization, the HA-2542 can's case potential, when powered-up, is equal to the V- potential. Therefore, contact with other circuitry or ground should be avoided.

Frequency Compensation

The HA-2542 may be externally compensated with a single capacitor to ground. This provides the user the additional flexibility in tailoring the frequency response of the amplifier. A guideline to the response is demonstrated on the typiical performance curve showing the normalized A.C. parameters versus compensation capacitance. It is suggested that the user check and tailor the accurate compensation value for each application. As shown additional phase margin is achieved at the loss of slew rate and bandwidth.

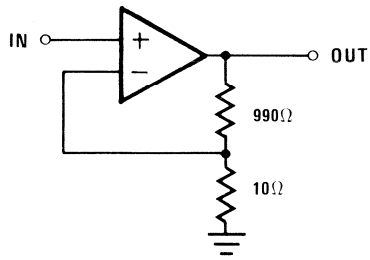
For example, for a voltage gain of +2 (or -1) and a load of 500pF/2kΩ, 20pF is needed for compensation to give a small signal bandwidth of 30MHz with 40° of phase margin. If a full power output voltage of ±10V is needed, this same configuration will provide a bandwidth of 5MHz and a slew rate of 200V/µs.

If maximum bandwidth is desired and no compensation is needed, care must be given to minimize parasitic capacitance at the compensation pin. In some cases where minimum gain applications are desired, bending up or totally removing this pin may be the solution. In this case, care must also be given to minimize load capacitance.

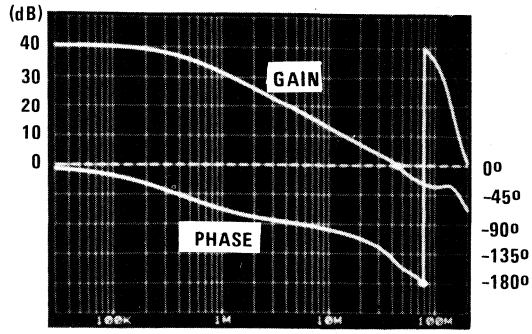
For wideband positive unity gain applications, the HA-2542 can also be over-compensated with capacitance greater than 30pF to achieve bandwidths of around 25MHz. This over-compensation will also improve capacitive load handling or lower the noise bandwidth. This versatility along with the ±100mA output current makes the HA-2542 an excellent high speed driver for many power applications.

Typical Applications

NONINVERTING CIRCUIT (A_{VCL} = 100)

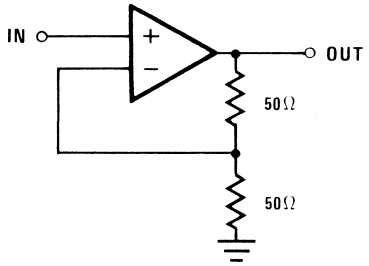


FREQUENCY (0dB) = 44.9MHz
PHASE MARGIN (0dB) = 40°

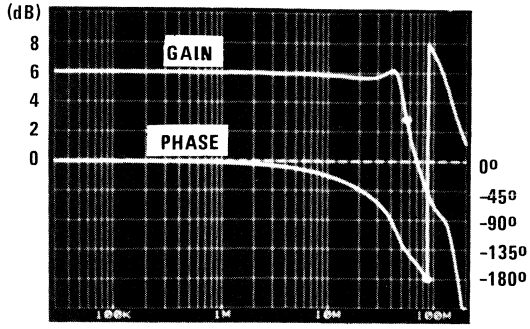


AV_{CL} = 100 PHASE AND GAIN

NONINVERTING CIRCUIT (A_{VCL} = 2)

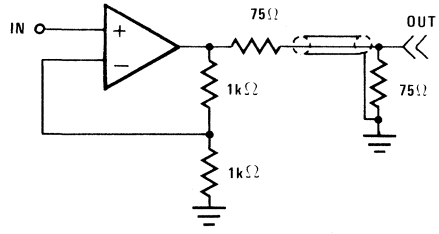


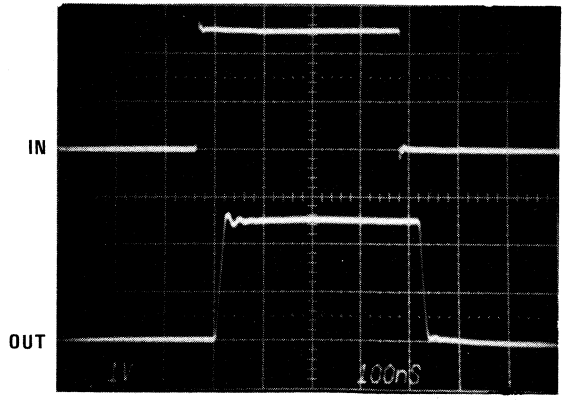
FREQUENCY (3dB) = 56MHz
PHASE (3dB) = 40°



AV_{CL} = 2 PHASE AND GAIN

VIDEO CABLE DRIVER (AV_{CL} = 2)





VIDEO CABLE DRIVER PULSE RESPONSE
(1V/Div.; 100ns/Div.)

HA-2544

Video Operational Amplifier

Features

- Gain Bandwidth 50MHz
- High Slew Rate 150V/μs
- Low Supply Current 10mA
- Differential Gain Error ..... <0.05dB
- Differential Phase Error ..... <0.1 degree
- Gain Tolerance at 5MHz ..... <0.15dB

Applications

- Video Systems
- Video Test Equipment
- Radar Displays
- Imaging Systems
- Pulse Amplifiers
- Signal Conditioning Circuits
- Data Acquisition Systems

Description

The HA-2544 is a fast, unity gain stable, monolithic op amp designed to meet the needs required for accurate reproduction of video or high speed signals. It offers high voltage gain (6kV/V) and high phase margin (65 degrees) while maintaining tight gain tolerance over the video bandwidth. Built from high quality Dielectric Isolation, the HA-2544 is another addition to the Harris series of high speed, wideband op-amps, and offers true video performance combined with the versatility of an op-amp.

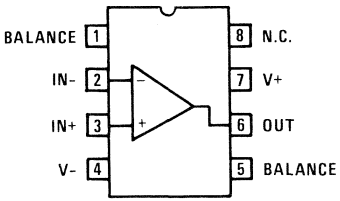
The primary features of the HA-2544 include 50MHz Gain Bandwidth, 150V/μs slew rate, < 0.05dB differential gain error and gain tolerance of just 0.15dB at 5MHz. High performance and low power requirements are met with a supply current of only 10mA.

Uses of the HA-2544 range from video test equipment guidance systems, radar displays and other precise imaging systems where stringent gain and phase requirements have previously been met with costly hybrids and discrete circuitry. The HA-2544 will also be used in non-video systems requiring high speed signal conditioning such as data acquisition systems, medical electronics, specialized instrumentation and communication systems.

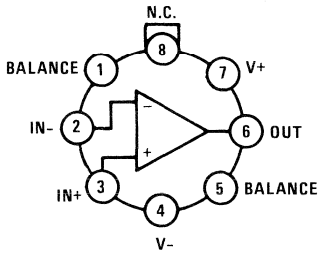
The HA-2544-2 is guaranteed over the military temperature range (-55°C to +125°C); the HA-2544-5 and the HA-2544C-5 over the commercial temperature range (0°C to +75°C). The HA-2544 is available in TO-99 Metal Can, and both Plastic and Ceramic Mini-DIP packages. Military (/883) product and data sheets are available upon request.

Pinouts

HA7-2544 (CERAMIC MINI-DIP)
HA3-2544/2544C (PLASTIC MINI-DIP)
TOP VIEW

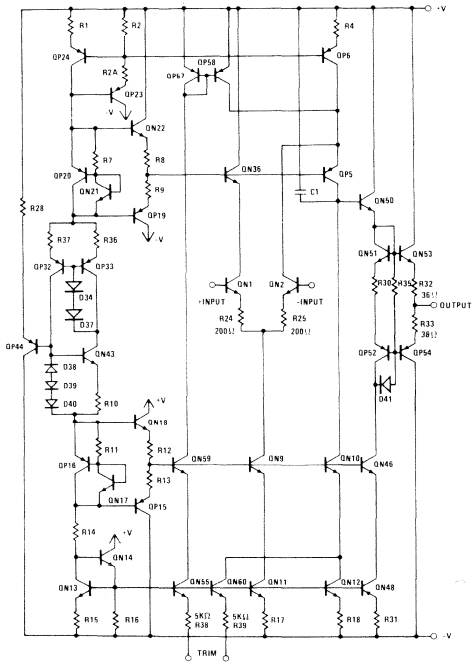


HA2-2544 (TO-99 METAL CAN)
TOP VIEW



NOTE: $V_{CASE} = V-$

Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Terminals 33V
Differential Input Voltage (Note 11) ..... ±6V
Output Current (Peak) ..... ±40mA
Internal Power Dissipation 700mW
Maximum Junction Temperature ..... +175°C

Operating Temperature Range

HA-2544C-5 ..... $0^{o}C \leq T_A \leq +75^{o}C$
HA-2544-5 ..... $0^{o}C \leq T_A \leq +75^{o}C$
HA-2544-2 ..... $-55^{o}C \leq T_A \leq +125^{o}C$
Storage Temperature Range ..... $-65^{o}C \leq T_A \leq +150^{o}C$

Electrical Specifications

$V_S = \pm 15V$, $C_L \leq 10pF$, $R_L = 1k\Omega$, Unless Otherwise Specified.

PARAMETER	TEMP	HA-2544-2/-5			HA-2544C-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Offset Voltage	+25°C	-	6	15	-	15	25	mV
	Full	-	-	20	-	-	40	mV
Average Offset Voltage Drift (Note 9)	Full	-	10	-	-	10	-	µV/°C
Bias Current	+25°C	-	7	15	-	9	18	µA
	Full	-	-	20	-	-	30	µA
Average Bias Current Drift (Note 9)	Full	-	0.04	-	-	0.04	-	µA/°C
Offset Current	+25°C	-	0.2	2	-	0.8	2	µA
	Full	-	-	3	-	-	3	µA
Offset Current Drift	Full	-	10	-	-	10	-	nA/°C
Common Mode Range	Full	±10	±11.5	-	±10	±11.5	-	V
Differential Input Resistance	+25°C	50	90	-	50	90	-	kΩ
Differential Input Capacitance	+25°C	-	3	-	-	3	-	pF
Input Noise Voltage (f = 1kHz)	+25°C	-	20	-	-	20	-	$nV/\sqrt{Hz}$
Input Noise Current (f = 1kHz)	+25°C	-	2.4	-	-	2.4	-	$pA/\sqrt{Hz}$
Input Noise Voltage								
0.1Hz to 10Hz (Note 9)	+25°C	-	1.5	-	-	1.5	-	µV p-p
0.1Hz to 1MHz	+25°C	-	4.6	-	-	4.6	-	µV r.m.s.
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Notes 4, 9)	+25°C	3.5	6	-	3	6	-	kV/V
	Full	2.5	-	-	2	-	-	kV/V
Common Mode Rejection Ratio (Notes 6, 9)	Full	75	89	-	70	89	-	dB
Minimum Stable Gain	+25°C	+1	-	-	+1	-	-	V/V
Unity Gain Bandwidth (Notes 3, 9)	+25°C	-	45	-	-	45	-	MHz
Gain Bandwidth Product (Notes 3, 9)	+25°C	-	50	-	-	50	-	MHz
Phase Margin	+25°C	-	65	-	-	65	-	Degrees

Electrical Specifications (Continued)

PARAMETER	TEMP	HA-2544-2/-5			HA-2544C-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT CHARACTERISTICS								
Output Voltage Swing	Full	±10	±11	-	±10	±11	-	V
Full Power Bandwidth (Note 7)	+25°C	3.2	4.2	-	3.2	4.2	-	MHz
Peak Output Current (Notes 9, 10)	+25°C	±25	±35	-	±25	±35	-	mA
Continuous Output Current (Notes 9, 10)	+25°C	±10	-	-	±10	-	-	mA
Output Resistance (Open Loop)	+25°C	-	20	-	-	20	-	Ω
TRANSIENT RESPONSE								
Rise Time (Note 3)	+25°C	-	7	-	-	7	-	ns
Overshoot (Note 3)	+25°C	-	10	-	-	10	-	%
Slew Rate	+25°C	100	150	-	100	150	-	V/μs
Settling Time (Note 5)	+25°C	-	120	-	-	120	-	ns
VIDEO PARAMETERS $R_S = 50\Omega$, $R_L = 1k\Omega$ (Notes 2,10)								
Differential Phase (Note 2,12)								
$R_S = 50\Omega$	+25°C	-	0.05	0.11	-	0.05	0.11	Degree
$R_S = 1k\Omega$	+25°C	-	0.4	-	-	0.4	-	Degree
Differential Gain (Note 2, 12, 14)							-	
$R_S = 50\Omega$	+25°C	-	0.02	0.04	-	0.02	0.04	dB
$R_S = 50\Omega$	+25°C	-	0.23	0.46	-	0.23	0.46	%
$R_S = 1k\Omega$	+25°C	-	0.15	-	-	0.15	-	dB
$R_S = 1k\Omega$	+25°C	-	1.7	-	-	1.7	-	%
Gain Tolerance (Note 2, 3)								
5MHz	+25°C	-	-0.10	±0.15	-	-0.10	±0.15	dB
10MHz	+25°C	-	-0.12	±0.35	-	-0.12	±0.35	dB
Chrominance to Luminance Gain (Note 13)	+25°C	-	0.1	-	-	0.1	-	dB
Chrominance to Luminance Delay (Note 13)	+25°C	-	7	-	-	7	-	ns
POWER SUPPLY CHARACTERISTICS								
Supply Current	Full	-	10	12	-	10	15	mA
Power Supply Rejection Ratio (Notes 8, 9)	Full	70	80	-	70	80	-	dB

NOTES:

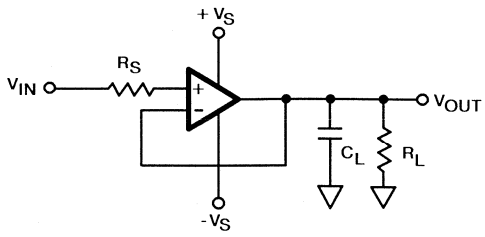
1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Guaranteed by sample test and not 100% tested.
3. $V_{OUT} = \pm 100mV$. For Rise Time and Overshoot testing, V_{OUT} is measured from 0 to +200mV and 0 to -200mV.
4. $V_{OUT} = \pm 5V$
5. Settling Time is specified to 0.1% of final value for a 10V step and $A_V = -1$
6. $\Delta V_{CM} = \pm 10V$
7. Full Power Bandwidth is guaranteed by equation:

   $$\text{Full Power Bandwidth} = \frac{\text{Slew Rate}}{2\pi\ V_{peak}} \quad (V_{peak} \text{ used} = 5V)$$

8. $\Delta V_S = \pm 10$ to $\pm 20V$
9. Refer to typical performance curve in Data Sheet.
10. The video parameter specifications will degrade as the output load resistance decreases.
11. To achieve optimum AC performance, the input stage was designed without protective diode clamps. Exceeding the maximum differential input voltage results in reverse breakdown of the base-emitter junction of the input transistors and probable degradation of the input parameters especially V_{OS}, I_{OS} and Noise.
12. Test signal used is ±200mV at 5MHz on a 0 and 1 Volt offset. For adaquate test repeatability, a minimum warm-up of 2 minutes is suggested.
13. C-L Gain and C-L Delay was less than the resolution of the test equipment used which is 0.1dB and 7ns, respectively.
14. $A_{D(\%)} = \left[10^{\frac{A_{D(dB)}}{20}} - 1 \right] \times 100$

Test Circuits

TRANSIENT RESPONSE

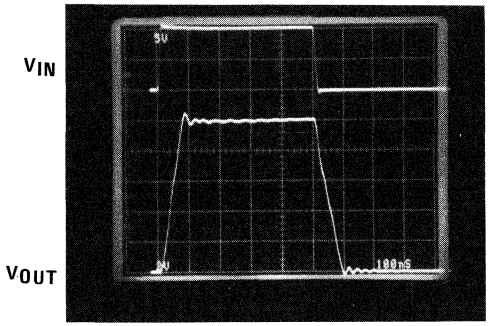


$V_S = \pm 15V$
$A_V = +1$
$R_S = 50$ or 75Ω (Optional)
$R_L = 1k\Omega$
$C_L < 10pF$

V_{IN} for Large Signal = ±5V
V_{IN} for Small Signal = 0 to +200mV and 0 to -200mV

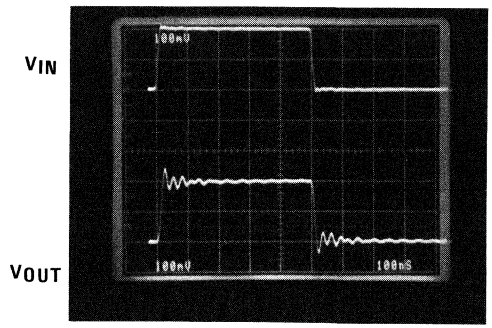
LARGE SIGNAL RESPONSE

V_{OUT} = 0 to +10V
Vertical Scale: (V_{IN} = 5V/Div.; V_{OUT} = 2V/Div.)
Horizontal Scale: (100ns/Div.)

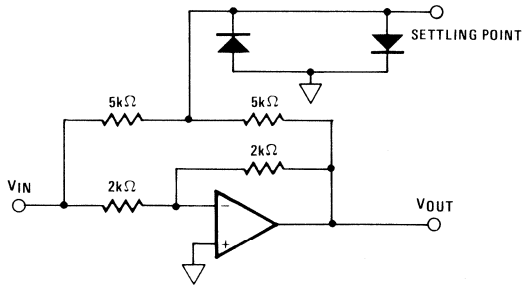


SMALL SIGNAL RESPONSE

V_{OUT} = 0 to +200mV
Vertical Scale: (V_{IN} = 100mV/Div.; V_{OUT} = 100mV/Div.)
Horizontal Scale: (100ns/Div.)

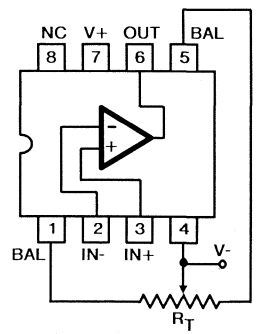


SETTLING TIME TEST CIRCUIT



- $A_V = -1$
- Feedback and Summing Resistors Must Be Matched (0.1%)
- HP5082-2810 Clipping Diodes Recommended.
- Tektronix P6201 FET Probe Used At Settling Point.

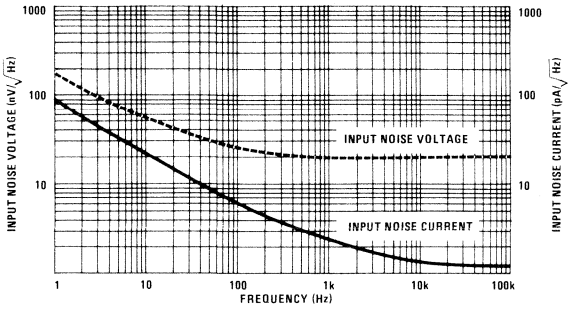
OFFSET VOLTAGE ADJUSTMENT



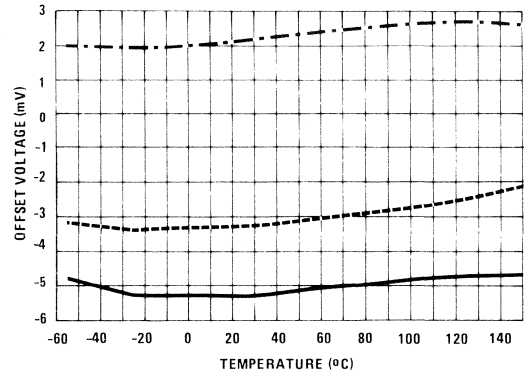
Tested Offset Adjustment Range Is | V_{OS} +1mV | Minimum Referred To Output. Typical Range For R_T = 20kΩ Is Approximately ±30mV

Typical Performance Curves

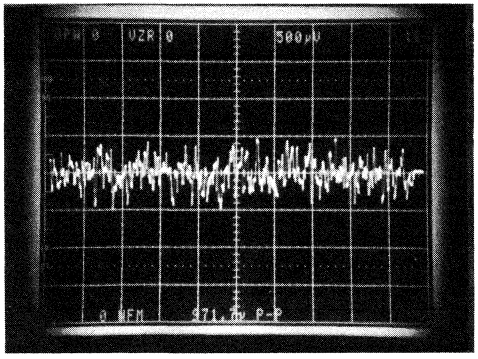
INPUT NOISE VOLTAGE AND NOISE CURRENT vs. FREQUENCY



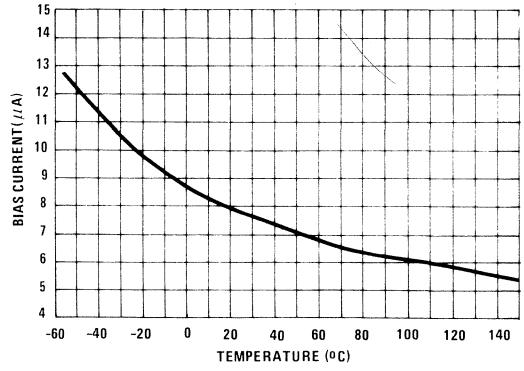
INPUT OFFSET VOLTAGE vs.TEMPERATURE
3 Typical Units



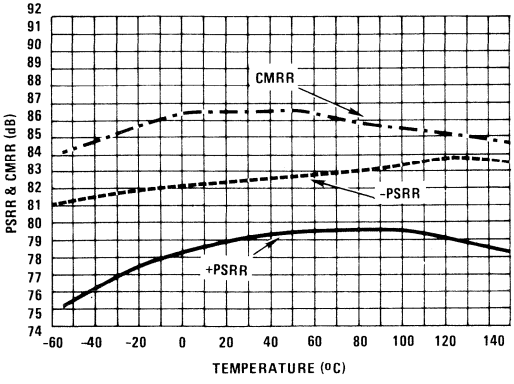
BROADBAND NOISE
(A_V = 1000)
0.1Hz to 10Hz, Noise Voltage = 0.97μVp-p



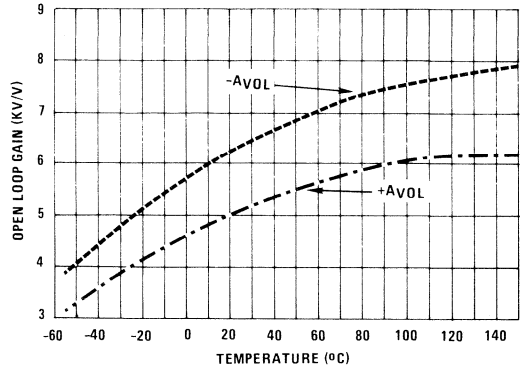
INPUT BIAS CURRENT vs. TEMPERATURE
V_S = ±15V, R_L = 1kΩ



PSRR and CMRR vs. TEMPERATURE
V_S = ±15V, R_L = 1kΩ

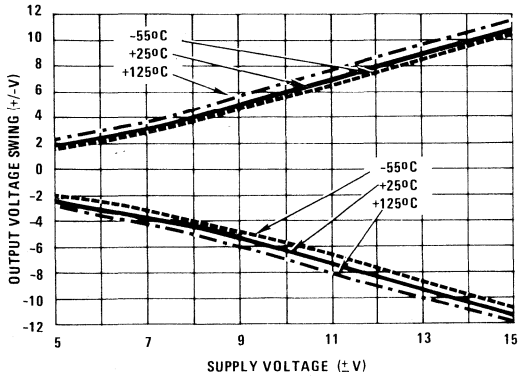


OPEN LOOP GAIN vs. TEMPERATURE
V_S = ±15V, R_L = 1kΩ

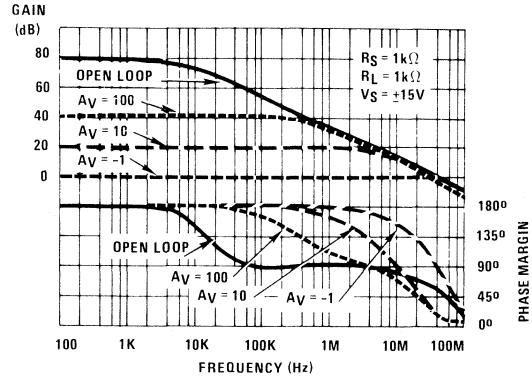


Typical Performance Curves (Continued)

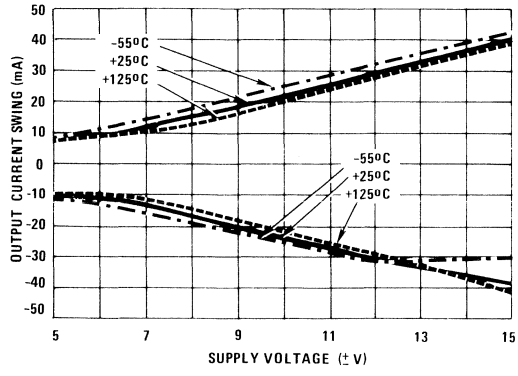
OUTPUT VOLTAGE SWING vs. SUPPLY VOLTAGE
(Over Full Temperature)



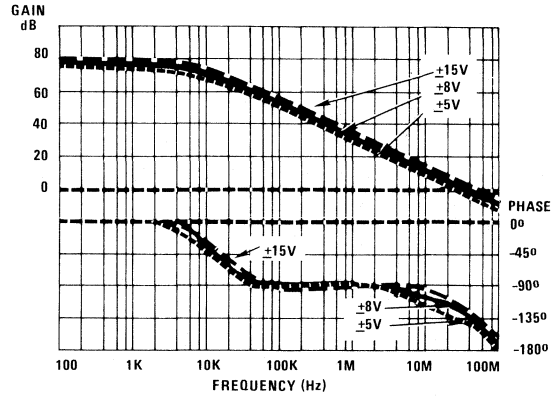
FREQUENCY RESPONSE AT VARIOUS GAINS
R_S = 1kΩ, R_L = 1kΩ, V_S = ±15V



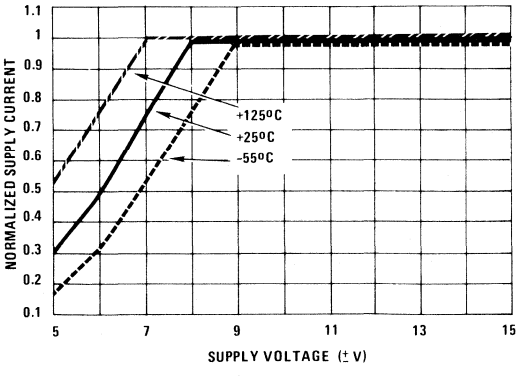
OUTPUT CURRENT vs. SUPPLY VOLTAGE
(Over Full Temperature)



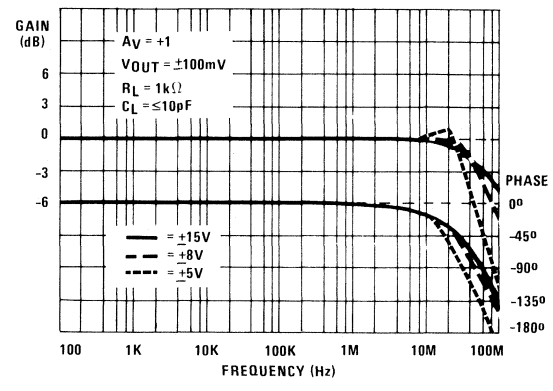
OPEN LOOP RESPONSE vs. SUPPLY VOLTAGE
V_{OUT} = ±100mV



SUPPLY CURRENT vs. SUPPLY VOLTAGE
Normalized at V_S = ±15V at +25°C

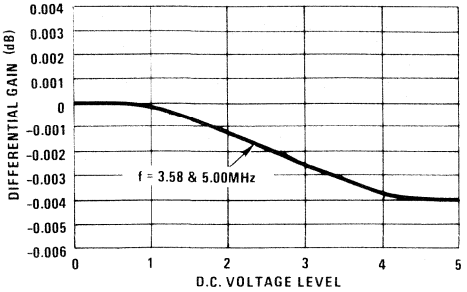


VOLTAGE FOLLOWER RESPONSE vs. SUPPLY VOLTAGE
A_V = +1, R_L = 1K, C_L < 10pF

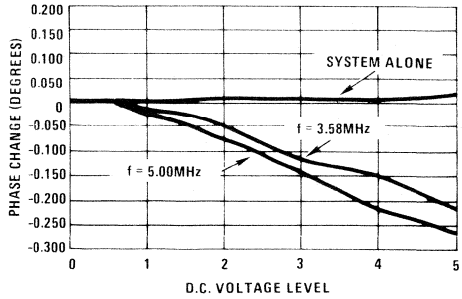


Typical Video Performance

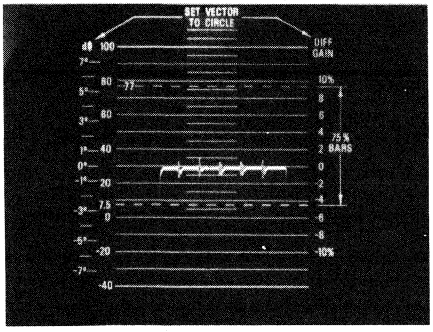
A.C. GAIN VARIATION vs. D.C. OFFSET LEVELS
(Differential Gain)



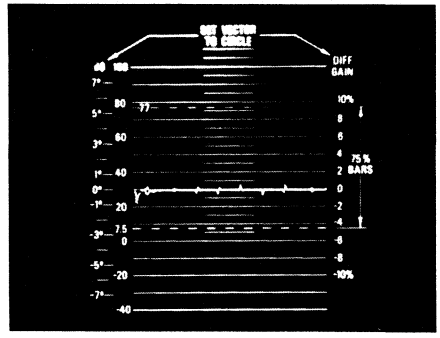
A.C. PHASE VARIATION vs. D.C. OFFSET LEVELS
(Differential Phase)



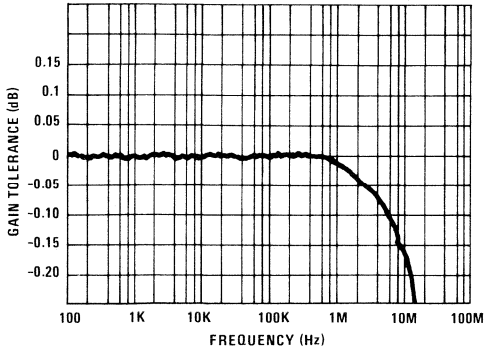
DIFFERENTIAL GAIN
NTSC Method, R_L = 1kΩ
Differential Gain < 0.05% at T_A = +75°C
No Visual Difference at T_A = -55°C or +125°C



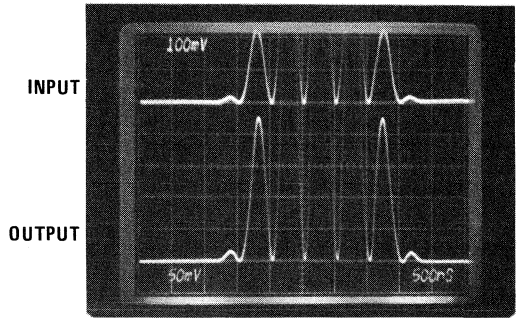
DIFFERENTIAL PHASE
NTSC Method, R_L = 1kΩ
Differential Phase < 0.05 Degree at T_A = +75°C
No Visual Difference at T_A = -55°C or +125°C



GAIN TOLERANCE
A_V = +1, V_{IN} = ±100mV
R_L = 1K, C_L < 10pF



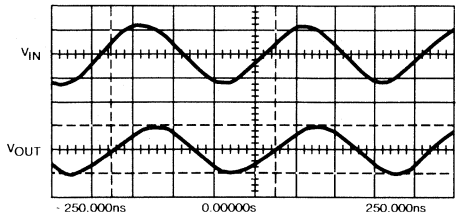
CHROMINANCE TO LUMINANCE DELAY
NTSC Method, R_L = 1kΩ
C-L Delay < 7ns at T_A = +75°C
No Visual Difference at T_A = -55°C or +125°C



Vertical Scale: Input = 100mV/Div.
Output = 50mV/Div.
Horizontal Scale: 500ns/Div.

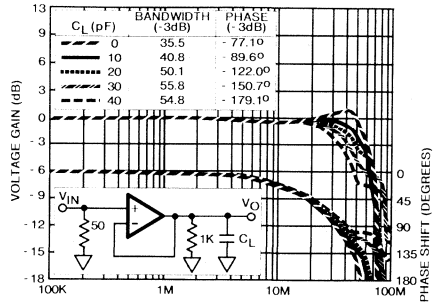
Typical Video Performance Curves (Continued)

±2 VOLT OUTPUT SWING
With R_{LOAD} = 75Ω (frequency = 5.00MHz)



V_{IN} = 2.0V/Div., V_{OUT} = 2.0V/Div.
Timebase = 50ns/Div.

BANDWIDTH vs. LOAD CAPACITANCE
A_V = +1, V_S = ±15V, R_L = 1kΩ



Applications And Product Guidelines

The HA-2544 is a true differential op amp that is as versatile as any op amp but offers the advantages of high unity gain bandwidth, high speed and low supply current. More important than its' general purpose applications is that the HA-2544 was especially designed to meet the requirements found in a video amplifier system. These requirements include fine picture resolution and accurate color rendition, and must meet broadcast quality standards.

In a video signal, the video information is carried in the amplitude and phase as well as in the D.C. level. The amplifier must pass the 30Hz line rate luminance level and the 3.58MHz (NTSC) or 4.43MHz (PAL) color band without altering phase or gain. The HA-2544's key specifications aimed at meeting this include high bandwidth (50MHz), very low gain tolerance (<±0.15dB at 5MHz), near unmeasurable differential gain and differential phase (<0.04dB and 0.11 degrees), and low noise (20nV/$\sqrt{Hz}$). The HA-2544 meets these quidelines and are sample tested for standard grade product (/883, -2, -7, -5) at 5 and/or 10MHz. If a customer wishes to 100% test these specifications, arrangement can be made.

The HA-2544 also offers the advantage of a full output voltage swing of ±10V into a 1K ohm load. This equates to a full power bandwidth of 2.4MHz for this ±10V signal. If video signal levels of ±2V maximum is used (with R_L = 1K ohm), the full power bandwidth would be 11.9MHz without clipping distortion. Another usage might be required for a direct 50 ohm or 75 ohm load where the HA-2544 will still swing this ±2V signal as shown in the above display. One important note that must be realized is that as load resistance decreases the video parameters are also degraded. For optimal video performance a 1kΩ load is recommended.

If lower supply voltage are required, such as ±5V, many of the characterization curves indicate where the parameters vary. As shown the bandwidth, slew rate and supply current are still very well maintained.

Prototyping and PC Board Layout

When designing with the HA-2544 video op amp as with any high performance device, care should be taken to use high frequency layout techniques to avoid unwanted parasitic effects. Short lead lengths, low source impedance and lower value feedback resistors help reduce unwanted poles or zeros. This layout would also include ground plane construction and power supply decoupling as close to the supply pins with suggested parallel capacitors of 0.1μF and .001μF ceramic to ground.

In the noninverting configuration, the amplifier is sensitive to stray capacitance (<40pF) to ground at the inverting input. Therefore, the inverting node connections should be kept to a minimum. Phase shift will also be introduced as load parasitic capacitance is increased. A small series resistor (20 ohm to 100 ohm) before the capacitance effectively decouples this effect.

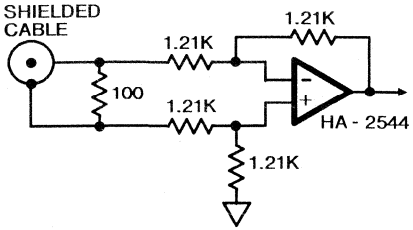
Stability/Phase Margin/Compensation

The HA-2544 has not sacrificed unity gain stability in achieving its superb AC performance. For this device, the phase margin exceeds 60 degrees at the unity crossing point of the open loop frequency response. Large phase margin is critical in order to reduce the differential phase and differential gain errors caused by most other op amps. Because this part is unity gain stable, no compensation pin is brought out. If compensation is desired to reduce the noise bandwidth, most standard methods may be used. One method suggested for an inverting scheme would be a series R-C from the inverting node to ground which will reduce bandwidth, but not effect slew rate. If the user wishes to achieve even higher bandwidth (>50MHz), and can tolerate some slight gain peaking and lower phase margin, experimenting with various load capacitance can be done.

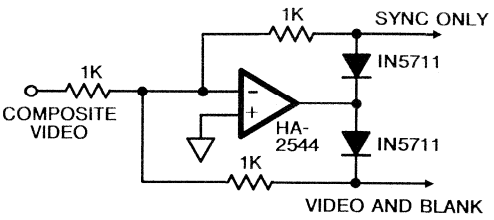
Shown in Application 1 is an excellent Differential Input, Unity Gain Buffer which also will terminate a cable to 75 ohm and reject common-mode voltages. Application 2 is a method of separating a video signal up into the Sync. only signal and the Video and Blanking signal. Application 3 shows the HA-2544 being used as a 100kHz High Pass 2-Pole Butterworth Filter. Also shown is the measured frequency response curves.

Typical Application

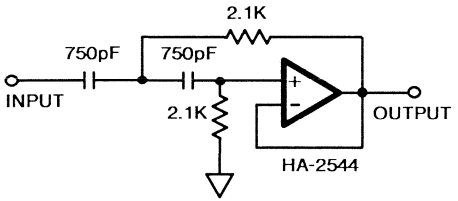
APPLICATION 1
75Ω Differential Input Buffer



APPLICATION 2
Composite Video Sync. Separator

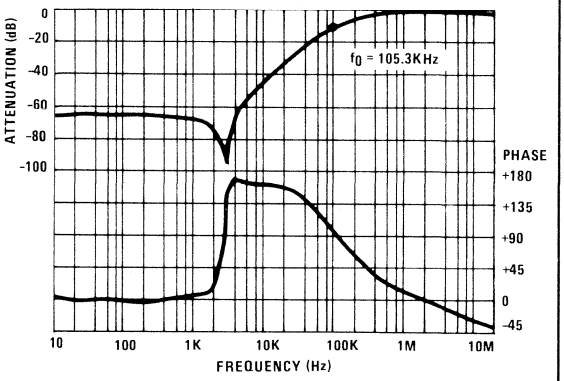


Application 3
100kHz High Pass 2-Pole Butterworth Filter



$$f_O = \frac{1}{2\pi(2.1K \cdot 750pF)}$$

Measured Frequency Response of Application 3



Die Characteristics

Transistor Count 44
Die Dimensions ..... 80 x 65 x 19 mils
(2030 x 1630 x 485μm)
Substrate Potential* ..... V-
Process ..... High Frequency Bipolar D.I.
Passivation ..... Nitride

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
Metal Can TO-99, HA2-2544	186	50
Plastic Mini-DIP, HA3-2544/2544C	80	20
Ceramic Mini-DIP, HA7-2544	185	98

*The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.

HARRIS

HA-2600/02/05

Wideband, High Impedance Operational Amplifiers

Features

- Wide Bandwidth 12MHz
- High Input Impedance 500MΩ
- Low Input Bias Current 1nA
- Low Input Offset Current 1nA
- Low Input Offset Voltage 0.5mV
- High Gain 150kV/V
- High Slew Rate 7V/μs
- Output Short Circuit Protection
- Unity Gain Stable

Applications

- Video Amplifier
- Pulse Amplifier
- Audio Amplifiers and Filters
- High-Q Active Filters
- High-Speed Comparators
- Low Distortion Oscillators

Description

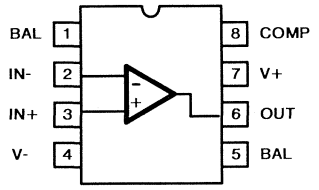
HA-2600/2602/2605 are internally compensated bipolar operational amplifiers that feature very high input impedance (500MΩ, HA-2600) coupled with wideband AC performance. The high resistance of the input stage is complemented by low offset voltage (0.5mV, HA-2600) and low bias and offset current (1nA, HA-2600) to facilitate accurate signal processing. Input offset can be reduced further by means of an external nulling potentiometer. 12MHz unity gain-bandwidth, 7V/μs slew rate and 150kV/V open-loop gain enables HA-2600/2602/2605 to perform high-gain amplification of fast, wideband signals. These dynamic characteristics, coupled with fast settling times, make these amplifiers ideally suited to pulse amplification designs as well as high frequency (e.g. video) applications. The frequency response of the amplifier can be tailored to exact design requirements by means of an external bandwidth control capacitor.

In addition to its application in pulse and video amplifier designs, HA-2600/2602/2605 is particularly suited to other high performance designs such as high-gain low distortion audio amplifiers, high-Q and wideband active filters and high-speed comparators. For more information, please refer to Application Note 515.

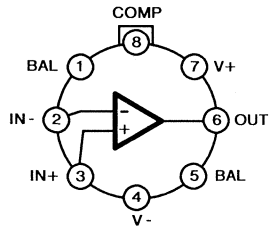
The HA-2600 and HA-2602 have guaranteed operation from -55°C to +125°C and are available in Metal Can and Ceramic Mini-DIP packages. Both are offered as /883 Military Grade; product and data sheets are available upon request. The HA-2605 has guaranteed operation from 0°C to +75°C and is available in Plastic and Ceramic Mini-DIP and Metal Can packages.

Pinouts

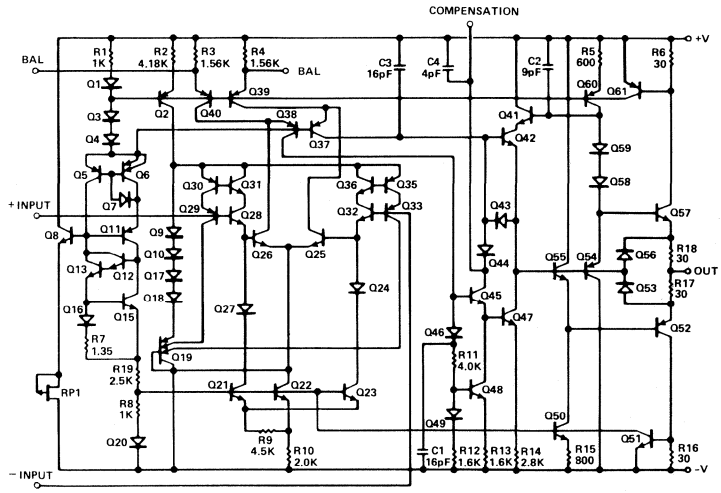
HA7-2600/02/05 (CERAMIC MINI-DIP)
HA3-2605 (PLASTIC MINI-DIP)
TOP VIEW



HA2-2600/02/05 (TO-99 METAL CAN)
TOP VIEW



Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 13)

Voltage Between V+ and V- Terminals 45.0V
Differential Input Voltage ..... ±12.0V
Peak Output Current ..... Full Short Circuit Protection
Internal Power Dissipation 300mW
Maximum Junction Temperature ..... +175°C

Operating Temperature Ranges

HA-2600/HA-2602 ..... $-55^{\circ}C \leq T_A \leq +125^{\circ}C$
HA-2605 ..... $0^{\circ}C \leq T_A \leq +75^{\circ}C$
Storage Temperature Range ..... $-65^{\circ}C \leq T_A \leq +150^{\circ}C$
Lead Solder Temperature (10 Seconds) ..... 275°C

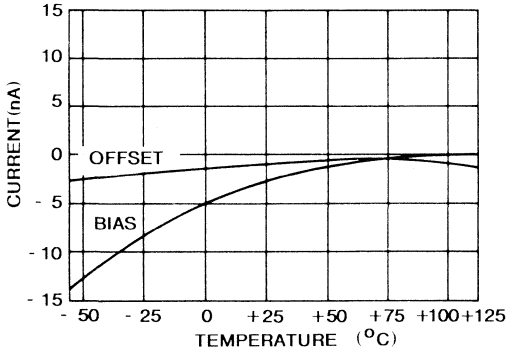
Electrical Specifications V_S = ±15V D.C., Unless Otherwise Specified.

PARAMETER	TEMP	HA-2600 -55°C to +125°C			HA-2602 -55°C to +125°C			HA-2605 0°C to +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS											
Offset Voltage	+25°C	-	0.5	4	-	3	5	-	3	5	mV
	Full	-	2	6	-	-	7	-	-	7	mV
Average Offset Voltage Drift	Full	-	5	-	-	5	-	-	5	-	µV/°C
Bias Current	+25°C	-	1	10	-	15	25	-	5	25	nA
	Full	-	10	30	-	-	60	-	-	40	nA
Offset Current	+25°C	-	1	10	-	5	25	-	5	25	nA
	Full	-	5	30	-	-	60	-	-	40	nA
Differential Input Resistance (Note 10)	+25°C	100	500	-	40	300	-	40	300	-	MΩ
Input Noise Voltage Density f_O = 1kHz	+25°C	-	11	-	-	11	-	-	11	-	$nV/\sqrt{Hz}$
Input Noise Current Density f_O = 1kHz	+25°C	-	0.16	-	-	0.16	-	-	0.16	-	$pA/\sqrt{Hz}$
Common Mode Range	Full	±11	±12	-	±11	±12	-	±11	±12	-	V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Notes 1, 4)	+25°C	100K	150K	-	80K	150K	-	80K	150K	-	V/V
	Full	70K	-	-	60K	-	-	70K	-	-	V/V
Common Mode Rejection Ratio (Note 2)	Full	80	100	-	74	100	-	74	100	-	dB
Minimum Stable Gain	+25°C	1	-	-	1	-	-	1	-	-	V/V
Gain Bandwidth Product (Note 3)	+25°C	-	12	-	-	12	-	-	12	-	MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10	±12	-	±10	±12	-	±10	±12	-	V
Output Current (Note 4)	+25°C	±15	±22	-	±10	±18	-	±10	±18	-	mA
Full Power Bandwidth (Notes 4, 11)	+25°C	50	75	-	50	75	-	50	75	-	kHz
TRANSIENT RESPONSE (Note 8)											
Rise Time (Notes 1, 5, 6 & 7)	+25°C	-	30	60	-	30	60	-	30	60	ns
Overshoot (Notes1, 5, 6 & 7)	+25°C	-	25	40	-	25	40	-	25	40	%
Slew Rate (Notes 1, 5, 7 & 12)	+25°C	±4	±7	-	±4	±7	-	±4	±7	-	V/µs
Settling Time (Notes 1, 5, & 14)	+25°C	-	1.5	-	-	1.5	-	-	1.5	-	µs
POWER SUPPLY CHARACTERISTICS											
Supply Current	+25°C	-	3	3.7	-	3	4	-	3	4	mA
Power Supply Rejection Ratio (Note 9)	Full	80	90	-	74	90	-	74	90	-	dB

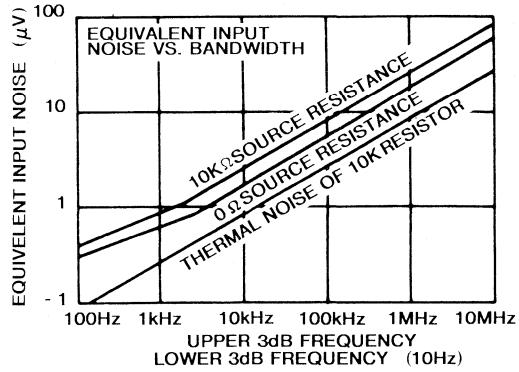
NOTES:
1. $R_L = 2k\Omega$
2. $V_{CM} = \pm 10V$
3. $V_{OUT} < 90mV$
4. $V_{OUT} = \pm 10V$
5. $C_L = 100pF$
6. $V_{OUT} = \pm 200mV$
7. $A_V = +1$
8. See Transient Response Test Circuits & Waveforms.
9. $\Delta V_S = \pm 5V$
10. This parameter value guaranteed by design calculations.
11. Full Power Bandwidth guaranteed by slew rate measurement: $FPBW = S.R./2\pi V_{PEAK}$.
12. $V_{OUT} = \pm 5V$
13. Absolute Maximum Ratings are limiting values applied individually beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
14. Settling time is characterized at $A_V = -1$ to 0.1% of a 10 Volt step.

Typical Performance Curves $V_S = \pm 15V$ D.C., $T_A = +25^oC$, Unless Otherwise Specified.

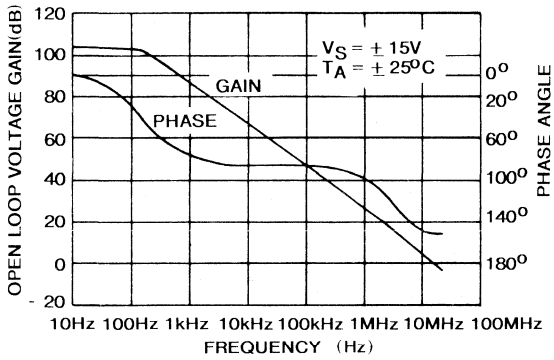
INPUT BIAS CURRENT AND OFFSET CURRENT AS A FUNCTION OF TEMPERATURE



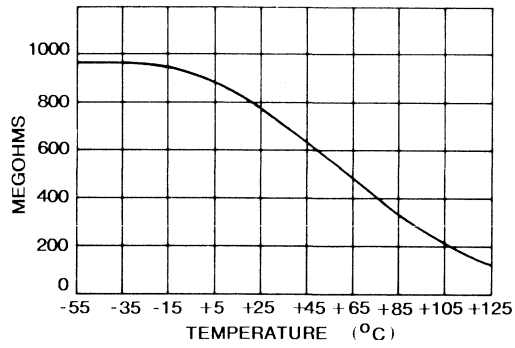
BROADBAND NOISE CHARACTERISTICS



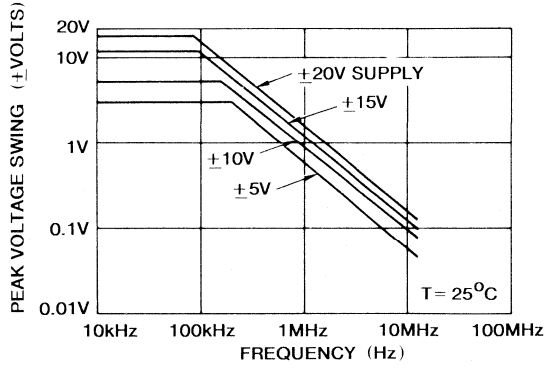
OPEN LOOP FREQUENCY AND PHASE RESPONSE



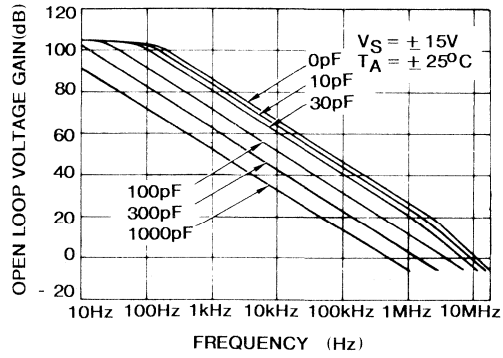
INPUT IMPEDANCE vs. TEMPERATURE, 100Hz



OUTPUT VOLTAGE SWING vs. FREQUENCY



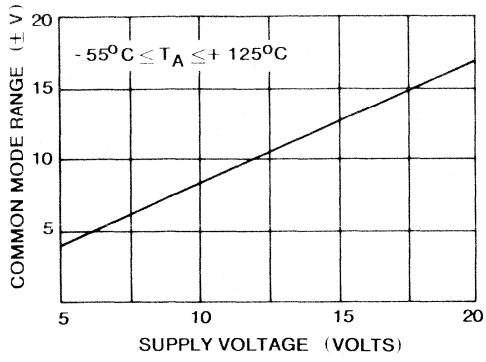
OPEN - LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMPENSATION PIN TO GROUND



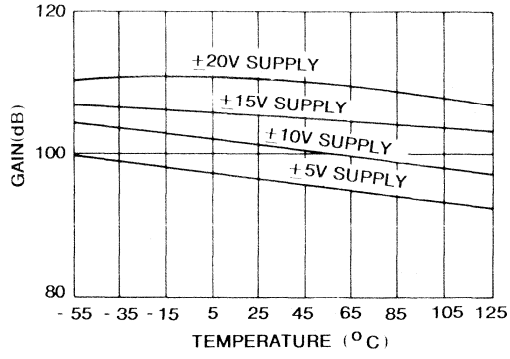
NOTE: External Compensation Components are not required for stability, but may be added to reduce bandwidth if desired. If External Compensation is used, also connect 100pF capacitor from output to ground.

Typical Performance Curves (Continued)

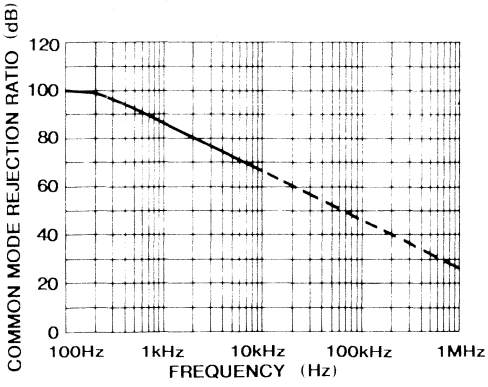
COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



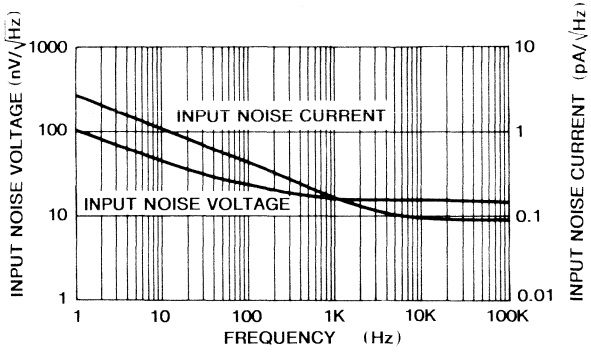
OPEN - LOOP VOLTAGE GAIN vs. TEMPERATURE



COMMON MODE REJECTION RATIO vs. FREQUENCY

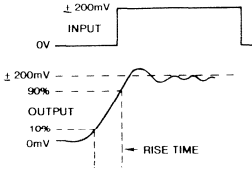


NOISE DENSITY vs. FREQUENCY

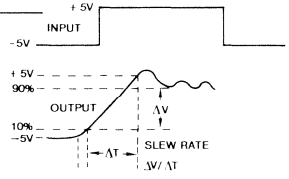


Test Circuits

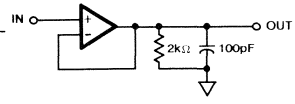
TRANSIENT RESPONSE



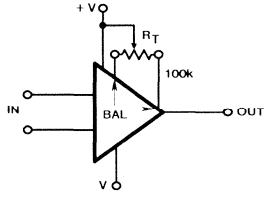
SLEW RATE



SLEW RATE AND TRANSIENT RESPONSE



SUGGESTED V_{OS} ADJUSTMENT AND COMPENSATION HOOK-UP

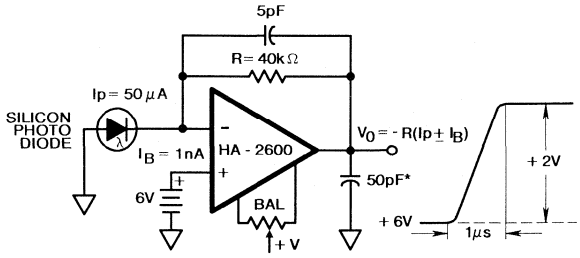


NOTE: Measured on both positive and negative transistions from 0 to +200mV and 0 to -200mV at output.

Tested Offset Adjustment is $|V_{OS} + 1mV|$ minimum referred to output. Typical range is ±10mV with $R_T = 100k\Omega$.

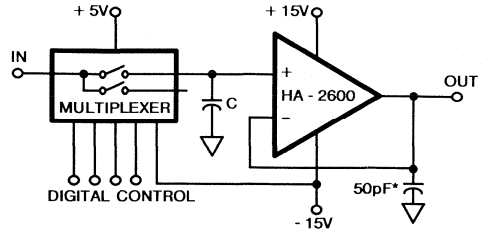
Typical Applications

PHOTO - CURRENT TO VOLTAGE CONVERTER



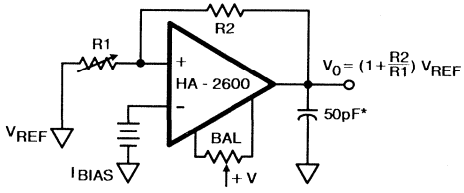
FEATURES:
1. Constant cell voltage
2. Minmum bias current error

SAMPLE - AND - HOLD



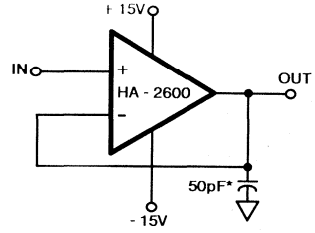
Drift rate $\frac{I_{bias}}{C}$ If C = 1000pF
Drift = 0.01V/ms Max.

REFERENCE VOLTAGE AMPLIFIER



FEATURES:
1. Minimum bias current in reference cell
2. Short circuit protection

VOLTAGE FOLLOWER



Z_{IN} = 10^{12} Min. B.W. = 12MHz Typ.
Z_{OUT} = 0.01 Max. Output Swing = ±10V Min. to 50kHz
Slew Rate = 4V/μs Min.

* A small load capacitance is recommended in all applications where practical to prevent possible high frequency oscillations resulting from external wiring parasitics. Capacitance up to 100pF has negligible effect on the bandwidth or slew rate.

Die Characteristics

Transistor Count 140
Die Dimensions ..... 73 x 52 x 19 mils
Substrate Potential ..... Unbiased

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
HA2-Metal Can (-2, -5, -7)	202	55
HA2-Metal Can (-8, /883)	161	48
HA3-Plastic DIP (-5)	83	33
HA4-Ceramic LCC (/883)	96	35
HA7-Ceramic DIP (-2, -5, -7)	204	112
HA7-Ceramic DIP (-8, /883)	81	32

HARRIS HA-2620/22/25

Very Wideband, Uncompensated Operational Amplifiers

Features

- Gain Bandwidth Product ($A_V \geq 5$) 100MHz
- High Input Impedance 500MΩ
- Low Input Bias Current 1nA
- Low Input Offset Current 1nA
- Low Input Offset Voltage 0.5mV
- High Gain 150kV/V
- High Slew Rate 35V/μs
- Output Short Circuit Protection

Applications

- Video and R.F. Amplifier
- Pulse Amplifier
- Audio Amplifiers and Filters
- High-Q Active Filters
- High-Speed Comparators
- Low Distortion Oscillators

Description

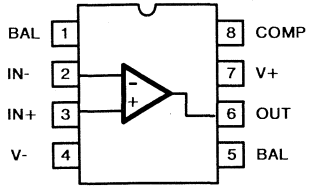
HA-2620/2622/2625 are bipolar operational amplifiers that feature very high input impedance (500MΩ, HA-2620) coupled with wideband AC performance. The high resistance of the input stage is complemented by low offset voltage (0.5mV, HA-2620) and low bias and offset current (1nA, HA-2620) to facilitate accurate signal processing. Input offset can be reduced further by means of an external nulling potentiometer. 100MHz gain-bandwidth product (HA-2620/2622/2625 are stable for closed loop gains greater than 5), 35V/μs slew rate and 150kV/V open-loop gain enables HA-2620/2622/2625 to perform high-gain amplification of very fast, wideband signals. These dynamic characteristics, coupled with fast settling times, make these amplifiers ideally suited to pulse amplification designs as well as high frequency (e.g. video) applications. The frequency response of the amplifier can be tailored to exact design requirements by means of an external bandwidth control capacitor.

In addition to its application in pulse and video amplifier designs, HA-2620/2622/2625 is particularly suited to other high performance designs such as high-gain low distortion audio amplifiers, high-Q and wideband active filters and high-speed comparators. For more information, please refer to Application Notes 509, 519 and 546.

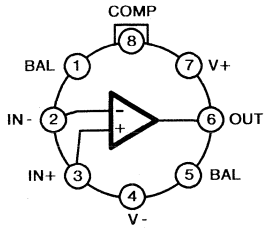
The HA-2620 and HA-2622 have guaranteed operation from -55°C to +125°C and are available in Metal Can and Ceramic Mini-DIP packages. Both are offered as /883 Military Grade with the HA-2622 also available in LCC packages. MIL-STD-883 data sheets are available upon request. The HA-2625 has guaranteed operation from 0°C to +75°C and is available in Plastic and Ceramic Mini-DIP and Metal Can packages.

Pinouts

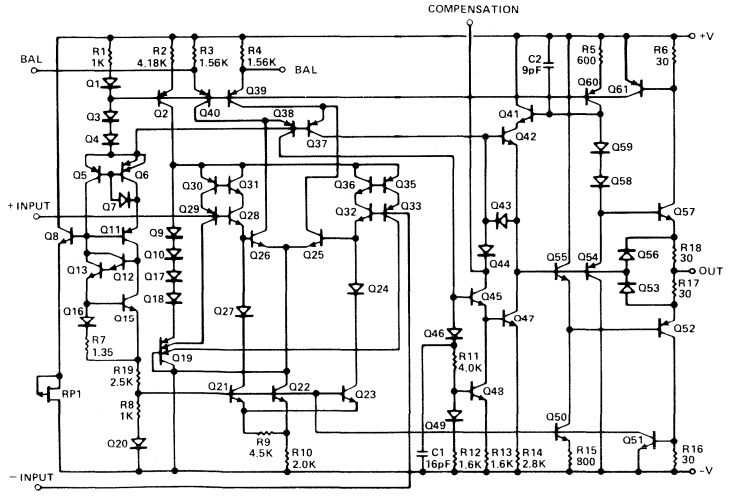
HA7-2620/22/25 (CERAMIC MINI-DIP)
HA3-2625 (PLASTIC MINI-DIP)
TOP VIEW



HA2-2620/22/25 (TO-99 METAL CAN)
TOP VIEW



Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 13)

Voltage Between V+ and V- Terminals 45.0V
Differential Input Voltage..... ±12.0V
Peak Output Current ..... Full Short Circuit Protection
Internal Power Dissipation 300mW
Maximum Junction Temperature..... +175°C

Operating Temperature Ranges

HA-2600/HA-2602.....$-55^{\circ}C \leq T_A \leq +125^{\circ}C$
HA-2605 ..... $0^{\circ}C \leq T_A \leq +75^{\circ}C$
Storage Temperature Range:.....$-65^{\circ}C \leq T_A \leq +150^{\circ}C$
Lead Solder Temperature (10 Seconds) ..... 275°C

Electrical Specifications

V_S = ±15V D.C., Unless Otherwise Specified.

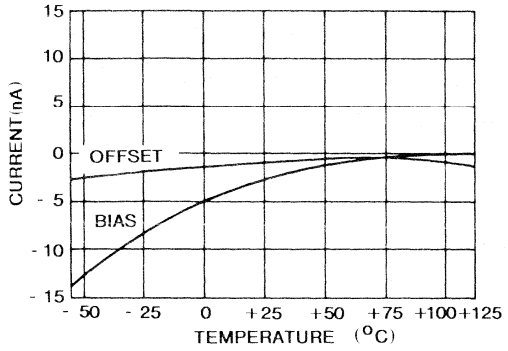
PARAMETER	TEMP	HA-2620 -55°C to +125°C			HA-2622 -55°C to +125°C			HA-2625 0°C to +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS											
Offset Voltage (Note 1)	+25°C	-	0.5	4	-	3	5	-	3	5	mV
	Full	-	2	6	-	-	7	-	-	7	mV
Average Offset Voltage Drift	Full	-	5	-	-	5	-	-	5	-	µV/°C
Bias Current	+25°C	-	1	15	-	5	25	-	5	25	nA
	Full	-	10	35	-	-	60	-	-	40	nA
Offset Current	+25°C	-	1	15	-	5	25	-	5	25	nA
	Full	-	5	35	-	-	60	-	-	40	nA
Differential Input Resistance (Note 11)	+25°C	65	500	-	40	300	-	40	300	-	MΩ
Input Noise Voltage Density f_0 = 1kHz	+25°C	-	11	-	-	11	-	-	11	-	$nV/\sqrt{Hz}$
Input Noise Current Density f_0 = 1kHz	+25°C	-	0.16	-	-	0.16	-	-	0.16	-	$pA/\sqrt{Hz}$
Common Mode Range	Full	±11	±12	-	±11	±12	-	±11	±12	-	V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Notes 2 & 3)	+25°C	100K	150K	-	80K	150K	-	80K	150K	-	V/V
	Full	70K	-	-	60K	-	-	70K	-	-	V/V
Common Mode Rejection Ratio (Note 4)	Full	80	100	-	74	100	-	74	100	-	dB
Minimum Stable Gain	+25°C	5	-	-	5	-	-	5	-	-	V/V
Gain Bandwidth Product (Notes 2, 5 & 6)	+25°C	-	100	-	-	100	-	-	100	-	MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 2)	Full	±10	±12	-	±10	±12	-	±10	±12	-	V
Output Current (Note 3)	+25°C	±15	±22	-	±10	±18	-	±10	±18	-	mA
Full Power Bandwidth (Notes 2, 3, 7 & 12)	+25°C	400	600	-	320	600	-	320	600	-	kHz
TRANSIENT RESPONSE (Note 8)											
Rise Time (Notes 2, 7 & 8)	+25°C	-	17	45	-	17	45	-	17	45	ns
Slew Rate (Notes 2, 7, 8 & 10)	+25°C	±25	±35	-	±20	±35	-	±20	±35	-	V/µs
POWER SUPPLY CHARACTERISTICS											
Supply Current	+25°C	-	3	3.7	-	3	4	-	3	4	mA
Power Supply Rejection Ratio (Note 9)	Full	80	90	-	74	90	-	74	90	-	dB

NOTES:

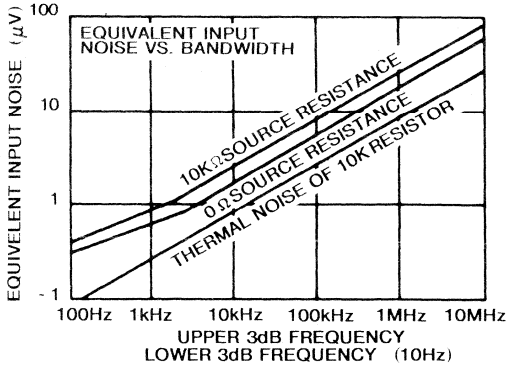
1. Offset may be externally adjusted to zero.
2. $R_L = 2k\Omega$
3. $V_{OUT} = \pm 10.0V$
4. $V_{CM} = \pm 10V$
5. $V_{OUT} < 90mV$
6. 40dB Gain
7. See Transient Response Test Circuits & Waveforms.
8. $A_V = 5$ (The HA-2620 family is not stable at unity gain without external compensation.)
9. $\Delta V_S = \pm 5V$
10. $V_{OUT} = \pm 5V$
11. This parameter value guaranteed by design calculations.
12. Full Power Bandwidth guaranteed by slew rate measurement: $FPBW = S.R./2\pi V_{PEAK}$.
13. Absolute Maximum Ratings are limiting values applied individually beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.

Typical Performance Curves $V_S = \pm 15V$ D.C., $T_A = +25^oC$, Unless Otherwise Specified.

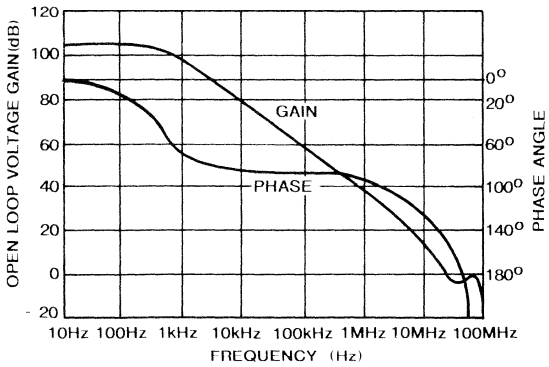
INPUT BIAS CURRENT AND OFFSET CURRENT AS A FUNCTION OF TEMPERATURE



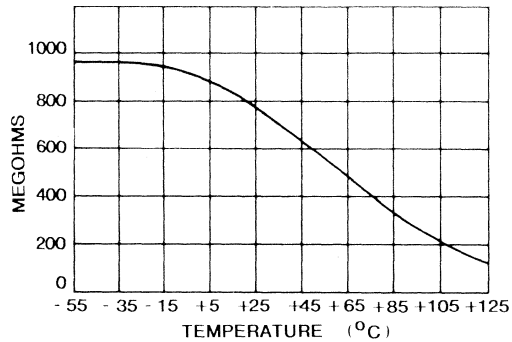
BROADBAND NOISE CHARACTERISTICS



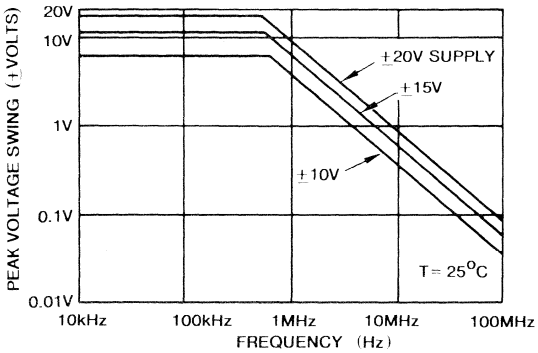
OPEN LOOP FREQUENCY AND PHASE RESPONSE



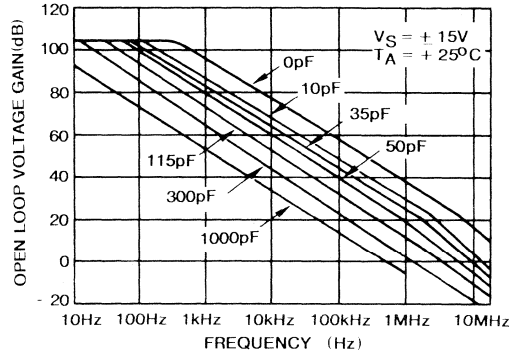
INPUT IMPEDANCE vs. TEMPERATURE, 100Hz



OUTPUT VOLTAGE SWING vs. FREQUENCY



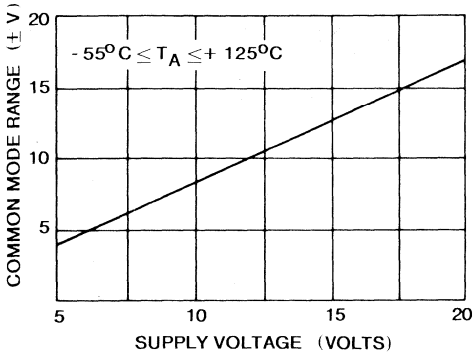
OPEN - LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMPENSATION PIN TO GROUND



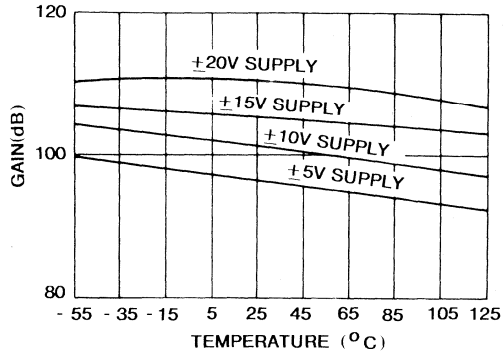
NOTE: External Compensation is required for closed loop gain < 5. If external compensation is used, also connect 100pF capacitor from output to ground.

Typical Performance Curves (Continued)

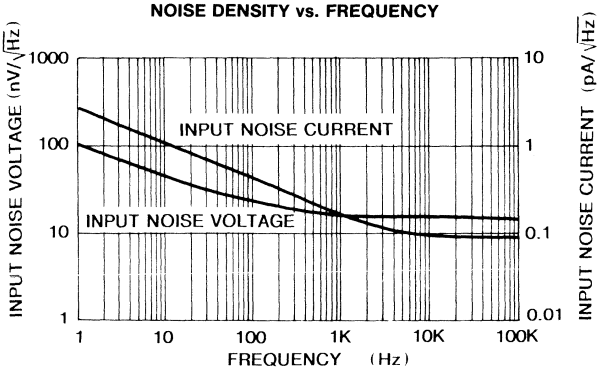
COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



OPEN - LOOP VOLTAGE GAIN vs. TEMPERATURE

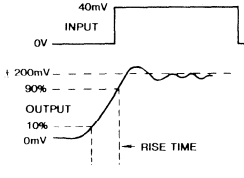


NOISE DENSITY vs. FREQUENCY

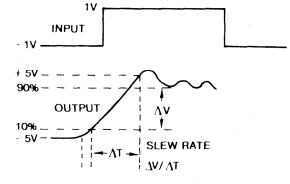


Test Circuits

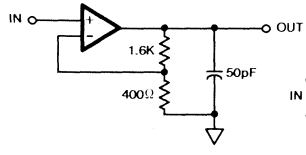
TRANSIENT RESPONSE



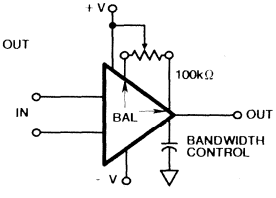
SLEW RATE



SLEW RATE AND TRANSIENT RESPONSE



SUGGESTED V_{OS} ADJUSTMENT AND COMPENSATION HOOK-UP

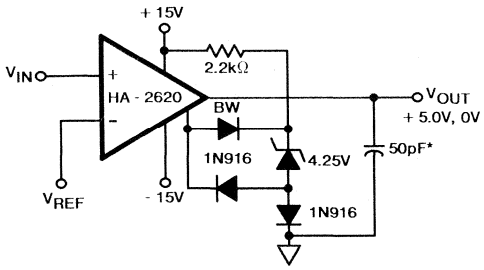


NOTE: Measured on both positive and negative transistions from 0 to +200mV and 0 to -200mV at output.

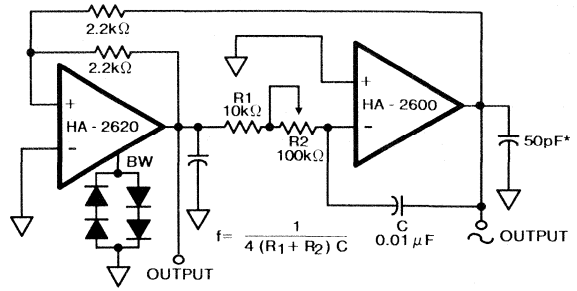
Tested Offset Adjustment is $|V_{OS} + 1mV|$ minimum referred to output. Typical range is ±10mV with R_T = 100kΩ.

Typical Applications

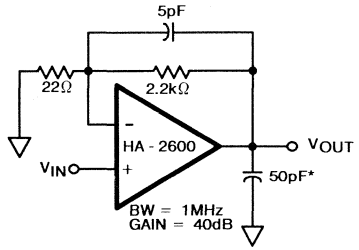
HIGH IMPEDANCE COMPARATOR



FUNCTION GENERATOR



VIDEO AMPLIFIER



* A small load capacitance of at least 30pF (including stray capacitance) is recommended to prevent possible high frequency oscillations.

Die Characteristics

Transistor Count 140
Die Dimensions ..... 73 x 52 x 19 mils
Substrate Potential ..... Unbiased

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
HA2-Metal Can (-2, -5, -7)	202	55
HA2-Metal Can (-8, /883)	161	48
HA3-Plastic DIP (-5)	83	33
HA4-Ceramic LCC (/883)	96	35
HA7-Ceramic DIP (-2, -5, -7)	204	112
HA7-Ceramic DIP (-8, /883)	81	32

HARRIS

HA-2640/45

High Voltage Operational Amplifiers

Features

- **Output Voltage Swing ..... ±35V**
- **Supply Voltage ..... ±10V to ±40V**
- **Offset Current 5nA**
- **Bandwidth 4MHz**
- **Slew Rate 5V/μs**
- **Common Mode Input Voltage Swing ..... ±35V**
- **Output Overload Protection**

Applications

- **Industrial Control Systems**
- **Power Supplies**
- **High Voltage Regulators**
- **Resolver Excitation**
- **Signal Conditioning**

Description

HA-2640 and HA-2645 are monolithic operational amplifiers which are designed to deliver unprecedented dynamic specifications for a high voltage internally compensated device. These dielectrically isolated devices offer very low values for offset voltage and offset current coupled with large output voltage swing and common mode input voltage.

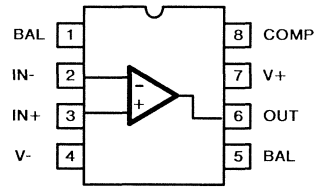
For maximum reliability, these amplifiers offer unconditional output overload protection through current limiting and a chip temperature sensing circuit. This sensing device turns the amplifier "off", when the chip reaches a certain temperature level.

These amplifiers deliver ±35V common mode input voltage swing, ±35V output voltage swing, and up to ±40V supply range for use in such designs as regulators, power supplies, and industrial control systems. 4MHz gain bandwidth and 5V/μs slew rate make these devices excellent components for high performance signal conditioning applications. Outstanding input and output voltage swings coupled with a low 5nA offset current make these amplifiers excellent components for resolver excitation designs.

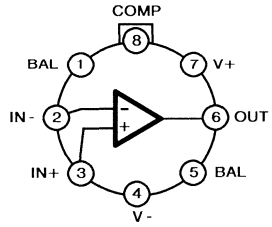
The HA-2640/2645 are available in Metal Can (TO-99) or Ceramic Mini-DIP and can be used as high performance pin-for-pin replacements for many general performance amplifiers. HA-2640 is specified from -55°C to +125°C and HA-2645 is specified over the 0°C to +75°C range.

Pinouts

HA7-2640/2645 (CERAMIC MINI-DIP)
TOP VIEW

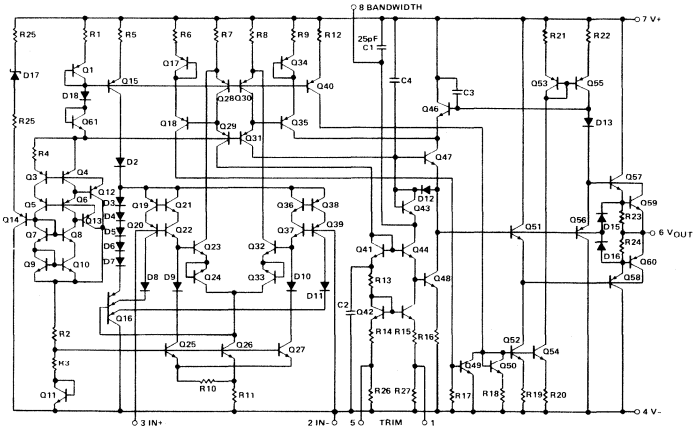


HA2-2640/2645 (TO-99 METAL CAN)
TOP VIEW



(TO-99 Case Voltage = -V)

Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 12)

Voltage Between V+ and V- Terminals 100V
Input Voltage Range ..... ±10V To ±37V
Output Current ..... Full Short Circuit Protection
Internal Power Dissipation ..... 680mW *
Maximum Junction Temperature ..... +175°C
* Derate by 4.6mW/°C above +25°C

Operating Temperature Ranges

HA-2640 ..... $-55^{\circ}C \leq T_A \leq +125^{\circ}C$
HA-2645 ..... $0^{\circ}C \leq T_A \leq +75^{\circ}C$
Storage Temperature Range ..... $-65^{\circ}C \leq T_A \leq +150^{\circ}C$

Electrical Specifications V_{SUPPLY} = ±40V, R_L = 5kΩ, Unless Otherwise Specified.

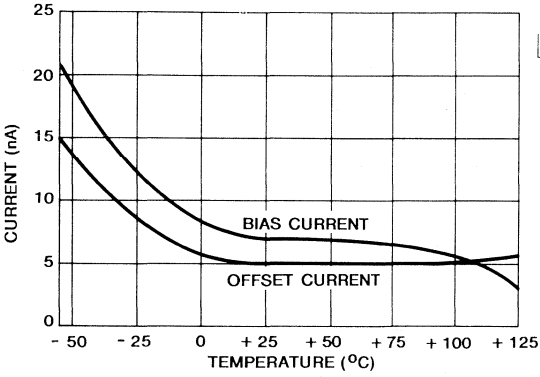
PARAMETER	TEMP	HA-2640 -55°C to +125°C			HA-2645 0°C to +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Offset Voltage	+25°C	-	2	4	-	2	6	mV
	Full	-	-	6	-	-	7	mV
Average Offset Voltage Drift	Full	-	15	-	-	15	-	µV/°C
Bias Current	+25°C	-	10	25	-	12	30	nA
	Full	-	-	50	-	-	50	nA
Offset Current	+25°C	-	5	12	-	15	30	nA
	Full	-	-	35	-	-	50	nA
Input Resistance (Note 10)	+25°C	50	250	-	40	200	-	MΩ
Common Mode Range	Full	±35	-	-	±35	-	-	V
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Notes 8)	+25°C	100K	200K	-	100K	200K	-	V/V
	Full	75K	-	-	75K	-	-	V/V
Common Mode Rejection Ratio (Note 1)	Full	80	100	-	74	100	-	dB
Minimum Stable Gain	+25°C	1	-	-	1	-	-	V/V
Unity Gain Bandwidth (Note 2)	+25°C	-	4	-	-	4	-	MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing	Full	±35	-	-	±35	-	-	V
Output Current (Note 9)	+25°C	±12	±15	-	±10	±12	-	mA
Output Resistance	+25°C	-	500	-	-	500	-	Ω
Full Power Bandwidth (Notes 3 & 11)	+25°C	-	23	-	-	23	-	kHz
TRANSIENT RESPONSE (Note 7)								
Rise Time (Notes 4 & 6)	+25°C	-	60	100	-	60	100	ns
Overshoot (Notes 4 & 6)	+25°C	-	15	30	-	15	40	%
Slew Rate (Note 6)	+25°C	±3	±5	-	±2.5	±5	-	V/µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C	-	3.2	3.8	-	3.2	4.5	mA
Supply Voltage Range	Full	±10	-	±40	±10	-	±40	V
Power Supply Rejection Ratio (Note 5)	Full	80	90	-	74	90	-	dB

NOTES:
1. V_{CM} = ±20V
2. V_{OUT} = 90mV
3. V_{OUT} = ±35V
4. V_{OUT} = ±200mV
5. V_S = ±10V to ±40V
6. A_V = +1
7. C_L = 50pF, R_L = 5kΩ
8. V_{OUT} = ±30V
9. R_L = 1kΩ
10. This parameter based upon design calculations.
11. Full Power Bandwidth guaranteed based upon slew rate measurement: FPBW = S.R./2πV_{PEAK}.
12. Absolute Maximum Ratings are limiting values applied individually beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.

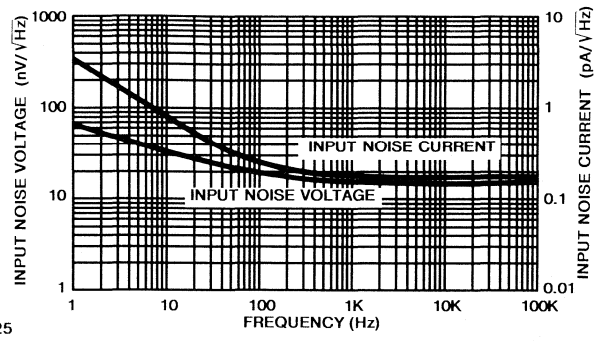
Typical Performance Curves

V+ = V- = 40V D.C., T_A = +25°C, Unless Otherwise Specified.

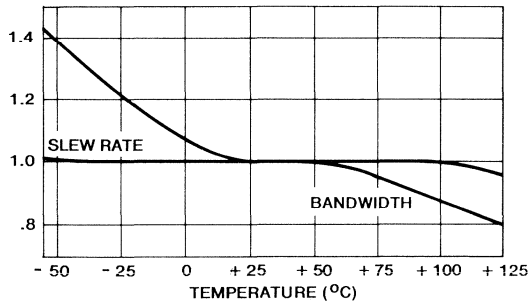
INPUT BIAS AND OFFSET CURRENT vs. TEMPERATURE



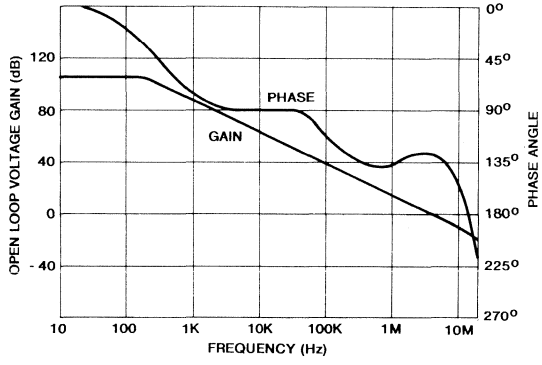
INPUT NOISE CHARACTERISTICS



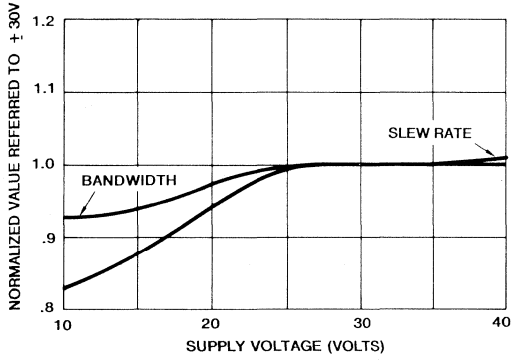
NORMALIZED AC PARAMETERS vs. TEMPERATURE



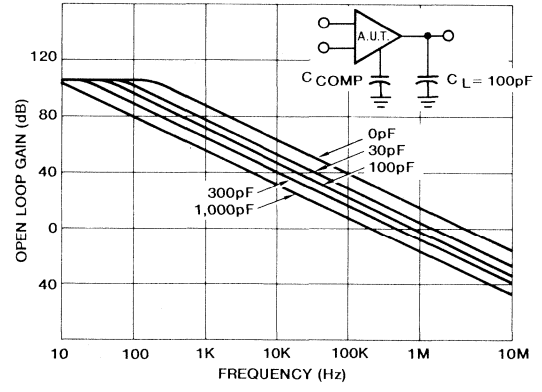
OPEN LOOP FREQUENCY AND PHASE RESPONSE



NORMALIZED AC PARAMETERS vs. SUPPLY VOLTAGE AT +25°C



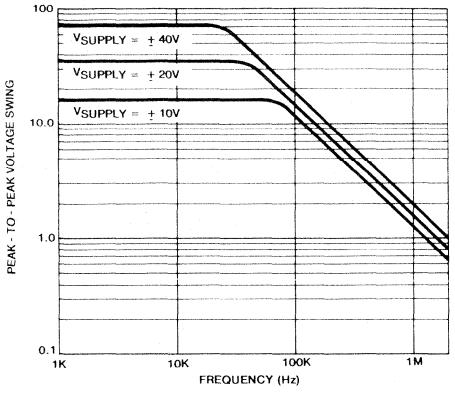
OPEN - LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMPENSATION PIN TO GROUND



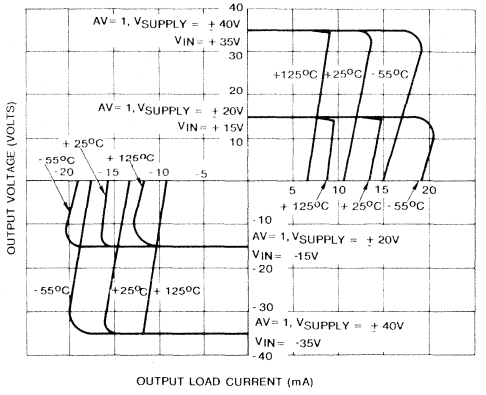
NOTE: External Compensation Components are not required for stability, but may be added to reduce bandwidth if desired. If External Compensation is used, also connect 100pF capacitor from output to ground.

Typical Performance Curves (Continued)

OUTPUT VOLTAGE SWING vs. FREQUENCY AT +25°C



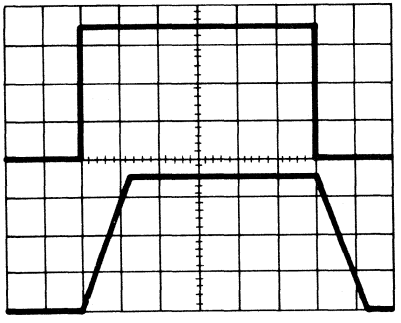
OUTPUT CURRENT CHARACTERISTIC



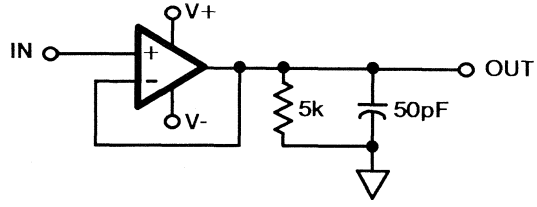
Switching Waveform and Test Circuits

VOLTAGE FOLLOWER PULSE RESPONSE

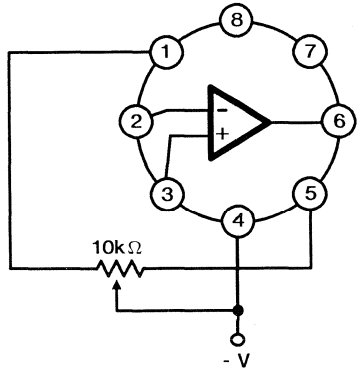
R_L = 5K, C_L = 50pF T_A = +25°C
Vertical = 10V/Div. V_S = ±40V
Horizontal = 5µs/Div.



SLEW RATE AND TRANSIENT RESPONSE TEST CIRCUIT



SUGGESTED V_{OS} ADJUSTMENT



Tested Offset Adjustment Range is $|V_{OS}$ +1mV$|$ minimum referred to output. Typical range is ±20mV with R_T = 10kΩ.

HARRIS

HA-2650/55

Dual High Performance Operational Amplifier

Not Recommended For New Designs See HA-5102 or HA-5152

Features

- SLEW RATE 5V/μs
- BANDWIDTH 8MHz
- BIAS CURRENT 35nA
- AVG. OFFSET VOLTAGE DRIFT 8μV/^{o}C
- POWER CONSUMPTION 75mW
- SUPPLY VOLTAGE RANGE $\pm$2V TO $\pm$20V

Applications

- VIDEO AMPLIFIERS
- HIGH IMPEDANCE, WIDEBAND BUFFERS
- INTEGRATORS
- AUDIO AMPLIFIERS
- ACTIVE FILTERS

Description

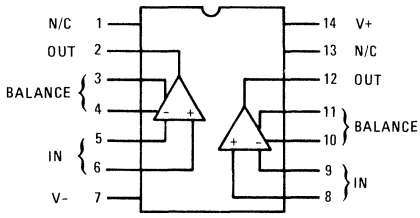
HA-2650/2655 contains two internally compensated operational amplifiers offering high slew rate and high frequency performance combined with exceptional DC characteristics. 5V/μsec slew rate and 8MHz bandwidth make these amplifiers suitable for processing fast, wideband signals extending into the video frequency spectrum. Signal processing accuracy is enhanced by front-end performance that includes 1.5mV offset voltage, 8μV/^{o}C offset voltage drift and low offset and bias current (1nA and 35nA respectively). Offset voltage can be trimmed to zero on the devices offered in dual-in-line packages. Signal conditioning is further enhanced by 500MΩ input impedance.

Applications for HA-2650/2655 include video circuit designs such as high impedance buffers, integrators, tone generators and filters. These amplifiers are also ideal components for active filtering of audio and voice signals.

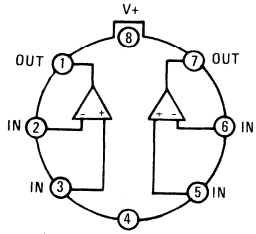
HA-2650/2655 are offered in 14 pin DIP and metal TO-99 packages and are also available in dice form. HA-2650 is specified form -55^{o}C to +125^{o}C. HA-2655 operates from 0^{o}C to +75^{o}C.

Pinouts

HA1-2650/2655 (CERAMIC DIP)
TOP VIEW

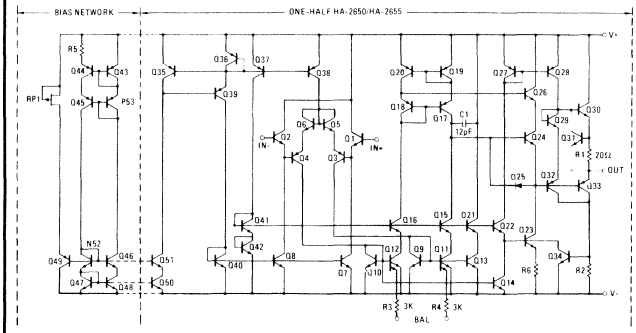


HA2-2650/2655 (TO-99 METAL CAN)
TOP VIEW



NOTE: Case Connected to V-

Schematic



Absolute Maximum Ratings (Note 1)

T_A = +25°C, Unless Otherwise Specified
Voltage Between V+ and V- Terminals 40V
Differential Input Voltage..... ±30V
Input Voltage (Note 1) ..... ±15V
Output Short Circuit Duration ..... Indefinite
Power Dissipation (Note 2)
TO-99 ..... 300mW

Operating Temperature Ranges

HA-2650 .....-55°C ≤ T_A ≤ +125°C
HA-2655 ..... 0°C ≤ T_A ≤ +75°C
Storage Temperature Range:.....-65°C ≤ T_A ≤ +150°C

Electrical Specifications

V+ = +15V D.C., V- = -15V D.C.

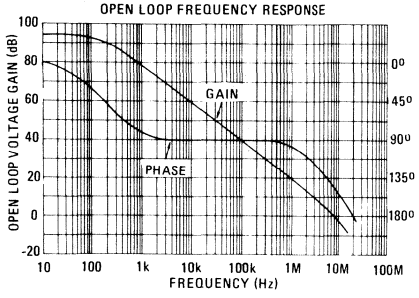
PARAMETER	TEMP.	HA-2650 -55°C to +125°C MIN.	HA-2650 -55°C to +125°C TYP.	HA-2650 -55°C to +125°C MAX.	HA-2655 0°C to +75°C MIN.	HA-2655 0°C to +75°C TYP.	HA-2655 0°C to +75°C MAX.	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		1.5	3		2	5	mV
	Full			5			7	mV
Av. Offset Voltage Drift	Full		8			8		µV/°C
Bias Current	+25°C		35	100		50	200	nA
	Full			200			300	nA
Offset Current	+25°C		1	30		2	60	nA
	Full			60			100	nA
Common Mode Range	Full	±13			±13			V
Differential Input Resistance (Note 9)	+25°C	5	20		5	20		MΩ
Common Mode Input Resistance	+25°C		500			500		MΩ
Input Capacitance	+25°C		5			5		pF
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 3ab)	+25°C	20K	40K		15K	40K		V/V
	Full	15K			10K			V/V
Common Mode Rejection Ratio (Note 4)	+25°C	80	100		74	100		dB
	Full	80			74			dB
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 3c)	+25°C	±13	±14		±13	±14		V
	Full	±13			±13			V
Full Power Bandwidth (Notes 5 &10)	+25°C	30	80		30	80		KHz
Output Current (Note 3a)	+25°C		±20			±18		mA
Output Resistance	+25°C		100			100		Ω
TRANSIENT RESPONSE (Note 6)								
Rise Time (Note 7)	+25°C		40	80		40	90	ns
Overshoot (Note 7)	+25°C		15	40		15	40	%
Slew Rate	+25°C	±2	±5		±2	±5		V/µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C		2.5	4		3	5	mA
Power Supply Rejection Ratio (Note 8)	+25°C	80	100		74	100		dB
	Full	80			74			dB

NOTES:
1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. Derate at 4.7mW/°C at ambient temperatures above +110°C.
3. (a) V_O = ±10V (b) R_L = 2K (c) R_L = 10K
4. V_{CM} = ±5.0V
5. A_V = 1, R_L = 2K, V_O = $20V_{pp}$
6. See transient response/slew rate circuit.
7. V_{in} = 200mV
8. Δ V = ±5.0V
9. This parameter value based upon design calculations.
10. Full power bandwidth guaranteed based upon slew rate measurement FPBW = S.R./$2\pi V_{peak}$.

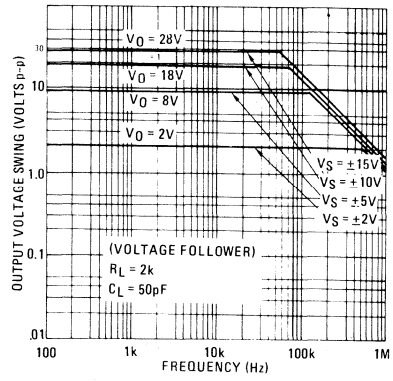
Typical Performance Curves

V+ = +15V, V- = -15V, T_A = +25°C, Unless Otherwise Specified.

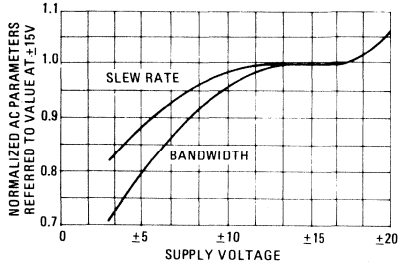
OPEN LOOP FREQUENCY RESPONSE



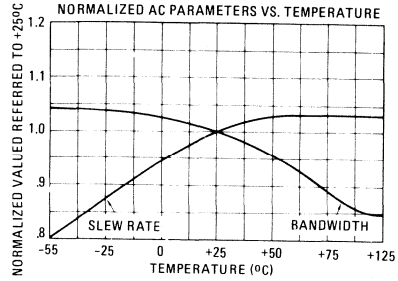
OUTPUT VOLTAGE SWING VS. FREQUENCY



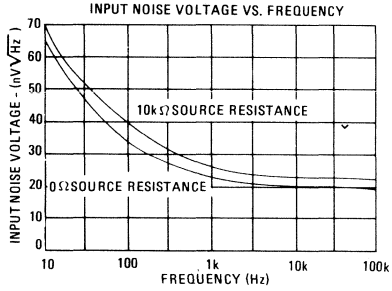
NORMALIZED AC PARAMETERS VS. SUPPLY VOLTAGE



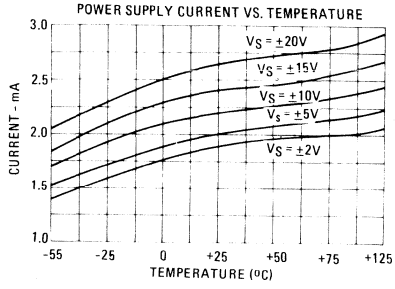
NORMALIZED AC PARAMETERS VS. TEMPERATURE



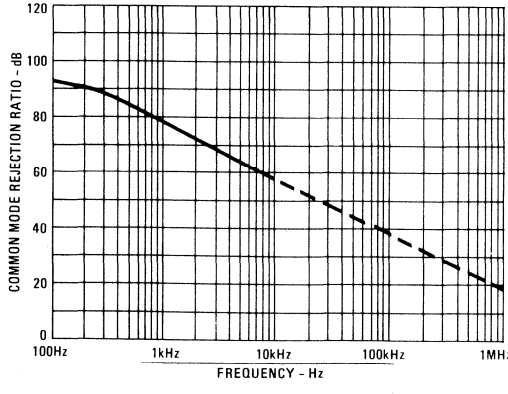
INPUT NOISE VOLTAGE VS. FREQUENCY



POWER SUPPLY CURRENT VS. TEMPERATURE

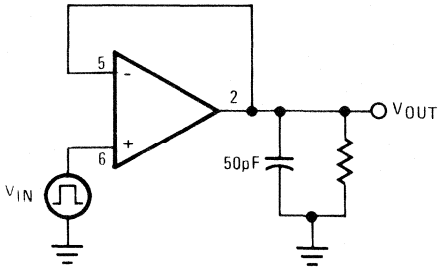


COMMON MODE REJECTION RATIO VS. FREQUENCY

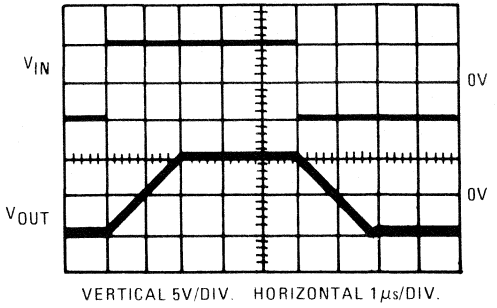


Test Circuits

TRANSIENT RESPONSE/SLEW RATE CIRCUIT



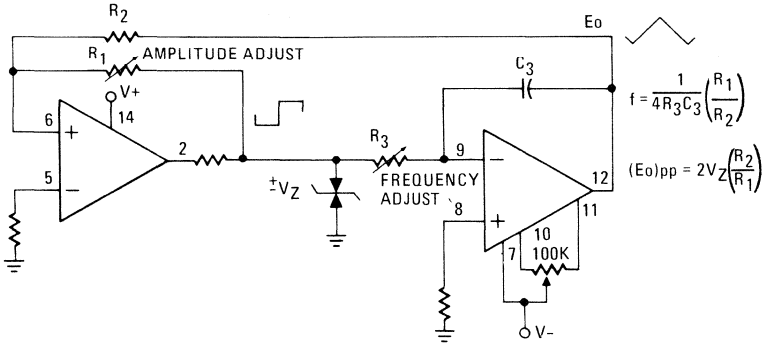
SLEWING WAVEFORM



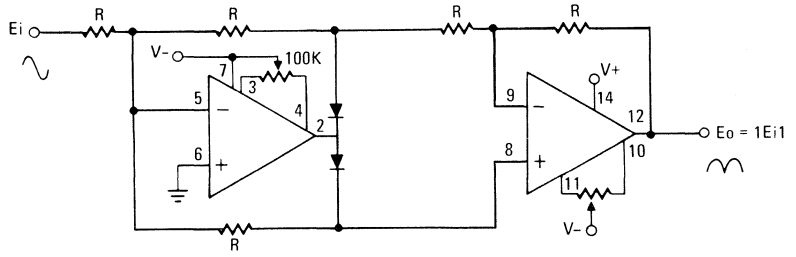
VERTICAL 5V/DIV. HORIZONTAL 1μs/DIV.

Typical Applications

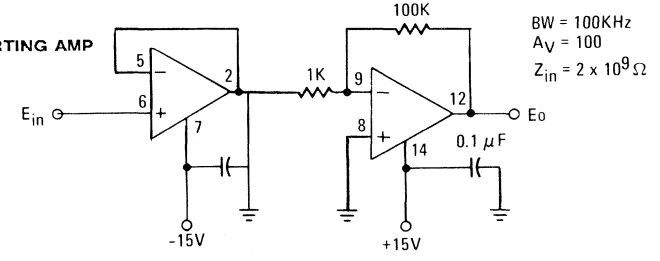
LOW COST HIGH FREQUENCY GENERATOR



ABSOLUTE - VALUE CIRCUIT



HIGH IMPEDANCE
HIGH GAIN
HIGH FREQUENCY INVERTING AMP



HARRIS

HA-2720/25

Wide Range Programmabl
Operational Amplifie

Not Recommended For New Designs See HA-5141 or HA-5151

Features

- WIDE PROGRAMMING RANGE

SLEW RATE	0.06 TO 6V/μs
BANDWIDTH	5kHz TO 10MHz
BIAS CURRENT	0.4 TO 50nA
SUPPLY CURRENT	1μA TO 1.5mA

- WIDE POWER SUPPLY RANGE ±1.2 TO ±18V
- CONSTANT AC PERFORMANCE OVER SUPPLY RANGE

Applications

- ACTIVE FILTERS
- CURRENT CONTROLLED OSCILLATORS
- VARIABLE ACTIVE FILTERS
- MODULATORS
- BATTERY-POWERED EQUIPMENT

Description

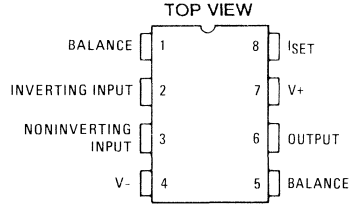
HA-2720/2725 programmable amplifiers are internally compensated monolithic devices offering a wide range of performance, that can be controlled by adjusting the circuits' "set" current (I_{SET}). By means of adjusting an external resistor or current source, power dissipation, slew rate, bandwidth, output current and input noise can be programmed to desired levels. This versatile adjustment capability enables HA-2720/2725 to provide optimum design solutions by delivering the required level of performance with minimum possible power dissipation. HA-2720 and HA-2725 can, therefore, be utilized as the standard amplifier for a variety of designs simply by adjusting their programming current.

A major advantage of HA-2720/2725 is that operating characteristics remain virtually constant over a wide supply range (±1.2V to ±15V), allowing the amplifiers to offer maximum performance in almost any system including battery-operated equipment. A primary application for HA-2720/2725 is in active filters for a wide variety of signals that differ in frequency and amplitude. Also, by modulating the "set" current, HA-2720/2725 can be used for designs such as current controlled oscillators modulators, sample and hold circuits and variable active filters.

HA-2720 is guaranteed over -55°C to +125°C. HA-2725 is specified from 0°C to +75°C. Both parts are available in TO-99 cans or dice form.

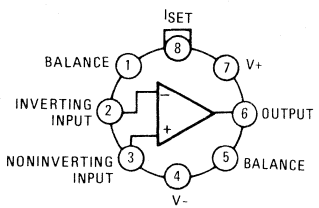
Pinouts

HA7-2720/2725 (CERAMIC MINI-DIP)
TOP VIEW

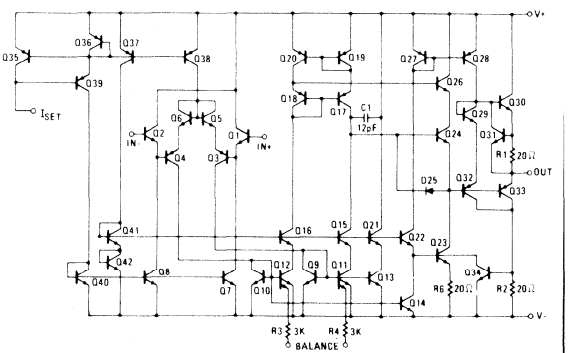


Note: Case tied to V-

HA2-2720/2725 (TO-99 METAL CAN)
TOP VIEW



Schematic



Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 45V
Differential Input Voltage ..... ±30V
Input Voltage (Note 1) ..... ±15V
I_{SET} (Current at I_{SET}) 500µA
V_{SET} (Voltage to GND at I_{SET}) ..... $V+ -2V \leq V_{SET} \leq V+$
Power Dissipation (Note 2) 300mW

Operating Temperature Ranges

HA-2720 ..... $-55^oC \leq T_A \leq +125^oC$
HA-2725 ..... $0^oC \leq T_A \leq +75^oC$
Storage Temperature Range: ..... $-65^oC \leq T_A \leq +150^oC$

Electrical Specifications

V+ = +3V, V- = -3V.

PARAMETER	TEMP.	HA-2720 -55°C to +125°C						HA-2725 0°C to +75°C						UNITS
		I_{SET} = 1.5µA			I_{SET} = 15µA			I_{SET} = 1.5µA			I_{SET} = 15µA			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
INPUT CHARACTERISTICS														
Offset Voltage	25°C		2.0	3.0		2.0	3.0		2.0	5.0		2.0	5.0	mV
	Full			5.0			5.0			7.0			7.0	mV
Offset Current	25°C		0.5	3.0		1.0	10		0.5	5.0		1.0	10	nA
	Full			7.5			20			7.5			20	nA
Bias Current	25°C		2.0	5.0		8.0	20		2.0	10		8.0	30	nA
	Full			10			40			10			40	nA
Input Resistance (Note 10)	25°C		50			5			50			5		MΩ
Input Capacitance	25°C		3.0			3.0			3.0			3.0		pF
TRANSFER CHARACTERISTICS														
Large Signal Voltage Gain (Note 9)	25°C	15K	40K		15K	40K		15K	40K		15K	40K		V/V
	Full	10K			10K			10K			10K			V/V
Common Mode Rejection Ratio (Note 4)	Full	80			80			74			74			dB
OUTPUT CHARACTERISTICS														
Output Voltage Swing (Note 3)	25°C	±2.0	±2.2		±2.0	±2.2		±2.0	±2.2		±2.0	±2.2		V
	Full	±2.0			±2.0			±2.0			±2.0			V
Output Current (Note 5)	25°C		±0.2			±2.0			±0.2			±2.0		mA
Output Resistance	25°C		2K			500			2K			500		Ω
Output Short-Circuit Current	25°C		2.8			14			2.8			14		mA
TRANSIENT RESPONSE														
Rise Time (Note 6)	25°C		2.5			0.25			2.5			0.25		µs
Overshoot (Note 6)	25°C		5			10			5			10		%
Slew Rate (Note 7)	25°C		0.07			0.70			0.07			0.70		V/µs
POWER SUPPLY CHARACTERISTICS														
Supply Current	25°C		15			170			15			170		µA
	Full			25			250			25			250	µA
Power Supply Rejection Ratio (Note 8)	Full	80			80			76			76			dB

Electrical Specifications (Continued) V+ = +15V, V- = -15V.

PARAMETER	TEMP.	HA-2720 -55°C to +125°C						HA-2725 0°C to +75°C						UNITS
		I_{SET} = 1.5μA			I_{SET} = 15μA			I_{SET} = 1.5μA			I_{SET} = 15μA			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
INPUT CHARACTERISTICS														
Offset Voltage	25°C		2.0	3.0		2.0	3.0		2.0	5.0		2.0	5.0	mV
	Full			5.0			5.0			7.0			7.0	mV
Offset Current	25°C		0.5	3.0		1.0	10		0.5	5.0		1.0	10	nA
	Full			7.5			20			7.5			20	nA
Bias Current	25°C		2.0	5.0		8.0	20		2.0	10		8.0	30	nA
	Full			10			40			10			40	nA
Input Resistance (Note 10)	25°C		50			5			50			5		MΩ
Input Capacitance	25°C		3.0			3.0			3.0			3.0		pF
TRANSFER CHARACTERISTICS														
Large Signal Voltage Gain (Notes 3 & 9)	25°C	30K	100K		30K	120K		25K	40K		25K	120K		V/V
	Full	20K			20K			20K			20K			V/V
Common Mode Rejection Ratio (Note 4)	25°C		90			90			90			90		dB
	Full	80			80			74			74			dB
OUTPUT CHARACTERISTICS														
Output Voltage Swing (Note 3)	25°C	±12	±13.5		±12	±13.5		±12	±13.5		±12	±13.5		V
	Full	±10			±10			±10			±10			V
Output Current (Note 5)	25°C		±0.5			±5.0			±0.5			±5.0		mA
Output Resistance	25°C		2K			500			2K			500		Ω
Output Short-Circuit Current	25°C		3.7			19			3.7			19		mA
TRANSIENT RESPONSE														
Rise Time (Note 6)	25°C		2.0			0.2			2.0			0.2		μs
Overshoot (Note 6)	25°C		5			15			5			15		%
Slew Rate (Note 7)	25°C		0.1			0.8			0.1			0.8		V/μs
POWER SUPPLY CHARACTERISTICS														
Supply Current	25°C		20			210			20			210		μA
	Full			50			450			50			450	μA
Power Supply Rejection Ratio (Note 8)	Full	80			80			76			76			dB

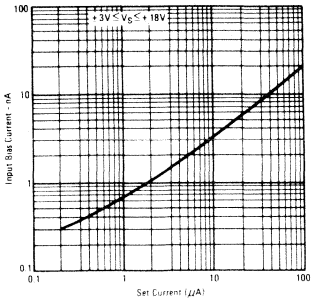
NOTES:
1. For supply voltages less than ±15.0V, the absolute maximum input voltage is equal to supply voltage.
2. Derate at 6.8mW/°C for operation ambient temperatures above 75°C.

	V_{SUPPLY} = ±3.0V	V_{SUPPLY} = ±15.0V	I_{SET} = 1.5μA	I_{SET} = 15μA
3.	T = +25°C and Full	T = +25°C	R_L = 75KΩ	R_L = 5KΩ
		T = Full	R_L = 75KΩ	R_L = 75KΩ
4.	V_{CM} = ±1.5V	V_{CM} = ±5.0V		
5.	V_O = ±2.0V	V_O = ±10.0V		
6.	← A_V = +1, V_{IN} = 400mV, R_L = 5K, C_L = 100pF →			
7.	V_O = ±2.0V	V_O = ±10.0V	R_L = 20K	R_L = 5K
8.	ΔV = ±1.5V	ΔV = ±5.0V		
9.	V_O = ±1.0V	V_O = ±10.0V		

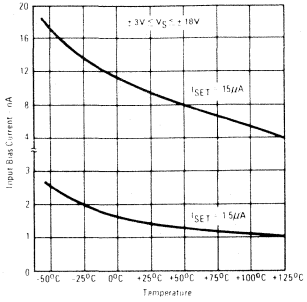
10. This parameter based upon design calculations.

Typical Performance Curves $T_A = +25^oC$, $V_S = \pm15V$ D.C. Unless Otherwise Specified.

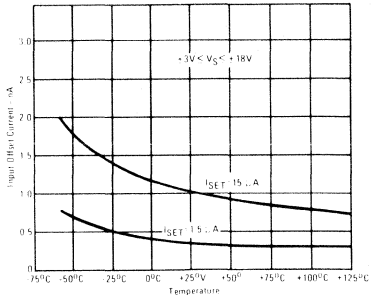
INPUT BIAS CURRENT vs. SET CURRENT



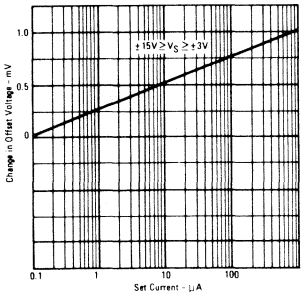
INPUT BIAS CURRENT vs. TEMPERATURE



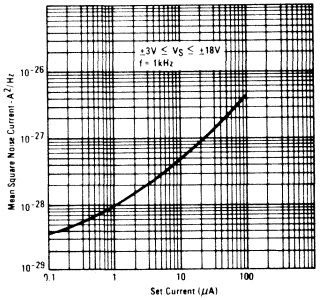
INPUT OFFSET CURRENT vs. TEMPERATURE



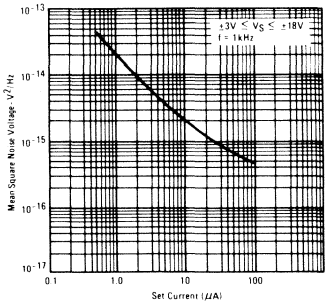
CHANGE IN OFFSET VOLTAGE vs. I_{SET} (UNNULLED)



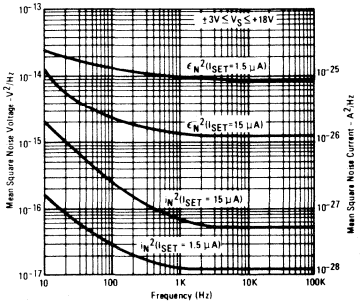
INPUT NOISE CURRENT vs. I_{SET}



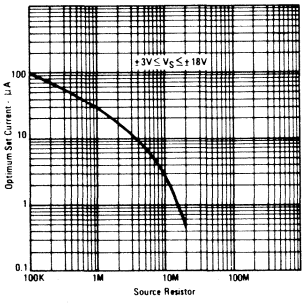
INPUT NOISE VOLTAGE vs. I_{SET}



INPUT NOISE VOLTAGE AND CURRENT vs. FREQUENCY

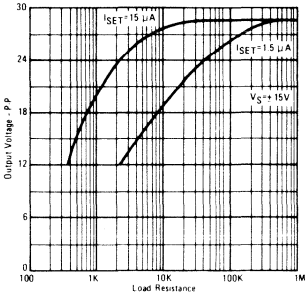


OPTIMUM SET CURRENT FOR MINIMUM NOISE vs. SOURCE RESISTOR

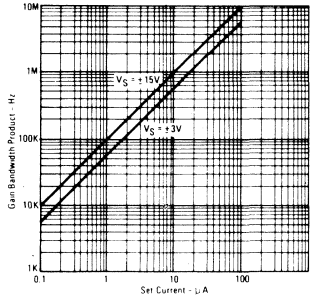


Typical Performance Curves (Continued) $T_A = +25^oC$, $V_S = \pm 15V$ D.C. Unless Otherwise Specified.

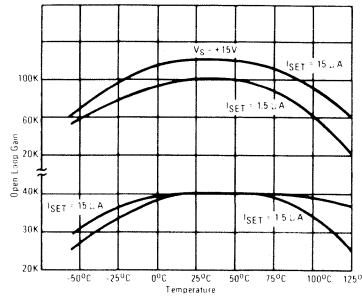
MAXIMUM OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE



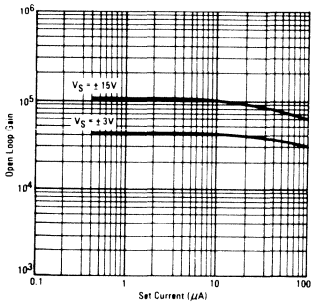
GAIN BANDWIDTH PRODUCT vs. I_{SET}



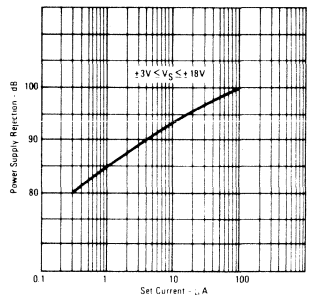
OPEN LOOP VOLTAGE GAIN vs. TEMPERATURE



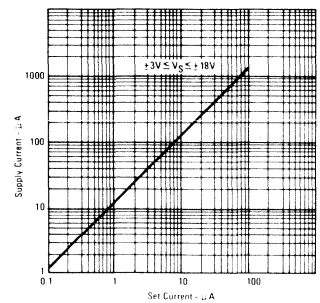
OPEN LOOP VOLTAGE GAIN vs. I_{SET}



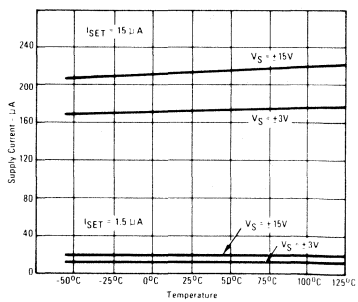
POWER SUPPLY REJECTION vs. I_{SET}



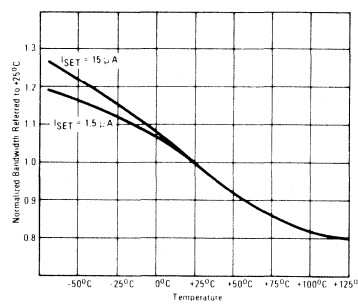
STANDBY SUPPLY CURRENT vs. I_{SET}



SUPPLY CURRENT vs. TEMPERATURE

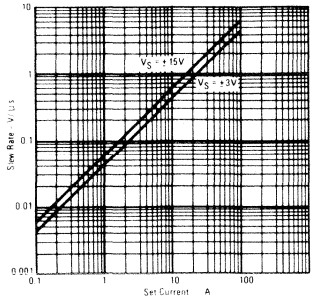


NORMALIZED BANDWIDTH vs. TEMPERATURE

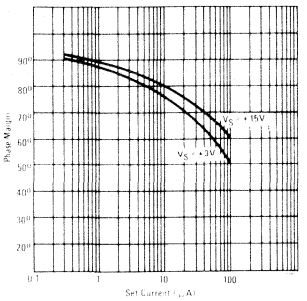


Typical Performance Curves (Continued) T_A = +25°C, V_S = ±15V D.C. Unless Otherwise Specified.

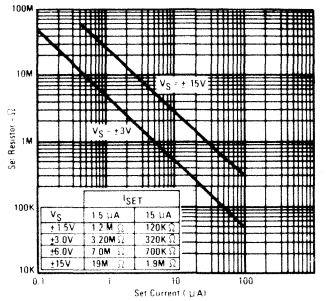
SLEW RATE vs. I_{SET}



PHASE MARGIN vs. SET CURRENT



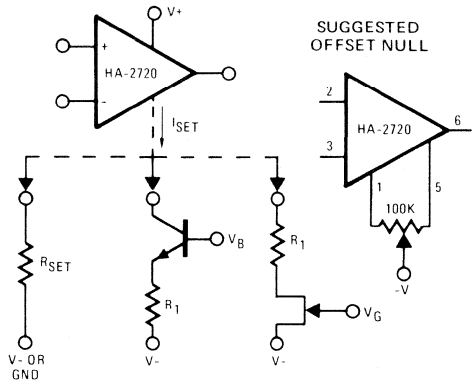
SET CURRENT vs. SET RESISTOR



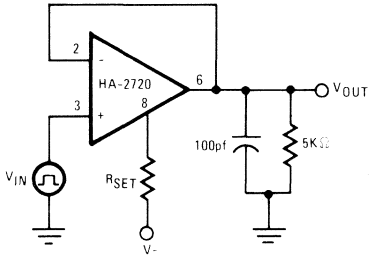
V_S	I_{SET} 1.5 µA	15 µA
±1.5V	1.2 MΩ	120KΩ
±3.0V	3.20MΩ	320KΩ
±6.0V	7.0MΩ	700KΩ
±15V	19MΩ	1.9MΩ

Test Circuits

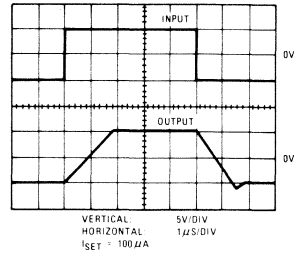
TYPICAL BIASING CIRCUITS



TRANSIENT RESPONSE/SLEW RATE CIRCUIT



SLEWING WAVEFORM



Die Characteristics

Transistor Count 44
Die Dimensions ..... 60 x 44 x 19mils
Substrate Potential ..... Unbiased

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
HA2-Metal Can (-2,-5)	212	58
HA2-Metal Can (-8)	173	52
HA7-Ceramic DIP (-2,-5)	218	123
HA7-Ceramic DIP (-8)	143	69
HA3-Plastic Mini-DIP (-5)	98	46

HARRIS

HA-4741

Quad Operational Amplifier

Features

- Slew Rate 1.6V/μs
- Bandwidth 3.5MHz
- Input Voltage Noise ..... 9nV/√Hz
- Input Offset Voltage 0.5mV
- Input Bias Current 60nA
- Supply Range ..... ±2V to ±20V
- No Crossover Distortion
- Standard Quad Pin-Out

Applications

- Universal Active Filters
- D3 Communications Filters
- Audio Amplifiers
- Battery-Powered Equipment

Description

HA-4741, which contains four amplifiers on a monolithic chip, provides a new measure of performance for general purpose operational amplifiers. Each amplifier in the HA-4741 has operating specifications that equal or exceed those of the 741-type amplifier in all categories of performance.

HA-4741 is well suited to applications requiring accurate signal processing by virtue of its low values of input offset voltage (0.5mV), input bias current (60nA) and input voltage noise (9nV/√Hz at 1kHz). 3.5MHz bandwidth, coupled with high open-loop gain, allow the HA-4741 to be used in designs requiring amplification of wide band signals, such as audio amplifiers. Audio application is further enhanced by the HA-4741's negligible output crossover distortion.

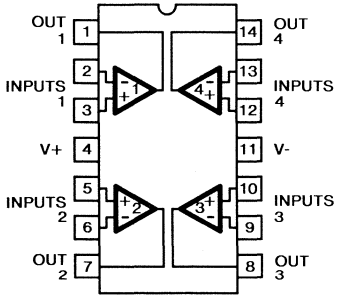
These excellent dynamic characteristics also make the HA-4741 ideal for a wide range of active filter designs. Performance integrity of multi-channel designs is assured by a high level of amplifier-to-amplifier isolation (108dB at 1kHz).

A wide range of supply voltages (±2V to ±20V) can be used to power the HA-4741, making it compatible with almost any system including battery-powered equipment.

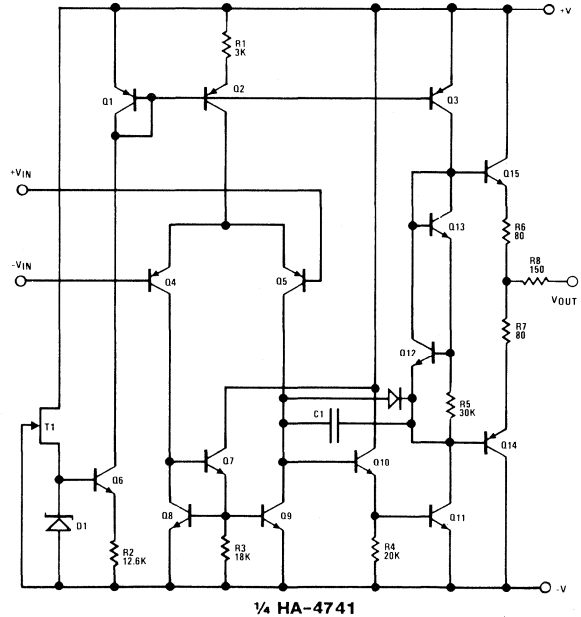
The HA-4741is available in a 14 Pin Ceramic and Epoxy Mini-DIPs. The HA-4741-2 operates from -55°C to +125°C and the HA-4741-5 operates over the 0°C to +75°C temperature range. HA-4741/883 product and data sheets available upon request.

Pinout

HA1-4741 (CERAMIC)
HA3-4741 (EPOXY)
TOP VIEW



Schematic



¼ HA-4741

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 13)

T_A = +25°C Unless Otherwise Stated
Voltage Between V+ and V- Terminals 40.0V
Differential Input Voltage ..... ±30.0V
Input Voltage (Note 1) ..... ±15.0V
Output Short Circuit Duration (Note 2) ..... Indefinite
Power Dissipation For Epoxy Package (Note 3) 880mW

Operating Temperature Ranges

HA-4741-2 ..... $-55°C \leq T_A \leq +125°C$
HA-4741-5 ..... $0°C \leq T_A \leq +75°C$
Storage Temperature Range ..... $-65°C \leq T_A \leq +150°C$

Electrical Specifications

V+ = +15V, V- = -15V, Unless Otherwise Specified.

PARAMETER	TEMP	HA-4741-2 -55°C to +125°C			HA-4741-5 0°C to +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Offset Voltage	+25°C	-	0.5	3	-	1	5	mV
	Full	-	4	5	-	4	6.5	mV
Average Offset Voltage Drift	Full	-	5	-	-	5	-	µV/°C
Bias Current	+25°C	-	60	200	-	60	300	nA
	Full	-	-	325	-	-	400	nA
Offset Current	+25°C	-	15	30	-	30	50	nA
	Full	-	-	75	-	-	100	nA
Common Mode Range	Full	±12	-	-	±12	-	-	V
Differential Input Resistance	+25°C	-	0.5	-	-	0.5	-	MΩ
Input Voltage Noise (f = 1kHz)	+25°C	-	9	-	-	9	-	$nV/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Notes 4)	+25°C	50K	100K	-	25K	50K	-	V/V
	Full	25K	-	-	15K	-	-	V/V
Common Mode Rejection Ratio	+25°C	80	95	-	80	95	-	dB
	Full	74	-	-	74	-	-	dB
Channel Separation (Note 5)	+25°C	90	108	-	90	108	-	dB
Small Signal Bandwidth	+25°C	2.5	3.5	-	2.5	3.5	-	MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (R_L = 10K)	Full	±12	±13.7	-	±12	±13.7	-	V
(R_L = 2K)	Full	±10	±12.5	-	±10	±12.5	-	V
Full Power Bandwidth (Notes 4 &9)	+25°C	14	25	-	14	25	-	kHz
Output Current (Note 6)	Full	±5	±15	-	±5	±15	-	mA
Output Resistance	+25°C	-	300	-	-	300	-	Ω
TRANSIENT RESPONSE (Note 7 & 10)								
Rise Time (Note 11)	+25°C	-	75	140	-	75	140	ns
Overshoot (Note 11)	+25°C	-	25	40	-	25	40	%
Slew Rate (Note 12)	+25°C	-	±1.6	-	-	±1.6	-	V/µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C	-	4.5	5	-	5	7	mA
Power Supply Rejection Ratio (Note 8)	Full	80	95	-	80	95	-	dB

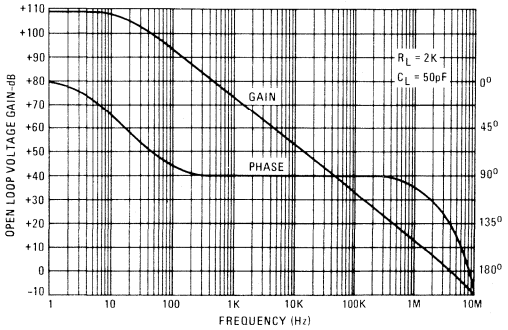
NOTES:

1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. One amplifier may be shorted to ground indefinitely.
3. Derate 5.8mW/°C above T_A = +25°C.
4. V_{OUT} = ±10, R_L = 2K.
5. Referred to input; f = 10kHz, R_S = 1K.
6. V_{OUT} = ±10.
7. See Pulse Response Characteristics.
8. ΔV = ±5V.
9. Full power bandwidth guaranteed based upon slew rate measurement FPBW = S.R./2π V_{PEAK}.
10. R_L = 2K, C_L = 50pF.
11. V_{OUT} = ±200mV.
12. V_{OUT} = ±5V.
13. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

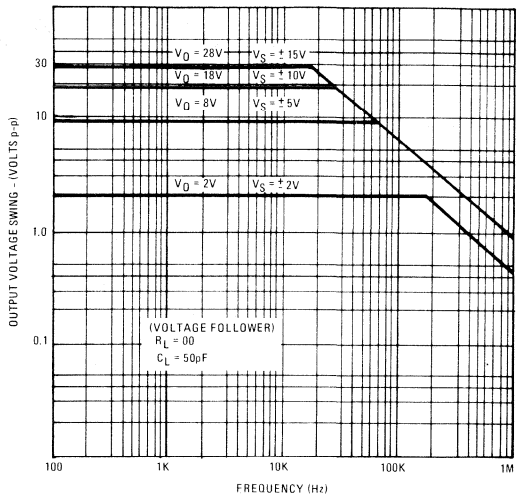
Typical Performance Curves

V+ =+15V, V- = -15V, T_A = +25°C, Unless Otherwise Specified.

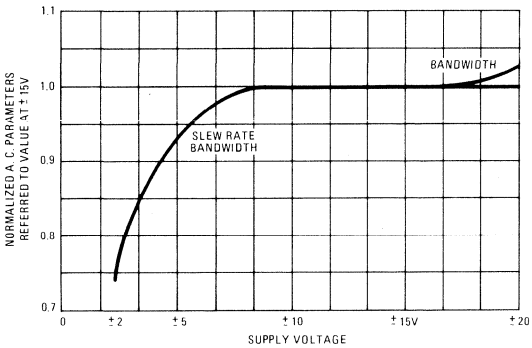
OPEN LOOP FREQUENCY RESPONSE



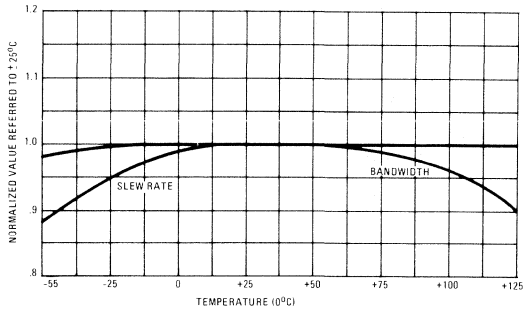
OUTPUT VOLTAGE SWING vs. FREQUENCY



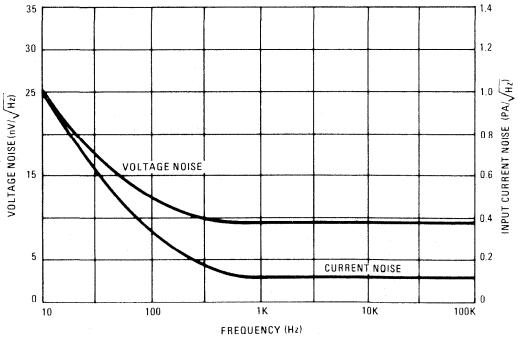
NORMALIZED AC PARAMETERS vs. SUPPLY VOLTAGE



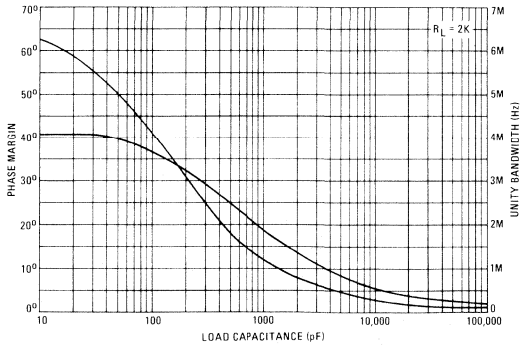
NORMALIZED AC PARAMETERS vs. TEMPERATURE



INPUT NOISE vs. FREQUENCY

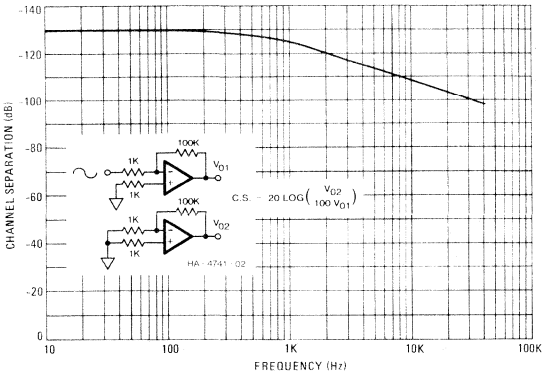


SMALL SIGNAL BANDWIDTH AND PHASE MARGIN vs. LOAD CAPACITANCE

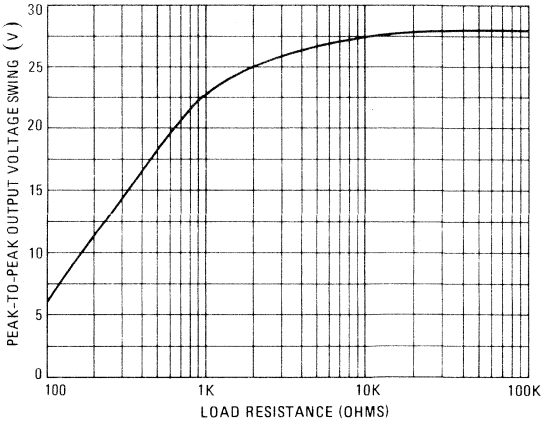


Typical Performance Curves (Continued)

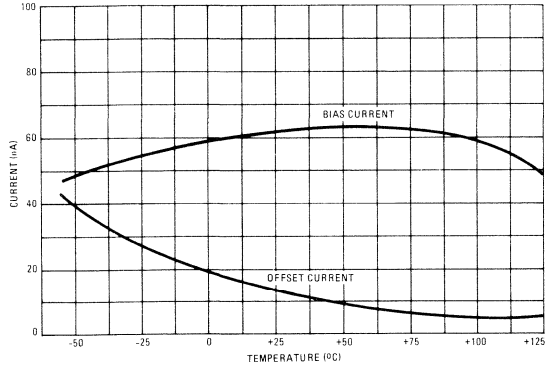
CHANNEL SEPARATION vs. FREQUENCY



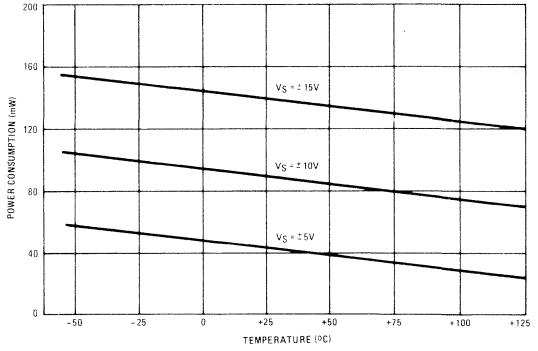
MAXIMUM OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE



INPUT BIAS AND OFFSET CURRENT vs. TEMPERATURE

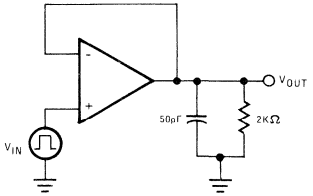


POWER CONSUMPTION vs. TEMPERATURE



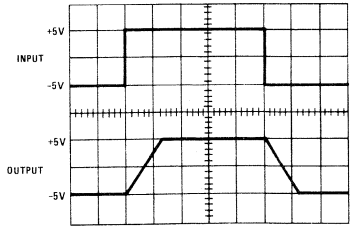
Pulse Response

TRANSIENT RESPONSE/SLEW RATE CIRCUIT



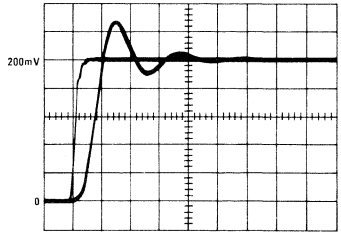
SLEW RESPONSE

(Volts: 5V/Div., Time: 5µs/Div.)



TRANSIENT RESPONSE

(Volts: 40mV/Div., Time: 100ns/Div.)



HARRIS

HA-4900/02/05

Precision Quad Comparator

Features

- **Fast Response Time 130ns**
- **Low Offset Voltage 2.0mV**
- **Low Offset Current 10nA**
- **Single or Dual-Voltage Supply Operation**
- **Selectable Output Logic Levels**
- **Active Pull-Up/Pull-Down Output Circuit-No External Resistors Required**

Applications

- **Threshold Detector**
- **Zero-Crossing Detector**
- **Window Detector**
- **Analog Interfaces for Microprocessors**
- **High Stability Oscillators**
- **Logic System Interfaces**

Description

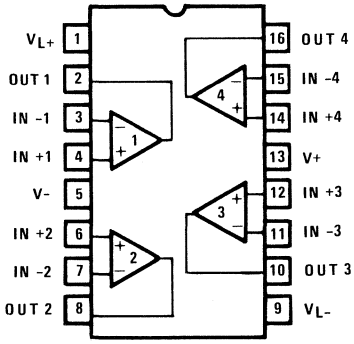
The HA-4900 series are monolithic, quad, precision comparators offering fast response time, low offset voltage, low offset current, and virtually no channel-to-channel crosstalk for applications requiring accurate, high speed, signal level detection. These comparators can sense signals at ground level while being operated from either a single +5 volt supply (digital systems) or from dual supplies (analog networks) up to ±15volts. The HA-4900 series contains a unique current driven output stage which can be connected to logic system supplies (V_{Logic} + and V_{Logic} -) to make the output levels directly compatible (no external components needed) with any standard logic or special system logic levels. In combination analog/digital systems, the design employed in the HA-4900 series input and output stages prevents troublesome ground coupling of signals between analog and digital portions of the system.

These comparators' combination of features makes them ideal components for signal detection and processing in data acquisition systems, test equipment, and microprocessor/analog signal interface networks.

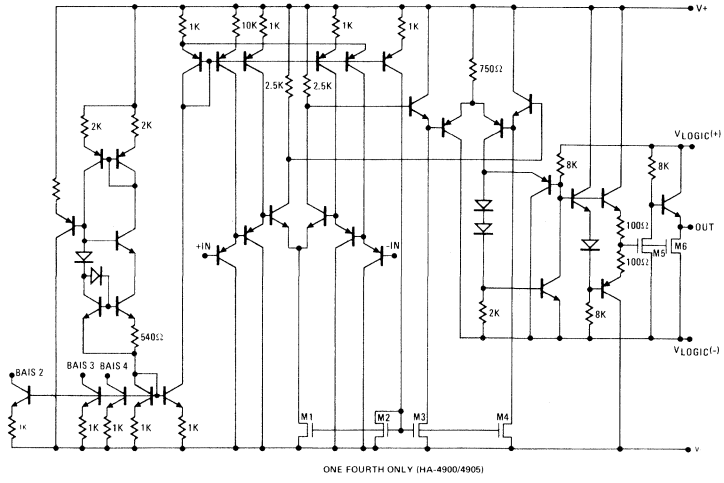
All devices are available in 16 pin dual-in-line ceramic packages. The HA-4900/4902-2 operates from -55°C to +125°C and the HA-4905-5 operates over a 0°C to +75°C temperature range. For military grade product, refer to the HA-4902/883 data sheet.

Pinouts

HA1-4900/02/05 (CERAMIC DIP)
TOP VIEW



Schematic



ONE FOURTH ONLY (HA-4900/4905)

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Terminals 33V
Differential Input Voltage..... ±15V
Voltage Between V_{Logic} (+) and V_{Logic}(-)..... 18V
Peak Output Current ..... ±50mA
Internal Power Dissipation (Note 7, 8) 2.0W

Operating Temperature Ranges

HA-4900-2 ..... $-55^oC \leq T_A \leq +125^oC$
HA-4902-2 ..... $-55^oC \quad T_A \quad +125^oC$
HA-4905-5 ..... $0^oC \leq T_A \leq +75^oC$
Storage Temperature Range: ..... $-65^oC \leq T_A \leq +150^oC$

Electrical Specifications

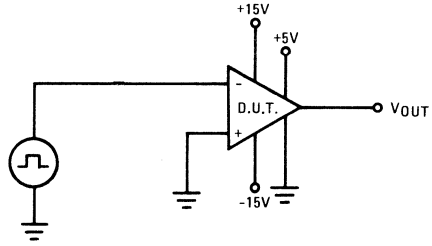
V+ = +15V, V- = -15V, V_{Logic} (+) = 5V, V_{Logic} (-) = GND.

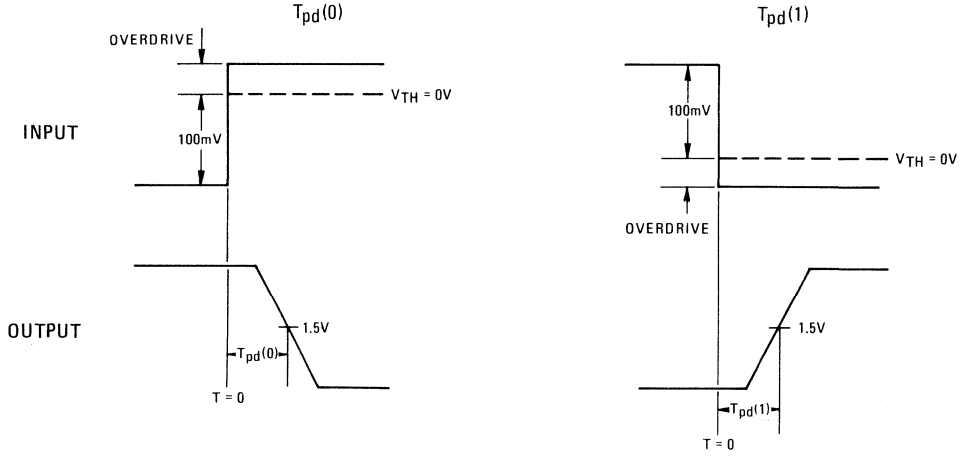
PARAMETER	TEMP	HA-4900-2 -55°C to +125°C MIN	TYP	MAX	HA-4902-2 -55°C to +125°C MIN	TYP	MAX	HA-4905-5 0°C to +75°C MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS											
Offset Voltage (Note 2)	25°C		2	3		2	5		4	7.5	mV
	Full			4			8			10	mV
Offset Current	25°C		10	25		10	35		25	50	nA
	Full			35			45			70	nA
Bias Current (Note 3)	25°C		50	75		50	150		100	150	nA
	Full			150			200			300	nA
Input Sensitivity (Note 4)	25°C			Vio +.3			Vio +.5			Vio +.5	mV
	Full			Vio +.4			Vio +.6			Vio +.7	mV
Common Mode Range	Full	V-		(V+)-2.4	V-		(V+)-2.6	V-		(V+)-2.4	V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain	25°C		400K			400K			400K		V/V
Response Time ($T_{pd}0$) (Note 5)	25°C		130	200		130	200		130	200	ns
Response Time ($T_{pd}1$) (Note 5)	25°C		180	215		180	215		180	215	ns
OUTPUT CHARACTERISITICS											
Output Voltage Level											
Logic "Low State" (V_{OL}) (Note 6)	Full		0.2	0.4		0.2	0.4		0.2	0.4	V
Logic "High State" (V_{OH}) (Note 6)	Full	3.5	4.2		3.5	4.2		3.5	4.2		V
Output Current											
I_{Sink}	Full	3.0			3.0			3.0			mA
I_{Source}	Full	3.0			3.0			3.0			mA
POWER SUPPLY CHARACTERISTICS											
Supply Current, I_{ps} (+)	25°C		6.5	20		6.5	20		7	20	mA
Supply Current , I_{ps} (-)	25°C		4	8		4	8		5	8	mA
Supply Current, I_{ps} (Logic)	25°C		3.5	6		3.5	6		3.5	6	mA
Supply Voltage Range											
V_{Logic} (+) (Note 7)	Full	0		+15.0	0		+15.0	0		+15.0	V
V_{Logic} (-) (Note 7)	Full	-15.0		0	-15.0		0	-15.0		0	V

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Minimum differential input voltage required to ensure a defined output state.
3. Input bias currents are essentially constant with differential input voltages up to ± 9 volts. With differential input voltages from ±9 to ±15 volts, bias current on the more negative input can rise to approximately 500µA. This will also cause higher supply currents.
4. $R_S \leq 200$ ohms; $V_{IN} \leq$ Common Mode Range. Input sensitivity is the worst case minimum differential input voltage required to guarantee a given output logic state. This parameter includes the effects of offset voltage, offset current, common mode rejection, and voltage gain.
5. For $T_{pd}(1)$; 100mV input step, -10mV overdrive. For $T_{pd}(0)$; -100mV input step, 10mV overdrive. Frequency ≈ 100Hz; Duty Cycle ≈ 50%; Inverting input driven. See Test Circuit below. All unused inverting inputs tie to +5V.
6. For V_{OH} and V_{OL}: $I_{Sink} = I_{Source} = 3.0$mA. For other values of V_{Logic}: V_{OH} (min.) = V_{Logic} + -1.5V.
7. Total Power Dissipation (T.P.D.) is the sum of individual dissipation contributions of V+, V- and V_{Logic} shown in curves of Power Dissipation vs. Supply Voltages (see Performance Curves). The calculated T.P.D. is then located on the graph of Maximum Allowable Package Dissipation vs. Ambient Temperature to determine ambient temperature operating limits imposed by the calculated T.P.D. (See Performance Curves). For instance, the combination of +15V, -15V, +5V, 0V (V+, V-, V_{Logic}+, V_{Logic}-) gives a T.P.D. of 350mW, the combination +15V, -15V, 0V gives a T.P.D. of 450mW.
8. Derate By 5.8mW/°C above $T_A = +75$°C. $\theta_{ja} = 75$°C/W, $\theta_{jc} = 20$°C/W.

Test Circuits



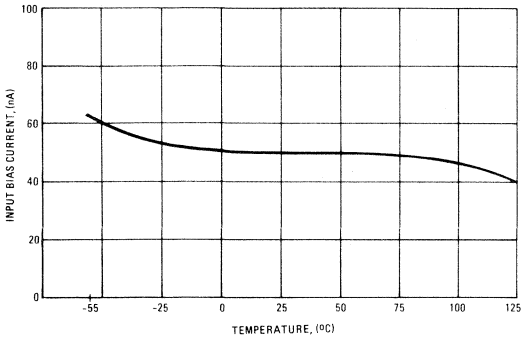


For input and output voltage waveforms for various input overdrives see Performance Curves.

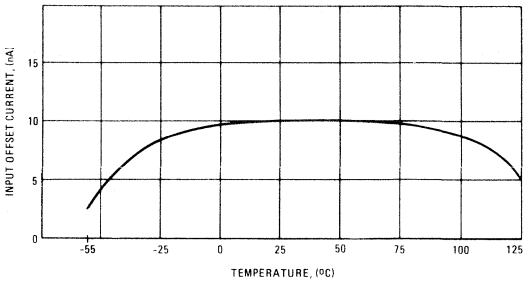
Typical Performance Curves

$V+ = 15V$, $V_{Logic}(+) = 5V$, $V_{Logic}(-) = 0V$, $T_A = +25^oC$, Unless Otherwise Specified.

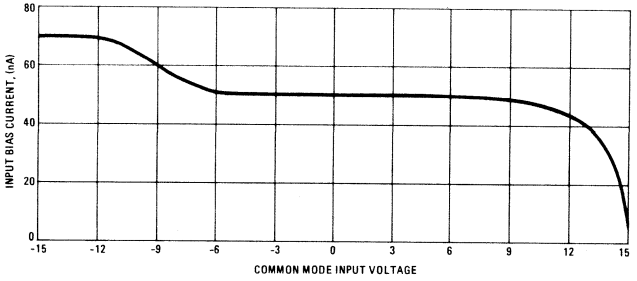
INPUT BIAS CURRENT vs. TEMPERATURE



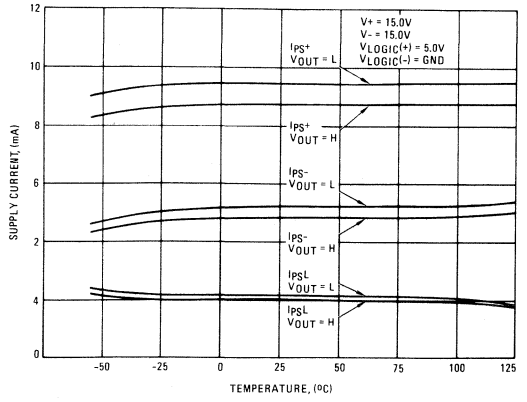
INPUT OFFSET CURRENT vs. TEMPERATURE



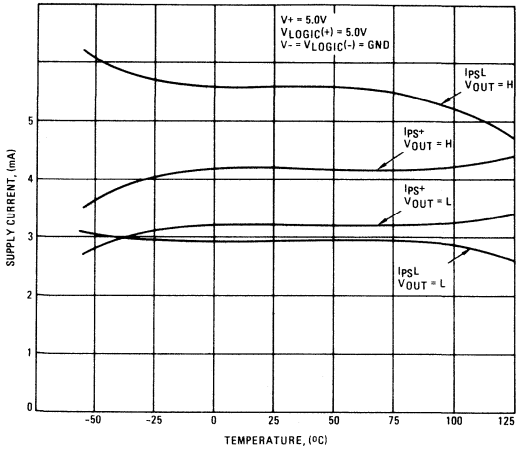
INPUT BIAS CURRENT vs. COMMON MODE INPUT VOLTAGE
($V_{DIFF.} = 0V$)



SUPPLY CURRENT vs. TEMPERATURE
FOR ±15V SUPPLIES AND +5V LOGIC SUPPLY

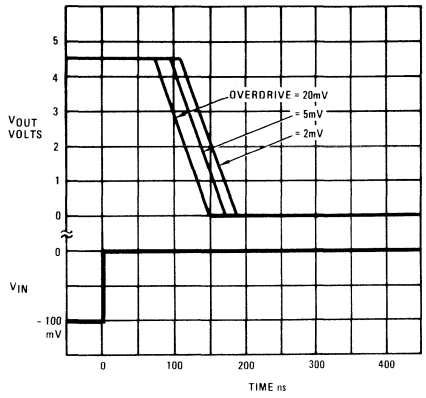


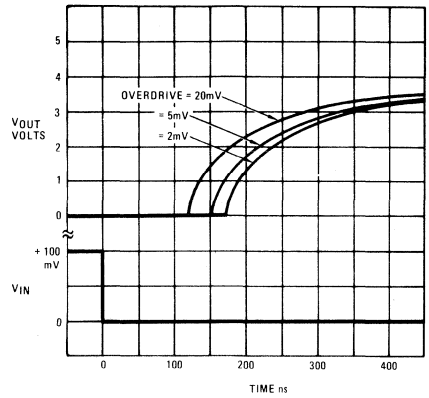
SUPPLY CURRENT vs. TEMPERATURE
FOR SINGLE +5V OPERATION



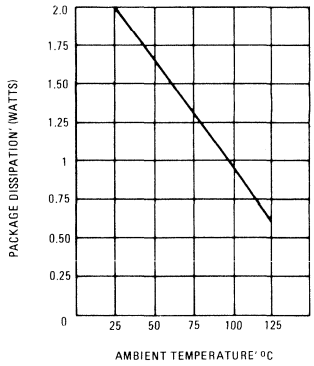
Typical Performance Curves (Continued)

RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

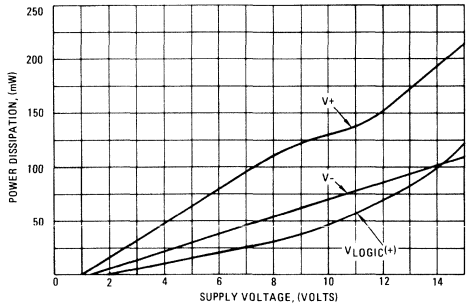




MAXIMUM PACKAGE DISSIPATION vs. $T_{AMBIENT}$



MAXIMUM POWER DISSIPATION vs. SUPPLY VOLTAGE (NO LOAD CONDITION)



Applying the HA-4900 Series Comparators

1. SUPPLY CONNECTIONS: This device is exceptionally versatile in working with most available power supplies. The voltage applied to the V+ and V- terminals determines the allowable input signal range; while the voltage applied to the V_L+ and V_L- determines the output swing. In systems where dual analog supplies are available, these would be connected to V+ and V-, while the logic supply and return would be connected to V_{Logic}+ and V_{Logic}-. The analog and logic supply commons can be connected together at one point in the system, since the comparator is immune to noise on the logic supply ground. A negative output swing may be obtained by connecting V_L+ to ground and V_L- to a negative supply. Bipolar output swings (15V P-P, max.) may be obtained using dual supplies. In systems where only a single logic supply is available (+5V to +15V), V+ and V_{Logic}+ may be connected together to the positive supply while V- and V_{Logic}- are grounded. If an input signal could swing negative with respect the V- terminal, a resistor should be connected in series with the input to limit input current to $< 5mA$ since the C-B junction of the input transistor would be forward biased.

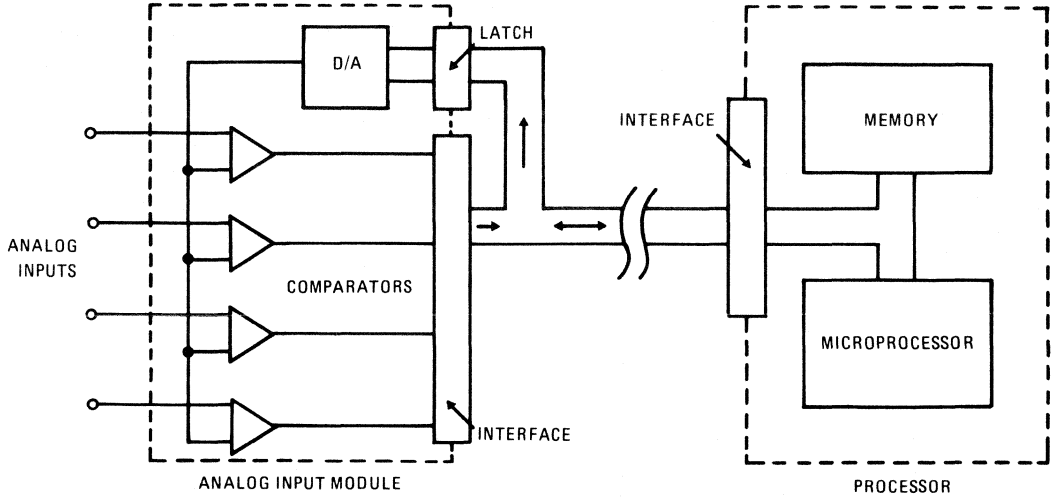
2. UNUSED INPUTS: Inputs of unused comparator sections should be tied to a differential voltage source to prevent output "chatter".

3. CROSSTALK: Simultaneous high frequency operation of all other channels in the package will not affect the output logic state of a given channel, provided that its differential input voltage is sufficient to define a given logic state ($\Delta V_{IN} \geq \pm V_{OS}$). Low level or high impedance input lines should be shielded from other signal sources to reduce crosstalk and interference.

4. POWER SUPPLY DECOUPLING: Decouple all power supply lines with .01 μ F ceramic capacitors to a ground line located near the package to reduce coupling between channnels or from external sources.

5. RESPONSE TIME: Fast rise time ($<$ 200ns) input pulses of several volts amplitude may result in delay times somewhat longer than those illustrated for 100mV steps. Operating speed is optimized by limiting the maximum differential input voltage applied, with resistor-diode clamping networks.

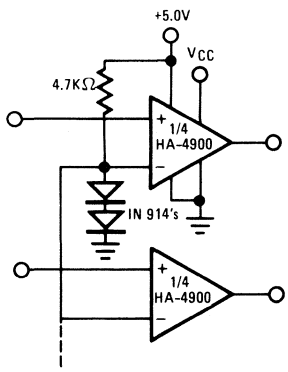
Typical Applications



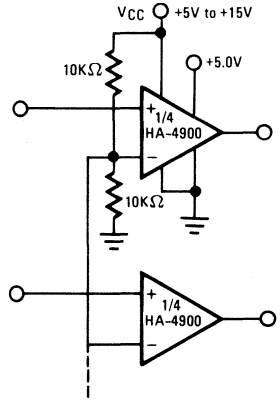
DATA ACQUISITION SYSTEM

In this circuit the HA-4900 series is used in conjunction with a D to A converter to form a simple, versatile, multi-channel analog input for a data acquisition system. In operation the processor first sends an address to the D to A, then the processor reads the digital word generated by the comparator outputs.

To perform a simple comparison, the processor sets the D to A to a given reference level, then examines one or more comparator outputs to determine if their inputs are above or below the reference. A window comparison consists of two such cycles with 2 reference levels set by the D to A. One way to digitize the inputs would be for the processor to increment the D to A in steps. The D to A address, as each comparator switches, is the digitized level of the input. While stairstepping the D to A is slower than successive approximation, all channels are digitized during one staircase ramp.



TTL TO CMOS



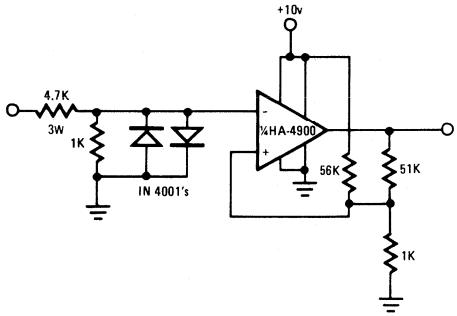
CMOS TO TTL

LOGIC LEVEL TRANSLATORS

The HA-4900 series comparators can be used as versatile logic interface devices as shown in the circuits above. Negative logic devices may also be interfaced with appropriate supply connections.

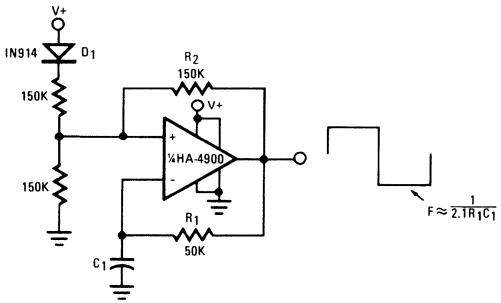
If separate supplies are used for V- and V_{Logic}-, these logic level translators will tolerate several volts of ground line differential noise.

Typical Applications (Continued)



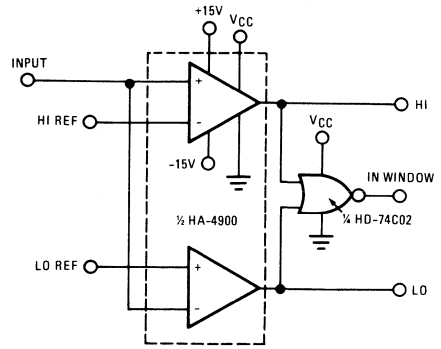
RS-232 TO CMOS LINE RECEIVER

This RS-232 type line receiver to drive CMOS logic uses a Schmitt trigger feedback network to give about 1 volt input hysteresis for added noise immunity. A possible problem in an interface which connects two equipments, each plugged into a different AC receptacle, is that the power line voltage may appear at the receiver input when the interface connection is made or broken. The two diodes and a 3 watt input resistor will protect the inputs under these conditions.



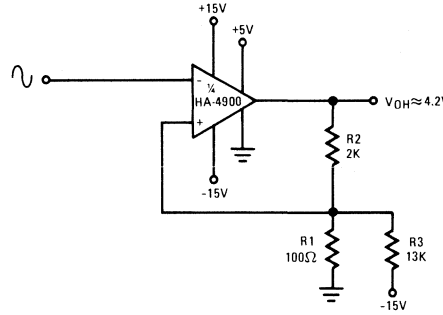
OSCILLATOR/CLOCK GENERATOR

This self-starting fixed frequency oscillator circuit gives excellent frequency stability. R_1 and C_1 comprise the frequency determining network while R_2 provides the regenerative feedback. Diode D_1 enhances the stability by compensating for the difference between V_{OH} and V_{Supply}. In applications where a precision clock generator up to 100kHz is required, such as in automatic test equipment, C_1 may be replaced by a crystal.



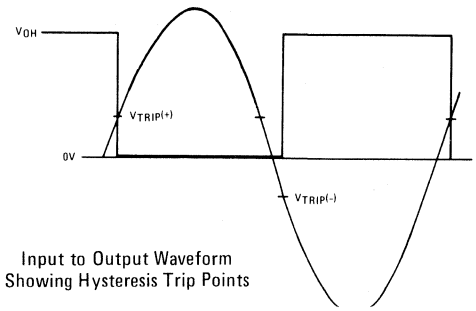
WINDOW DETECTOR

The high switching speed, low offset current and low offset voltage of the HA-4900 series makes this window detector circuit extremely well suited to applications requiring fast, accurate, decision-making. The circuit above is ideal for industrial process system feedback controllers or "out-of-limit" alarm indicators.



SCHMITT TRIGGER (ZERO CROSSING DETECTOR WITH HYSTERESIS)

This circuit has a 100mV hysteresis which can be used in applications where very fast transition times are required at the output even though the signal input is very slow. The hysteresis loop also reduces false triggering due to noise on the input. The waveforms below show the trip points developed by the hysteresis loop.



Input to Output Waveform
Showing Hysteresis Trip Points

HA-5002

Monolithic, Wideband, High Slew Rate, High Output Current Buffer

Features

- Voltage Gain 0.995
- High Input Impedance 3000kΩ
- Low Output Impedance 3Ω
- Very High Slew Rate 1300V/μsec
- Very Wide Bandwidth 110MHz
- High Output Current ..... ±200mA
- Pulsed Output Current 400mA
- Monolithic Construction

Applications

- Line Driver
- Data Acquisition
- 110MHz Buffer
- High Power Current Booster
- High Power Current Source
- Sample and Holds
- Radar Cable Driver
- Video Products

Description

The HA-5002 is a monolithic, wideband, high slew rate, high output current, buffer amplifier.

Utilizing the advantages of the Harris D.I. technologies, the HA-5002 current buffer offers 1300V/μsec slew rate with 110MHz of bandwidth. The ±200mA output current capability is enhanced by a 3 ohm output impedance.

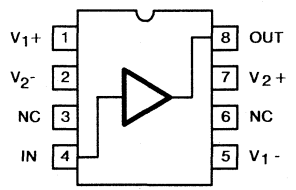
The monolithic HA-5002 will replace the hybrid LH0002 with corresponding performance increases. These characteristics range from the 3000K ohm input impedance to the increased output voltage swing. Monolithic design technologies have allowed a more precise buffer to be developed with more than an order of magnitude smaller gain error.

The HA-5002 will provide many present hybrid users with a higher degree of reliability and at the same time increase overall circuit performance.

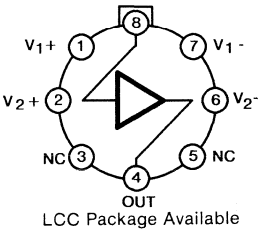
The HA-5002 is available in an 8 pin Metal Can, and 8 pin Ceramic and Plastic Mini-DIPs. For the military grade product, refer to the HA-5002/883 Data Sheet.

Pinouts

HA7-5002 (CERAMIC MINI-DIP)
HA3-5002 (PLASTIC MINI-DIP)
TOP VIEW

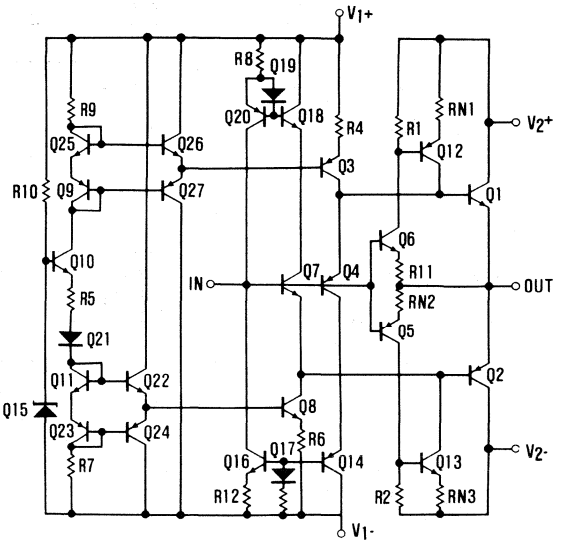


HA2-5002 (TO-99 METAL CAN)
TOP VIEW



LCC Package Available for HA-5002/883.
See HA-5002/883 Data Sheet

Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- pins 44V
Input Voltage ..... Equal to Supplies
Output Current ..... Continuous ±200mA
Output Current ..... (50ms On, 1s Off) ± 400mA
Internal Power Dissipation (Note 2)
TO-99 (+25°C) 1.11W
Mini-DIP (+25°C) 1.21W
LCC (+25°C) 1.51W

Operating Temperature Range

Maximum Junction Temperature ..... +175°C
HA-5002-2 ..... $-55^{\circ}C \leq T_A \leq +125^{\circ}C$
HA-5002-5 ..... $0^{\circ}C \leq T_A \leq +75^{\circ}C$
Storage Temperature Range ..... $-65^{\circ}C \leq T_A \leq +150^{\circ}C$

Electrical Specifications

V_{SUPPLY} = ± 12V to ± 15V, R_S = 50Ω, R_L = 1kΩ, C_L = 10pF, Unless Otherwise Specified.

PARAMETER	TEMP	HA-5002-2			HA-5002-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		5	20		5	20	mV
	Full		10	30		10	30	mV
Avg. Offset Voltage Drift	Full		30			30		µV/°C
Bias Current	+25°C		2	7		2	7	µA
	Full		3.4	10		2.4	10	µA
Input Resistance	Full	1.5	3		1.5	3		MΩ
Input Noise Voltage (10Hz-1MHz)	+25°C		4			4		µVp-p
TRANSFER CHARACTERISTICS								
Voltage Gain (Note 7)								
R_L = 100Ω	+25°C		0.971			0.971		V/V
R_L = 1kΩ	+25°C		0.995			0.995		V/V
R_L = 1kΩ	Full	0.990			0.980			V/V
-3dB Bandwidth (Note 4)	+25°C		110			110		MHz
AC Current Gain	+25°C		40			40		A/mA
OUTPUT CHARACTERISTICS								
Output Voltage Swing								
R_L = 100Ω	+25°C	±10	±10.7		±10	±11.2		V
R_L = 1kΩ (Note 3)	Full	±10	±13.5		±10	±13.9		V
R_L = 1kΩ (Note 5)	Full	±10	±10.5		±10	±10.5		V
Output Resistance	Full		3	10		3	10	Ω
Harmonic Distortion (Note 6)	+25°C		<0.005			<0.005		%
TRANSIENT RESPONSE								
Full Power Bandwidth (Note 8)	+25°C		11			11		MHz
Rise Time	+25°C		3.6			3.6		ns
Propagation Delay	+25°C		2			2		ns
Overshoot	+25°C		30			30		%
Slew Rate	+25°C	1.0	1.3		1.0	1.3		V/ns
Settling Time to 0.1%	+25°C		50			50		ns
POWER REQUIREMENTS								
Supply Current	+25°C		8.3			8.3		mA
	Full			10			10	mA
Power Supply Rejection Ratio (Note 9)	Full	54	64		54	64		dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. See thermal constants data in Die Characteristics section.
3. V_{SUPPLY} = ± 15V
4. V_{IN} = 1 V_{RMS}
5. V_{SUPPLY} = ±12V
6. V_{IN} = 1V_{RMS}; f = 10kHz.
7. V_{OUT} = ±10V
8. V_{OUT} = 10V_{p-p}
9. ΔV_{SUPPLY} = 10V

Operating Instructions

Layout Considerations

The wide bandwidth of the HA-5002 necessitates that high frequency circuit layout procedures be followed. Failure to follow these guidelines can result in marginal performance.

Probably the most crucial of the RF/video layout rules is the use of a ground plane. A ground plane provides isolation and minimizes distributed circuit capacitance and inductance which will degrade high frequency performance.

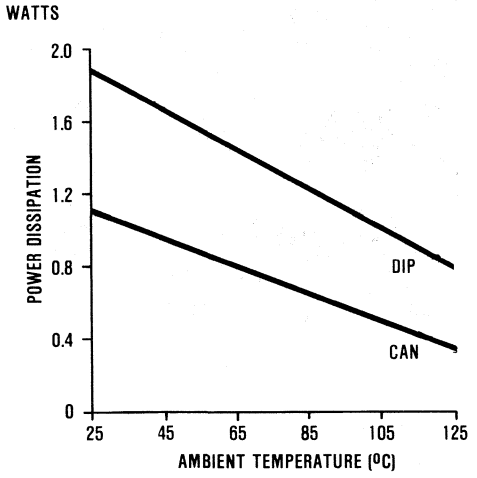
Other considerations are proper power supply bypassing and keeping the input and output connections as short as possible which minimizes distributed capacitance and reduces board space.

Power Supply Decoupling

For optimal device performance, it is recommended that the positive and negative power supplies be bypassed with capacitors to ground. Ceramic capacitors ranging in value from 0.01 to 0.1μF will minimize high frequency variations in supply voltage, while low frequency bypassing requires larger valued capacitors since the impedance of the capacitor is dependent on frequency.

It is also recommended that the bypass capacitors be connected close to the HA-5002 (preferably directly to the supply pins).

FREE AIR POWER DISSIPATION



$$P_{dmax} = \frac{T_{jmax} - T_A}{\theta_{j\text{-}c} + \theta_{c\text{-}s} + \theta_{s\text{-}a}}$$

Where: T_{jmax} = Maximum Junction Temperature of the Device

T_A = Ambient

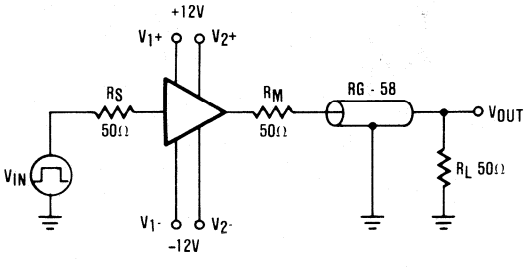
$\theta_{j\text{-}c}$ = Junction to Case Thermal Resistance

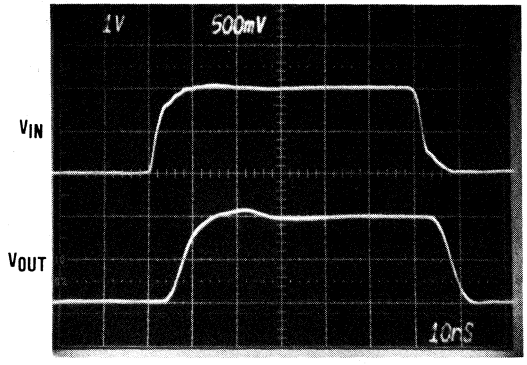
$\theta_{c\text{-}s}$ = Case to Heat Sink Thermal Resistance

$\theta_{s\text{-}a}$ = Heat Sink to Ambient Thermal Resistance

Test Circuits

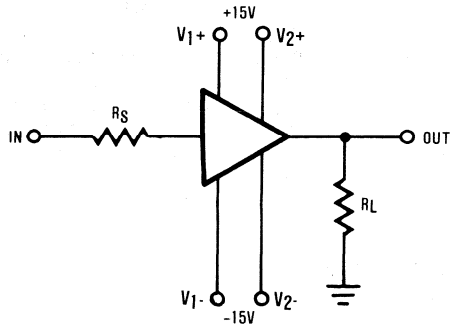
COAXIAL CABLE DRIVER - 50Ω SYSTEM



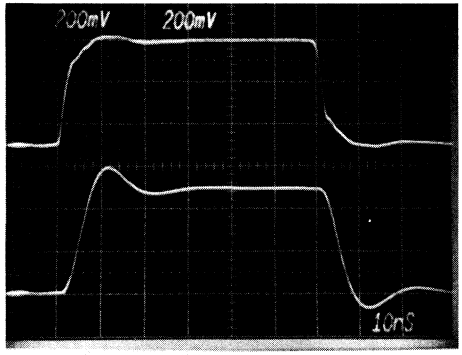


Test Circuits

LARGE AND SMALL SIGNAL RESPONSE

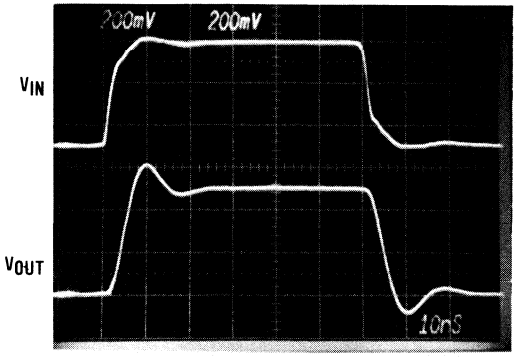


SMALL SIGNAL WAVEFORMS



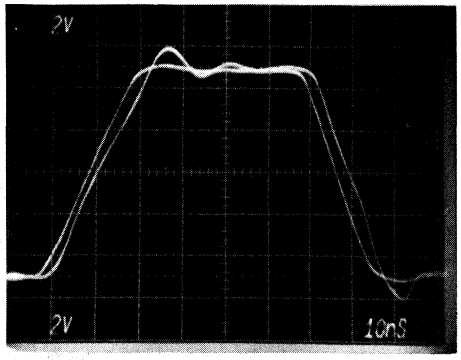
$R_S = 50\Omega$
$R_L = 100\Omega$

SMALL SIGNAL WAVEFORMS



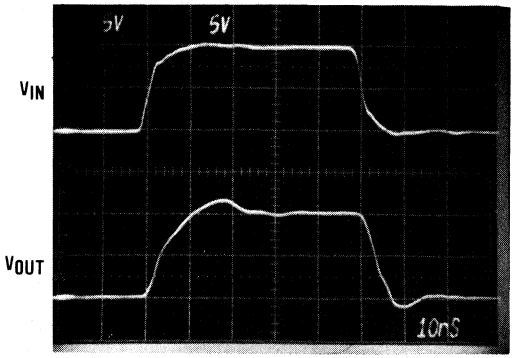
$R_S = 50\Omega$
$R_L = 1k\Omega$

LARGE SIGNAL WAVEFORMS



$R_S = 50\Omega$
$R_L = 1k\Omega$

LARGE SIGNAL WAVEFORMS

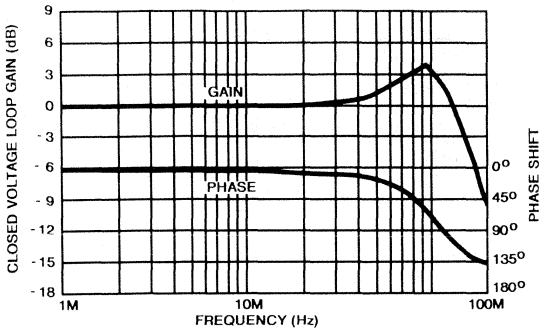


$R_S = 50\Omega$
$R_L = 1k\Omega$

Typical Performance Curves

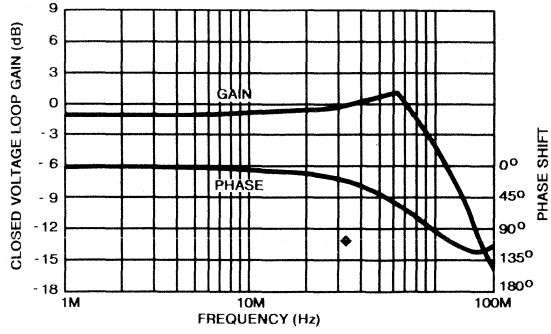
GAIN/PHASE vs. FREQUENCY

V_{CC} = ±15V, R_L = 1K, R_S = 50Ω



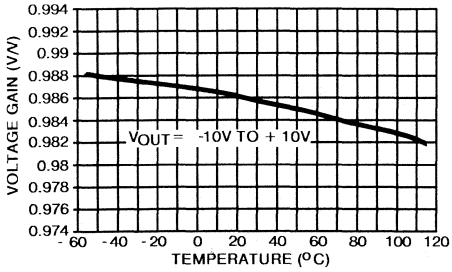
GAIN/PHASE vs. FREQUENCY

V_{CC} = ±15V, R_L = 50Ω, R_S = 50Ω



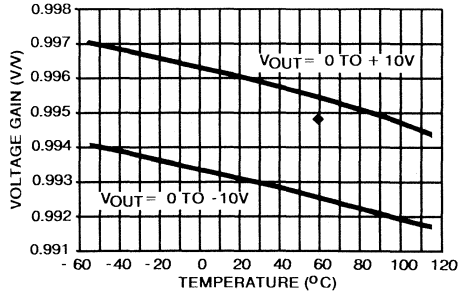
VOLTAGE GAIN vs. TEMPERATURE

V_{CC} = ±15V, R_{LOAD} = 100Ω



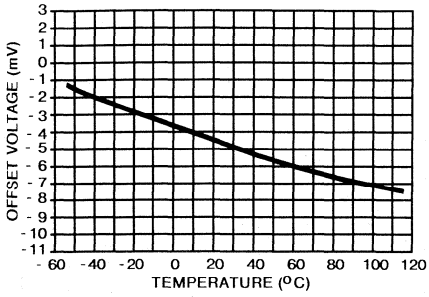
VOLTAGE GAIN vs. TEMPERATURE

V_{CC} = ±15V, R_{LOAD} = 1kΩ



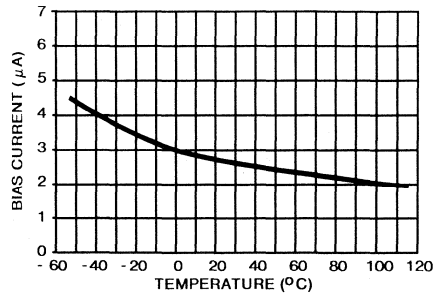
OFFSET VOLTAGE vs. TEMPERATURE

V_{CC} = ±15V



BIAS CURRENT vs. TEMPERATURE

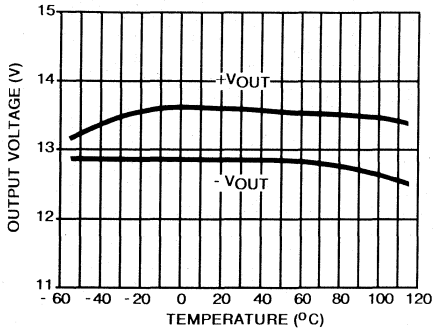
V_{CC} = ±15V



Typical Performance Curves (Continued)

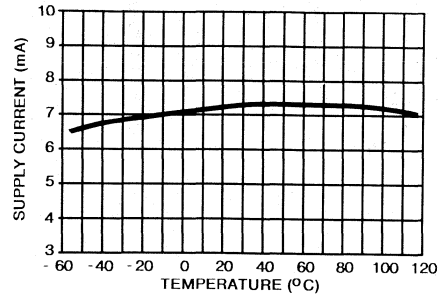
MAXIMUM OUTPUT VOLTAGE vs. TEMPERATURE

V_{CC} = ±15V, R_{LOAD} = 100Ω



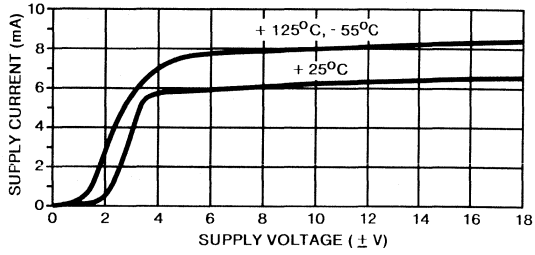
SUPPLY CURRENT vs. TEMPERATURE

V_{CC} = ±15V, I_{OUT} = 0mA



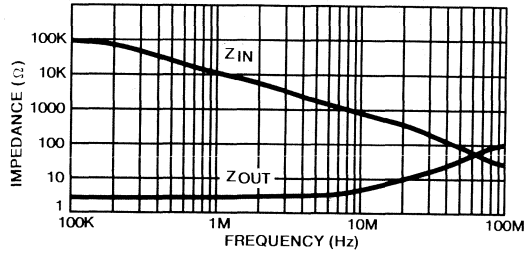
SUPPLY CURRENT vs. SUPPLY VOLTAGE

I_{OUT} = 0mA



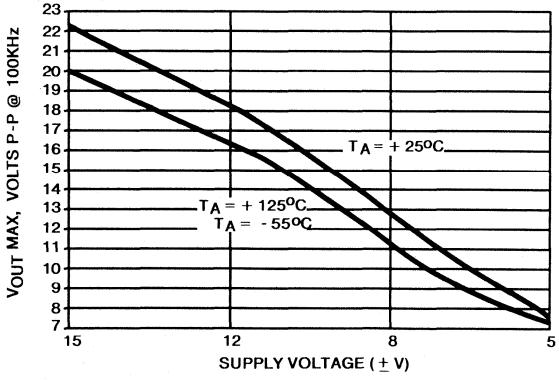
INPUT/OUTPUT IMPEDANCE vs. FREQUENCY

V_{CC} = ±15V

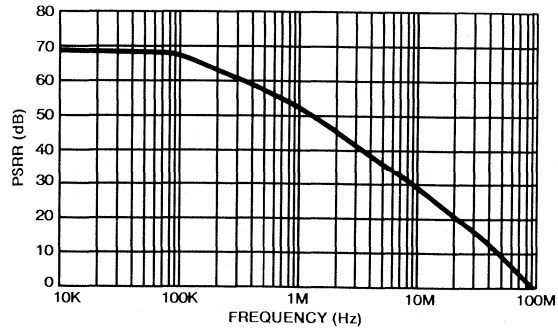


V_{OUT} MAXIMUM vs. V_{SUPPLY}

R_{LOAD} = 100Ω

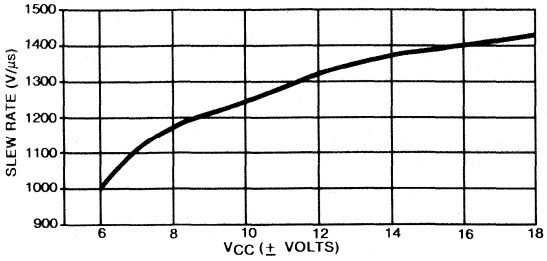


PSRR vs. FREQUENCY

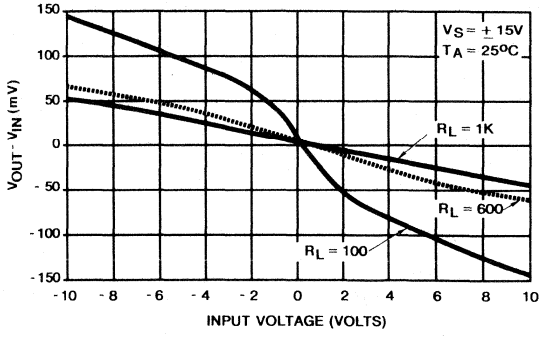


Typical Performance Curves (Continued)

SLEW RATE vs. SUPPLY VOLTAGE



GAIN ERROR vs. INPUT VOLTAGE



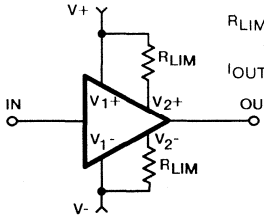
Typical Applications

OPERATION AT REDUCED SUPPLY LEVELS

The HA-5002 can operate at supply voltage levels as low as ±5V and lower. Output swing is directly affected as well as slight reductions in slew rate and bandwidth.

SHORT CIRCUIT PROTECTION

The output current can be limited by using the following circuit:



$$R_{LIM} = \frac{V+}{I_{OUTMAX}} = \frac{V-}{I_{OUTMAX}}$$

I_{OUTMAX} = 200mA (CONTINUOUS)

CAPACITIVE LOADING

The HA-5002 will drive large capacitive loads without oscillation but peak current limits should not be exceeded. Following the formula $I = C\frac{dv}{dt}$ implies that the slew rate or the capacitive load must be controlled to keep peak current below the maximum or use the current limiting approach as shown. The HA-5002 can become unstable with small capacitive loads (50pF) if certain precautions are not taken. Stability is enhanced by any one of the following: a source resistance in series with the input of 50 ohms to 1K; increasing capacitive load to 150pF or greater; decreasing C_{LOAD} to 20pF or less; adding an output resistor of 10 ohms to 50 ohms; or adding feedback capacitance of 50pF or greater. Adding source resistance generally yields the best results.

Die Characteristics

Transistor Count 27
Die Dimensions ..... 80 x 81 x 19mils (2030 x 2050 x 480μm)
Substrate Potential* ..... V-
Process ..... Bipolar-DI

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
HA7-5002, Ceramic Mini-DIP	123	46
HA3-5002, Plastic DIP	80	20
HA2-5002, Metal Can	133	40

*The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.

HARRIS

HA-5033

Video Buffer

Features

- **Differential Phase Error .....0.1 Degree**
- **Differential Gain Error 0.1%**
- **High Slew Rate 1300V/μs**
- **Wide Bandwidth (Small Signal) 250MHz**
- **Wide Power Bandwidth .....DC to 65MHz**
- **Fast Rise Time 3ns**
- **High Output Drive ..... ±8V With 100Ω Load**
- **Wide Power Supply Range ..... ±5V to ±16V**
- **Replace Costly Hybrids**

Applications

- Video Buffer
- High Frequency Buffer
- Isolation Buffer
- High Speed Line Driver
- Impedance Matching
- Current Boosters
- High Speed A/D Input Buffers
- For Further Application Ideas, See App. Note 548

Description

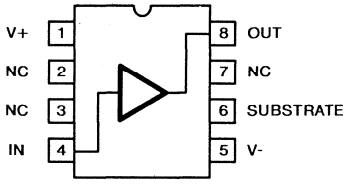
The HA-5033 is a unity gain monolithic I.C. designed for any application requiring a fast, wideband buffer. Featuring a bandwidth of 250MHz and outsanding differential phase/gain characteristics, this high performance voltage follower is an excellent choice for video circuit design. Other features, which include a minimum slew rate of 1000V/μs and high output drive capability, make the HA-5033 applicable for line driver and high speed data conversion circuits.

The high performance of this product is a result of the Harris Dielectric Isolation process. A major feature of this process is that it produces both PNP and NPN high frequency transistors which makes wide bandwidth designs, such as the HA-5033, practical. Alternative process methods typically produce a lower AC performance.

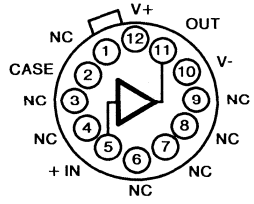
The HA-5033 is available in a 12 pin (TO-8) Metal Can or an 8 pin Plastic Mini-DIP.

Pinouts

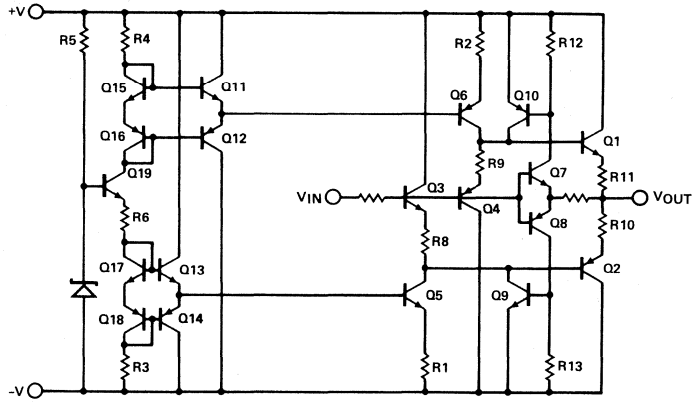
HA3-5033 (PLASTIC MINI-DIP)
TOP VIEW



HA2-5033 (TO-8 METAL CAN)
TOP VIEW



Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Pins 40V
Input Voltage ..... Equal to Supplies
Output Current (Peak) (50ms On/1 Second Off) ..... ±200mA
Internal Power Dissipation (Note 2)
TO-8 (+25°C) 1.75W
Mini-DIP (+25°C) 1.95W
Maximum Junction Temperature ..... +175°C

Operating Temperature Ranges

HA-5033-2 ..... $-55°C \leq T_A \leq +125°C$
HA-5033-5 ..... $0°C \leq T_A \leq +75°C$
Storage Temperature Range ..... $-65°C \leq T_A \leq +150°C$

Electrical Specifications

$V_{SUPPLY} = \pm 12V$, $R_S = 50\Omega$, $R_L = 100\Omega$, $C_L = 10pF$, Unless Otherwise Specified.

PARAMETER	TEMP	HA-5033-2 -55°C to +125°C			HA-5033-5 0°C to +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Offset Voltage	+25°C	-	5	15	-	5	15	mV
	Full	-	6	25	-	6	25	mV
Average Offset Voltage Drift	Full	-	33	-	-	33	-	µV/°C
Bias Current	+25°C	-	20	35	-	20	35	µA
	Full	-	30	50	-	30	50	µA
Input Resistance	+25°C	-	1.5	-	-	1.5	-	MΩ
Input Capacitance	+25°C	-	1.6	-	-	1.6	-	pF
Input Noise Voltage (Note 3)	+25°C	-	20	-	-	20	-	µVp-p
TRANSFER CHARACTERISTICS								
Voltage Gain								
$R_L = 100\Omega$	+25°C	0.93	-	-	0.93	-	-	V/V
$R_L = 1k\Omega$	+25°C	0.93	0.99	-	0.93	0.99	-	V/V
$R_L = 100\Omega$	Full	0.92	-	-	0.92	-	-	V/V
-3dB Bandwidth	+25°C	-	250	-	-	250	-	MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing								
$R_L = 100\Omega$	Full	+8	±10	-	±8	±10	-	V
$R_L = 1k\Omega$ (Note 4)	Full	±11	±12	-	±11	±12	-	V
Output Current	+25°C	±80	±100	-	±80	±100	-	mA
Output Resistance	+25°C	-	5	-	-	5	-	Ω
Full Power Bandwidth								
(Note 5)	+25°C	-	65	-	-	65	-	MHz
(Note 7)	+25°C	15.9	-	-	15.9	-	-	MHz
TRANSIENT RESPONSE								
Rise Time (Note 6)	+25°C	-	3	-	-	3	-	ns
Propagation Delay	+25°C	-	1	-	-	1	-	ns
Overshoot	+25°C	-	10	-	-	10	-	%
Slew Rate (Note 7)	+25°C	1	1.3	-	1	1.3	-	V/ns
Settling Time to 0.1%	+25°C	-	50	-	-	50	-	ns
Differential Phase Error (Note 8)	+25°C	-	0.1	-	-	0.1	-	Degree
Differential Gain Error (Note 8)	+25°C	-	0.1	-	-	0.1	-	%
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C	-	21	25	-	21	25	mA
	Full	-	21	30	-	21	30	mA
Power Supply Rejection Ratio	Full	54	-	-	54	-	-	dB
Harmonic Distortion (Note 9)	+25°C	-	<0.1	-	-	<0.1	-	%

NOTES:

1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. TO-8: θ_{ja} =101°C/W, θ_{jc} = 33°C/W Recommended heat sinks for the TO-8: Thermalloy 2240A, θ_{sa} = 27°C/W, IERC Up-TO-8-48CB, θ_{sa} = 10°C/W. Mini-DIP: θ_{ja} = 91°C/W, θ_{sa} = 40°C/W.
3. 10Hz to 1MHz
4. $\pm V_{SUPPLY} = \pm 15V$
5. $V_{OUT} = 1V_{RMS}$, $R_L = 1k\Omega$
6. $V_{OUT} = 500mV$
7. $\pm V_{SUPPLY} = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L = 1k\Omega$.
8. Differential gain and phase error are non-linear signal distortions found in video systems and are defined as follows: Differential gain error is defined as the change in amplitude at the color subcarrier frequency as the picture signal is varied from blanking to white level. Differential phase error is defined as the change in the phase of the color subcarrier as the picture signal is varied from blanking to white level. Differential gain and phase error were too small to be measured with a Tektronix 520A NTSC Vector Scope.
9. $V_{IN} = 1V_{RMS}$

Operating Instructions

Layout Considerations

The wide bandwidth of the HA-5033 necessitates that high frequency circuit layout procedures be followed. Failure to follow these guidelines can result in marginal performance.

Probably the most crucial of the RF/video layout rules is the use of a ground plane. A ground plane provides isolation and minimizes distributed circuit capacitance and inductance which will degrade high frequency performance. This ground plane shielding can also incorporate the metal case of the HA-5033 since pin #2 is internally tied to the package. This feature allows the user to make metal to metal contact between the ground plane and the package, which extends shielding, provides additional heat sinking and eliminates the use of a socket, IC sockets contribute inter-lead capacitance which limits device bandwidth and should be avoided.

For the epoxy Mini-DIP, pin 6 can be tied to either supply, grounded, or simply not used. But to optimize device performance and improve isolation, it is recommended that this pin be grounded.

Other considerations are proper power supply bypassing and keeping the input and output connections as short as possible which minimizes distributed capacitance and reduces board space.

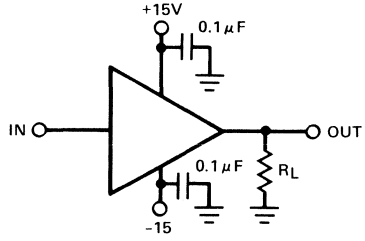
Power Supply Decoupling

For optimum device performance, it is recommended that the positive and negative power supplies be bypassed with capacitors to ground. Ceramic capacitors ranging in value from 0.01 to 0.1μF will minimize high frequency variations in supply voltage. Solid tantalum capacitors 1μF or larger will optimize low frequency performance.

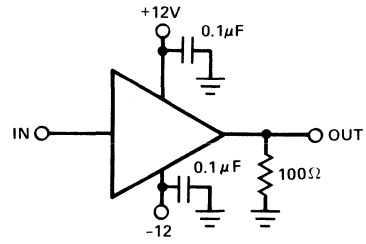
It is also recommended that the bypass capacitors be connected close to the HA-5033 (preferably directly to the supply pins).

Test Circuits

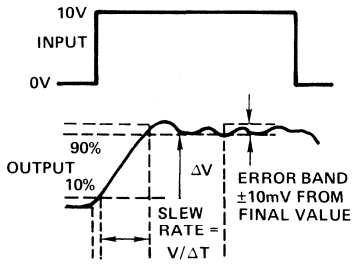
SLEW RATE AND SETTLING TIME



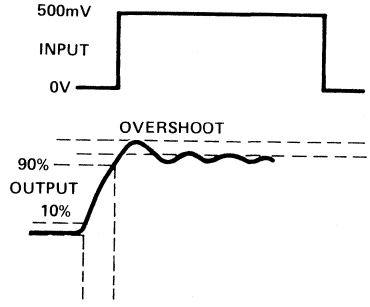
TRANSIENT RESPONSE



SETTLING TIME



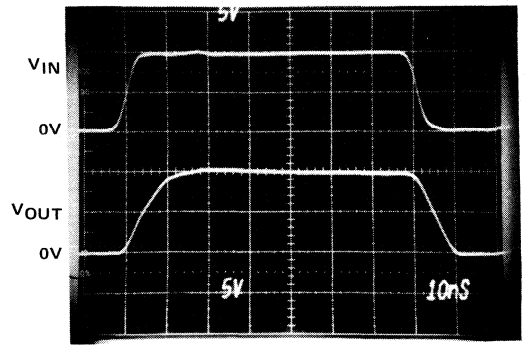
RISE TIME



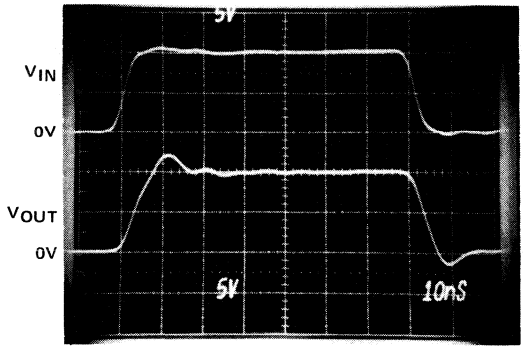
NOTE: Measured on both positive and negative transitions.

Test Circuits (Continued)

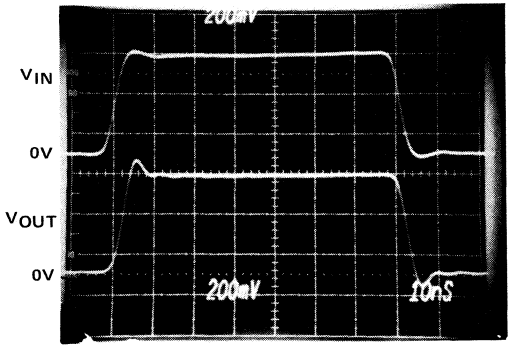
+10V RESPONSE
$T_A = +25^oC$, $R_S = 50\Omega$, $R_L = 100\Omega$



+10V RESPONSE
$T_A = +25^oC$, $R_S = 50\Omega$, $R_L = 1k\Omega$

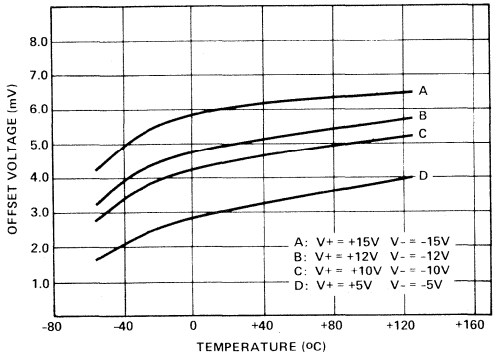


+0.5V PULSE RESPONSE
$T_A = +25^oC$, $R_S = 50\Omega$, $R_L = 100\Omega$

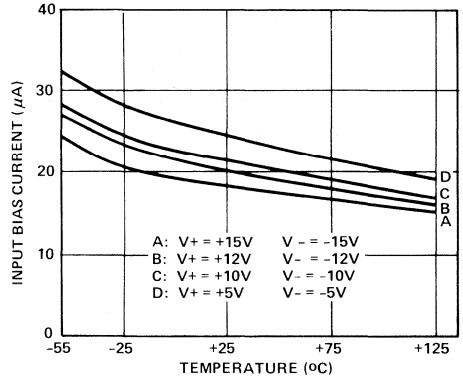


Typical Performance Curves

INPUT OFFSET VOLTAGE vs. TEMPERATURE vs. SUPPLY VOLTAGE

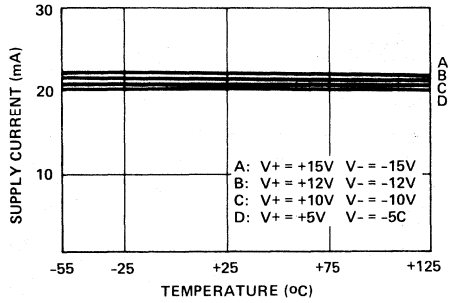


INPUT BIAS CURRENT vs. TEMPERATURE vs. SUPPLY VOLTAGE

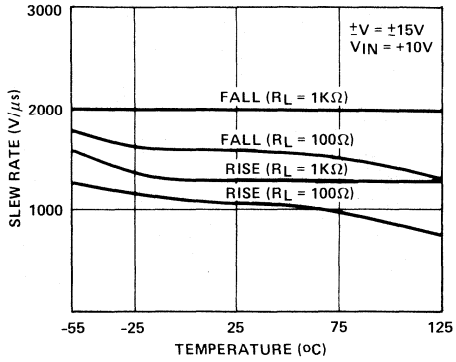


Typical Performance Curves (Continued)

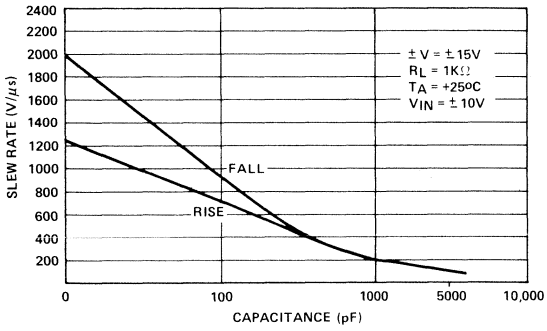
SUPPLY CURRENT vs. TEMPERATURE vs. SUPPLY VOLTAGE



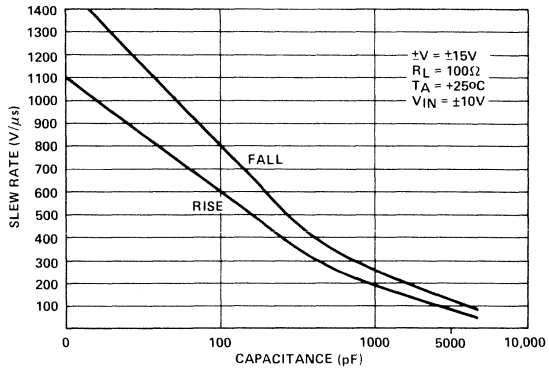
SLEW RATE vs. TEMPERATURE



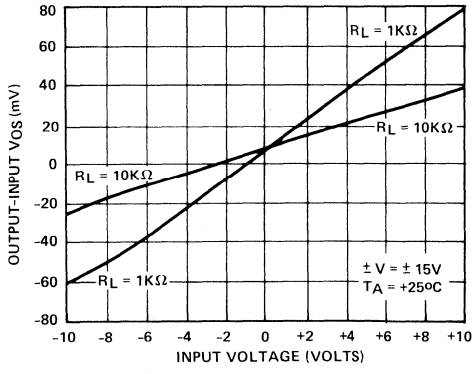
SLEW RATE vs. LOAD CAPACITANCE (R_L = 1kΩ)



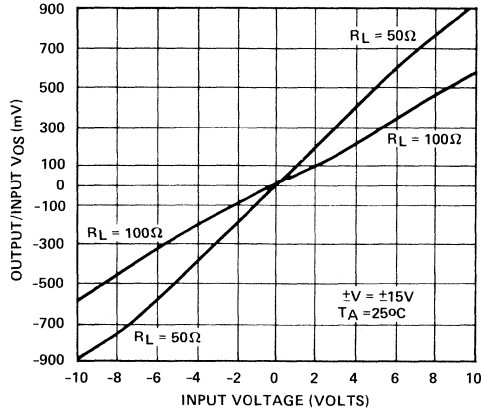
SLEW RATE vs. LOAD CAPACITANCE (R_L = 100Ω)



GAIN ERROR vs. INPUT VOLTAGE

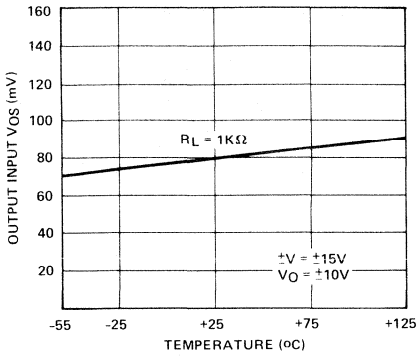


GAIN ERROR vs. INPUT VOLTAGE

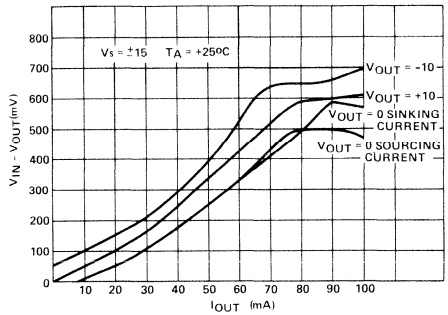


Typical Performance Curves (Continued)

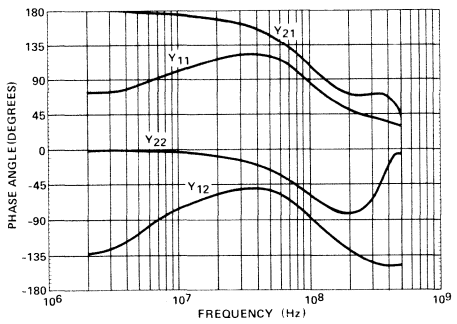
GAIN ERROR vs. TEMPERATURE



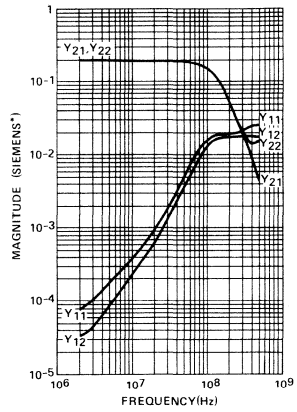
$V_{IN} - V_{OUT}$ vs. I_{OUT}



Y - PARAMETERS PHASE vs. FREQUENCY

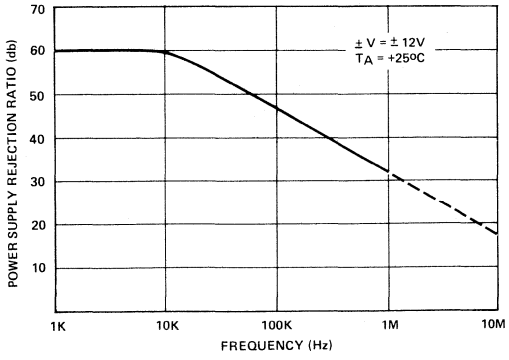


Y - PARAMETER MAGNITUDE vs. FREQUENCY

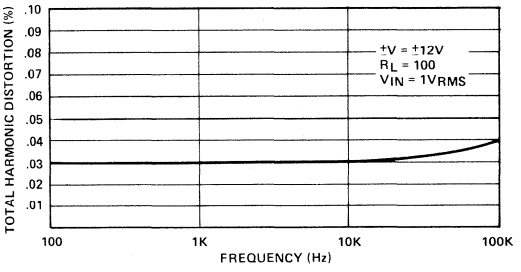


* Siemens = Ω -1

POWER SUPPLY REJECTION RATIO vs. FREQUENCY

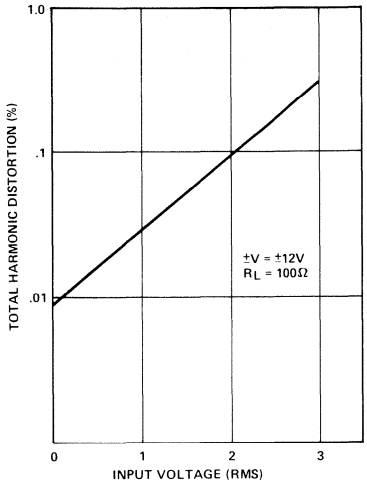


TOTAL HARMONIC DISTORTION vs. FREQUENCY

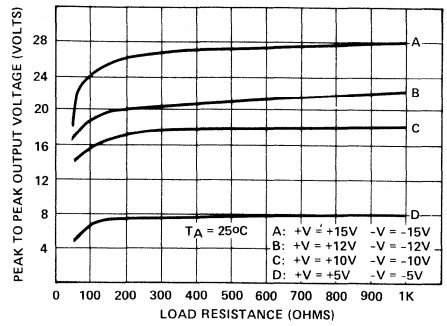


Typical Performance Curves (Continued)

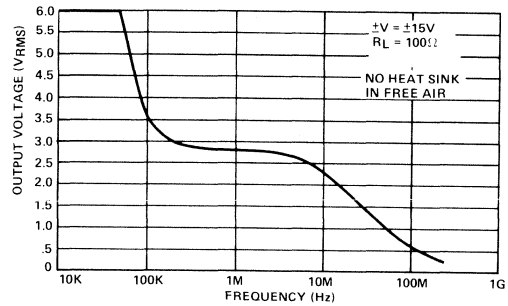
TOTAL HARMONIC DISTORTION vs. RMS INPUT VOLTAGE



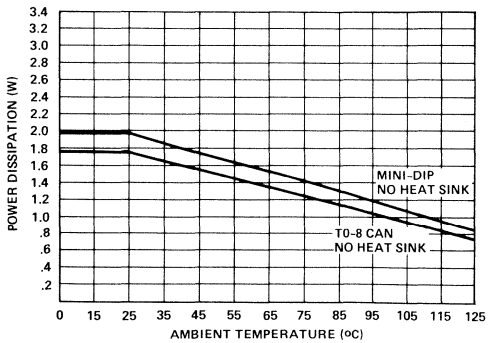
OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE vs. SUPPLY VOLTAGE



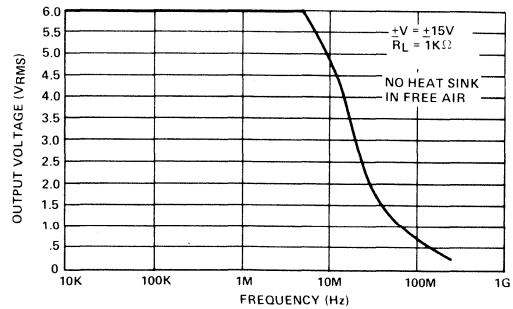
OUTPUT SWING vs. FREQUENCY*



MAXIMUM POWER DISSIPATION vs. AMBIENT TEMPERATURE



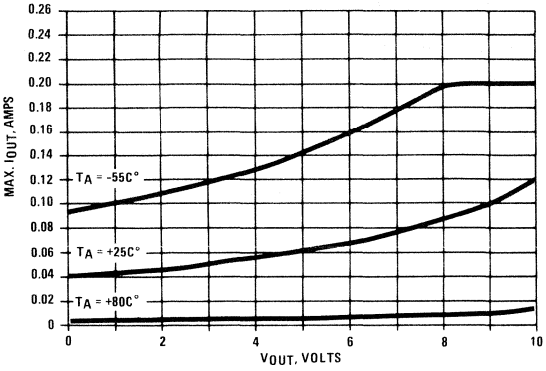
OUTPUT SWING vs. FREQUENCY*



Typical Performance Curves (Continued)

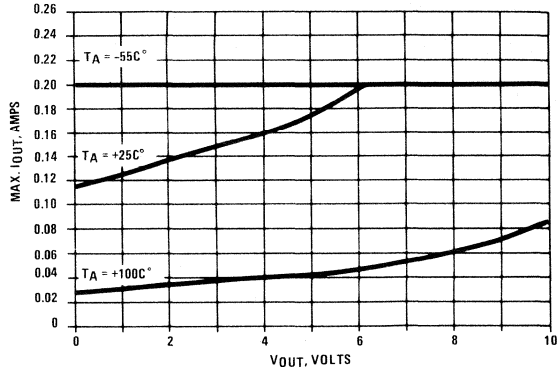
HA-5033 SOA, TO-8, NO SINK

T_J = +175, I_{CC} = 30mA, V_{CC} = ±15, θ_{ja} = 101°C/W



HA-5033, TO-8, AAVID 5792 θ_{sa} = 25°C/W

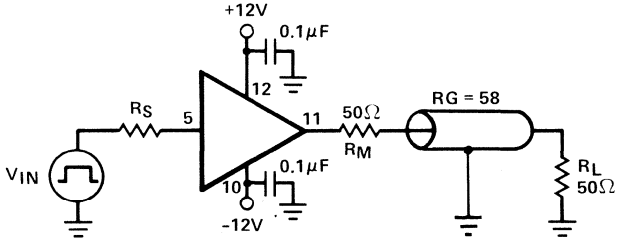
T_J = +175, I_{CC} = 30mA, V_{CC} = ±15, θ_{jc} = 33°C/W



* This curve was obtained by noting the output voltage necessary to produce an observable distortion for a given frequency. If higher distortion is acceptable, then a higher output voltage for a given frequency can be obtained.
However, operating the HA-5033 with increased distortion (to the right of curve shown), will also be accompanied by an increase in supply current. The resulting increase in chip temperature must be considered and heat sinking will be necessary to prevent thermal runaway.
This characteristic is the result of the output transistor operation. If the signal amplitude or signal frequency or both are increased beyond the curve shown, the NPN, PNP output transistors will approach a condition of being simultaneously on. Under this condition, thermal runaway can occur.

Typical Applications (Also See Application Note 548)

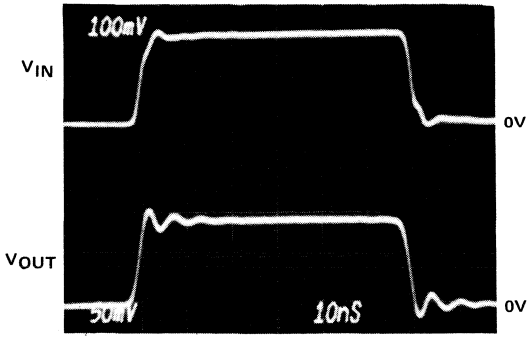
VIDEO COAXIAL LINE DRIVER - 50V SYSTEM



POSITIVE PULSE RESPONSE

T_A = +25°C, R_S = 50Ω, R_M = RL = 50Ω

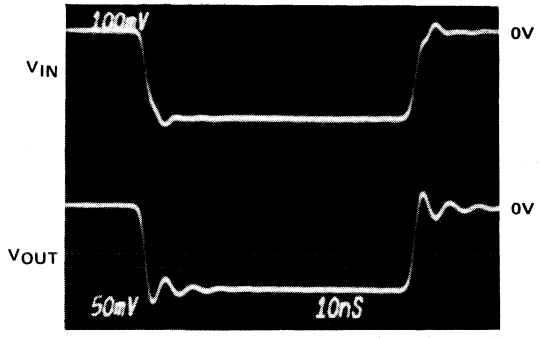
$V_O = V_{IN} \left(\frac{R_L}{R_L + R_M} \right) = ½ V_{IN}$



NEGATIVE PULSE RESPONSE

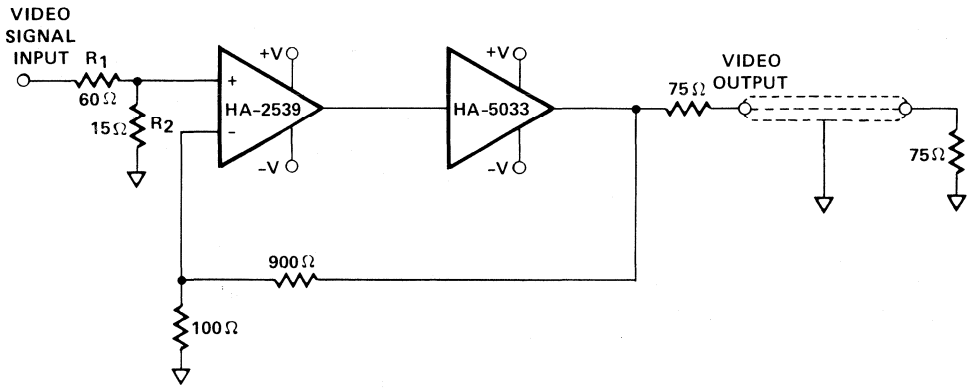
T_A = +25°C, R_S = 50Ω, R_M = RL = 50Ω

$V_O = -V_{IN} \left(\frac{R_L}{R_L + R_M} \right) = ½ V_{IN}$



Typical Applications (Continued)

VIDEO GAIN BLOCK



Die Characteristics

Transistor Count 20
Die Dimensions ..... 50 x 66 x 19mils
(1270 x 1660 x 480μm)
Substrate Potential* ..... V-
Process ..... High Frequency Bipolar-DI
Passivation ..... Nitride

*The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.

HARRIS HA-5101/5111

Low Noise, High Performance Operational Amplifiers

Features

- Low Noise ..... 3.3nV/$\sqrt{Hz}$ at 1kHz
- Wide Bandwidth ..... 10MHz (Compensated)
  100MHz (Uncompensated)
- High Slew Rate ..... 10V/μs (Compensated)
  50V/μs (Uncompensated)
- Low Offset Voltage Drift ..... 3μV/°C
- High Gain ..... 1 x 10^6V/V
- High CMRR/PSRR 100dB
- High Output Drive Capability 30mA

Applications

- High Quality Audio Preamplifiers
- High Q Active Filters
- Low Noise Function Generators
- Low Distortion Oscillators
- Low Noise Comparators
- For Further Design Ideas, See App. Note 554

Description

The HA-5101/5111 are dielectrically isolated operational amplifiers featuring low noise and high performance. Both amplifiers have an excellent noise voltage density of 3.5nV/$\sqrt{Hz}$ at 1kHz. The uncompensated HA-5111 is stable at a minimum gain of 10 and has the same DC specifications as the unity gain stable HA-5101. The difference in compensation yields a 100MHz gain-bandwidth product and a 50V/μs slew rate for the HA-5111 versus a 10MHz unity gain bandwidth and a 10V/μs slew rate for the HA-5101.

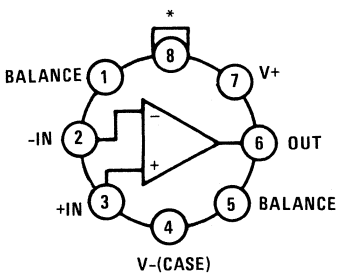
DC characteristics of the HA-5101/5111 assure accurate performance. The 1mV offset voltage is externally adjustable and offset voltage drift is just 3μV/°C. An offset current of only 30nA reduces input current errors and an open loop voltage gain of 1 x 10^6V/V increases loop gain for low distortion amplification.

The HA-5101/5111 are ideal for audio applications, especially low-level signal amplifiers such as microphone, tape head and phono cartridge preamplifiers. Additionally, it is well suited for low distortion oscillators, low noise function generators and high Q filters.

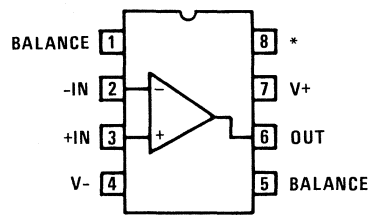
The HA-5101/5111-2 has guaranteed operation from -55°C to +125°C and can be ordered as a military grade part. The HA-5101/5111-5 has guaranteed operation from 0°C to +75°C. All devices are available in Ceramic Mini-DIP and TO-99 Can packages. Additionally, the HA-5101/5111-5 is available in a Plastic Mini-DIP package.

Pinouts

HA2-5101/5111 (TO-99 METAL CAN)
TOP VIEW



HA3-5101/5111 (PLASTIC MINI-DIP)
HA7-5101/5111 (CERAMIC MINI-DIP)
TOP VIEW



*HA-5101 No Connect
HA-5111 Compensation

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

T_A = +25°C Unless Otherwise Stated
Voltage Between V+ and V- Terminals 40.0V
Differential Input Voltage ..... ±7V
Voltage (at any pin) ..... $\pm V_{SUPPLY}$
Output Current ..... Full Short Circuit Protection
Junction Temperature ..... +175°C

Operating Temperature

HA-5101/5111-2 ..... -55°C to +125°C
HA-5101/5111-5 ..... 0°C to +75°C
Storage Temperature ..... -65°C to +150°C
Internal Power Dissipation 560mW

(Derate at 5.3mW/°C Above 70°C Ambient)

Electrical Specifications

V+ = +15V, V- = -15V, R_S = 100Ω, R_L = 2kΩ, C_L = 50pF, Unless Otherwise Specified.

PARAMETER	TEMP	HA-5101-2 HA-5111-2 -55°C to +125°C			HA-5101-5 HA-5111-5 0°C to +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Offset Voltage	+25°C	-	0.5	3	-	0.5	3	mV
	Full	-	-	4	-	-	4	mV
Offset Voltage Drift	Full	-	3	-	-	3	-	µV/°C
Bias Current	+25°C	-	100	200	-	100	200	nA
	Full	-	-	325	-	-	325	nA
Offset Current	+25°C	-	30	75	-	30	75	nA
	Full	-	-	125	-	-	125	nA
Input Resistance	+25°C	-	500	-	-	500	-	kΩ
Common Mode Range	Full	±12	-	-	±12	-	-	V/V
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 2)	+25°C	-	1000K	-	-	1000K	-	V/V
	Full	100K	250K	-	100K	250K	-	V/V
Common Mode Rejection Ratio (Note 3)	Full	80	100	-	80	100	-	dB
Small Signal Bandwidth								
HA-5101 (A_V = 1)	+25°C	-	10	-	-	10	-	MHz
Minimum Stable Gain								
HA-5101	Full	1	-	-	1	-	-	V/V
HA-5111	Full	10	-	-	10	-	-	V/V
Gain Bandwidth Product HA-5111 (A_V = 10)	+25°C	-	100	-	-	100	-	MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing								
R_L = 10K	Full	±12	±13	-	±12	±13	-	V
R_L = 2K	Full	±12	±13	-	±12	±13	-	V
(V_{PS} = ±18, R_L = 600)	+25°C	±15	-	-	±15	-	-	V
Output Current (Note 4)	+25°C	25	30	-	25	30	-	mA
Full Power Bandwidth (Note 5)								
HA-5101	+25°C	95	160	-	95	160	-	kHz
HA-5111	+25°C	630	790	-	630	790	-	kHz
Output Resistance	+25°C	-	110	-	-	110	-	Ω
Maximum Load Capacitance	+25°C	-	800	-	-	800	-	pF

Electrical Specifications (Continued)

$V+ = 15V$, $V- = -15V$, $R_S = 100$, $R_L = 2K$, $C_L = 50pF$ Unless Otherwise Specified.

PARAMETER	TEMP	HA-5101-2 HA-5111-2 -55°C to +125°C			HA-5101-5 HA-5111-5 0°C to +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TRANSIENT RESPONSE (Note 6)								
Rise Time								
HA-5101	+25°C	-	50	100	-	50	100	ns
HA-5111	+25°C	-	30	60	-	30	60	ns
Overshoot								
HA-5101	+25°C	-	20	35	-	20	35	%
HA-5111	+25°C	-	20	40	-	20	40	%
Slew Rate								
HA-5101	+25°C	6	10	-	6	10	-	V/µs
HA-5111	+25°C	40	50	-	40	50	-	V/µs
Settling Time (Note 7)								
HA-5101 0.01%	-	-	2.6	-	-	2.6	-	µs
HA-5111 0.01%	-	-	0.5	-	-	0.5	-	µs
NOISE CHARACTERISTICS (Note 8)								
Input Noise Voltage								
f = 10Hz	+25°C	-	7	17	-	7	17	$nV/\sqrt{Hz}$
f = 1kHz	+25°C	-	3.3	4.5	-	3.3	4.5	$nV/\sqrt{Hz}$
Input Noise Current								
f = 10Hz	+25°C	-	5.1	28	-	5.1	28	$pA/\sqrt{Hz}$
f = 1kHz	+25°C	-	1.1	3	-	1.1	3	$pA/\sqrt{Hz}$
Broadband Noise Voltage f = DC to 30kHz	+25°C	-	0.870	-	-	0.870	-	µVrms
POWER SUPPLY CHARACTERISTICS								
Supply Current HA-5101/5111	Full	-	4	6	-	4	6	mA
Power Supply Rejection Ratio (Note 9)	Full	80	100	-	80	100	-	dB

NOTES:

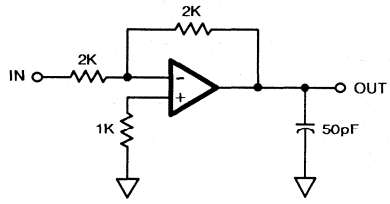
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. $V_{OUT} = \pm 10V$, $R_L = 2K$.
3. $V_{CM} = \pm 10V$.
4. Output current is measured with $V_{OUT} = \pm 15V$ with $V_{SUPPLY} = \pm 18V$.
5. Full power bandwidth is guaranteed by equation:

   $$\text{Full power bandwidth} = \frac{\text{Slew Rate}}{2\pi V_{Peak}}, \quad V_{peak} = 10V.$$

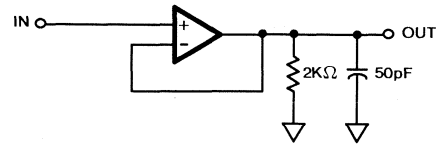
6. Refer to Test Circuits section of the data sheet.
7. Settling time is measured to 0.01% of final value for a 10V output step, and $A_V = -10$ for HA-5111 and 0.01% of final value for a 10V output step, $A_V = -1$ for HA-5101.
8. Sample Tested.
9. Delta $V_{SUPPLY} = \pm 5V$.

Test Circuits

HA-5101 LARGE SIGNAL RESPONSE CIRCUIT

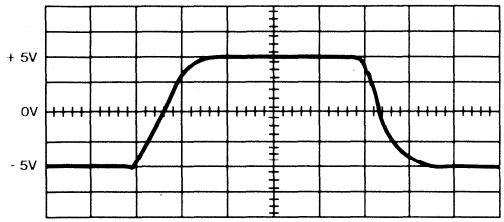


HA-5101 SMALL SIGNAL RESPONSE CIRCUIT



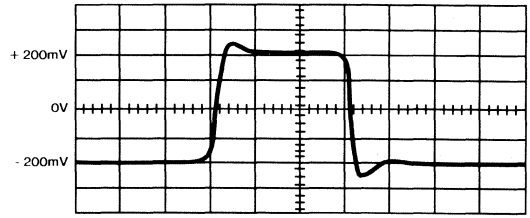
HA-5111 LARGE SIGNAL TRANSIENT RESPONSE

Ch. 1 = 2.5V/Div.
Timebase = 200ns/Div.



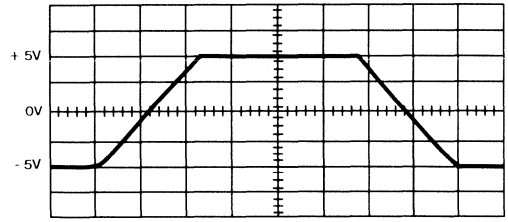
HA-5111 SMALL SIGNAL TRANSIENT RESPONSE

Ch. 1 = 100mV/Div.
Timebase = 100ns/Div.



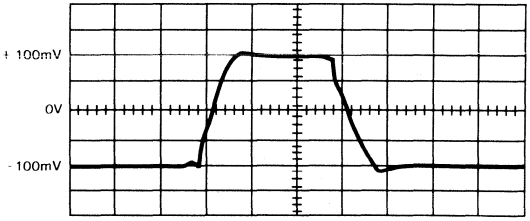
HA-5101 LARGE SIGNAL TRANSIENT RESPONSE

Ch. 1 = 2.5V/Div.
Timebase = 1.00µs/Div.

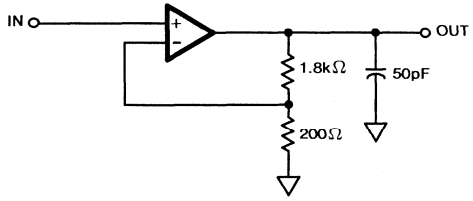


HA-5101 SMALL SIGNAL TRANSIENT RESPONSE

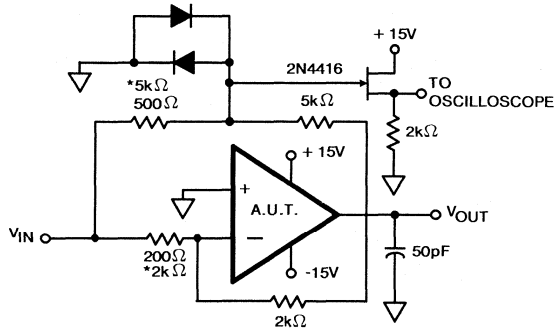
Ch. 1 = 50mV/Div.
Timebase = 100ns/Div.



HA-5111 LARGE AND SMALL RESPONSE CIRCUIT



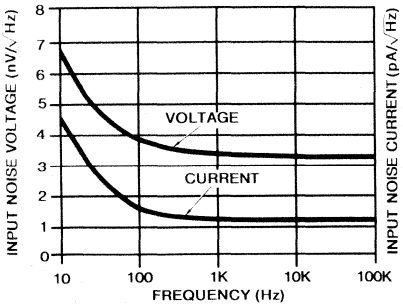
SETTLING TIME CIRCUIT



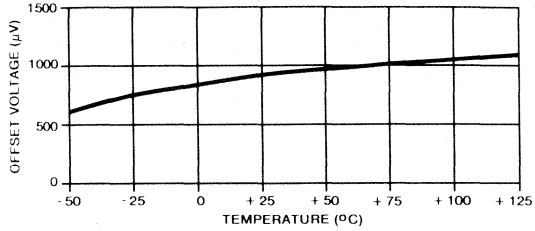
- A_V = -1 (HA-5101), *A_V = -10 (HA-5101)
- Feedback and summing resistors should be 0.1% matched.
- Clipping diodes are optional, HP5082-2810 recommended.

Typical Characteristics

HA-5101/11 NOISE SPECTRUM

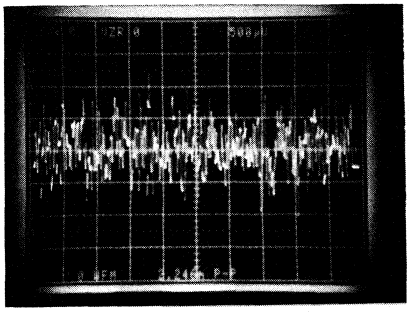


OFFSET VOLTAGE vs. TEMPERATURE



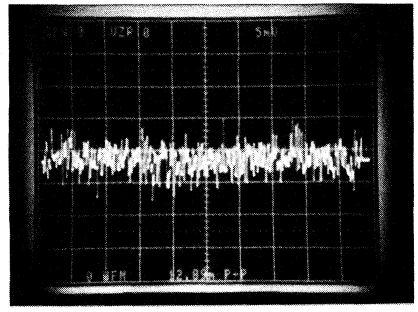
PEAK-TO-PEAK NOISE 0.1Hz to 10Hz

A_V = 25000 V_{CC} = ±15V
(2.25μVp-p RTI)

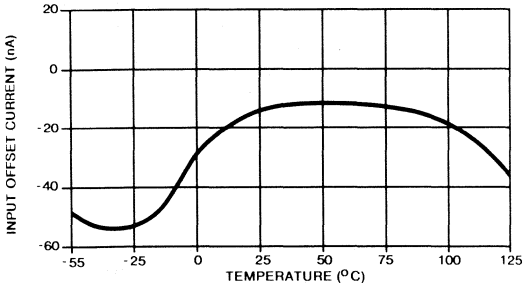


PEAK-TO-PEAK TOTAL NOISE 0.1Hz to 1MHz

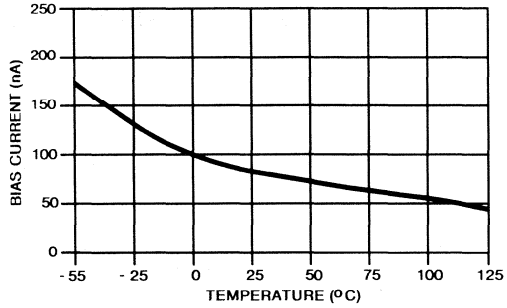
A_V = 25000, V_{CC} = ±15V
(12.89mVp-p RTO)



INPUT OFFSET CURRENT vs. TEMPERATURE

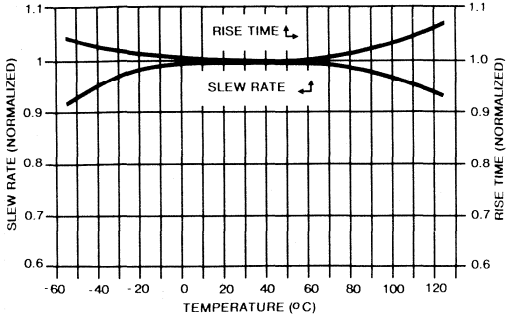


INPUT BIAS CURRENT vs. TEMPERATURE

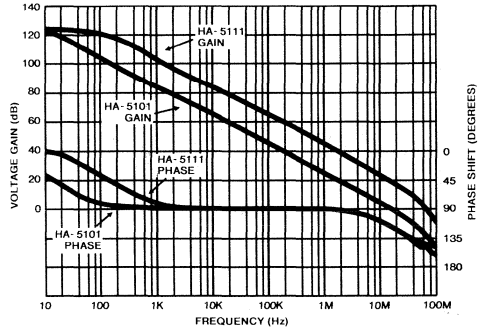


SLEW RATE/RISE TIME vs. TEMPERATURE

R_L = 2K, C_L = 50pF, V_{CC} = ±15V

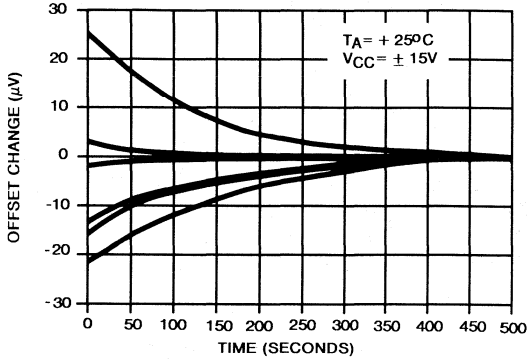


OPEN-LOOP GAIN/PHASE VS. FREQUENCY

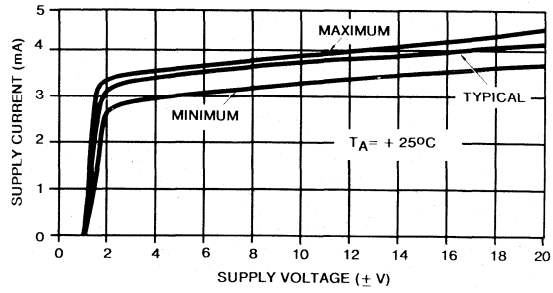


Typical Characteristics (Continued)

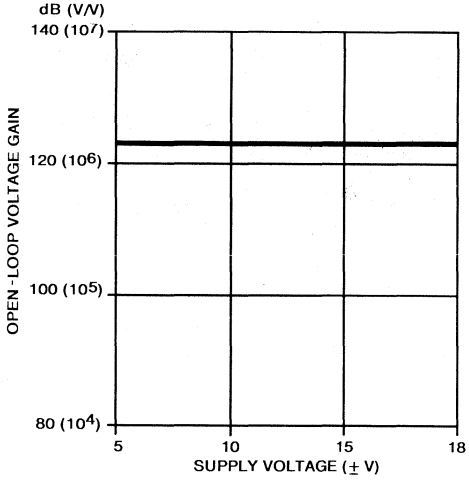
INPUT OFFSET WARMUP DRIFT vs. TIME
(Normalized To Zero Final Value)
(Six Representative Units)



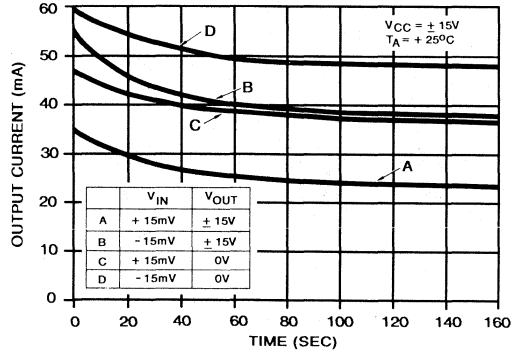
SUPPLY CURRENT vs. SUPPLY VOLTAGE



DC OPEN-LOOP VOLTAGE GAIN vs. SUPPLY VOLTAGE

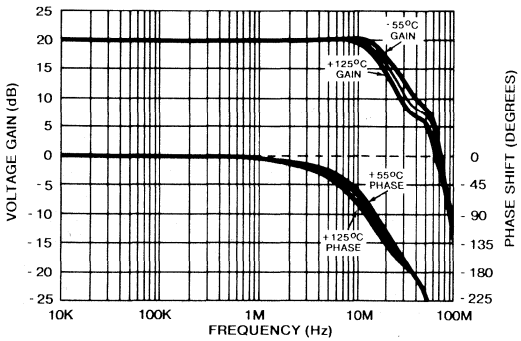


SHORT CIRCUIT CURRENT vs. TIME

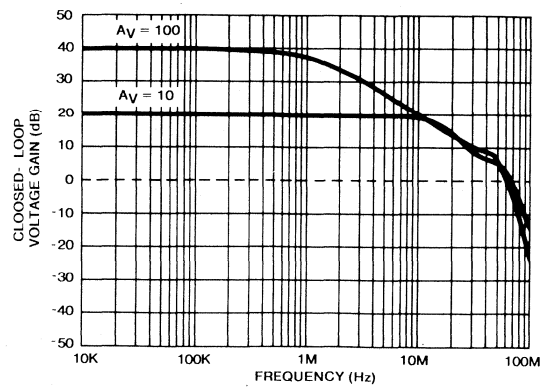


	V_{IN}	V_{OUT}
A	+ 15mV	± 15V
B	- 15mV	± 15V
C	+ 15mV	0V
D	- 15mV	0V

HA-5111 CLOSED-LOOP GAIN AND PHASE AT HIGH AND LOW TEMPERATURE
(Typical Response Of One Amplifier)
V_{CC} = ±15V, A_V = 10V/V, R_L = 2K, C_L = 50pF



HA-5111 CLOSED-LOOP VOLTAGE GAIN FREQUENCY AT DIFFERENT CLOSED-LOOP GAINS
T_A = +25°C, V_{CC} = ±15V, A_V = 100,
10V/V, R_L = 2K, C_L = 50pF

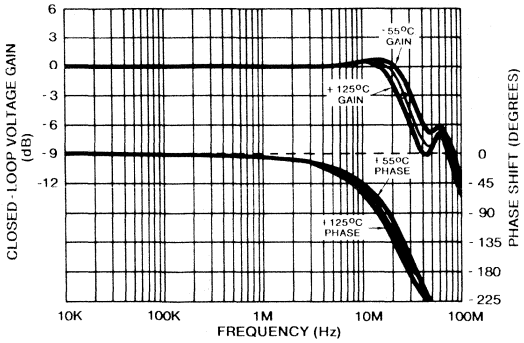


Typical Characteristics (Continued)

HA-5101 CLOSED-LOOP GAIN AND PHASE AT HIGH AND LOW TEMPERATURE

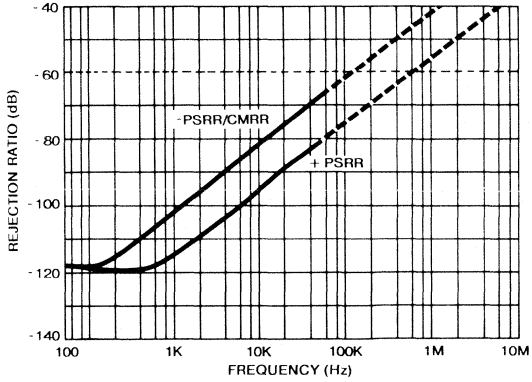
(Typical Response Of One Amplifier)

V_{CC} = ±15V, AV = 1V/V, R_L = 2K, C_L = 50pF



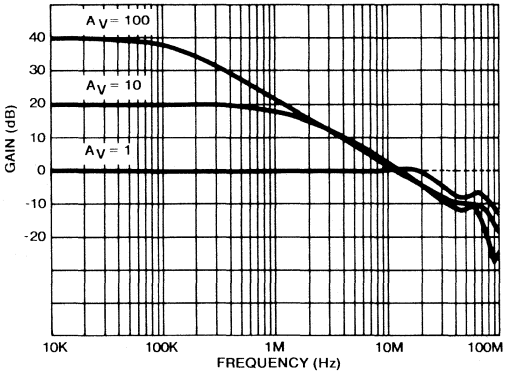
HA-5111 REJECTION RATIOS vs. FREQUENCY

T_A = +25°C, V_{CC} = ± 15V



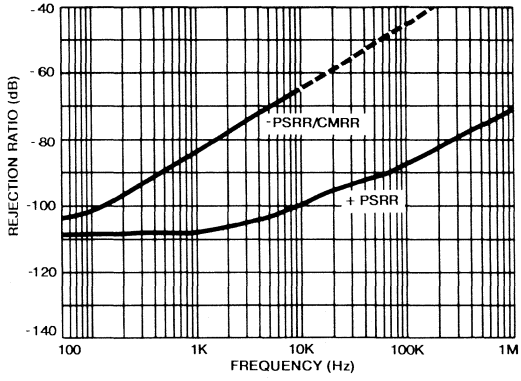
HA-5101 CLOSED-LOOP VOLTAGE GAIN vs. FREQUENCY AT DIFFERENT CLOSED-LOOP GAINS

T_A = +25°C, V_{CC} = ±15V, R_L = 2K, C_L = 50pF

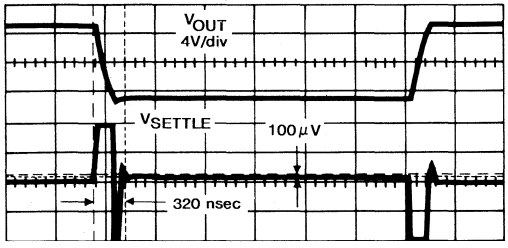


HA-5101 REJECTION RATIOS vs. FREQUENCY

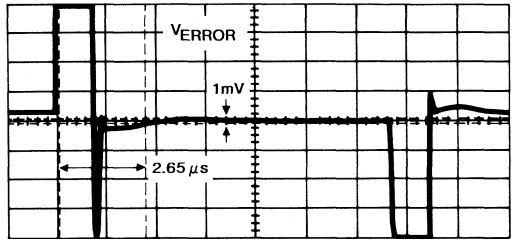
T_A = +25°C, V_{CC} = ±15V



HA-5111 SETTLING WAVEFORM 500nsec/DIV.



HA-5101 SETTLING WAVEFORM 1.5μsec./DIV.



Applications Information

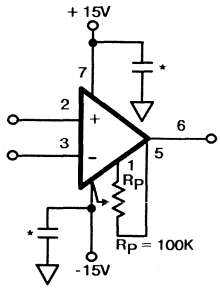
OPERATION AT ±5V SUPPLY

The HA-5101/11 performs well at V_{CC} = ±5V exhibiting typical characteristics as listed below:

I_{CC}	3.7	mA
V_{IO}	0.5	mA
I_{BIAS}	56	nA
A_{VOL} (V_O = ±3V)	106	KV/V
V_{OUT}	3.7	V
I_{OUT}	13	mA
CMRR (ΔV_{CM} = ±2.5V)	90	dB
PSRR (ΔV_{CC} = 0.5V)	90	dB
Unity Bandwidth (5101)	10	MHz
GBW (5111)	100	MHz
Slew Rate (5101)	7	V/µs
Slew Rate (5111)	40	V/µs

OFFSET ADJUSTMENT

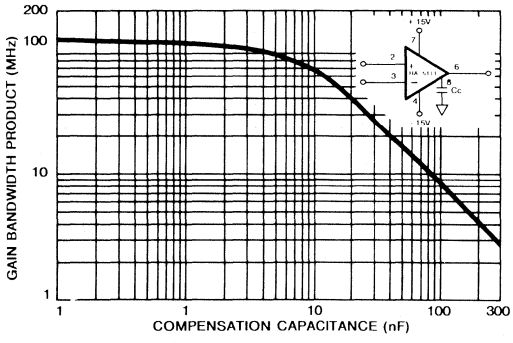
The following is the recommended V_{IO} adjust configuration:



* Proper decoupling is always recommended, 0.1µF high quality capacitor should be at or very near the devices's supply pins.

COMPENSATION

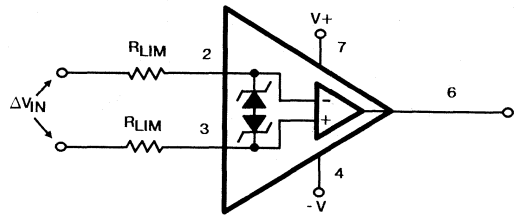
An external compensation capacitor can be used with the HA-5111 connected between pin 8 and ground (or V-, V+ not Recommended). A plot of gain bandwidth product vs. compensation capacitor has been included as a design aid. The capacitor should be a high frequency type mounted near the device leads to minimize parasitics.



INPUT PROTECTION

The HA-5101/11 has built-in back-to-back protection diodes which will limit the differential input voltage to approximately 7V. If the 5101/11 will be used in conditions where that voltage may be exceeded, then current limiting resistors must be used. No more than 25mA should be allowed to flow in the HA-5101/11's input.

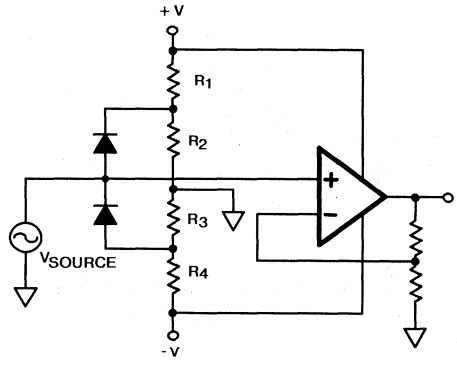
COMPARATOR CIRCUIT



Choose RLIM Such That: $\frac{(\Delta V_{IN}MAX - 7V)}{25mA} \leq 2RLIM$

OUTPUT SATURATION

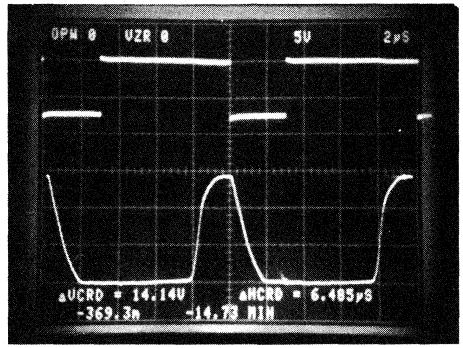
When an op amp is overdriven, output devices can saturate and sometimes take a long time to recover. Saturation can be avoided (sometimes) by using circuits such as:



If saturation cannot be avoided the HA-5101/11 recovers from a 25% overdrive in about 6.5µs (see photos).

Applications Information (Continued)

TOP: Input
BOTTOM: Output, 5V/Div., 2μs/Div.



Output is overdriven negative and recovers in 6μs.

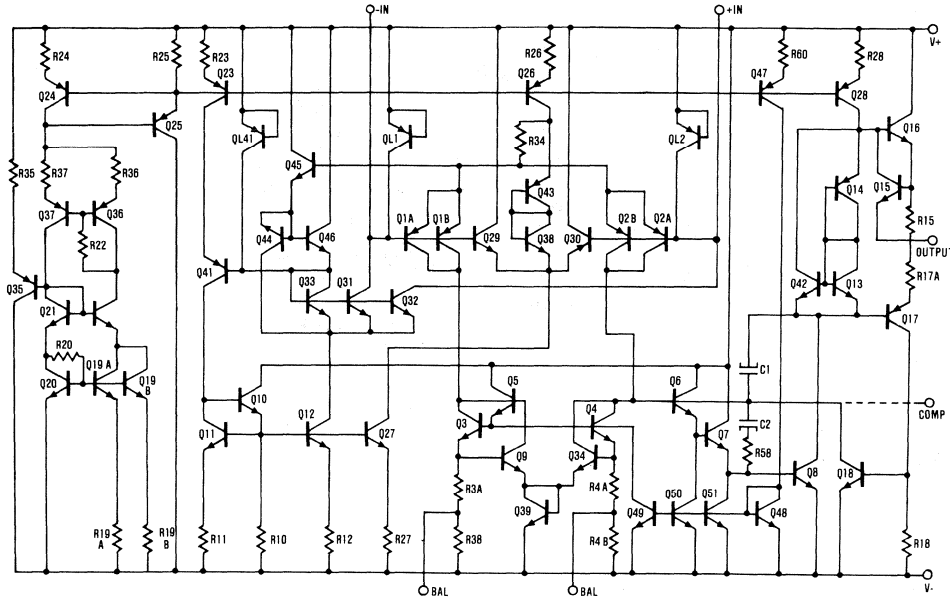
Die Characteristics

Transistor Count 54
Die Dimensions ..... 69 x 69 x 19 mils
(1800 x 1800 x 480μm)
Substrate Potential* ..... V- or Float
Process ..... Bipolar DI

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
HA2-5101/5111 (-2/-5/-7)	192	52
HA2-5101/5111 (/883)	158	48
HA3-5101/5111 (-5)	80	29
HA7-5101/5111 (-2/-5/-7)	190	102
HA7-5101/5111 (/883)	136	61

*The Substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.

Schematic


-IN
+IN
V+
V-
OUTPUT
COMP
BAL
BAL
R24
R25
R23
Q23
Q24
Q25
R26
Q26
R60
Q47
R28
Q28
Q16
QL41
QL1
QL2
R34
R35
R37
R36
Q37
Q36
R22
Q45
Q43
Q1A
Q1B
Q29
Q38
Q30
Q2B
Q2A
Q44
Q46
Q14
Q15
R15
Q41
Q33
Q31
Q32
Q42
Q13
R17A
Q35
Q21
Q17
R20
Q19 A
Q20
Q19 B
C1
Q5
Q6
Q10
Q12
Q3
Q4
Q7
C2
Q11
Q27
Q9
Q34
R58
Q8
Q18
R3A
R4 A
Q39
Q50
Q51
Q49
Q48
R19 A
R19 B
R11
R10
R12
R27
R38
R4 B
R18

HARRIS HA-5102/04/12/14

Low Noise High Performance Operational Amplifiers

Features

- Low Noise ..... 4.3nV$\sqrt{Hz}$
- Wide Bandwidth ..... 8MHz (Compensated)
  60MHz (Uncompensated)
- High Slew Rate ..... 3V/µs (Compensated)
  20V/µs (Uncompensated)
- Low Offset Voltage 0.5mV
- Available in Duals or Quads

Applications

- High Q, Active Filters
- Audio Amplifiers
- Instrumentation Amplifiers
- Integrators
- Signal Generators
- For Further Design Ideas, See App. Note 554.

Description

Low noise and high performance are key words describing HA-5102/04/12/14. These general purpose amplifiers offer an array of dynamic specifications ranging from a 3V/µs slew rate and 8MHz bandwidth (5102/04) to 20V/µs slew rate and 60MHz gain-bandwidth-product (HA-5112/14). Complementing these outstanding parameters is a very low noise specification of 4.3nV/$\sqrt{Hz}$ at 1kHz.

Fabricated using the Harris high frequency DI process, these operational amplifiers also offer excellent input specifications such as a 0.5mV offset voltage and 30nA offset current. Complementing these specifications are 108dB open loop gain and 108dB channel separation. Consuming a very modest amount of power (90mW/package for duals and 150mW/package for quads), HA-5102/04/12/14 also provide 15mA of output current.

This impressive combination of features make this series of amplifiers ideally suited for designs ranging from audio amplifiers and active filters to the most demanding signal conditioning and instrumentation circuits.

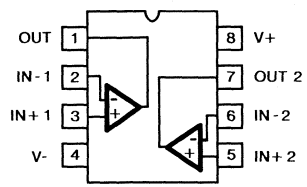
These operational amplifiers are available in dual or quad form with industry standard pinouts allowing for immediate inter-changeability with most other dual and quad operational amplifiers.

HA-5102	Dual, Compensated
HA-5112	Dual, Uncompensated
HA-5104	Quad, Compensated
HA-5114	Quad, Uncompensated

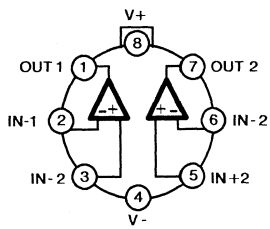
Each of these products are available in -2 (-55°C to +125°C), -5 and -7 (0°C to +75°C), or /883 grades. Refer to the /883 data sheet for military product.

Pinouts

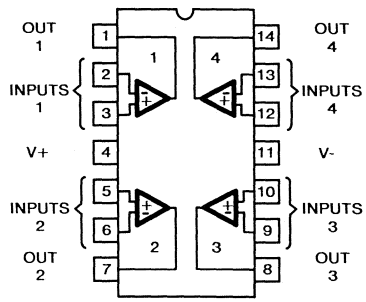
HA3-5102/5112 (PLASTIC MINI-DIP)
HA7-5102/5112 (CERAMIC MINI-DIP)
TOP VIEW



HA2-5102/5112 (TO-99 METAL CAN)
TOP VIEW



HA1-5104/5114 (CERAMIC DIP)
HA3-5104/5114 (PLASTIC DIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

T_A = +25°C Unless Otherwise Stated
Voltage Between V+ and V- Terminals 40.0V
Differential Input Voltage ..... ±7V
Input Voltage (Note 2) ..... ±15.0V
Output Short Circuit Duration (Note 3) ..... Indefinite
Power Dissipation (Note 4) 880mW

Operating Temperature Ranges

HA-5102/5104/5112/5114-2 ..... $-55°C \leq T_A \leq +125°C$
HA-5102/5104/5112/5114-5 ..... $-0°C \leq T_A \leq +75°C$
Storage Temperature Range ..... $-65°C \leq T_A \leq +150°C$

Electrical Specifications

V+ = 15V D.C., V- = -15V D.C., Unless Otherwise Specified

PARAMETER	TEMP	HA-5102-2 HA-5112-2 -55°C to +125°C			HA-5104-2 HA-5114-2 -55°C to +125°C			HA-5102-5 HA-5112-5 0°C to +75°C			HA-5104-5 HA-5114-5 0°C to 75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS														
Offset Voltage	+25°C	-	0.5	2.0	-	0.5	2.5	-	0.5	2.0	-	0.5	2.5	mV
	Full	-	-	2.5	-	-	3.0	-	-	2.5	-	-	3.0	mV
Offset Voltage Average Drift	Full	-	3	-	-	3	-	-	3	-	-	3	-	µV/°C
Bias Current	+25°C	-	130	200	-	130	200	-	130	200	-	130	200	nA
	Full	-	-	325	-	-	325	-	-	325	-	-	325	nA
Offset Current	+25°C	-	30	75	-	30	75	-	30	75	-	30	75	nA
	Full	-	-	125	-	-	125	-	-	125	-	-	125	nA
Input Resistance	+25°C	-	500	-	-	500	-	-	500	-	-	500	-	kΩ
Common Mode Range	Full	±12	-	-	±12	-	-	±12	-	-	±12	-	-	V
TRANSFER CHARACTERISTICS														
Large Signal Voltage Gain	+25°C	-	250	-	-	250	-	-	250	-	-	250	-	kV/V
(Note 5)	Full	100	-	-	100	-	-	100	-	-	100	-	-	kV/V
Common Mode Rejection Ratio (Note 6)	Full	86	95	-	86	95	-	86	95	-	86	95	-	dB
Small Signal Bandwidth														
HA-5102/5104 (A_V = 1)	+25°C	-	8	-	-	8	-	-	8	-	-	8	-	MHz
Gain Bandwidth Product														
HA-5112/5114 (A_V = 10)	+25°C	-	60	-	60		-	-	60		-	60	-	MHz
Channel Separation (Note 7)	+25°C	-	108	-	108		-	-	108	-	-	108	-	dB
OUTPUT CHARACTERISTICS														
Output Voltage Swing														
(R_L = 10K)	Full	±12	±13	-	±12	±13	-	±12	±13	-	±12	±13	-	V
(R_L = 2K)	Full	±10	±12	-	±10	±12	-	±10	±12	-	±10	±12	-	V
Output Current (Note 8)	Full	±10	±15	-	±10	±15	-	±10	±15	-	±10	±15	-	mA
Full Power Bandwidth (Note 9)														
HA-5102/5104	+25°C	16	47	-	16	47	-	16	47	-	16	47	-	kHz
HA-5112/5114	+25°C	191	318	-	191	318	-	191	318	-	191	318	-	kHz
Output Resistance	+25°C	-	110	-	-	110	-	-	110	-	-	110	-	Ω
STABILITY														
Minimum Stable Closed Loop Gain														
HA-5102/5104	Full	1	-	-	1	-	-	1	-	-	1	-	-	V/V
HA-5112/5114	Full	10	-	-	10	-	-	10	-	-	10	-	-	V/V

Electrical Specifications **(Continued)** V+ =15V D.C., V- = -15V D.C., Unless Otherwise Specified

PARAMETER	TEMP	HA-5102-2 HA-5112-2 -55°C to +125°C			HA-5104-2 HA-5114-2 -55°C to +125°C			HA-5102-5 HA-5112-5 0°C to +75°C			HA-5104-5 HA-5114-5 0°C to +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TRANSIENT RESPONSE (Note 10)														
Rise Time														
HA-5102/5104	+25°C	-	108	200	-	108	200	-	108	200	-	108	200	ns
HA-5112/5114	+25°C	-	48	100	-	48	100	-	48	100	-	48	100	ns
Overshoot														
HA-5102/5104	+25°C	-	20	35	-	20	35	-	20	35	-	20	35	%
HA-5112/5114	+25°C	-	30	40	-	30	40	-	30	40	-	30	40	%
Slew Rate														
HA-5102/5104	+25°C	±1	±3	-	±1	±3	-	±1	±3	-	±1	±3	-	V/µs
HA-5112/5114	+25°C	±12	±20	-	±12	±20	-	±12	±20	-	±12	±20	-	V/µs
Settling Time (Note 11)														
HA-5102/5104	+25°C	-	4.5	-	-	4.5	-	-	4.5	-	-	4.5	-	µs
HA-5112/5114	+25°C	-	0.6	-	-	0.6	-	-	0.6	-	-	0.6	-	µs
NOISE CHARACTERISTICS														
Input Noise Voltage (Note 12)														
f = 10Hz	+25°C	-	9	17	-	9	17	-	9	17	-	9	17	$nV/\sqrt{Hz}$
f = 1kHz	+25°C	-	4.3	6.0	-	4.3	6.0	-	4.3	6.0	-	4.3	6.0	$nV/\sqrt{Hz}$
Input Noise Current (Note 12)														
f =10Hz	+25°C	-	5.1	12	-	5.1	12	-	5.1	12	-	5.1	12	$pA/\sqrt{Hz}$
f = 1kHz	+25°C	-	0.57	3	-	0.57	3	-	0.57	3	-	0.57	3	$pA/\sqrt{Hz}$
Broadband Noise Voltage														
f = DC to 30kHz	+25°C	-	870	-	-	870	-	-	870	-	-	870	-	nVrms
POWER SUPPLY CHARACTERISTICS														
Supply Current														
HA-5102/5112	+25°C	-	3.0	5.0	-	3.0	5.0	-	3.0	5.0	-	3.0	5.0	mA
HA-5104/5114	+25°C	-	5.0	6.5	-	5.0	6.5	-	5.0	6.5	-	5.0	6.5	mA
Power Supply Rejection Ratio (Note 6)	Full	86	100	-	86	100	-	86	100	-	86	100	-	dB

NOTES:

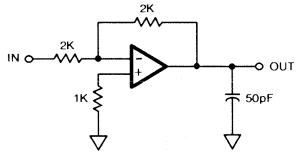
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For supply voltages < ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Any one amplifier may be shorted to ground indefinitely.
4. Derate 9.6mW/°C above T_A = +25°C.
5. V_{OUT} = ±10V, R_L = 2K
6. V_{CM} = ±5.0V
7. Channel separation value is referred to the input of the amplifier. Input test conditions are: f = 10kHz; V_{IN} = 200mV peak to peak; R_S = 1kΩ. (Refer to Channel Separation vs. Frequency Curve for test circuits.)
8. Output current is measured with V_{OUT} = ±5V.
9. Full power bandwidth is guaranteed by equation:

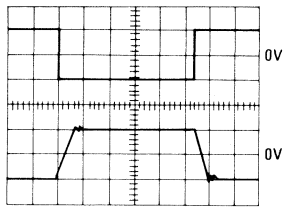
$$\text{Full power bandwidth} = \frac{\text{Slew Rate}}{2\pi\ V_{peak}}$$

10. Refer to Test Circuits section of the data sheet.
11. Settling time is measured to 0.1% of final value for a 1 volt input step, and A_V = -10 for HA-5112/5114, and a 10 volt input step, A_V = -1 for HA-5102/5104.
12. Sample tested.

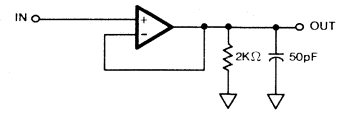
Test Circuits

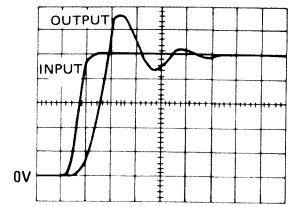
LARGE SIGNAL RESPONSE CIRCUIT
Volts: 5V/Div., Time: 5µs/Div. (A_V =-1)
HA-5102/5104



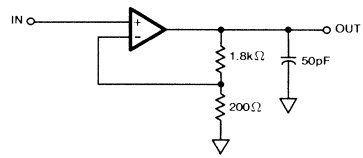


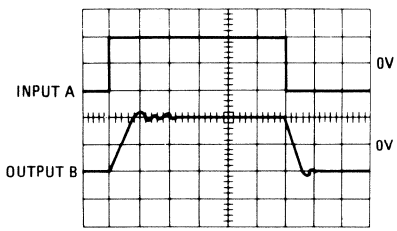
SMALL SIGNAL RESPONSE CIRCUIT
Volts: 40mV/Div., Time: 50ns/Div. (A_V = +1)
HA-5102/5104



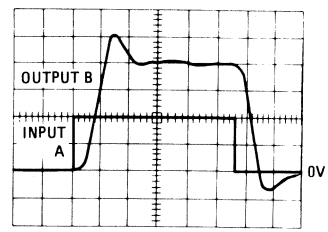


LARGE AND SMALL SIGNAL RESPONSE CIRCUIT
HA-5112/5114 (A_V = +10)



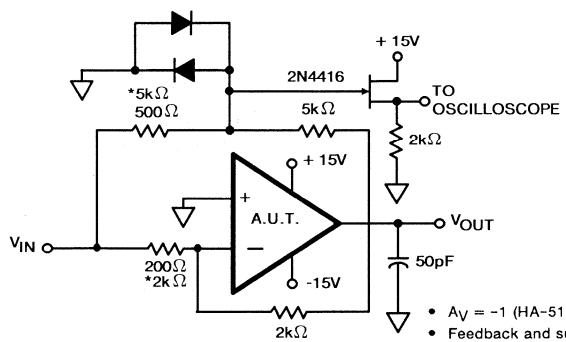


Volts: Input A: 0.5V/Div., Output B: 5V/Div.
Time: 50ns/Div.



Volts: Input A: 0.01V/Div., Output B: 50mV/Div.
Time: 50ns/Div.

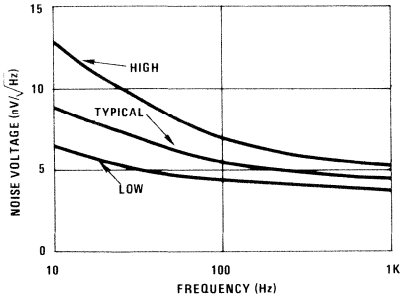
SETTLING TIME CIRCUIT



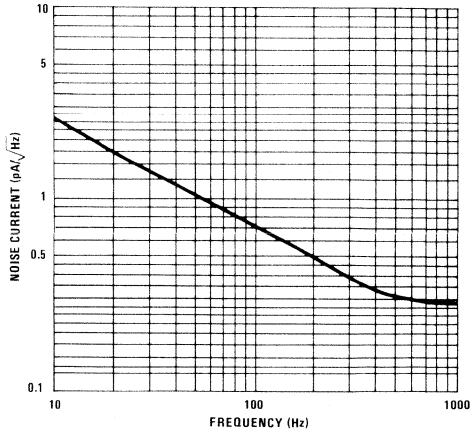
- A_V = -1 (HA-5102/5104), *A_V = -10 (HA-5112/5114)
- Feedback and summing resistors should be 0.1% matched.
- Clipping diodes are optional, HP5082-2810 recommended.

Typical Performance Curves

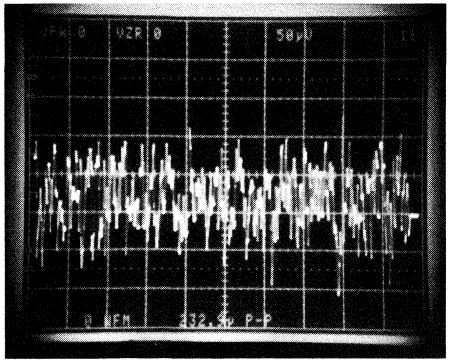
INPUT NOISE VOLTAGE DENSITY
V_{CC} = ±15V, T_A = +25°C



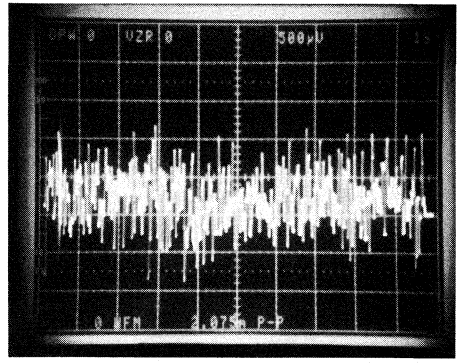
INPUT NOISE CURRENT DENSITY
V_{CC} = ±15V, T_A = +25°C



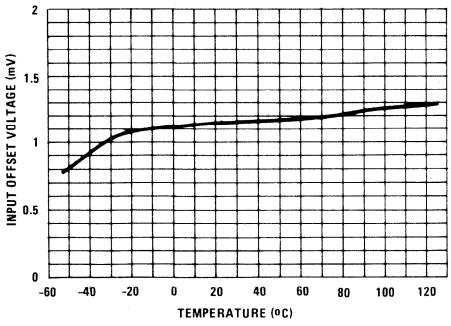
0.1Hz TO 10Hz NOISE
V_{CC} = ±15V, T_A = +25°C
50µV/Div., 1s/Div., A_V = 1000 V/V
Input Noise = 0.232µVp-p



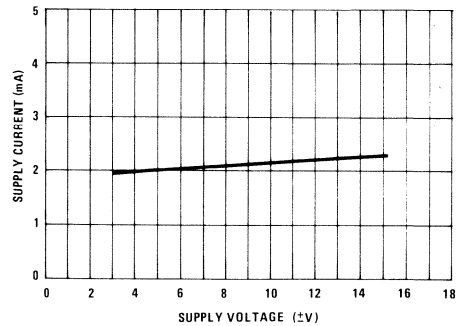
0.1Hz TO 1MHz NOISE
V_{CC} = ±15V, T_A = +25°C
500µV/Div., 1s/Div., A_V = 1000 V/V
Total Output Noise = 2.075µVp-p



V_{IO} vs. TEMPERATURE
V_{CC} = ±15V

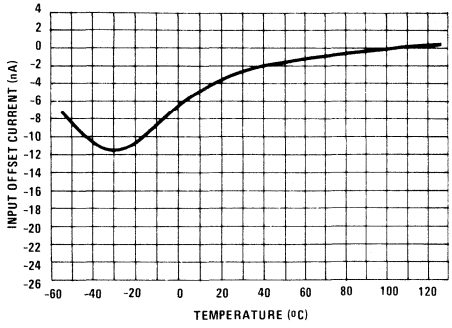


V_{IO} vs. V_{CC}
T_A = +25°C

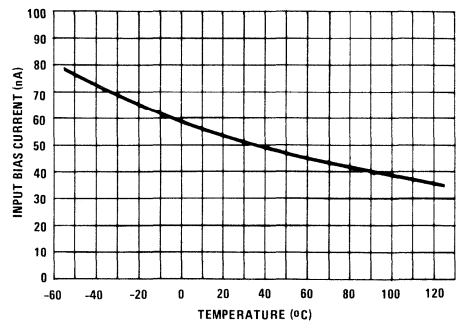


Typical Performance (Continued)

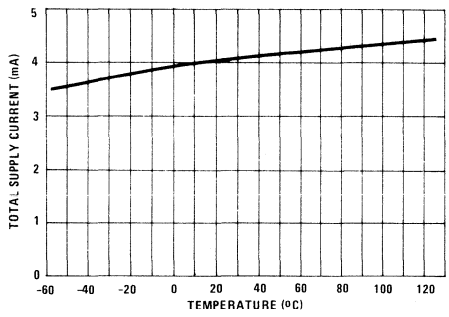
I_{IO} vs. TEMPERATURE
V_{CC} = ±15V



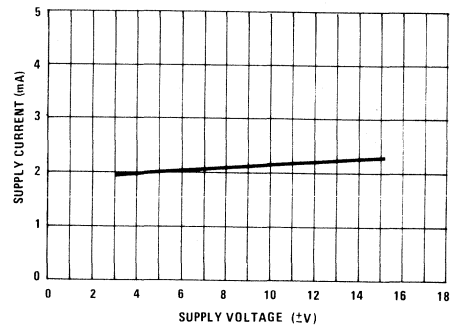
IBIAS vs. TEMPERATURE
V_{CC} = ±15V



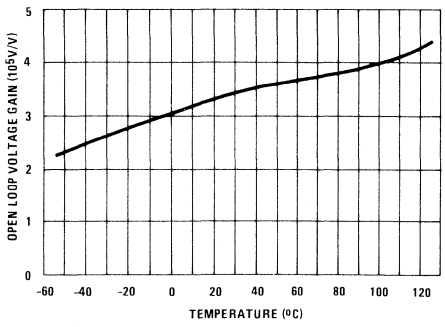
I_{CC} vs. TEMPERATURE
V_{CC} = ±15V, I_{OUT} = 0



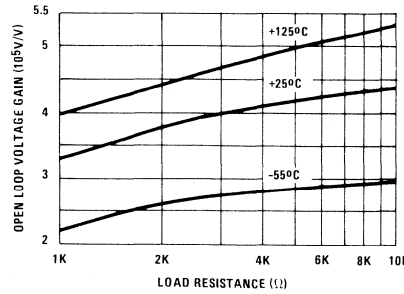
I_{CC} vs. V_{CC}
T_A = +25°C, I_{OUT} = 0



A_{VOL} vs. TEMPERATURE
V_{CC} = ±15V, ΔV_O = ±10V, R_L = 2K

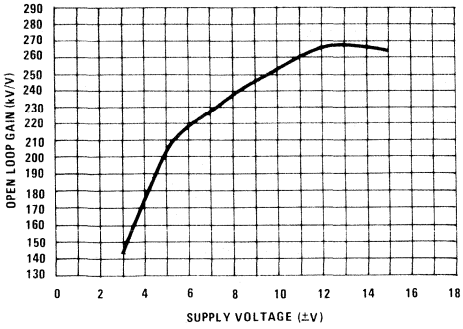


A_{VOL} vs. LOAD RESISTANCE
V_O = ±10V, V_{CC} = ±15V, T_A = +25°C

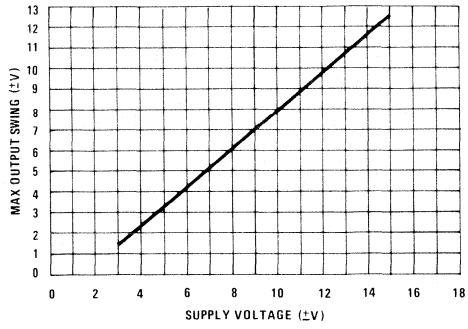


Typical Performance (Continued)

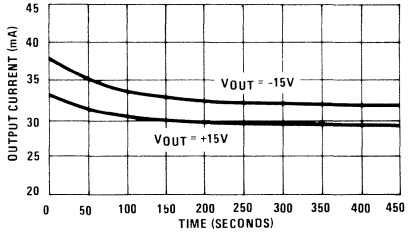
A_{VOL} vs. V_{CC}
$T_A = +25^oC$, $R_L = 2K$



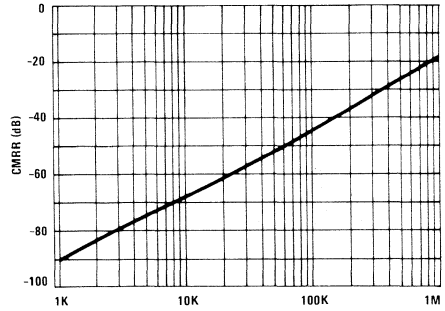
V_{OUT} vs. V_{CC}
$T_A = +25^oC$, $R_L = 2K$



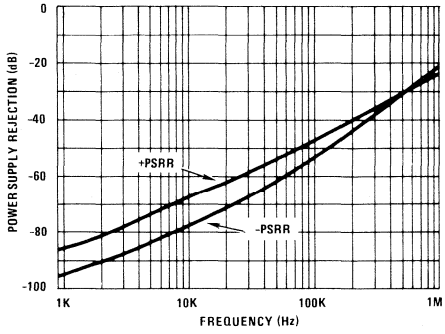
OUTPUT SHORT-CIRCUIT CURRENT vs. TIME
$V_{CC} = \pm 15V$, $T_A = +25^oC$



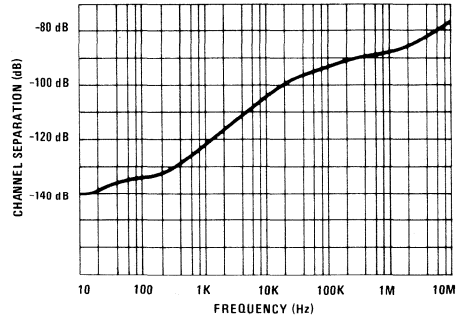
CMRR vs. FREQUENCY



PSRR vs. FREQUENCY

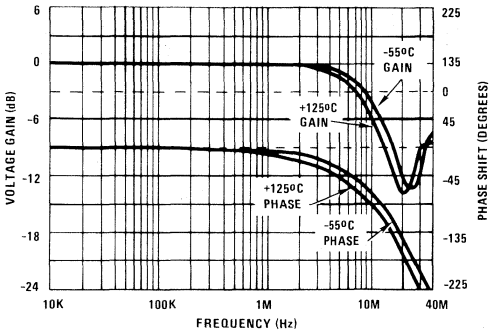


HA-5104 CHANNEL SEPARATION vs. FREQUENCY
$10Hz \leq f \leq 10MHz$

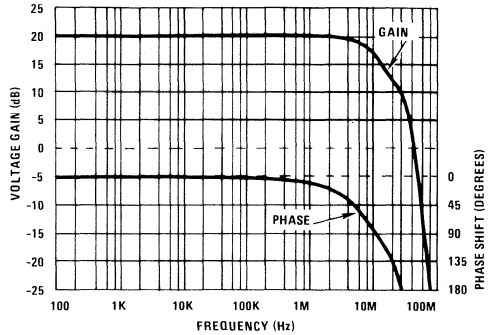


Typical Performance (Continued)

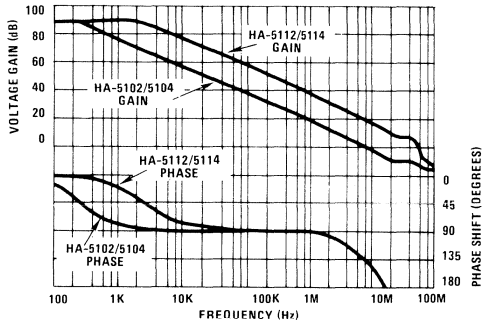
HA-5104/02 UNITY GAIN FREQUENCY RESPONSE
V_{CC} = ±15V, R_L = 2K, C_L = 50pF



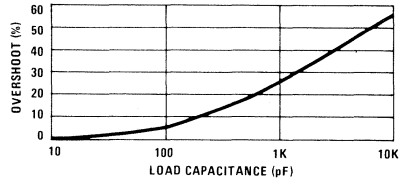
HA-5112/14 FREQUENCY RESPONSE
A_{VCL} = 10, T_A = +25°C, R_L = 2K, C_L = 50pF



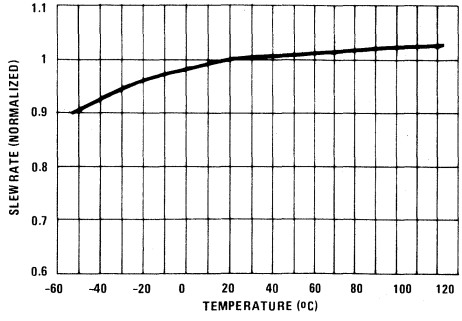
OPEN-LOOP GAIN vs. FREQUENCY
V_{CC} = ±15V, R_L = 2K, C_L = 50pF, T_A = +25°C



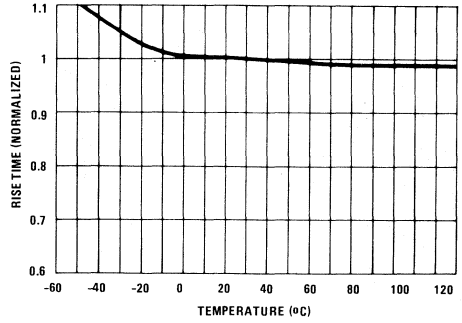
SMALL SIGNAL OVERSHOOT vs. CLOAD
V_{CC} = ±15V, T_A = +25°C, R_L = 2K



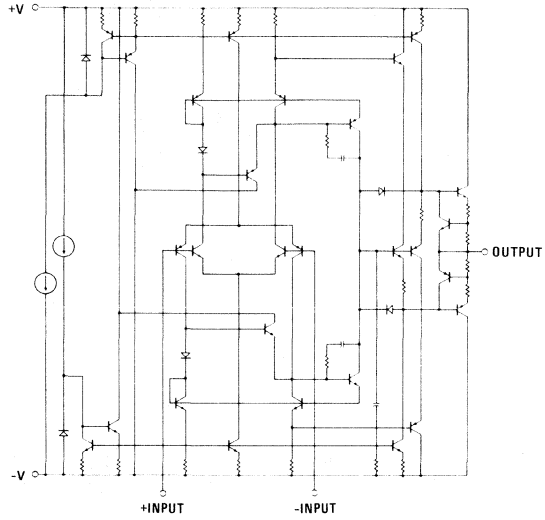
SLEW RATE vs. TEMPERATURE
R_L = 2K, C_L = 50pF, V_{CC} = ±15V



RISE TIME vs. TEMPERATURE
R_L = 2K, C_L = 50pF, V_{CC} = ±15V



Simplified Schematic



Die Characteristics

Transistor Count

HA-5102/5112 93

HA-5104/5114 175

Die Dimensions

HA-5102/5112 ..... 98.4 x 67.3 x 19 mils (2500 x 1710 x 480µm)

HA-5104/5114 ..... 99.6 x 95.3 x 19 mils (2530 x 2420 x 480µm)

Substrate Potential* ..... V-

Process ..... Bipolar-DI

Passivation ..... Nitride

*The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.

Thermal Constants (oC/W)	θ_{ja}	θ_{jc}
HA1-5104 (-2, -5, -7)	103	35
HA1-5104 (/883)	78	25
HA2-5102/5112 (-2, -5, -7)	174	48
HA2-5102/5112 (/883)	134	40
HA3-5102/5112 (-5)	80	20
HA3-5104/5114 (-5)	75	23
HA7-5102/5112 (-2, -5, -7)	163	82
HA7-5102/5112 (/883)	124	47

HARRIS

HA-5127

Ultra-Low Noise Precisio
Operational Amplifie

Features

- High Speed 10V/μs
- Wide Unity Gain Bandwidth 8.5MHz
- Low Noise ..... 3nV/$\sqrt{Hz}$ at 1KHz
- Low V_{OS} 10μV
- High CMRR 126dB
- High Gain 1800V/mV

Applications

- High Speed Signal Conditioners
- Wide Bandwidth Instrumentation Amplifiers
- Low Level Transducer Amplifiers
- Fast, Low Level Voltage Comparators
- Highest Quality Audio Preamplifiers
- Pulse/RF Amplifiers

Description

The HA-5127 monolithic operational amplifier features an unparalleled combination of precision DC and wideband high speed characteristics. Utilizing the Harris D. I. technology and advanced processing techniques, this unique design unites low noise (3nV/$\sqrt{Hz}$) precision instrumentation performance with high speed (10V/μs) wideband capability.

This amplifier's impressive list of features include low V_{OS} (10μV), wide unity gain-bandwidth (8.5MHz), high open loop gain (1800V/mV), and high CMRR (126 dB). Additionally, this flexible device operates over a wide supply range ($\pm$5V to $\pm$20V) while consuming only 140mW of power.

Using the HA-5127 allows designers to minimize errors while maximizing speed and bandwidth.

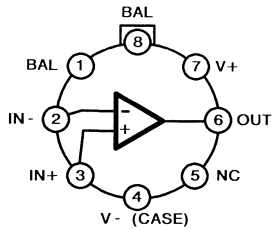
This device is ideally suited for low level transducer signal amplifier circuits. Other applications which can utilize the HA-5127's qualities include instrumentation amplifiers, pulse amplifiers, audio preamplifiers, and signal conditioning circuits.

This device can easily be used as a design enhancement by directly replacing the 725, OP25, OP06, OP07, OP27 and OP37. The HA-5127 is available in TO-99 Metal Can and Ceramic 8 pin Mini-DIPs. For the military grade product, refer to the HA-5127/883 data sheet.

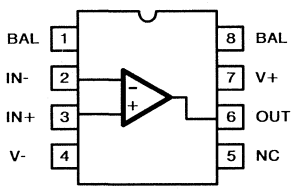
Pinouts

TOP VIEWS

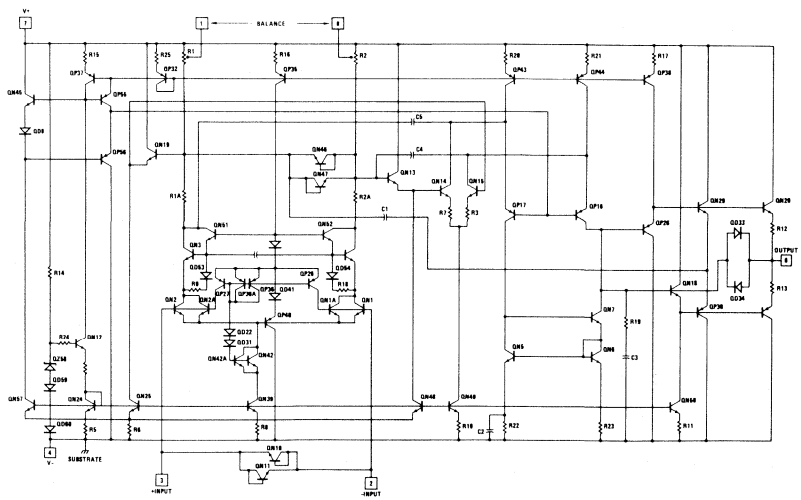
HA2-5127 (TO-99 METAL CAN)



HA7-5127 (CERAMIC MINI-DIP)



Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

T_A = +25°C Unless Otherwise Stated
Voltage Between V+ and V− Terminals ..... ±22V
Differential Input Voltage (Note 2) ..... ±0.7V
Internal Power Dissipation 500mW
Output Current ..... Full Short Circuit Protection

Operating Temperature Ranges

HA-5127/27A-2 ..... −55°C ≤ TA ≤ +125°C
HA-5127/27A-5 ..... 0°C ≤ TA ≤ +75°C
Storage Temperature Range ..... −65°C ≤ TA ≤ +150°C

Electrical Specifications

V+ = 15V, V− = −15V, $C_L \leq 50pF$, $R_S \leq 100\Omega$

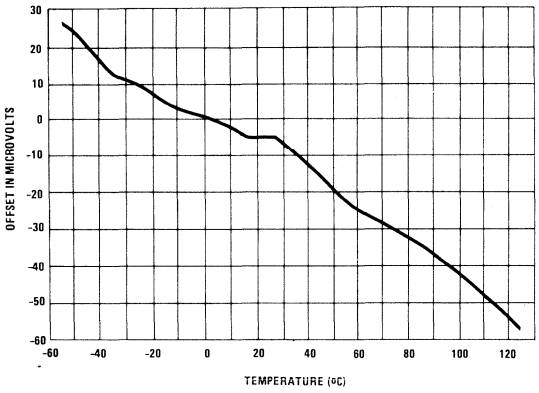
PARAMETER	TEMP	HA-5127A MIN	HA-5127A TYP	HA-5127A MAX	HA-5127 MIN	HA-5127 TYP	HA-5127 MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		10	25		30	100	μV
	Full		30	60		70	300	μV
Average Offset Voltage Drift	Full		0.2	0.6		0.4	1.8	μV/°C
Bias Current	+25°C		±10	±40		±15	±80	nA
	Full		±20	±60		±35	±150	nA
Offset Current	+25°C		7	35		12	75	nA
	Full		15	50		30	135	nA
Common Mode Range	Full	±10.3	±11.5		±10.3	±11.5		V
Differential Input Resistance (Note 3)	+25°C	1.5	6		0.8	4		MΩ
Input Noise Voltage 0.1Hz to 10Hz (Note 4)	+25°C		0.08	.18		0.09	0.25	μVp-p
Input Noise Voltage Density (Note 5)	+25°C							nV/√Hz
f_0 = 10 Hz			3.5	5.5		3.8	8.0	
f_0 = 30 Hz			3.1	4.5		3.3	5.6	
f_0 = 1000 Hz			3.0	3.8		3.2	4.5	
Input Noise Current Density (Note 5)	+25°C							pA/√Hz
f_0 = 10 Hz			1.7	4.0		1.7		
f_0 = 30 Hz			1.0	2.3		1.0		
f_0 = 1000 Hz			0.4	0.6		0.4	0.6	
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 6)	+25°C	1000	1800		700	1500		V/mV
	Full	600	1200		300	800		V/mV
Common Mode Rejection Ratio (Note 7)	Full	114	126		100	120		dB
Minimum Stable Gain	+25°C	1			1			V/V
Unity-Gain-Bandwidth	+25°C	5	8.5		5	8.5		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing R_L = 600Ω	+25°C	±10.0	±11.5		±10.0	±11.5		V
R_L = 2KΩ	Full	±11.7	±13.8		±11.4	±13.5		V
Full Power Bandwidth (Note 8)	+25°C	111	160		111	160		KHz
Output Resistance, Open Loop	+25°C		70			70		Ω
TRANSIENT RESPONSE (Note 9)								
Rise Time	+25°C			150			150	ns
Slew Rate (Note 11)	+25°C	7	10		7	10		V/μs
Settling Time (Note 10)	+25°C		1.5			1.5		μs
Overshoot	+25°C		20	40		20	40	%
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C		3.5			3.5		mA
	Full			4.0			4.0	mA
Power Supply Rejection Ratio (Note 12)	Full		2	4		16	51	μV/V

NOTES:

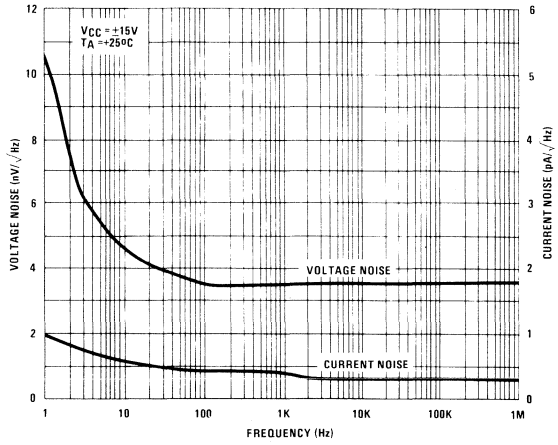
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For differential input voltages greater than 0.7V, the input current must be limited to 25mA to protect the back-to-back input diodes.
3. This parameter value is based upon design calculations.
4. Refer to Typical Performance section of the data sheet.
5. Sample tested.
6. $V_{OUT} = \pm 10V$, $R_L = 2K\Omega$
7. $V_{CM} = \pm 10V$
8. Full power bandwidth guaranteed based on slew rate measurement using: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$
9. Refer to Test Circuits section of the data sheet.
10. Settling time is specified to 0.1% of final value for a 10V output step and Av = −1.
11. V_{OUT} = 10V Step
12. $V_S = \pm 4V$ to $\pm 18V$

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm 15V$

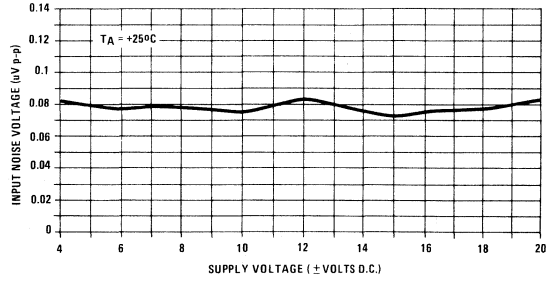
OFFSET VOLTAGE TYPICAL DRIFT vs. TEMPERATURE



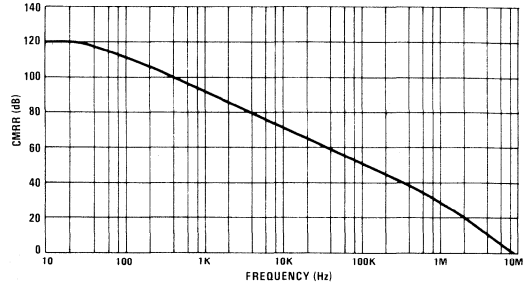
NOISE CHARACTERISTICS



NOISE vs. SUPPLY VOLTAGE

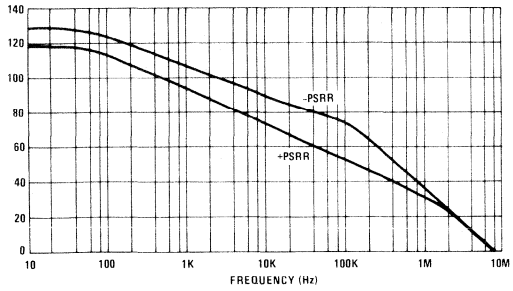


CMRR vs. FREQUENCY

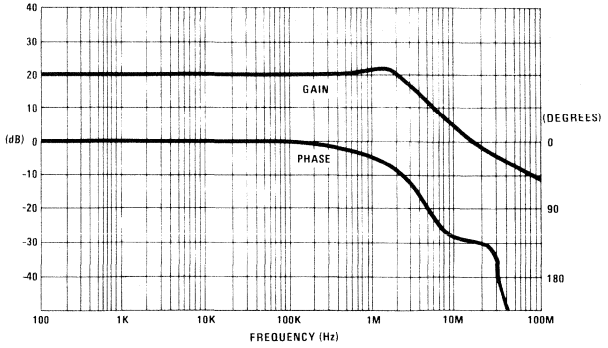


Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm 15V$

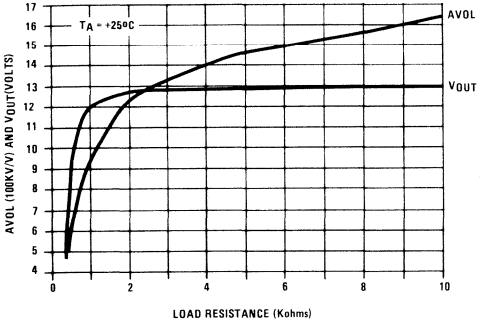
PSRR vs. FREQUENCY



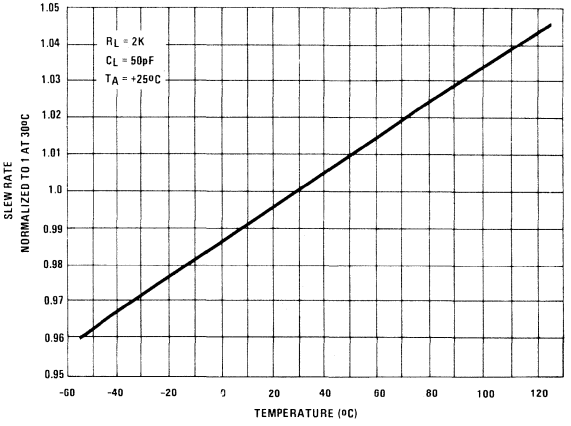
CLOSED LOOP GAIN AND PHASE vs. FREQUENCY



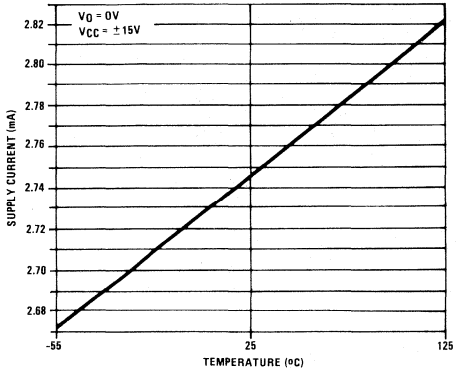
AVOL AND V_{OUT} vs. LOAD RESISTANCE



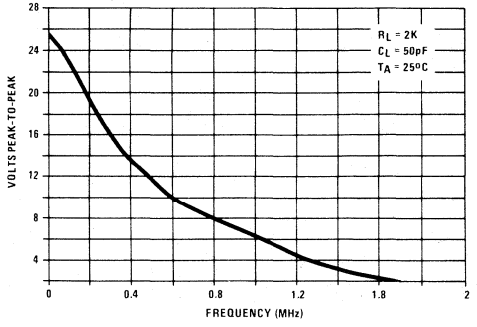
NORMALIZED SLEW RATE vs. TEMPERATURE



SUPPLY CURRENT vs. TEMPERATURE

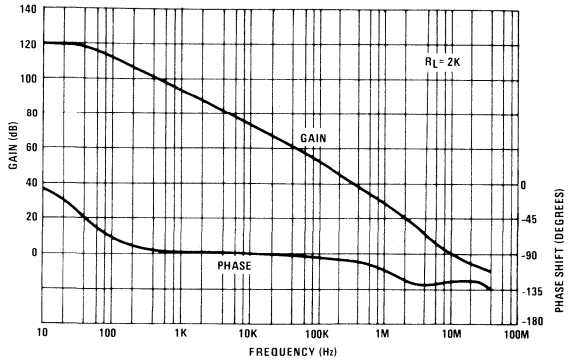


V_{OUT} MAX vs. FREQUENCY UNDISTORTED SINEWAVE OUTPUT

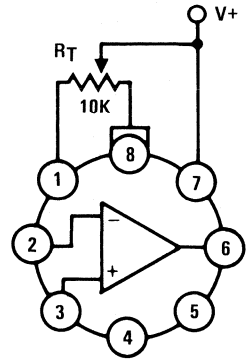


Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm 15V$

OPEN LOOP GAIN AND PHASE vs. FREQUENCY

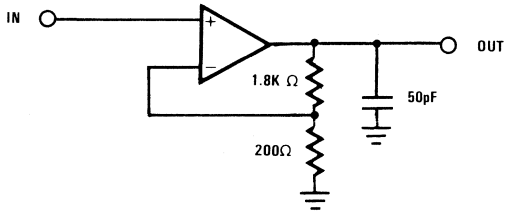


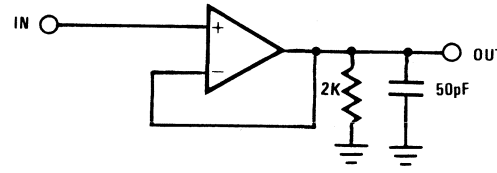
SUGGESTED OFFSET VOLTAGE ADJUSTMENT



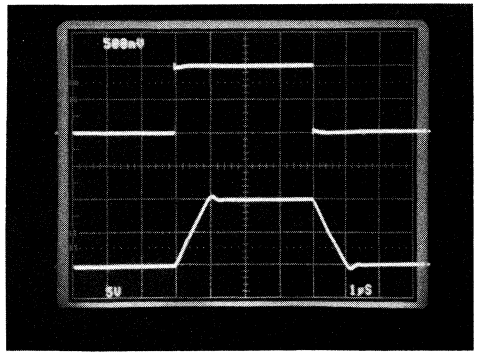
Tested Offset Adjustment Range is $|V_{OS} + 1mV|$ minimum referred to output. Typical range is $\pm 4mV$ with $R_T = 10k\Omega$.

LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT



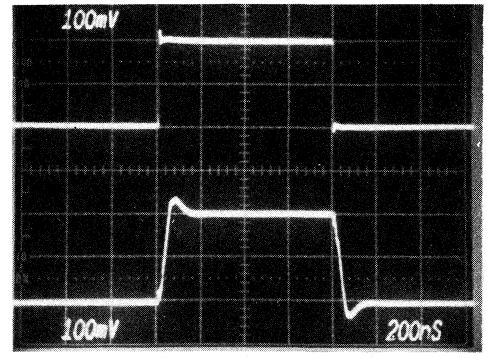


LARGE SIGNAL RESPONSE



Vertical Scale: (Volts: Input = 0.5V/Div.)
(Output = 5V/Div.)
Horizontal Scale: (Time = 1μS/Div.)

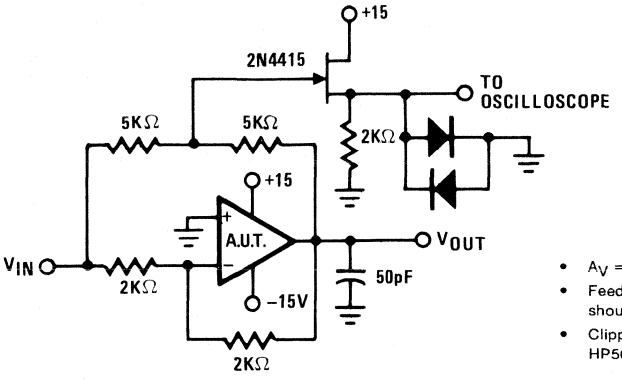
SMALL SIGNAL RESPONSE



Vertical Scale: (Volts: 100mV/Div.)
Horizontal Scale: (200nS/Div.)

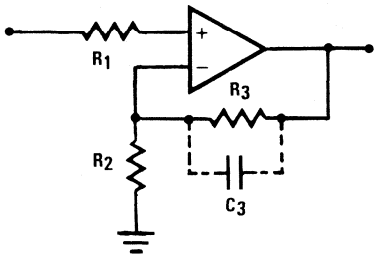
Typical Performance Curves Unless Otherwise Specified: T_A = +25°C, V_{SUPPLY} = ±15V

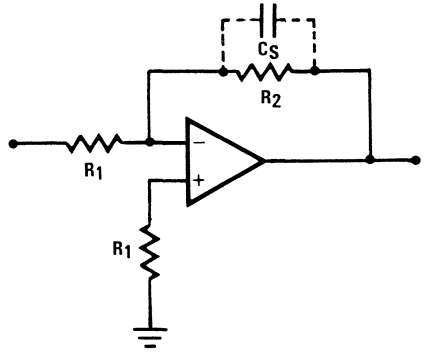
SETTLING TIME TEST CIRCUIT



- A_V = -1
- Feedback and summing resistors should be 0.1% matched.
- Clipping diodes are optional. HP5082-2810 recommended.

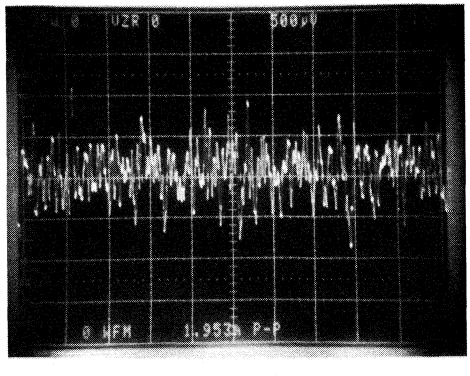
SUGGESTED STABILITY CIRCUITS





Low resistances are preferred for low noise applications as a 1KΩ resistor has 4nV/√Hz of thermal noise. Total resistances of greater than 10KΩ on either input can reduce stability. In most high resistance applications, a few picofarads of capacitance across the feedback resistor will improve stability.

0.1Hz TO 10Hz NOISE WITH A_{CL} = 25,000V/V



Horizontal Scale = 1sec/Div.
Vertical Scale = 0.002μV/Div.
0.08μVp-p

Die Characteristics

Transistor Count 63
Die Dimensions ..... 65 x 104.3 x 19mils
(1700 x 2600 x 480μm)
Substrate Potential* ..... V-
Process ..... Bipolar-DI

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
HA7-5127, Ceramic Mini-DIP	160	79
HA2-5127, TO-99 Metal Can	172	48

*The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.

HA-5130/35

Precision Operational Amplifier

Features

- Low Offset Voltage 10μV
- Low Offset Voltage Drift ..... 0.4μV/°C
- Low Noise ..... 9nV/$\sqrt{Hz}$
- Open Loop Gain 140dB
- Unity Gain Bandwidth 2.5MHz
- All Bipolar Construction

Applications

- High Gain Instrumentation
- Precision Data Acquisition
- Precision Integrators
- Biomedical Amplifiers
- Precision Threshold Detectors

Description

The Harris HA-5130/5135 are precision operational amplifiers manufactured using a combination of key technological advancements to provide outstanding input characteristics.

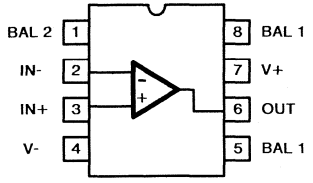
A Super Beta input stage is combined with laser trimming, dielectric isolation and matching techniques to produce 25μV (Maximum) input offset voltage and 0.4μV/°C input offset voltage average drift. Other features enhanced by this process include 9nV/$\sqrt{Hz}$ (Typ.) Input Noise Voltage, 1nA Input Bias Current and 140dB Open Loop Gain.

These features coupled with 120dB CMRR and PSRR make HA-5130/5135 an ideal device for precision DC instrumentation amplifiers. Excellent input characteristics in conjunction with 2.5MHz bandwidth and 0.8V/μs slew rate, makes this amplifier extremely useful for precision integrator and biomedical amplifier designs. These amplifiers are also well suited for precision data acquisition and for accurate threshold detector applications.

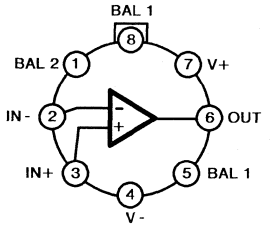
HA-5130/5135 is packaged in an 8 pin (TO-99) Metal Can and an 8 lead Cerdip and is pin compatible with many existing op amp configurations. It offers added features over the industry standard OP-07 in regards to bandwidth and slew rate specifications. For the military grade product, refer to the HA-5135/883 data sheet.

Pinouts

HA7-5130/5135 (CERAMIC MINI-DIP)
TOP VIEW

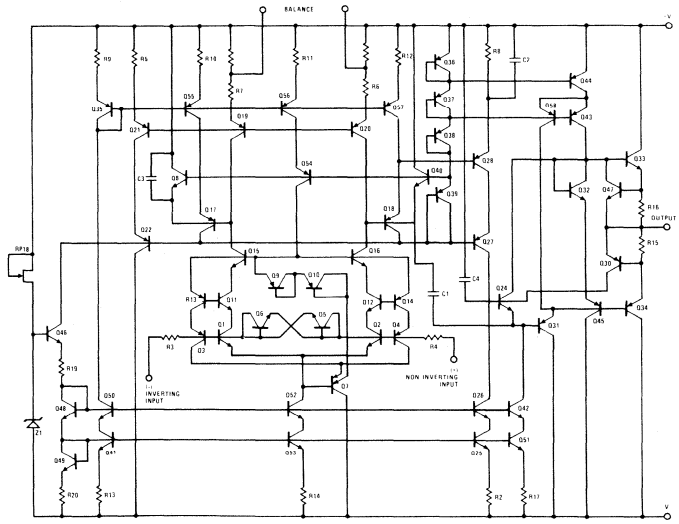


HA2-5130/5135 (TO-99 METAL CAN)
TOP VIEW



(Both BAL 1 Pins are Internally Connected)

Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

T_A = +25°C Unless Otherwise Stated
Voltage Between V+ and V- Terminals 40.0V
Differential Input Voltage ..... ±15.0V
Output Short Circuit Duration ..... Indefinite
Power Dissipation (Note 2) 300mW

Operating Temperature Ranges

HA-5130/5135-2 ..... -55°C ≤ T_A ≤ +125°C
HA-5130/5135-5 ..... 0°C ≤ T_A ≤ +75°C
Storage Temperature Range ..... -65°C ≤ T_A ≤ +150°C

Electrical Specifications V+ = +15V, V- = -15V

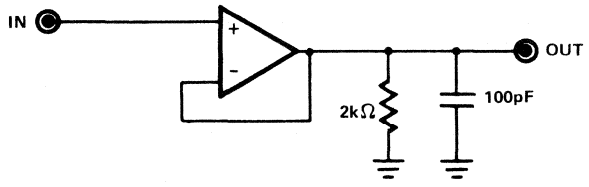
PARAMETER	TEMP	HA-5130-2/-5 MIN	HA-5130-2/-5 TYP	HA-5130-2/-5 MAX	HA-5135-2/-5 MIN	HA-5135-2/-5 TYP	HA-5135-2/-5 MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C	—	10	25	—	10	75	μV
	Full	—	50	60	—	50	130	μV
Average Offset Voltage Drift	Full	—	0.4	0.6	—	0.4	1.3	μV/°C
Bias Current	+25°C	—	±1	±2	—	±1	±4	nA
	Full	—	—	±4	—	—	±6	nA
Bias Current Average Drift	Full	—	0.02	0.04	—	0.02	0.04	nA/°C
Offset Current	+25°C	—	—	2	—	—	4	nA
	Full	—	—	4	—	—	5.5	nA
Offset Current Average Drift	Full	—	0.02	0.04	—	0.02	0.04	nA/°C
Common Mode Range	Full	±12	—	—	±12	—	—	V
Differential Input Resistance	+25°C	20	30	—	20	30	—	MΩ
Input Noise Voltage 0.1Hz to 10Hz (Note 3)	+25°C	—	—	0.6	—	—	0.6	μV_{p-p}
Input Noise Voltage Density (Note 3)	+25°C							$nV/\sqrt{Hz}$
f_0 = 10Hz		—	13.0	18.0	—	13.0	18.0	
f_0 = 100Hz		—	10.0	13.0	—	10.0	13.0	
f_0 = 1000Hz		—	9.0	11.0	—	9.0	11.0	
Input Noise Current 0.1Hz to 10Hz (Note 3)	+25°C	—	15	30	—	15	30	pA_{p-p}
Input Noise Current Density (Note 3)	+25°C							$pA/\sqrt{Hz}$
f_0 = 10Hz		—	0.4	0.8	—	0.4	0.8	
f_0 = 100Hz		—	0.17	0.23	—	0.17	0.23	
f_0 = 1000Hz		—	0.14	0.17	—	0.14	0.17	
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 4)	+25°C	120	140	—	120	140	—	dB
	Full	120	—	—	120	—	—	dB
Common Mode Rejection Ratio (Note 5)	Full	110	120	—	106	120	—	dB
Closed Loop Bandwidth (A_{VCL} = +1)	+25°C	0.6	2.5	—	0.6	2.5	—	MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 6)	+25°C	±10	±12	—	±10	±12	—	V
	Full	±10	—	—	±10	—	—	V
Full Power Bandwidth (Note 7)	+25°C	8	10	—	8	10	—	kHz
Output Current (Note 8)	+25°C	±15	±20	—	±15	±20	—	mA
Output Resistance (Note 8)	+25°C	—	45	—	—	45	—	Ω
TRANSIENT RESPONSE (Note 10)								
Rise Time	+25°C	—	340	—	—	340	—	ns
Slew Rate	+25°C	0.5	0.8	—	0.5	0.8	—	V/μs
Settling Time (Note 11)	+25°C	—	11	—	—	11	—	μs
POWER SUPPLY CHARACTERISTICS								
Supply Current	Full	—	1.0	1.3	—	1.0	1.7	mA
Power Supply Rejection Ratio (Note 12)	Full	100	130	—	94	130	—	dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Funtional operability under any of these conditions is not necessarily implied.
2. Derate at 6.8mW/°C for operation at ambient temperatures above +75°C.
3. Not tested. 90% of units meet or exceed these specifications.
4. V_{OUT} = ±10V; R_L = 2K. Gain dB = 20 $\log_{10}$ Av
   ∴ 120dB = **1MV/V**
   140dB = **10MV/V**
5. V_{CM} = ±10V DC
6. R_L = 600Ω
7. R_L = 2K; Full power bandwidth guaranteed based on slew rate measurement using FPBW = $\frac{\text{SLEW RATE}}{2\pi V_{PEAK}}$
8. V_{OUT} = 10V
9. Output resistance measured under open loop conditions (f = 100Hz).
10. Refer to test circuits section of the data sheet.
11. Settling time is measured to 0.1% of final value for a 10V output step and A_V = -1.
12. V_{SUPPLY} = ±5V DC to ±20V DC.

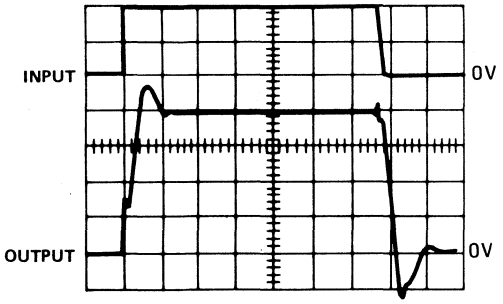
Test Circuits

SLEW RATE AND TRANSIENT RESPONSE TEST CIRCUIT



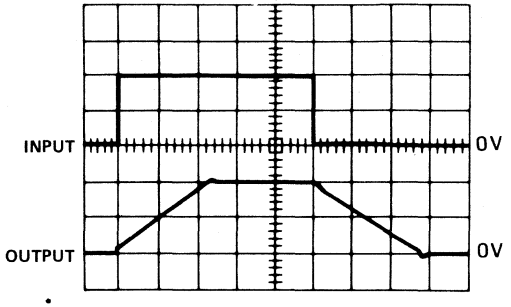
SMALL SIGNAL RESPONSE

Vertical Scale: (Volts: 50mV/Div. Output)
(Volts: 100mV/Div. Input)
Horizontal Scale: (Time: 1μs/Div.)

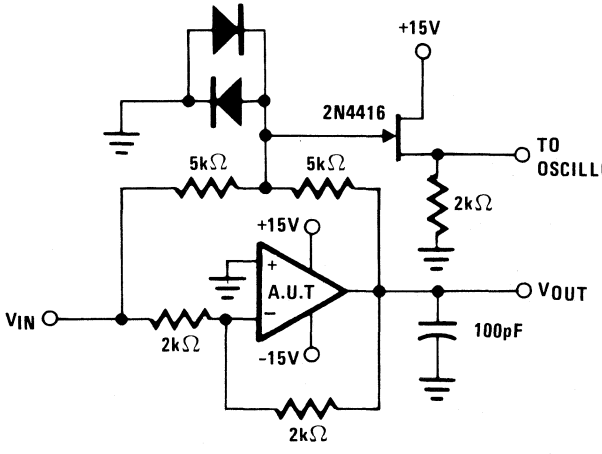


LARGE SIGNAL RESPONSE

Vertical Scale: (Volts: 5V/Div.)
Horizontal Scale: (Time: 5μs/Div.)



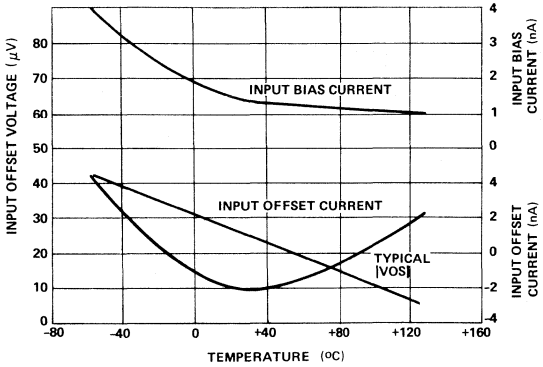
SETTLING TIME CIRCUIT



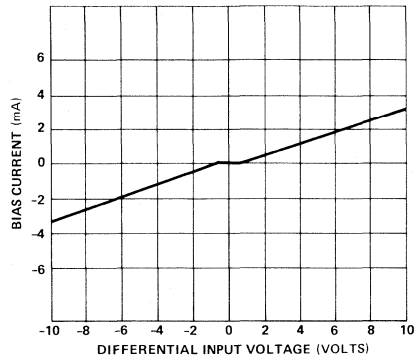
- $A_V = -1$
- Feedback and summing resistors should be 0.1% matched.
- Clipping diodes are optional. HP5082-2810 recommended.

Performance Curves

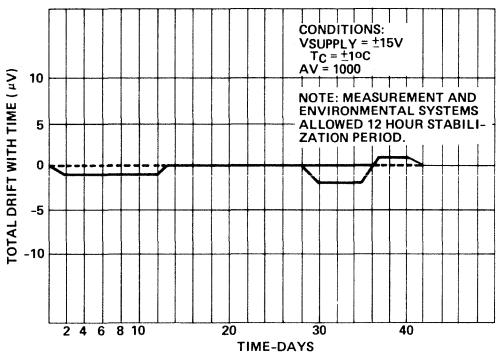
INPUT OFFSET VOLTAGE, INPUT BIAS AND OFFSET CURRENT vs. TEMPERATURE



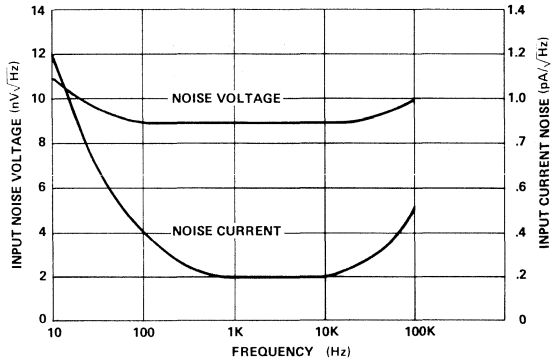
INPUT BIAS CURRENT vs. DIFFERENTIAL INPUT VOLTAGE



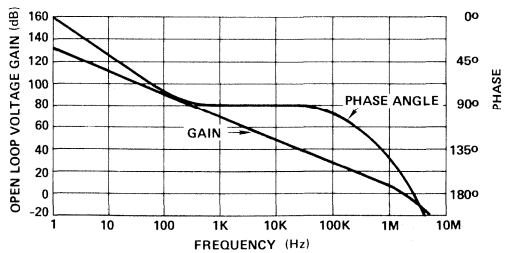
HA-5130 OFFSET VOLTAGE STABILITY vs. TIME



INPUT NOISE vs. FREQUENCY

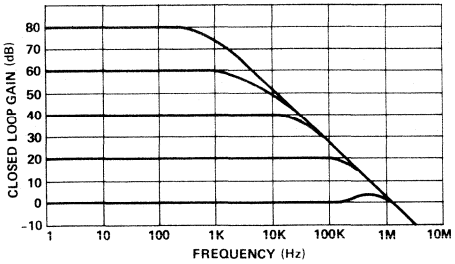


OPEN LOOP FREQUENCY RESPONSE

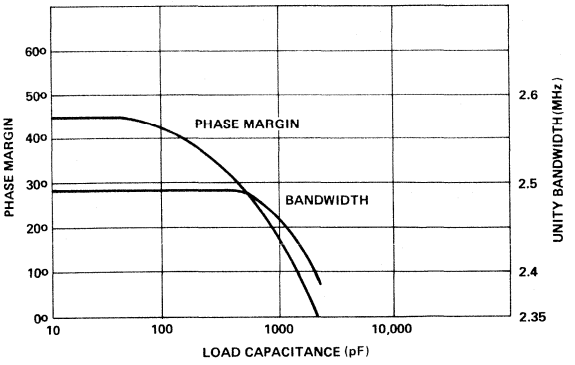


Performance Curves (Continued)

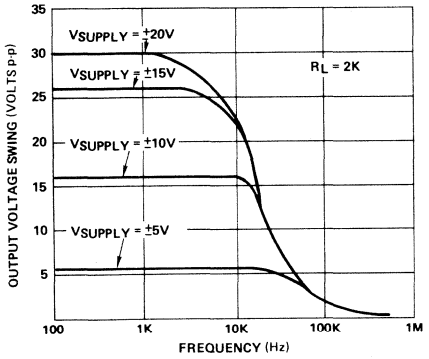
CLOSED LOOP FREQUENCY RESPONSE FOR VARIOUS CLOSED LOOP GAINS



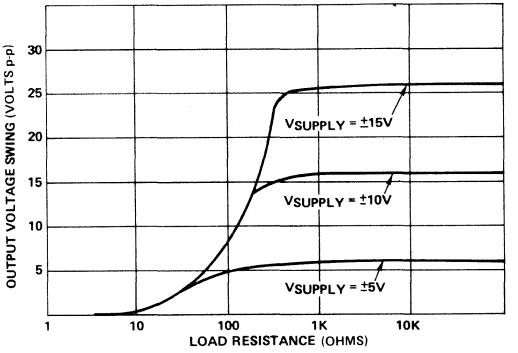
SMALL SIGNAL BANDWIDTH AND PHASE MARGIN vs. LOAD CAPACITANCE



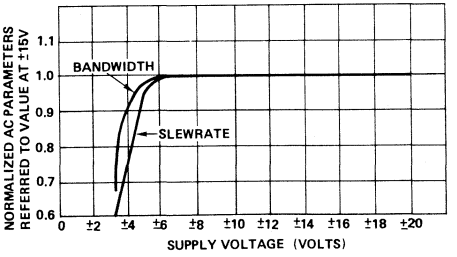
OUTPUT VOLTAGE SWING vs. FREQUENCY AND SUPPLY VOLTAGE



MAXIMUM OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE AND SUPPLY VOLTAGE

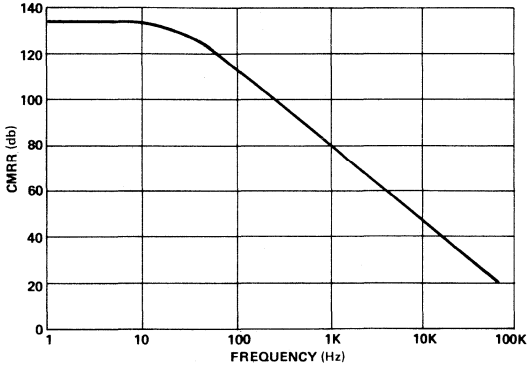


NORMALIZED AC PARAMETERS vs. SUPPLY VOLTAGE

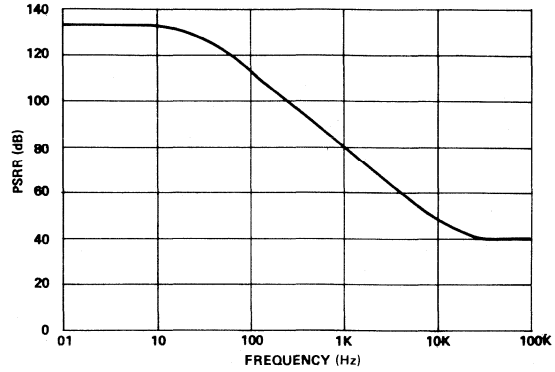


Performance Curves (Continued)

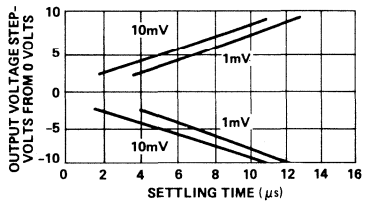
CMRR vs. FREQUENCY



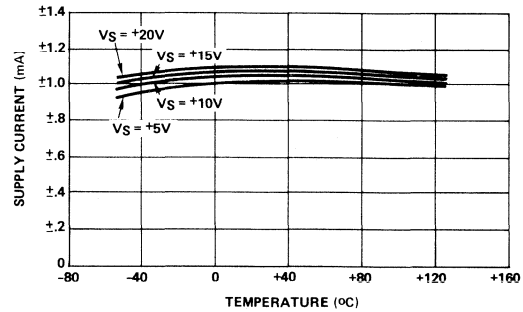
PSRR vs. FREQUENCY



SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES



POWER SUPPLY CURRENT vs. TEMPERATURE AND SUPPLY VOLTAGE

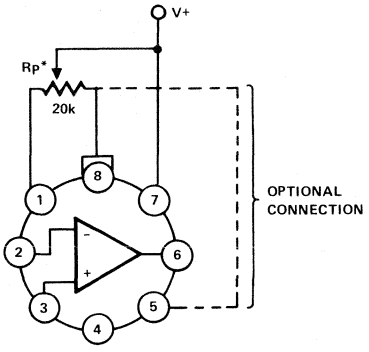


Applying the HA-5130/35 Operational Amplifiers

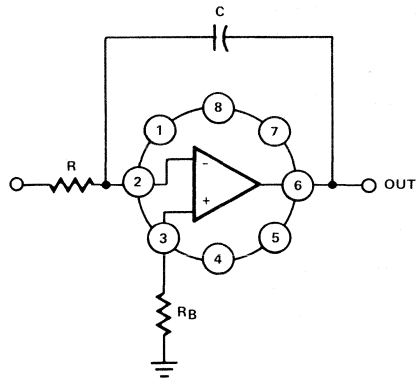
1. POWER SUPPLY DECOUPLING: Although not absolutely necessary, it is recommended that all power supply lines be decoupled with 0.01μF ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.
2. CONSIDERATIONS FOR PROTOTYPING: The following list of recommendations are suggested for prototyping.
   - Resolving low level signals requires minimizing leakage currents caused by external circuitry. Use of quality insulating materials, thorough cleaning of insulating surfaces and implementation of moisture barriers when required is suggested.
   - Error voltages generated by theromocouples formed between dissimilar metals in the presence of temperature gradients should be minimized. Isolation of low level circuity from heat generating components is recommended.
   - Shielded cable input leads, guard rings and shield drivers are recommended for the most critical applications.
3. When driving large capacitive loads (>500pF), as small value resistor (≈ 50Ω) should be connected in series with the output and inside the feedback loop.
4. OFFSET VOLTAGE ADJUSTMENT: A 20kΩ balance potentiometer is recommended if offset nulling is required. However, other potentiometer values such as 10kΩ, 50kΩ and 100kΩ may be used. The minimum adjustment range for given values is ±2mV.
5. SATURATION RECOVER: Input and output saturation recovery time is negligible in most applications. However, care should be exercised to avoid exceeding the absolute maximum ratings of the device.
6. DIFFERENTIAL INPUT VOLTAGES: Inputs are shunted with back-to-back diodes for overvoltage protection. In applications where differential input voltages in excess of 1V are applied between the inputs, the use of limiting resistors at the inputs is recommended.

Applications

OFFSET NULLING CONNECTIONS



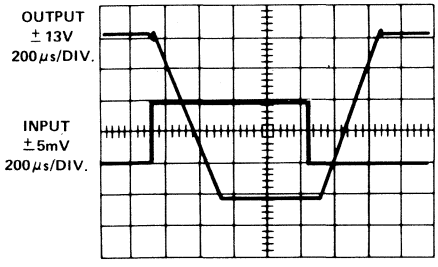
PRECISION INTEGRATOR

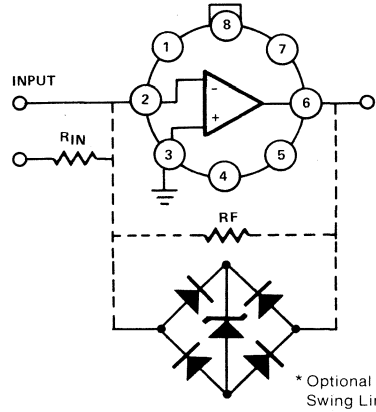


* Although R_P is shown equal to 20K, other values such as 50K, 100K and 1M may be used. Range of adjustment is approximately ±2.5mV. V_{OS} TC of the amplifier is optimized at minimal V_{OS}.
Tested Offset Adjustment is $|V_{OS} + 1mV|$ minimum referred to output.

The excellent inputs and gain characteristics of HA-5130 are well suited for precision integrator applications. Accurate integration over seven decades of frequency using HA-5130, virtually nullifies the need for more expensive chopper-type amplifiers.

ZERO CROSSING DETECTOR

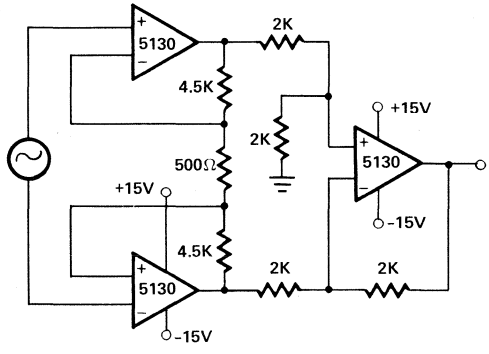




Low V_{OS} coupled with high open loop Gain, high CMRR and high PSRR make HA-5130 ideally suited for precision detector applications.

* Optional for Output Swing Limiting

PRECISION INSTRUMENTATION AMPLIFIER (A_V = 100)



HARRIS

HA-5134

Precision Quad Operational Amplifier

Features

- Low Offset Voltage ..... Max 200μV
- Low Offset Voltage Drift ..... Max 2μV/^{o}C
- Offset Voltage Match (5134A)... Full Temp. Max 250μV
- High Channel Separation 120dB
- Low Noise ..... 7nV/$\sqrt{Hz}$
- Wide Unity Gain Bandwidth 4MHz
- High CMRR/PSRR (Typ) 120dB
- Dielectric Isolation

Applications

- Instrumentation Amplifiers
- State-Variable Filters
- Precision Integrators
- Threshold Detectors
- Precision Data Acquisition Systems
- Low-Level Transducer Amplifiers

Description

The HA-5134 is a precision quad operational amplifier that is pin compatible with the OP-400, LT1014, OP11, RM4156, and LM148 as well as the HA-4741. Each amplifier features guaranteed maximum values for offset voltage of 200μV, offset voltage drift of 2μV/^{o}C, and offset current of 75nA over the full military temperature range while CMRR/PSRR is guaranteed greater than 94dB and A_{VOL} is guaranteed above 750kV/V from -55^{o}C to +125^{o}C.

Precision performance of the HA-5134 is enhanced by a noise voltage density of 7nV/$\sqrt{Hz}$ at 1kHz, noise current density of 2pA/$\sqrt{Hz}$ at 1kHz and channel separation of 120dB. Each unity-gain stable quad amplifier is fabricated using the dielectric isolation process to assure performance in the most demanding applications.

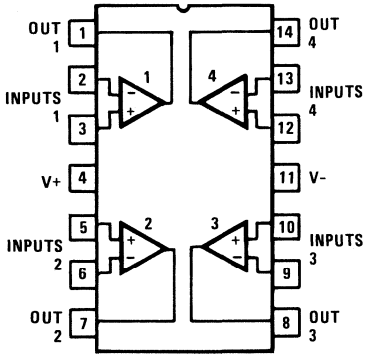
The HA-5134 is ideal for compact circuits such as instrumentation amplifiers, state-variable filters, and low-level transducer amplifiers. Other applications include precision data acquisition, precision integrators, and accurate threshold detectors in designs where board space is a limitation.

The HA-5134-2 has guaranteed operation from -55^{o}C to +125^{o}C and can be ordered as a military grade part. The HA-5134-5 is guaranteed from 0^{o}C to +75^{o}C and all devices are available in ceramic dual-in-line packages. For military grade product, refer to the HA-5134/883 Data Sheet.

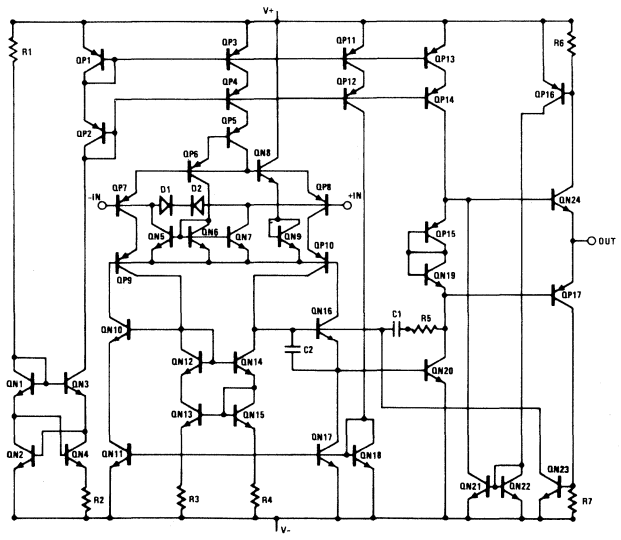
Pinout

HA1-5134 (CERAMIC DIP)

TOP VIEW



Schematic (Each Amplifier)



CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

T_A = +25°C Unless Otherwise Stated

Voltage Between V+ and V- Terminals 40.0V
Differential Input Voltage (Note 2) ..... ±6.0V
Internal Power Dissipation (Note 3) 800mW
Output Current ..... Full Short Circuit Protection
Voltage at any Op Amp Terminal ..... V+, V-
Maximum Junction Temperature ..... +175°C

Operating Temperature Ranges

HA-5134A/5134-2 ..... $-55°C \leq T_A \leq +125°C$
HA-5134A/5134-5 ..... $0°C \leq T_A \leq +75°C$
Storage Temperature Range ..... $-65°C \leq T_A \leq +150°C$

Electrical Specifications

V_{CC} = ±15V, R_{LOAD} = 2K, C_{LOAD} = 50pF, $R_S \leq 100\Omega$ Unless Otherwise Specified

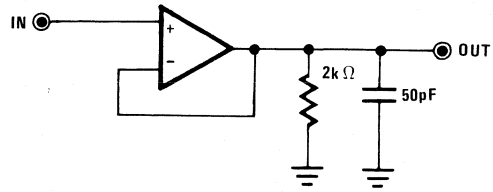
PARAMETER	TEMP	HA-5134A-2/-5 MIN	HA-5134A-2/-5 TYP	HA-5134A-2/-5 MAX	HA-5134-2/-5 MIN	HA-5134-2/-5 TYP	HA-5134-2/-5 MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C	—	50	100	—	50	200	μV
	Full	—	75	250	—	75	350	μV
Average Offset Voltage Drift	Full	—	0.3	1.2	—	0.3	2	μV/°C
Offset Voltage Match	Full	—	—	250	—	—	—	μV
Bias Current	+25°C	—	±10	±25	—	±10	±50	nA
	Full	—	±20	±50	—	±20	±75	nA
Offset Current	+25°C	—	10	25	—	10	50	nA
	Full	—	15	50	—	15	75	nA
Average Offset Current Drift	Full	—	0.05	—	—	0.05	—	nA/°C
Common Mode Range	Full	±10	—	—	±10	—	—	V
Differential Input Resistance	+25°C	—	30	—	—	30	—	MΩ
Input Noise Voltage (0.1Hz to 10Hz)	+25°C	—	0.2	—	—	0.2	—	μV_{p-p}
Input Noise Voltage Density	+25°C							$nV/\sqrt{Hz}$
f_0 = 10Hz		—	10	—	—	10	—	
f_0 = 100Hz		—	7.5	—	—	7.5	—	
f_0 = 1kHz		—	7	—	—	7	—	
Input Noise Current Density	+25°C							$pA/\sqrt{Hz}$
f_0 = 10Hz		—	3	—	—	3	—	
f_0 = 100Hz		—	1.5	—	—	1.5	—	
f_0 = 1kHz		—	1	—	—	1	—	
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain	+25°C	1500	3000	—	1200	3000	—	V/mV
(V_{OUT} = ±10V)	Full	1000	2000	—	750	2000	—	V/mV
Common Mode Rejection Ratio	+25°C	115	120	—	100	120	—	dB
(V_{CM} = ±10V)	Full	110	115	—	94	115	—	dB
Minimum Stable Gain	+25°C	1	—	—	1	—	—	V/V
Unity-Gain Bandwidth	+25°C	—	4	—	—	4	—	MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing	Full	12	13.5	—	12	13.5	—	V
Output Current	+25°C	—	20	—	—	20	—	mA
Full Power Bandwidth (Note 4)	+25°C	12	16	—	12	16	—	kHz
Channel Separation (V_{OUT} = ±10V)	+25°C	120	136	—	120	136	—	dB
TRANSIENT RESPONSE (Note 5)								
Rise Time (Note 6)	+25°C	—	200	400	—	200	400	ns
Slew Rate	+25°C	0.75	1.0	—	0.75	1.0	—	V/μs
Overshoot	+25°C	—	20	40	—	20	40	%
Settling Time (Note 7)	+25°C	—	13	—	—	13	—	μs
POWER SUPPLY CHARACTERISTICS								
Supply Current (All Amps)	Full	—	6.5	8	—	6.5	8	mA
Power Supply Rejection Ratio (Note 8)	+25°C	110	120	—	100	120	—	dB
	Full	100	115	—	94	115	—	dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For differential input voltages greater than 6V, the input current must be limited to 25mA to protect the back-to-back input diodes.
3. Derate at 10mW/°C for ambient temperatures greater than +95°C.
4. Full power bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{SLEW\ RATE}{2\pi V_{PEAK}}$; V_{peak} = 10V
5. Refer to Test Circuits section of the data sheet.
6. Time from 10% to 90% of 200mV output step, A_V = 1.
7. Specified to 0.01% of a 10V step, A_V = -1.
8. V_S = ±5V to ±18V.

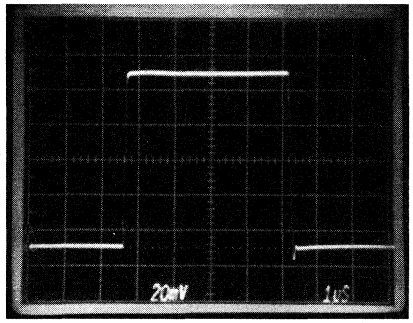
Test Circuits

SLEW RATE AND TRANSIENT RESPONSE TEST CIRCUIT



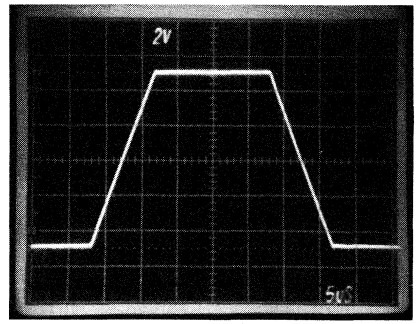
SMALL SIGNAL RESPONSE

Vertical: 20mV/Div.
Horizontal: 1μs/Div.
T_A = +25°C, V_{CC} = ±15V
A_V = +1, R_L = 2K, C_L = 50pF

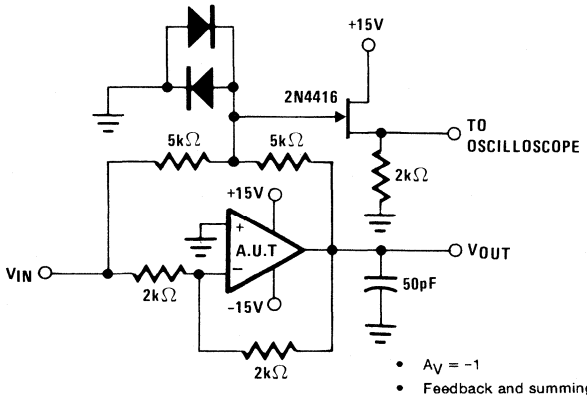


LARGE SIGNAL RESPONSE

Vertical: 2V/Div.
Horizontal: 5μs/Div.
T_A = +25°C, V_{CC} = ±15V
A_V = +1, R_L = 2K, C_L = 50pF



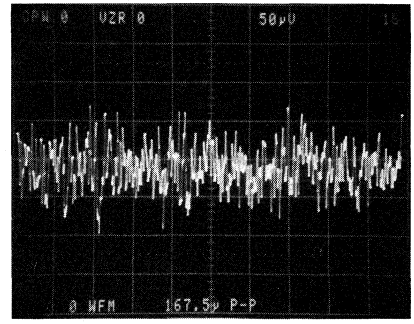
SETTLING TIME CIRCUIT



- A_V = -1
- Feedback and summing resistors should be 0.1% matched.
- Clipping diodes are optional. HP5082-2810 recommended.

PEAK-TO-PEAK NOISE 0.1Hz TO 10Hz

T_A = +25°C, V_{CC} = ±15V, A_V = 1000

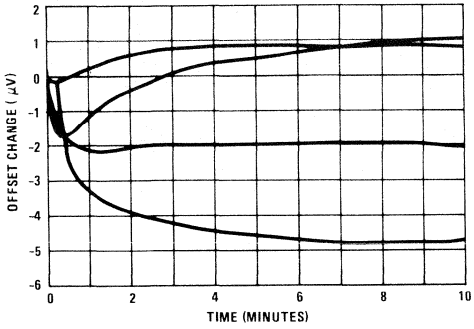


en_{p-p} = 0.167μV_{p-p}
0.05μV/Div., 1s/Div.

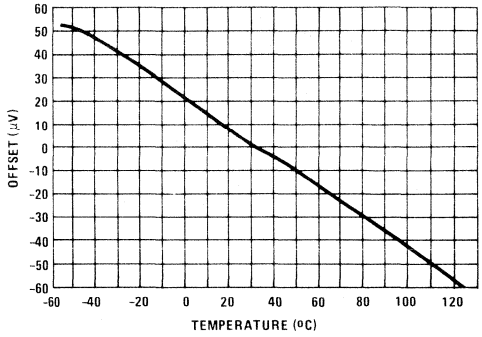
Performance Curves

V_{IO} WARMUP DRIFT

$T_A = +25^oC$, $V_{CC} = \pm15V$

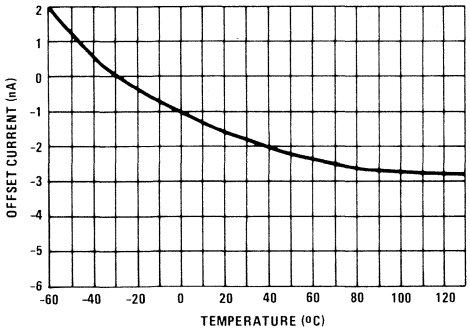


INPUT OFFSET VOLTAGE vs. TEMPERATURE

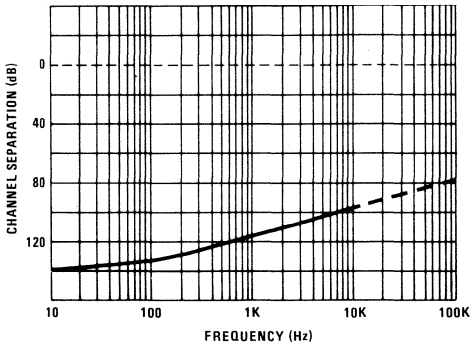


OFFSET CURRENT vs. TEMPERATURE

$A_{CL} = +1$, $V_{CC} = \pm15V$

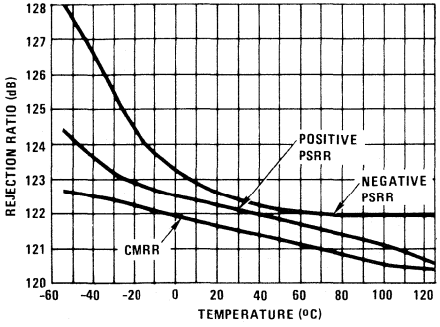


CHANNEL SEPARATION vs. FREQUENCY

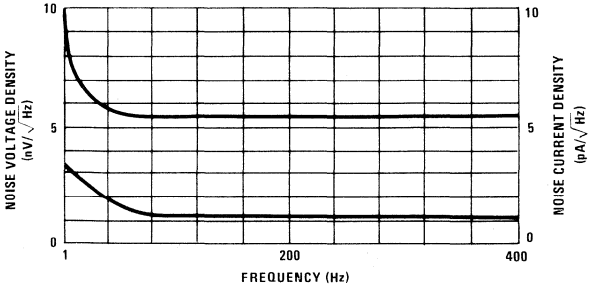


REJECTION RATIOS vs. TEMPERATURE

$V_{CC} = \pm5V$ to $\pm20V$, $V_{CM} = \pm10V$

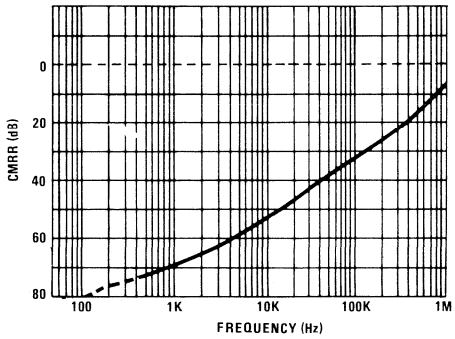


NOISE VOLTAGE DENSITY vs. FREQUENCY

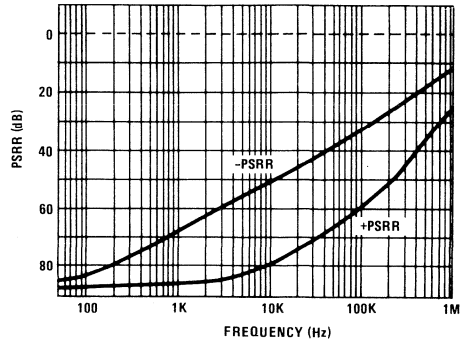


Performance Curves (Continued)

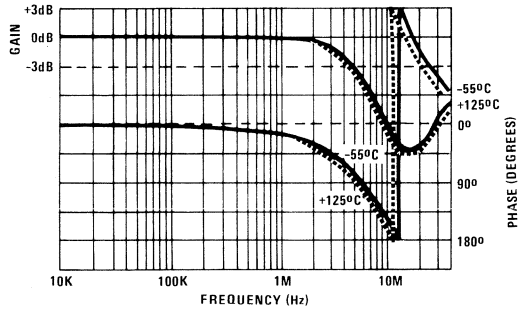
CMRR vs. FREQUENCY



PSRR vs. FREQUENCY

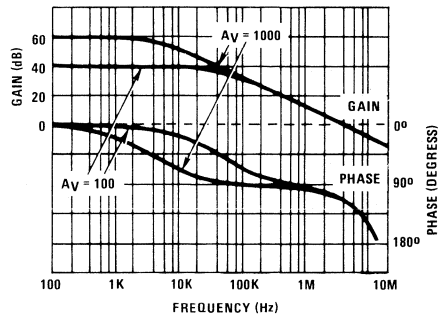


CLOSED-LOOP FREQUENCY RESPONSE vs. TEMPERATURE



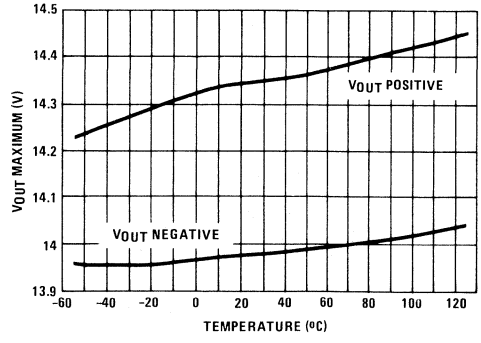
CLOSED-LOOP GAIN/PHASE vs. FREQUENCY

$T_A = +25^oC$, $V_{CC} = \pm 15V$



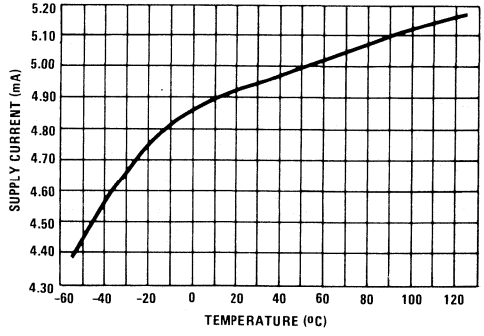
MAXIMUM OUTPUT VOLTAGE vs. TEMPERATURE

$R_{LOAD} = 2K$, $A_V = 1000$, $V_{IN} = \pm 2V$



SUPPLY CURRENT vs. TEMPERATURE

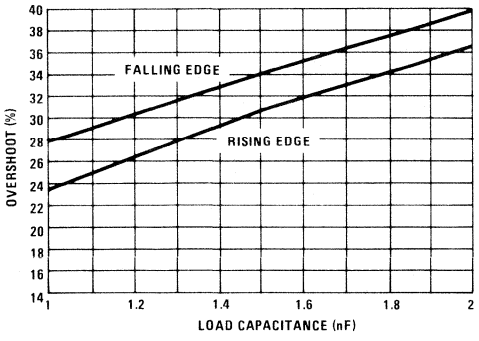
$V_{CC} = \pm 15V$



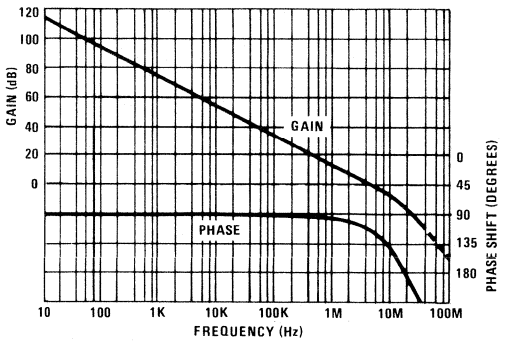
Performance Curves (Continued)

OVERSHOOT vs. C_{LOAD}

V_{CC} = ±15V, T_A = +25°C, A_V = 1, V_{OUT} = 200mV

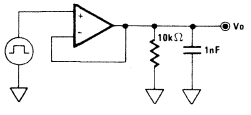


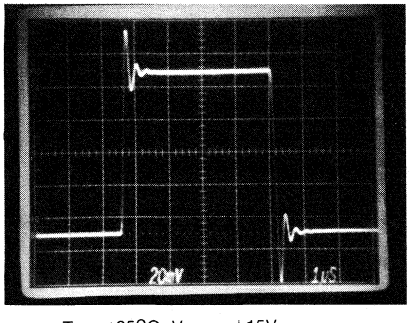
OPEN LOOP GAIN & PHASE vs. FREQUENCY



Applications Information

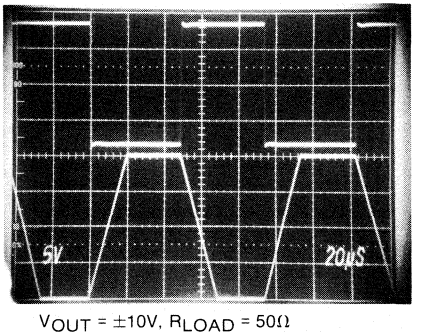
SMALL SIGNAL TRANSIENT RESPONSE
C_{LOAD} = 1nF





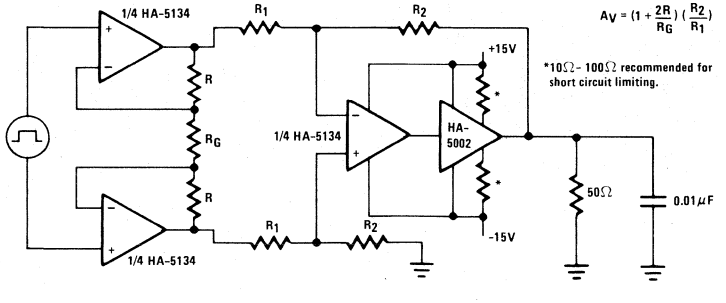
T_A = +25°C, V_{CC} = ±15V,
A_V = 1, R_L = 10K
20mV/Div, 1μs/Div.

TRANSIENT RESPONSE OF APPLICATION CIRCUIT #1



V_{OUT} = ±10V, R_{LOAD} = 50Ω
C_{LOAD} = 0.01μF, A_V = 3, V_{CC} = ±15V
Top: Input, 2V/Div., 20μs/Div
Bottom: Output, 5V/Div, 20μs/Div.

APPLICATION CIRCUIT #1:
INSTRUMENTATION AMPLIFIER WITH POWER OUTPUT

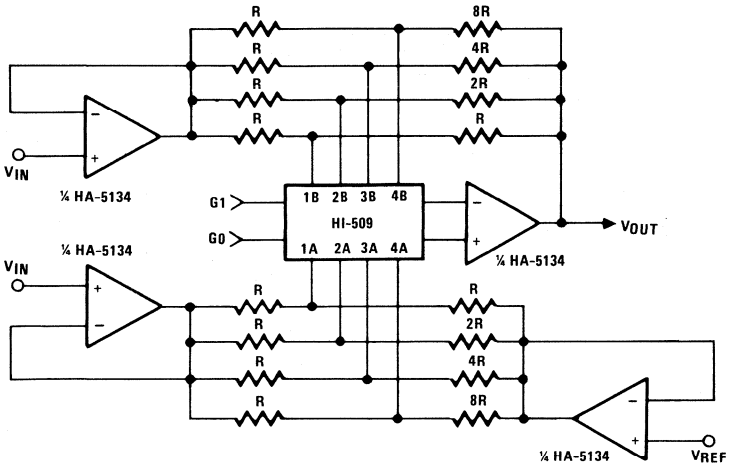


$A_V = (1 + \frac{2R}{R_G})(\frac{R_2}{R_1})$

NOTE: When driving heavy loads the HA-5002 may contribute to thermal errors. Proper thermal shielding is recommended.

Applications Information (Continued)

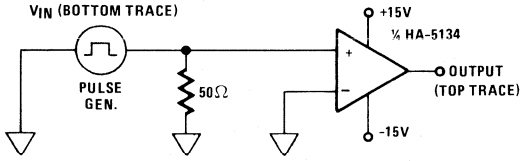
APPLICATION CIRCUIT #2:
PROGRAMMABLE GAIN AMPLIFIER

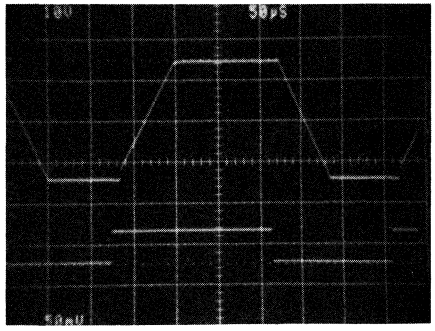


G_1	G_0	A_V
0	0	-1
0	1	-2
1	0	-4
1	1	-8

High A_{VOL} of HA-5134 reduces gain error.
Gain Error ≅ 0.004% @ A_V = 8

APPLICATION CIRCUIT #3:
PRECISION COMPARATOR





Horizontal: 50μs/Div
V_{IN} = ±25mV, V_{OUT} = ±14V

NOTE: If differential input voltages greater than 6V are present, input current must be limited to less than 25mA.

General Considerations

1. POWER SUPPLY DECOUPLING: Although not absolutely necessary, it is recommended that all power supply lines be decoupled with 0.01μF ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.

2. CONSIDERATIONS FOR PROTOTYPING: The following list of recommendations are suggested for prototyping.

   - Resolving low level signals requires minimizing leakage currents caused by external circuitry. Use of quality insulating materials, thorough cleaning of insulating surfaces and implementation of moisture barriers when required is suggested.

   - Error voltages generated by thermocouples formed between dissimilar metals in the presence of temperature gradients should be minimized. Isolation of low level circuitry from heat generating components is recommended.

   - Shielded cable input leads, guard rings and shield drivers are recommended for the most critical applications.

HA-5137

Ultra-Low Noise Precision Wideband Operational Amplifier

Features

- High Speed 20V/μs
- Wide Gain Bandwidth ($A_V \geq 5$) 63MHz
- Low Noise ..... 3nV/$\sqrt{Hz}$ at 1KHz
- Low V_{OS} 10μV
- High CMRR 126dB
- High Gain 1800V/mV

Applications

- High Speed Signal Conditioners
- Wide Bandwidth Instrumentation Amplifiers
- Low Level Transducer Amplifiers
- Fast, Low Level Voltage Comparators
- Highest Quality Audio Preamplifiers
- Pulse/RF Amplifiers
- For Further Design Ideas See App. Note 553

Description

The HA-5137 monolithic operational amplifier features an unparalleled combination of precision DC and wideband high speed characteristics. Utilizing the Harris D. I. technology and advanced processing techniques, this unique design unites low noise (3nV/$\sqrt{Hz}$) precision instrumentation performance with high speed (20V/μs) wideband capability.

This amplifier's impressive list of features include low V_{OS} (10μV), wide gain-bandwidth (63MHz), high open loop gain (1800V/mV), and high CMRR (126 dB). Additionally, this flexible device operates over a wide supply range ($\pm$5V to $\pm$20V) while consuming only 140mW of power.

Using the HA-5137 allows designers to minimize errors while maximizing speed and bandwidth in applications requiring gains greater than five.

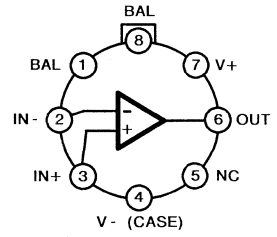
This device is ideally suited for low level transducer signal amplifier circuits. Other applications which can utilize the HA-5137's qualities include instrumentation amplifiers, pulse or RF amplifiers, audio preamplifiers, and signal conditioning circuits.

This device can easily be used as a design enhancement by directly replacing the 725, OP25, OP06, OP07, OP27 and OP37 where gains are greater than five. The HA-5137 is available in TO-99 Metal Can and Ceramic 8 pin Mini-DIPs. For the military grade product, refer to the HA-5137/883 data sheet.

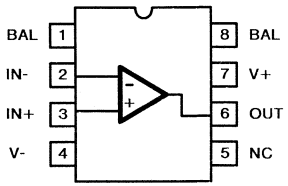
Pinouts

TOP VIEWS

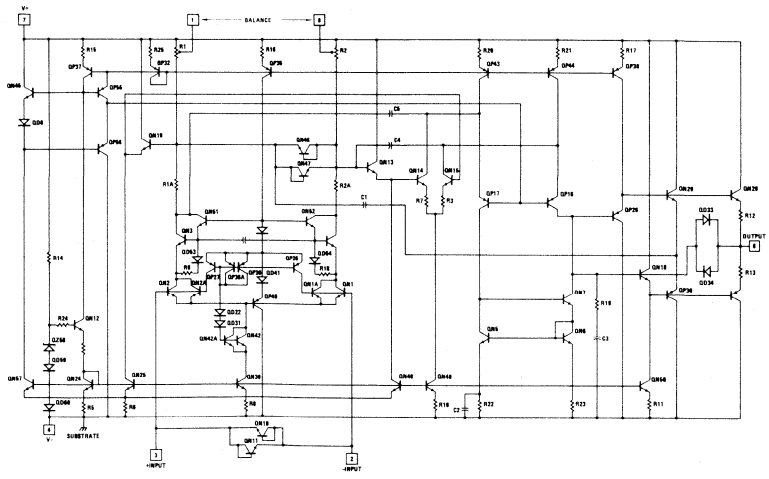
HA2-5137 (TO-99 METAL CAN)



HA7-5137 (CERAMIC MINI-DIP)



Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

T_A = +25°C Unless Otherwise Stated
Voltage Between V+ and V− Terminals ..... ±22V
Differential Input Voltage (Note 2) ..... ±0.7V
Internal Power Dissipation 500mW
Output Current ..... Full Short Circuit Protection

Operating Temperature Ranges

HA-5137/37A-2 ..... −55°C ≤ TA ≤ +125°C
HA-5137/37A-5 ..... 0°C ≤ TA ≤ +75°C
Storage Temperature Range ..... −65°C ≤ TA ≤ +150°C

Electrical Specifications

V+ = 15V, V− = −15V, $C_L \leq 50pF$, $R_S \leq 100\Omega$

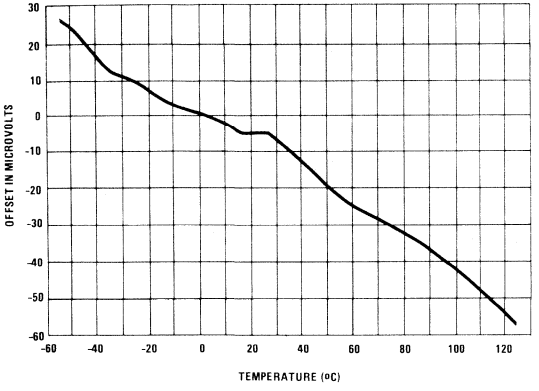
PARAMETER	TEMP	HA-5137A			HA-5137			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		10	25		30	100	μV
	Full		30	60		70	300	μV
Average Offset Voltage Drift	Full		0.2	0.6		0.4	1.8	μV/°C
Bias Current	+25°C		±10	±40		±15	±80	nA
	Full		±20	±60		±35	±150	nA
Offset Current	+25°C		7	35		12	75	nA
	Full		15	50		30	135	nA
Common Mode Range	Full	±10.3	±11.5		±10.3	±11.5		V
Differential Input Resistance (Note 3)	+25°C	1.5	6		0.8	4		MΩ
Input Noise Voltage 0.1Hz to 10Hz (Note 4)	+25°C		0.08	.18		0.09	0.25	μVp-p
Input Noise Voltage Density (Note 5)	+25°C							$nV/\sqrt{Hz}$
f_0 = 10 Hz			3.5	5.5		3.8	8.0	
f_0 = 30 Hz			3.1	4.5		3.3	5.6	
f_0 = 1000 Hz			3.0	3.8		3.2	4.5	
Input Noise Current Density (Note 5)	+25°C							$pA/\sqrt{Hz}$
f_0 = 10 Hz			1.7	4.0		1.7		
f_0 = 30 Hz			1.0	2.3		1.0		
f_0 = 1000 Hz			0.4	0.6		0.4	0.6	
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 6)	+25°C	1000	1800		700	1500		V/mV
	Full	600	1200		300	800		V/mV
Common Mode Rejection Ratio (Note 7)	Full	114	126		100	120		dB
Minimum Stable Gain	+25°C	5			5			V/V
Gain-Bandwidth-Product f_0 = 10KHz)	+25°C	60	80		60	80		MHz
f_0 = 1MHz	+25°C		63			63		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing R_L = 600Ω	+25°C	±10.0	±11.5		±10.0	±11.5		V
R_L = 2KΩ	Full	±11.7	±13.8		±11.4	±13.5		V
Full Power Bandwidth (Note 8)	+25°C	220	320		220	320		KHz
Output Resistance, Open Loop	+25°C		70			70		Ω
TRANSIENT RESPONSE (Note 9)								
Rise Time	+25°C			100			100	ns
Slew Rate (Note 11)	+25°C	14	20		14	20		V/μs
Settling Time (Note 10)	+25°C		1.0			1.0		μs
Overshoot	+25°C		20	40		20	40	%
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C		3.5			3.5		mA
	Full			4.0			4.0	mA
Power Supply Rejection Ratio (Note 12)	Full		2	4		16	51	μV/V

NOTES:

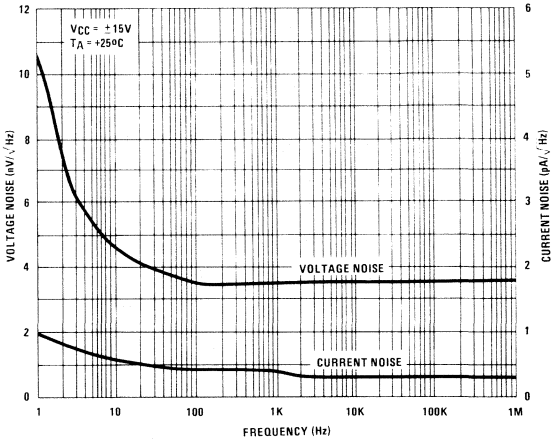
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For differential input voltages greater than 0.7V, the input current must be limited to 25mA to protect the back-to-back input diodes.
3. This parameter value is based upon design calculations.
4. Refer to Typical Performance section of the data sheet.
5. Sample tested.
6. $V_{OUT} = \pm 10V$, $R_L = 2K\Omega$
7. $V_{CM} = \pm 10V$
8. Full power bandwidth guaranteed based on slew rate measurement using: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$
9. Refer to Test Circuits section of the data sheet.
10. Settling time is specified to 0.1% of final value for a 10V output step and Av = -5.
11. V_{OUT} = 10V Step
12. $V_S = \pm 4V$ to $\pm 18V$

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm 15V$

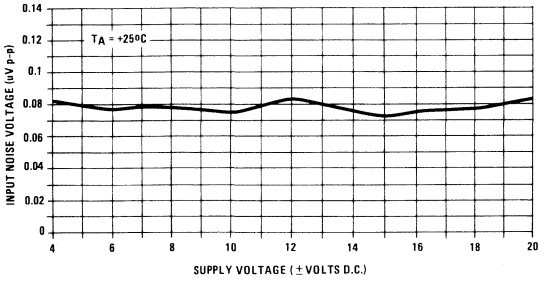
OFFSET VOLTAGE TYPICAL DRIFT vs. TEMPERATURE



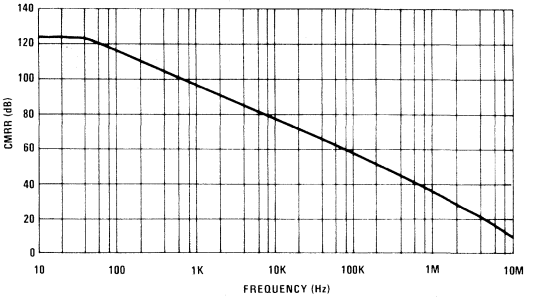
NOISE CHARACTERISTICS



NOISE vs. SUPPLY VOLTAGE

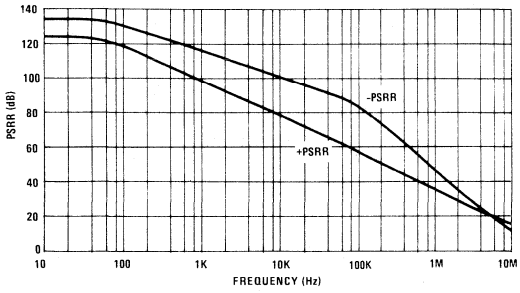


CMRR vs. FREQUENCY

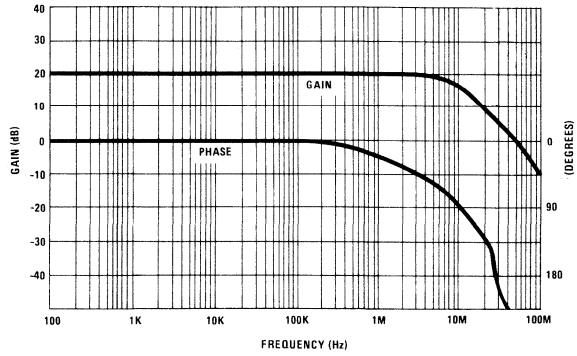


Typical Performance Curves Unless Otherwise Specified: T_A = +25°C, V_{SUPPLY} = ±15V

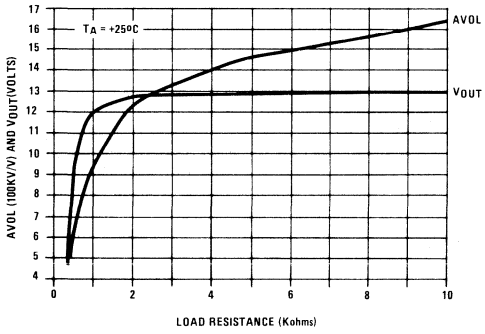
PSRR vs. FREQUENCY



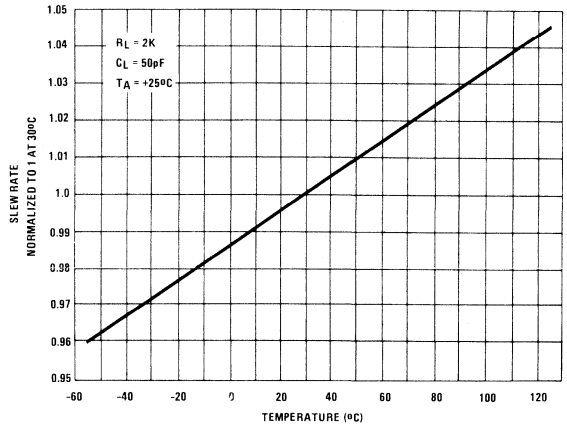
CLOSED LOOP GAIN AND PHASE vs. FREQUENCY



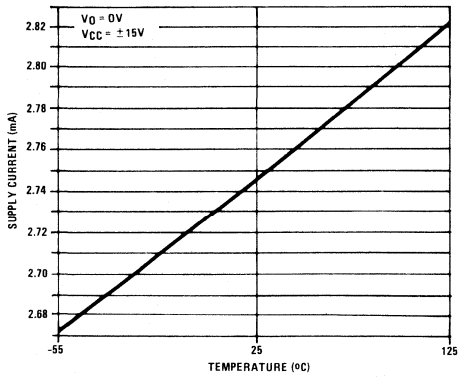
AVOL AND V_{OUT} vs. LOAD RESISTANCE



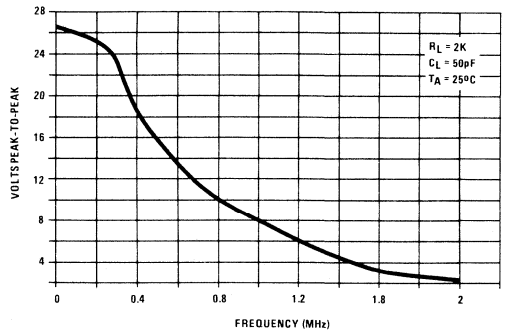
NORMALIZED SLEW RATE vs. TEMPERATURE



SUPPLY CURRENT vs. TEMPERATURE

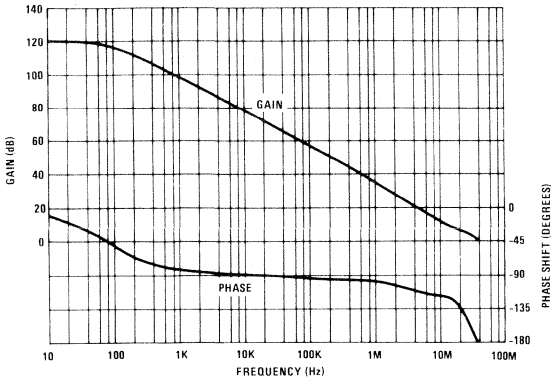


V_{OUT} MAX vs. FREQUENCY UNDISTORTED SINEWAVE OUTPUT

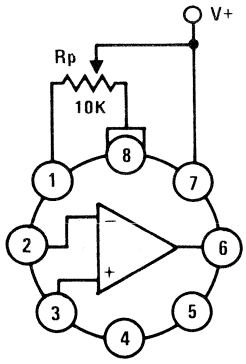


Typical Performance Curves Unless Otherwise Specified: T_A = +25°C, V_{SUPPLY} = ±15V

OPEN LOOP GAIN AND PHASE vs. FREQUENCY

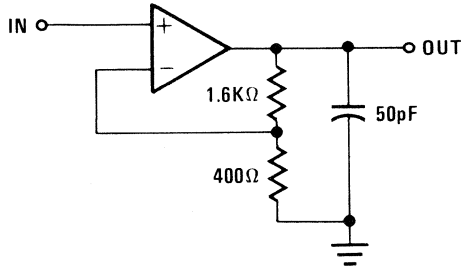


SUGGESTED OFFSET VOLTAGE ADJUSTMENT

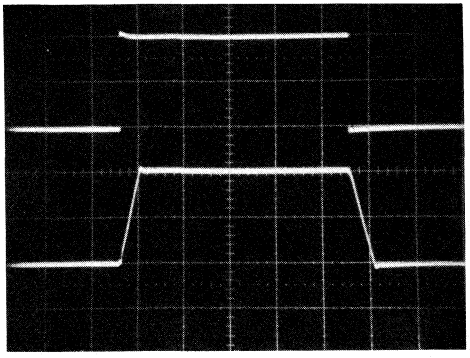


Tested Offset Adjustment Range is $|V_{OS} \pm 1mV|$ minimum referred to output. Typical range is ±4mV with R_P = 10kΩ.

LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT

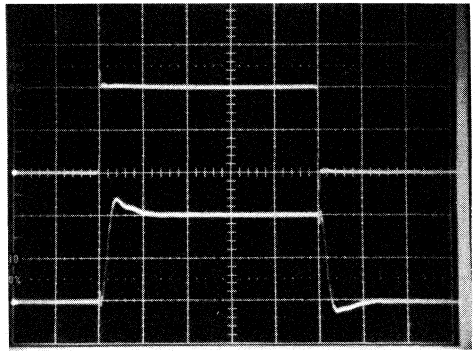


LARGE SIGNAL RESPONSE



Vertical Scale: (Volts: Input = 1V/Div.)
(Volts: Output = 5V/Div.)
Horizontal Scale: (Time = 1µs/Div.)

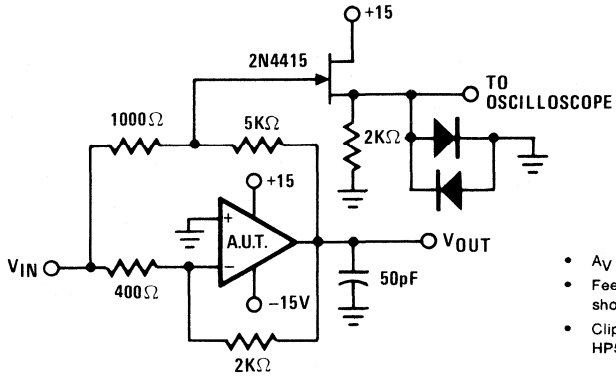
SMALL SIGNAL RESPONSE



Vertical Scale: (Volts: Input = 20mV/Div.)
(Volts: Output = 100mV/Div.)
Horizontal Scale: (Time = 100ns/Div.)

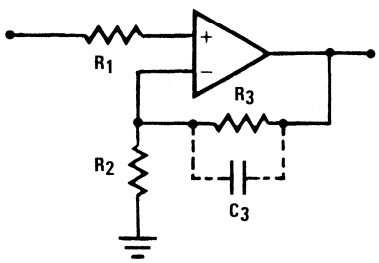
Typical Performance Curves Unless Otherwise Specified: T_A = +25°C, V_{SUPPLY} = ±15V

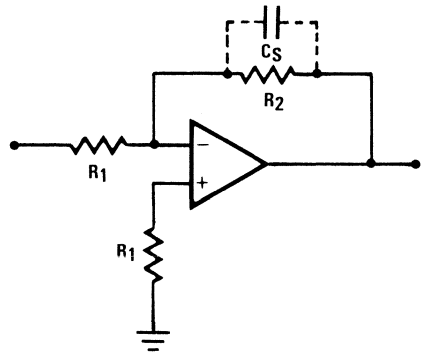
SETTLING TIME TEST CIRCUIT



- A_V = -5
- Feedback and summing resistors should be 0.1% matched.
- Clipping diodes are optional. HP5082-2810 recommended

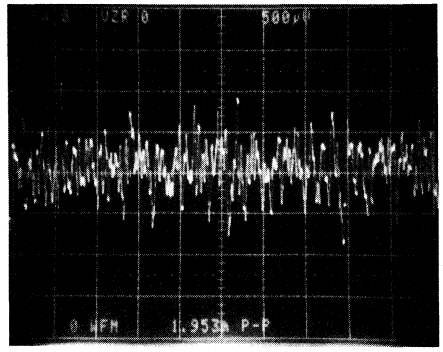
SUGGESTED STABILITY CIRCUITS





Low resistances are preferred for low noise applications as a 1KΩ resistor has 4nV/$\sqrt{Hz}$ of thermal noise. Total resistances of greater than 10KΩ on either input can reduce stability. In most high resistance applications, a few picofarads of capacitance across the feedback resistor will improve stability.

0.1Hz TO 10Hz NOISE WITH A_{CL} = 25,000V/V



Horizontal Scale = 1sec/Div.
Vertical Scale = 0.002μV/Div.
0.08μVp-p

Die Characteristics

Transistor Count 63
Die Dimensions ..... 65 x 104.3 x 19mils
(1700 x 2600 x 480μm)
Substrate Potential* ..... V-
Process ..... Bipolar-DI

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
HA7-5137, Ceramic Mini-DIP	160	79
HA2-5137, TO-99 Metal Can	172	48

*The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.

HARRIS

HA-5141/42/44

Single/Dual/Quad Ultra-Low Power Operational Amplifiers

Features

- Low Supply Current 45μA/Amp
- Wide Supply Voltage Range ..... Single 3V to 30V or Dual ±1.5V to ±15V
- High Slew Rate 1.5V/μs
- High Gain 100kV/V
- Unity Gain Stable
- Available in Singles, Duals and Quads

Applications

- Portable Instruments
- Meter Amplifiers
- Telephone Headsets
- Microphone Amplifiers
- Instrumentation
- For Further Design Ideas See App. Note 544

Description

The HA-5141/42/44 ultra-low power operational amplifiers provided AC and DC performance characteristics similar to or better than most general purpose amplifiers while only drawing 1/30 of the supply current of most general purpose amplifiers. In applications which require low power dissipation and good A.C. electrical characteristics, this family offers the industry's best speed/power ratio.

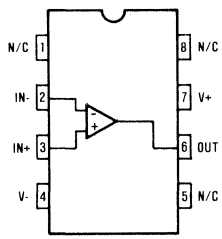
The HA-5141/42/44 provides accurate signal processing by virtue of their low input offset voltage (0.5mV), low input bias current (45nA), high open loop gain (100kV/V) and low noise, for low power operational amplifiers (20nV/$\sqrt{Hz}$). These characteristics coupled with a 1.5/μs slew rate and a 400kHz bandwidth make the HA-5141/42/44 ideal for use in low power instrumentation, audio amplifier and active filter designs. The wide range of supply voltages (3V to 30V) also allow these amplifiers to be very useful in low voltage battery powered equipment. These parts are also tested and guaranteed at both ±15V and single ended +5V supplies.

These amplifiers are available in singles (HA-5141, Can or Mini-DIP), duals (HA-5142, Can, Mini-DIP or 20 pin LCC) or quads (HA-5144, 14 pin DIP or 20 pin LCC) with industry standards pinouts which allow the HA-5141/5142/5144's to be interchangeable with most other operational amplifiers. For military grade product refer to the 5141, 5142, 5144/883 data sheet.

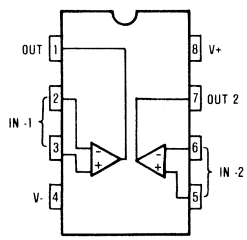
Pinouts

TOP VIEWS

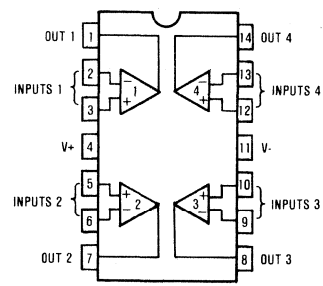
HA1-5141 (CERAMIC MINI-DIP)
HA3-5141 (PLASTIC MINI-DIP)



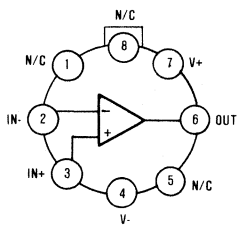
HA3-5142 (PLASTIC MINI-DIP)
HA7-5142 (CERAMIC MINI-DIP)



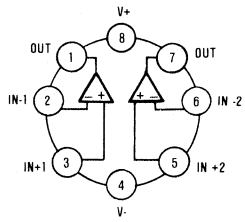
HA1-5144 (CERAMIC DIP)
HA3-5144 (PLASTIC DIP)



HA2-5141 (TO-99 METAL CAN)



HA2-5142 (TO-99 METAL CAN)



CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Terminals 35V
Differential Input Voltage ..... ±7V
Output Current ..... S/C Protected
Internal Power Dissipation 500mW

Operating Temperature Range

HA-5141/42/44-5 ..... $0^oC \leq T_A \leq +75^oC$
HA-5141/42/44-2 ..... $-55^oC \leq T_A \leq +125^oC$
Storage Temperature Range ..... $-65^oC \leq T_A \leq +150^oC$

Electrical Specifications

$R_S = 100\Omega$, $C_L \leq 10pF$ Unless Otherwise Specified.

PARAMETER	TEMP	V+ = +5V, V- = 0V			V+ = +15V, V- = -15V			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Offset Voltage (Note 11)	+25°C		2	6		2	6	mV
	Full			8			8	mV
Average Offset Voltage Drift	Full		3			3		µV/°C
Bias Current (Note 11)	+25°C		45	100		45	100	nA
	Full			125			125	nA
Offset Current (Note 11)	+25°C		0.3	10		0.3	10	nA
	Full			20			20	nA
Common Mode Range	Full	0 to 3			±10			V
Differential Input Resistance	+25°C		0.6			0.6		MΩ
Input Noise Voltage (f = 1kHz)	+25°C		20			20		$nV/\sqrt{Hz}$
Input Noise Current (f = 1kHz)	+25°C		0.25			0.25		$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Notes 2, 4)	+25°C	20k	100k		20k	100k		V/V
	Full	15k			15k			V/V
Common Mode Rejection Ratio (Note 7)	Full	77	105		77	105		dB
Bandwidth (Notes 2, 3)	+25°C		0.4			0.4		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Notes 2, 10)	+25°C	1.0 to 3.8	0.7 to 4.2		±10	±13		V
	Full	1.2 to 3.5	0.9 to 4.0		±10	±13		V
Full Power Bandwidth (Notes 2, 4, 8)	+25°C		240			24		kHz
TRANSIENT RESPONSE (Notes 2, 3)								
Rise Time	+25°C		600			600		ns
Slew Rate (Note 6)	+25°C	0.8	1.5		0.8	1.5		V/µs
Settling Time (Note 5)	+25°C		10			10		µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C		45	80		100	150	µA/Amp
	Full			100			200	µA/Amp
Power Supply Rejection Ratio (Note 9)	Full	77	105		77	105		dB

NOTES:

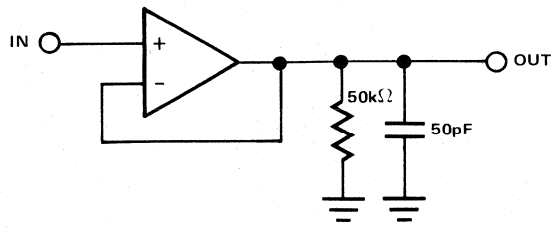
1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. $R_L = 50k\Omega$
3. $C_L = 50pF$
4. $V_O = 1.4$ to 2.5V for $V_{CC} = +5, 0V$; $V_O = \pm 10V$ for $V_{CC} = \pm 15V$.
5. Settling Time is specified to 0.1% of final value for a 3V output step and $A_V = -1$ for $V_{CC} = +5V, 0V$. Output step = 10V for $V_{CC} = \pm 15V$.
6. Maximum input slew rate = 10V/µs.
7. $V_{CM} = 0$ to 3V for $V_{CC} = +5, 0V$; $V_{CM} = \pm 10V$ for $V_{CC} = \pm 15V$
8. Full Power Bandwidth is guaranteed by equation:

$$\text{Full Power Bandwidth} = \frac{\text{Slew Rate}}{2\pi \text{ V Peak}}$$

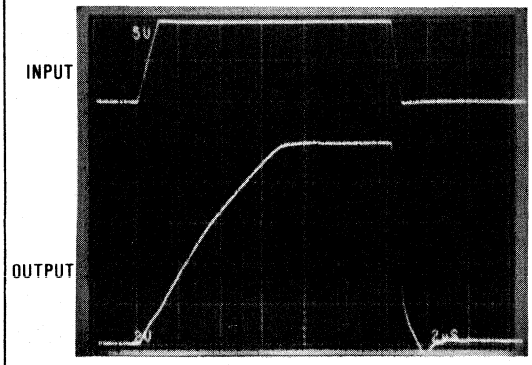
9. $\Delta V_S = +10V$ for $V_{CC} = +5, 0V$; $\Delta V_S = \pm 5V$ for $V_{CC} = \pm 15V$.
10. For $V_{CC} = +5, 0V$ terminate R_L at +2.5V. Typical output current is ±3mA.
11. $V_O = 1.4V$ for $V_{CC} = +5V, 0V$.

Test Circuits

SLEW RATE AND TRANSIENT RESPONSE TEST CIRCUIT

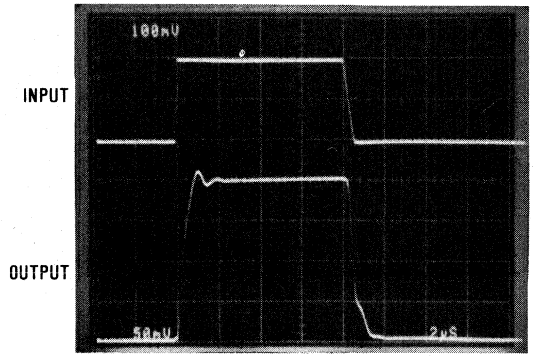


LARGE SIGNAL RESPONSE
Vertical Scale: (Volts: Input = 5V/Div.; Output = 2V/Div.)
Horizontal Scale: (Time: 2µs/Div.)



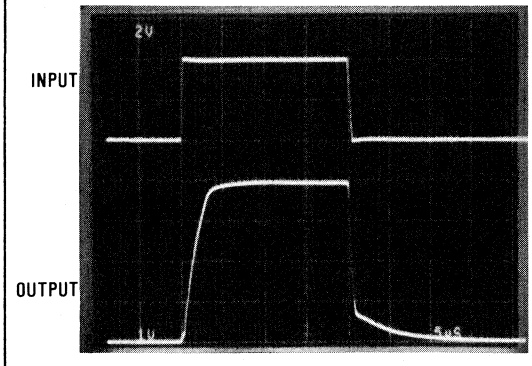
$+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V

SMALL SIGNAL RESPONSE
Vertical Scale: (Volts: Input = 100mV/Div.; Output = 50mV/Div.)
Horizontal Scale: (Time: 2µs/Div.)



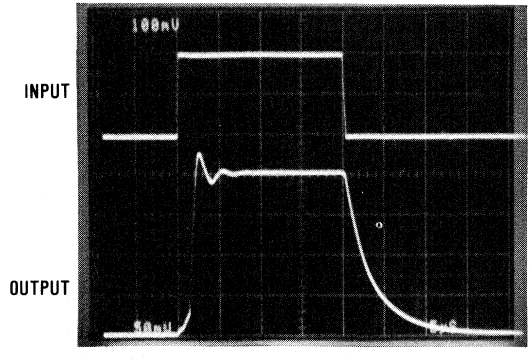
$+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V

LARGE SIGNAL RESPONSE
Vertical Scale: (Volts: Input = 2V/Div.; Output = 1V/Div.)
Horizontal Scale: (Time: 5µs/Div.)



$+V_{SUPPLY}$ = +5V, $-V_{SUPPLY}$ = 0V

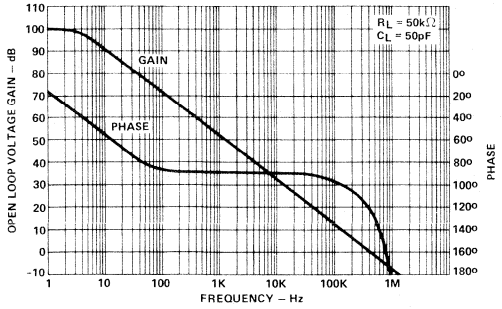
SMALL SIGNAL RESPONSE
Vertical Scale: (Volts: Input = 100mV/Div.; Output = 50mV/Div.)
Horizontal Scale: (Time: 5µs/Div.)



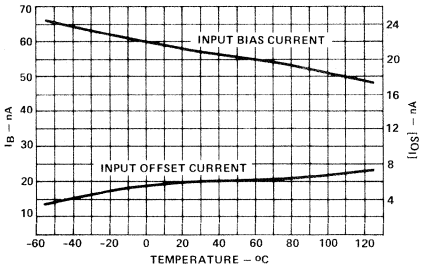
$+V_{SUPPLY}$ = +5V, $-V_{SUPPLY}$ = 0V

Performance Curves $V_S = \pm 2.5V$, $T_A = +25^oC$ Unless Otherwise Specified

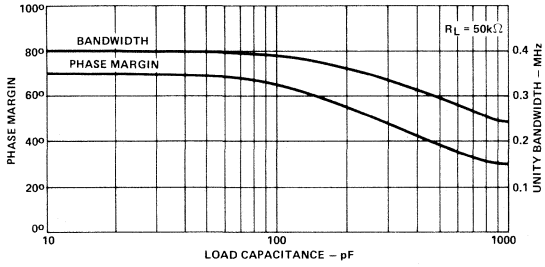
OPEN LOOP FREQUENCY RESPONSE



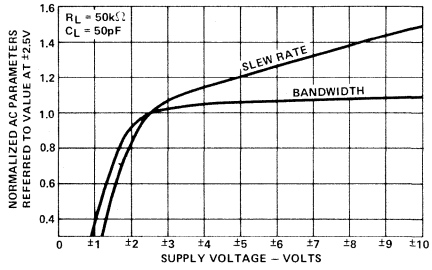
INPUT OFFSET CURRENT AND BIAS CURRENT vs. TEMPERATURE



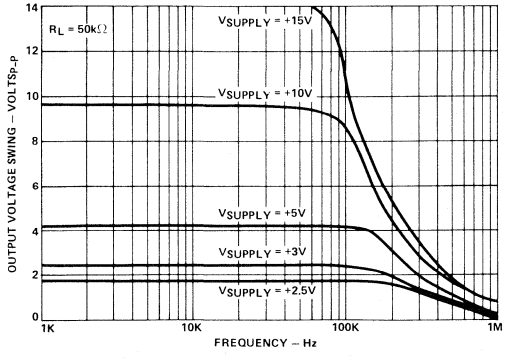
BANDWIDTH AND PHASE MARGIN vs. LOAD CAPACITANCE



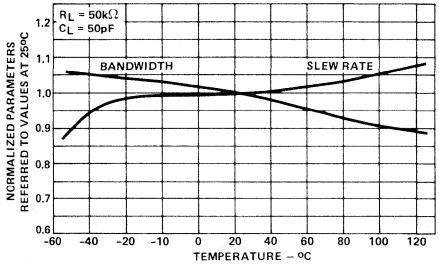
NORMALIZED AC PARAMETERS vs. SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING vs. FREQUENCY AND SINGLE SUPPLY VOLTAGE



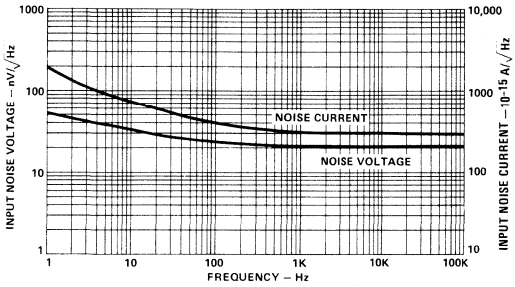
NORMALIZED AC PARAMETERS vs. TEMPERATURE



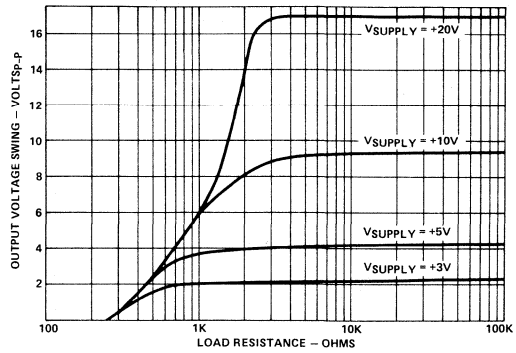
Performance Curves Continued

$V_S = \pm 2.5V$, $T_A = +25^oC$ Unless Otherwise Specified

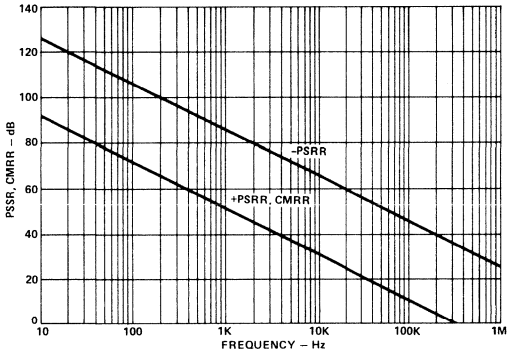
INPUT NOISE vs. FREQUENCY



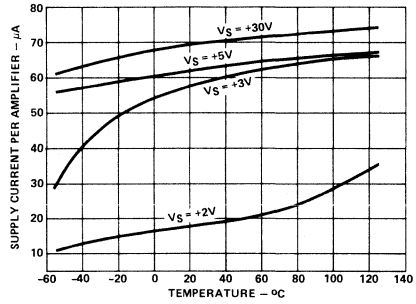
MAXIMUM OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE AND SINGLE SUPPLY VOLTAGE



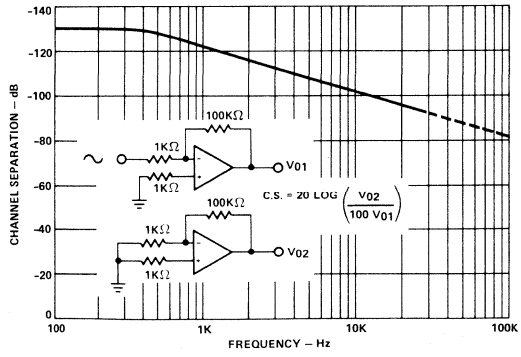
PSRR AND CMRR vs. FREQUENCY



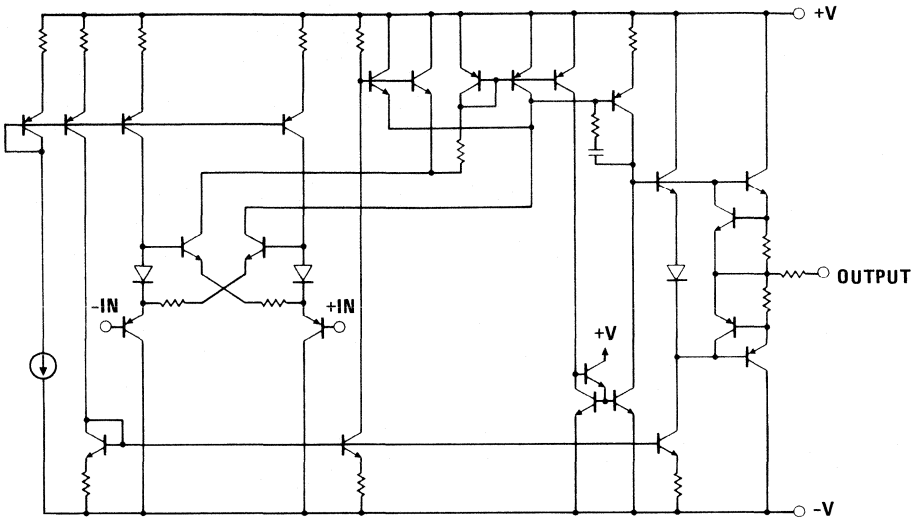
POWER SUPPLY CURRENT vs. TEMPERATURE AND SINGLE SUPPLY VOLTAGE



CHANNEL SEPARATION vs. FREQUENCY



Schematic



Die Characteristics

Transistor Count

HA-5141	33
HA-5142	66
HA-5144	132

Substrate Potential* ..... V-

Process ..... Bipolar-DI

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
HA1-5144 (-2, -5, -7)	101	33
HA1-5144 (/883)	75	22
HA2-5141 (-2, -5, -7)	206	56
HA2-5141 (/883)	168	50
HA2-5142 (-2, -5, -7)	184	50
HA2-5142 (/883)	143	43
HA3-5141 (-5)	90	40
HA3-5142 (-5)	80	20
HA3-5144 (-5)	75	20
HA7-5141 (-2, -5, -7)	210	117
HA7-5141 (/883)	90	40
HA7-5142 (-2, -5, -7)	177	92
HA7-5142 (/883)	80	20

*The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.

NOTE: Consult Harris for LCC/PLCC information.

HARRIS

HA-5147

Ultra-Low Noise Precision High Slew Rate Wideband Operational Amplifier

Features

- High Speed 35V/μs
- Wide Gain Bandwidth ($A_V \geq 10$) ..... 120 MHz
- Low Noise ..... 3 nV/$\sqrt{Hz}$ at 1 KHz
- Low V_{OS} 10μV
- High CMRR ..... 126 dB
- High Gain 1800V/mV

Applications

- High Speed Signal Conditioners
- Wide Bandwidth Instrumentation Amplifiers
- Low Level Transducer Amplifiers
- Fast, Low Level Voltage Comparators
- Highest Quality Audio Preamplifiers
- Pulse/RF Amplifiers

Description

The HA-5147 monolithic operational amplifier features an unparalleled combination of precision DC and wideband high speed characteristics. Utilizing the Harris D. I. technology and advanced processing techniques, this unique design unites low noise (3 nV/$\sqrt{Hz}$) precision instrumentation performance with high speed (35V/μs) wideband capability.

This amplifier's impressive list of features include low V_{OS} (10 μV), wide gain-bandwidth (120 MHz), high open loop gain (1800V/mV), and high CMRR (126 dB). Additionally, this flexible device operates over a wide supply range (±5V to ±20V) while consuming only 140 mW of power.

Using the HA-5147 allows designers to minimize errors while maximizing speed and bandwidth in applications requiring gains greater than ten.

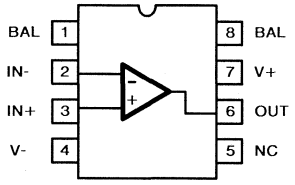
This device is ideally suited for low level transducer signal amplifier circuits. Other applications which can utilize the HA-5147's qualities include instrumentation amplifiers, pulse or RF amplifiers, audio preamplifiers, and signal conditioning circuits. Further application ideas are given in Application Note 553.

This device can easily be used as a design enhancement by directly replacing the 725, OP25, OP06, OP07, OP27 and OP37 where gains are greater than ten. The HA-5147 is available in TO-99 Metal Can and Ceramic 8 pin Mini-DIPs. For military grade product, refer to the HA-5147/883 data sheet.

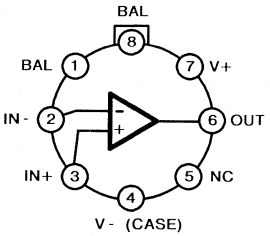
Pinouts

TOP VIEWS

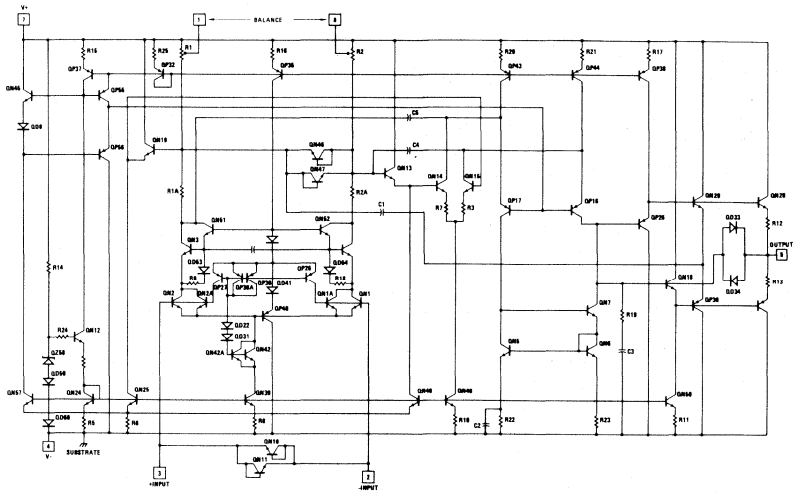
HA7-5147 (CERAMIC MINI-DIP)



HA2-5147 (TO-99 METAL CAN)



Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

T_A = +25°C Unless Otherwise Stated
Voltage Between V+ and V− Terminals ..... ±22V
Differential Input Voltage (Note 2) ..... ±0.7V
Internal Power Dissipation ..... 500 mW
Output Current ..... Full Short Circuit Protection

Operating Temperature Ranges:

HA-5147/47A-2 ..... −55°C ≤ TA ≤ +125°C
HA-5147/47A-5 ..... 0°C ≤ TA ≤ +75°C
Storage Temperature Range ..... −65°C ≤ TA ≤ +150°C

Electrical Specifications V+ = 15V, V− = −15V, $C_L \leq 50pF$, $R_S \leq 100\Omega$

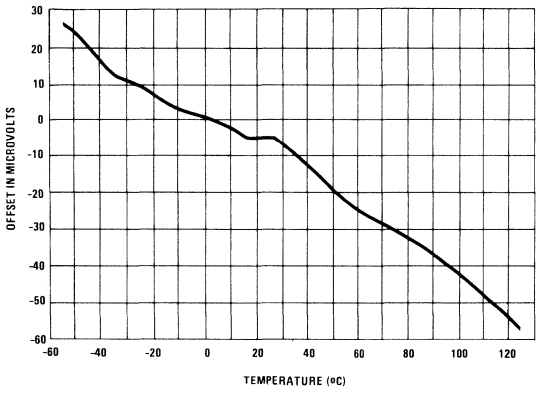
PARAMETER	TEMP	HA-5147A MIN	HA-5147A TYP	HA-5147A MAX	HA-5147 MIN	HA-5147 TYP	HA-5147 MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		10	25		30	100	μV
	Full		30	60		70	300	μV
Average Offset Voltage Drift	Full		0.2	0.6		0.4	1.8	μV/°C
Bias Current	+25°C		±10	±40		±15	±80	nA
	Full		±20	±60		±35	±150	nA
Offset Current	+25°C		7	35		12	75	nA
	Full		15	50		30	135	nA
Common Mode Range	Full	±10.3	±11.5		±10.3	±11.5		V
Differential Input Resistance (Note 3)	+25°C	1.5	6		0.8	4		MΩ
Input Noise Voltage 0.1 Hz to 10 Hz (Note 4)	+25°C		0.08	.18		0.09	0.25	$\mu Vp\text{-}p$
Input Noise Voltage Density (Note 5)	+25°C							$nV/\sqrt{Hz}$
f_0 = 10 Hz			3.5	5.5		3.8	8.0	
f_0 = 30 Hz			3.1	4.5		3.3	5.6	
f_0 = 1000 Hz			3.0	3.8		3.2	4.5	
Input Noise Current Density (Note 5)	+25°C							$pA/\sqrt{Hz}$
f_0 = 10 Hz			1.7	4.0		1.7		
f_0 = 30 Hz			1.0	2.3		1.0		
f_0 = 1000 Hz			0.4	0.6		0.4	0.6	
TRANSFER CHARACTERISTICS								
Minimum Stable Gain	+25°C	10			10			V/V
Large Signal Voltage Gain (Note 6)	+25°C	1000	1800		700	1500		V/mV
	Full	600	1200		300	800		V/mV
Common Mode Rejection Ratio (Note 7)	Full	114	126		100	120		dB
Gain-Bandwidth-Product f_0 = 10 KHz	+25°C	120	140		120	140		MHz
f_0 = 1 MHz	+25°C		120			120		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing R_L = 600 Ω	+25°C	±10.0	±11.5		±10.0	±11.5		V
R_L = 2K Ω	Full	±11.7	±13.8		±11.4	±13.5		V
Full Power Bandwidth (Note 8)	+25°C	445	500		445	500		KHz
Output Resistance, Open Loop	+25°C		70			70		Ω
TRANSIENT RESPONSE (Note 9)								
Rise Time	+25°C		22	50		22	50	ns
Slew Rate (Note 11)	+25°C	28	35		28	35		V/μs
Settling Time (Note 10)	+25°C		400			400		ns
Overshoot	+25°C		20	40		20	40	%
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C		3.5			3.5		mA
	Full			4.0			4.0	mA
Power Supply Rejection Ratio (Note 12)	Full		2	4		16	51	μV/V

NOTES:

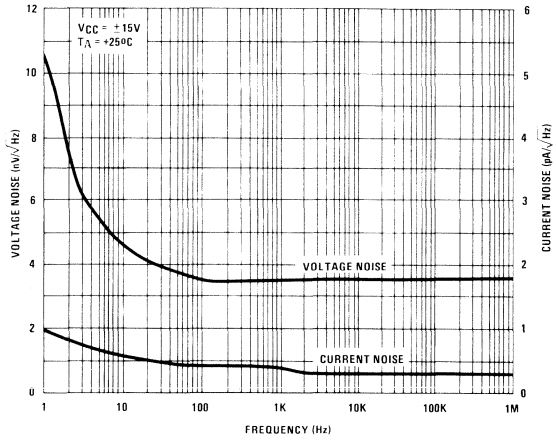
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For differential input voltages greater than 0.7V, the input current must be limited to 25 mA to protect the back-to-back input diodes.
3. This parameter value is based upon design calculations.
4. Refer to Typical Performance section of the data sheet.
5. Sample tested.
6. $V_{OUT} = \pm 10V$, $R_L = 2K\ \Omega$
7. $V_{CM} = \pm 10V$
8. Full power bandwidth guaranteed based on slew rate measurement using: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$
9. Refer to Test Circuits section of the data sheet.
10. Settling time is specified to 0.1% of final value for a 10V output step and Av = −10.
11. $V_{OUT} = 10V$ Step
12. $V_S = \pm 4V$ to $\pm 18V$

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm 15V$

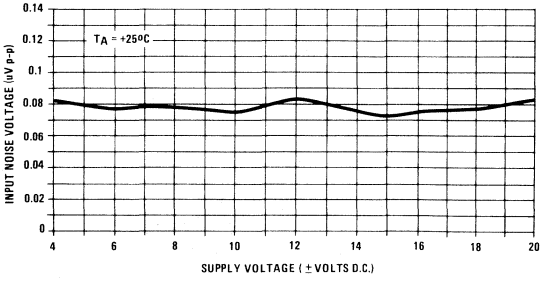
OFFSET VOLTAGE TYPICAL DRIFT vs. TEMPERATURE



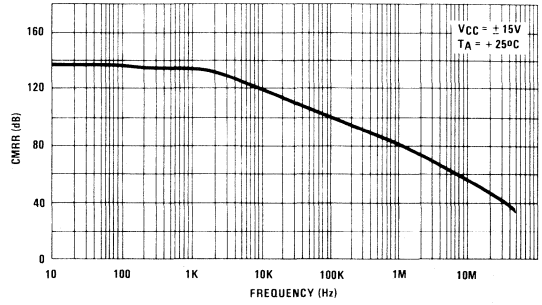
NOISE CHARACTERISTICS



NOISE vs. SUPPLY VOLTAGE

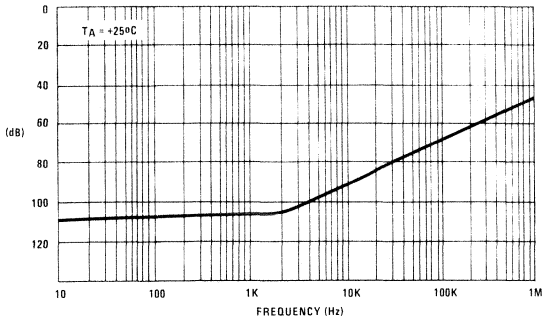


CMRR vs. FREQUENCY

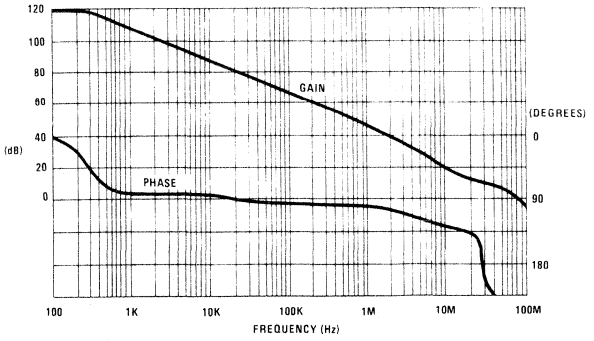


Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm 15V$

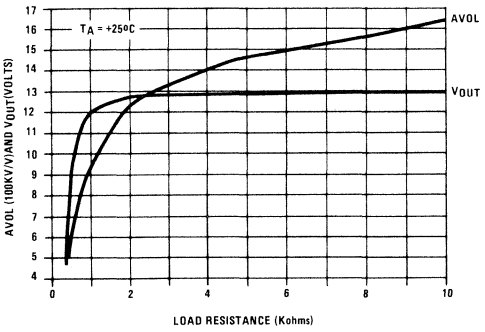
PSRR vs. FREQUENCY



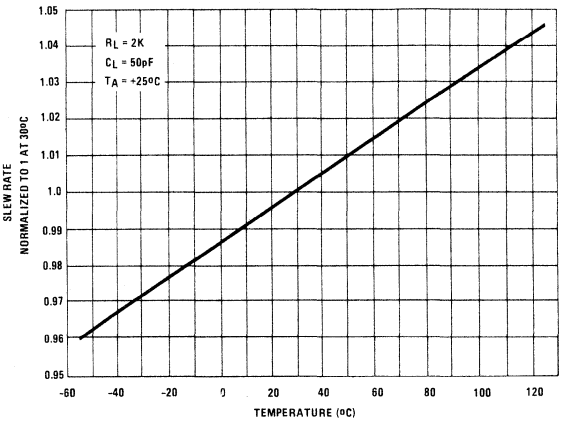
OPEN LOOP GAIN AND PHASE vs. FREQUENCY



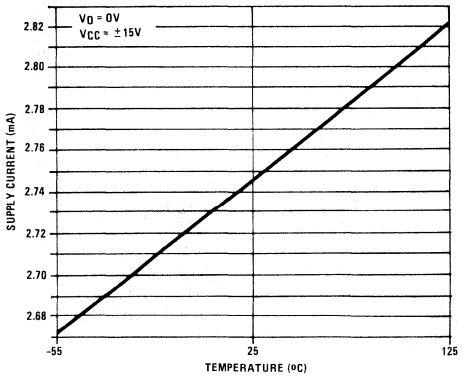
AVOL AND V_{OUT} vs. LOAD RESISTANCE



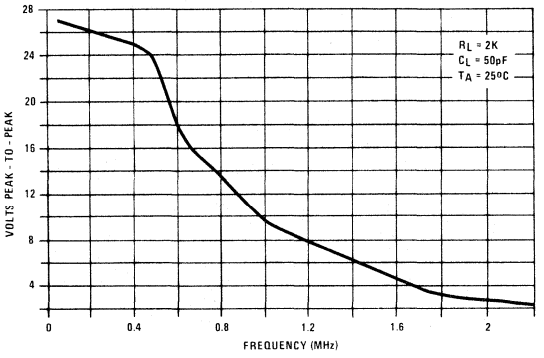
NORMALIZED SLEW RATE vs. TEMPERATURE



SUPPLY CURRENT vs. TEMPERATURE

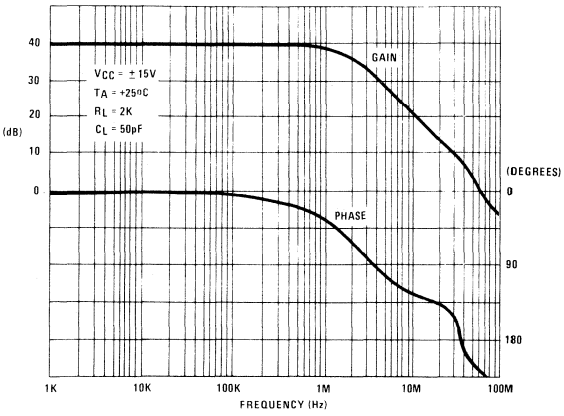


V_{OUT} MAX vs. FREQUENCY UNDISTORTED SINEWAVE OUTPUT

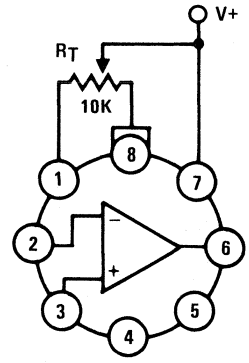


Typical Performance Curves Unless Otherwise Specified: T_A = +25°C, V_{SUPPLY} = ±15V

CLOSED LOOP GAIN AND PHASE vs. FREQUENCY

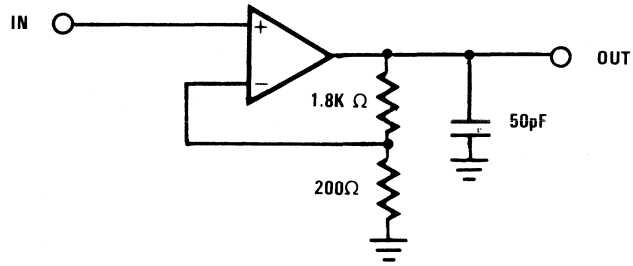


SUGGESTED OFFSET VOLTAGE ADJUSTMENT

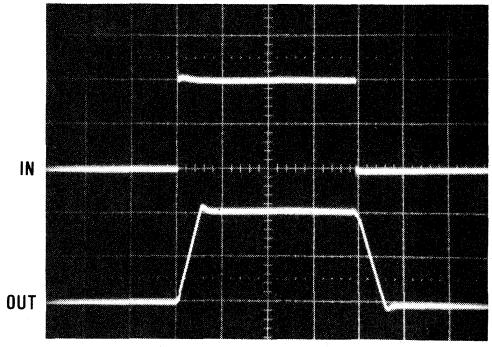


Tested Offset Adjustment Range is $|V_{OS} \pm 1mV|$ minimum referred to output. Typical range is ±4mV with R_T = 10kΩ.

LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT

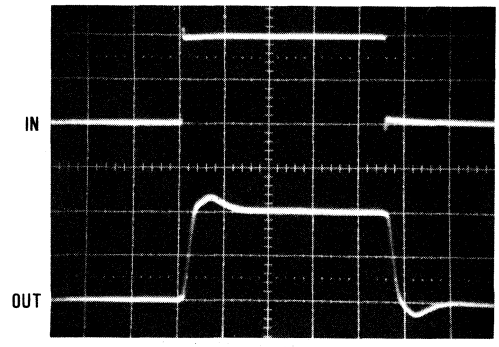


LARGE SIGNAL RESPONSE



Vertical Scale: (Volts: Input = 0.5V/Div.)
(Volts: Output = 5V/Div.)
Horizontal Scale: (Time: 500ns/Div)

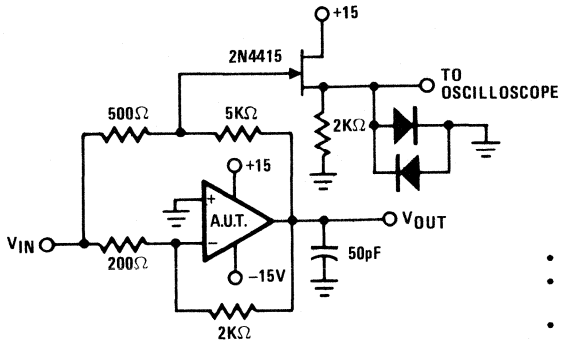
SMALL SIGNAL RESPONSE



Vertical Scale: (Volts: Input = 10mV/Div)
(Volts: Output = 100mV/Div)
Horizontal Scale: (Time: 100ns/Div)

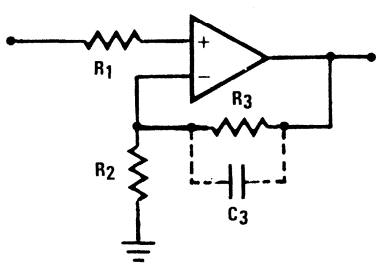
Typical Performance Curves Unless Otherwise Specified: T_A = +25°C, V_{SUPPLY} = ±15V

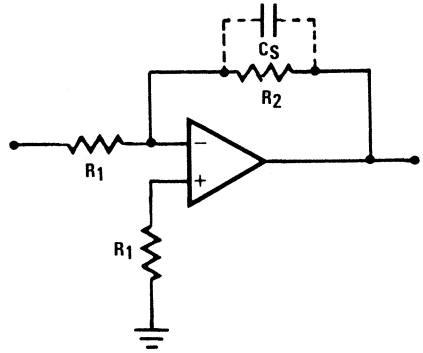
SETTLING TIME TEST CIRCUIT



- A_V = -10
- Feedback and summing resistors should be 0.1% matched.
- Clipping diodes are optional. HP5082-2810 recommended

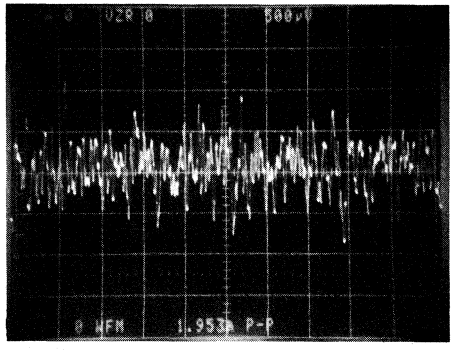
SUGGESTED STABILITY CIRCUITS





Low resistances are preferred for low noise applications as a 1KΩ resistor has 4nV/$\sqrt{\text{Hz}}$ of thermal noise. Total resistances of greater than 10KΩ on either input can reduce stability. In most high resistance applications, a few picofarads of capacitance across the feedback resistor will improve stability.

0.1Hz TO 10Hz NOISE WITH A_{CL} = 25,000V/V



Horizontal Scale = 1sec/Div.
Vertical Scale = 0.002μV/Div.
0.08μVp-p

Die Characteristics

Transistor Count		63
Die Dimensions		65 x 104.3 x 19mils
Substrate Potential*		V-
Process		Bipolar-DI
Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
HA7-5147, Ceramic Mini-DIP	160	79
HA2-5147, TO-99 Metal Can	172	48

*The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.

HARRIS

HA-5151/52/54

Single/Dual/Quad Low Power Operational Amplifiers

Features

- Low Supply Current ..... < 200μA/Amplifier
- Dual Supply Voltage Range ..... ±1.5V to ±15V
- Single Supply Voltage Range ..... 3V to 30V
- High Slew Rate 6V/μs
- Low V_{OS} Drift ..... 3μV/°C
- Low Noise ..... 15nV/$\sqrt{Hz}$
- Dielectric Isolation

Applications

- Portable Instruments
- Meter Amplifiers
- Telephone Headsets
- Microphone Amplifiers
- Remote Sensor/Transmitter
- Battery Powered Equipment
- For Further Design Ideas See App. Note 544.

Description

The HA-5151/52/54 series is a group of dielectrically isolated bipolar amplifiers designed to provide excellent AC performance while drawing less than 200μA of supply current per amplifier. These unity gain stable amplifiers are especially well suited for portable and lightweight equipment where available power is limited.

The HA-5151/52/54 series combines superior low power AC performance with DC precision not usually found in general purpose amplifiers. The DC performance is centered around low input offset voltage (0.5mV), low offset voltage drift (3μV/°C), and low input bias current (70nA). This is combined with a very low input noise voltage of 15nV/$\sqrt{Hz}$ at 1kHz.

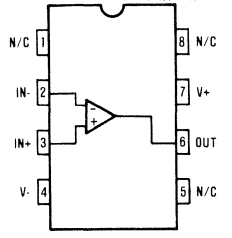
The AC performance of the HA-5151/52/54 series surpasses that of typical low power amplifiers with 6V/μs slew rate and a full power bandwidth of 95kHZ. This makes the HA-5151/52/54 series an excellent choice for virtually all audio processing applications as well as remote sensor/transmitter designs requiring both low power and high speed. The suitability of the HA-5151/52/54 series for remote and low power operation is further enchaced by the wide range of supply voltages (±1.5V to ±15V) as well as single supply operation (3V to 30V). These parts are also tested and guaranteed at both ±15 and single ended +5V supplies.

These amplifiers are available in singles (HA-5151, Can or Mini-DIP), duals (HA-5152, Can or Mini-DIP) or quads (HA-5154, 14 pin DIP), as well as over both the commercial (0°C to +75°C) and military (-55°C to +125°C) temperature ranges. These amplifiers also carry industry standard pinouts which allow the HA-5151/52/54's to be interchangeable with most other operational amplifiers. For military grade product refer to the HA-5151, 5152, 5154/883 data sheets.

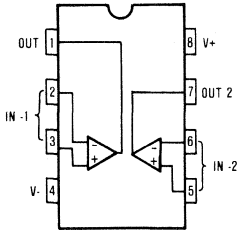
Pinouts

TOP VIEWS

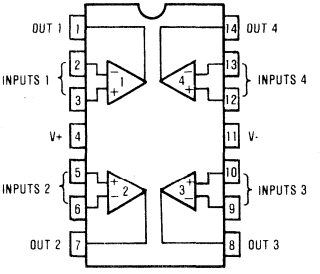
HA3-5151 (PLASTIC MINI-DIP)
HA7-5151 (CERAMIC MINI-DIP)



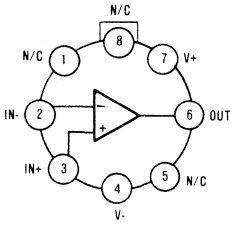
HA3-5152 (PLASTIC MINI-DIP)
HA7-5152 (CERAMIC MINI-DIP)



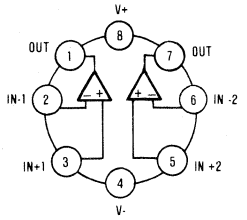
HA1-5154 (CERAMIC DIP)
HA3-5154 (PLASTIC DIP)



HA2-5151 (TO-99 METAL CAN)



HA2-5152 (TO-99 METAL CAN)



CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Terminals 35V
Differential Input Voltage ..... ±7V
Output Current ..... S/C Protected
Internal Power Dissipation 500mW

Operating Temperature Range

HA-5151/52/54-5 ..... $0^oC \leq T_A \leq +75^oC$
HA-5151/52/54-2 ..... $-55^oC \leq T_A \leq +125^oC$
Storage Temperature Range ..... $-65^oC \leq T_A \leq +150^oC$

Electrical Specifications

$R_S = 100\Omega$, $C_L \leq 10pF$ Unless Otherwise Specified.

PARAMETER	TEMP	V+ = +5V, V- = 0V			V+ = +15V, V- = -15V			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		0.5	3		0.5	3	mV
	Full			4			4	mV
Average Offset Voltage Drift	Full		3			3		µV/°C
Bias Current	+25°C		100	250		100	250	nA
	Full			400			400	nA
Offset Current	+25°C		5	50		5	50	nA
	Full			80			80	nA
Common Mode Range	Full	0 to 3			±10			V
Differential Input Resistance	+25°C		1.5			1.5		MΩ
Input Noise Voltage (f = 1kHz)	+25°C		14.8			14.8		$nV/\sqrt{Hz}$
Input Noise Current (f = 1kHz)	+25°C		0.25			0.25		$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Notes 2, 4)	+25°C	50k	100k		50k	100k		V/V
	Full	25k	50k		25k	50k		V/V
Common Mode Rejection Ratio (Note 7)	Full	80	105		80	105		dB
Bandwidth (Notes 2, 3)	+25°C		1.3			1.3		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Notes 2, 10)	+25°C	1 to 3.2	0.7 to 3.5		±10	±13		V
	Full	1.2 to 2.9	0.9 to 3.2		±10	±13		V
Full Power Bandwidth (Notes 2, 4, 8)	+25°C		700			95		kHz
TRANSIENT RESPONSE (Notes 2, 3)								
Rise Time	+25°C		300			300		ns
Slew Rate (Note 6)	+25°C	2	4.5		4	6		V/µs
Settling Time (Note 5)	+25°C		5			5		µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C		200	250		200	250	µA/Amp
	Full			275			275	µA/Amp
Power Supply Rejection Ratio (Note 9)	Full	80	105		80	105		dB

NOTES:

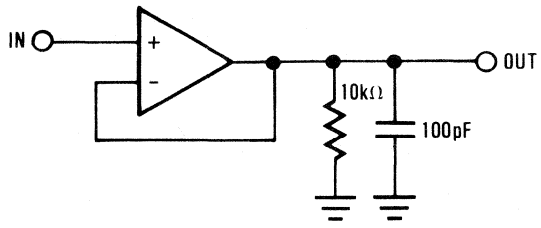
1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. $R_L = 10k\Omega$
3. $C_L = 100pF$
4. $V_O = 1.4$ to 2.5V for $V_{CC} = +5, 0V$; $V_O = \pm 10V$ for $V_{CC} = \pm 15V$.
5. Settling Time is specified to 0.1% of final value for a 3V output step and $A_V = -1$. For $V_{CC} = +5V, 0V$; output step = 10V for $V_{CC} = \pm 15V$.
6. Maximum input slew rate = 25V/µs.
7. $V_{CM} = 0$ to 3V for $V_{CC} = +5, 0V$; $V_{CM} = \pm 10V$ for $V_{CC} = \pm 15V$
8. Full Power Bandwidth is guaranteed by equation:

$$\text{Full Power Bandwidth} = \frac{\text{Slew Rate}}{2\pi \text{ V Peak}}$$

9. $\Delta V_S = +10V$ for $V_{CC} = +5, 0V$; $\Delta V_S = \pm 5V$ for $V_{CC} = \pm 15V$.
10. For $V_{CC} = +5, 0V$ terminate R_L at +2.5V.

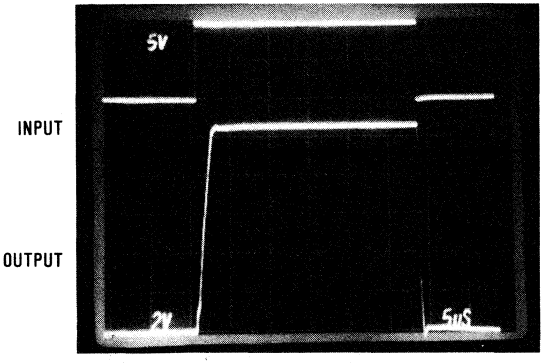
Test Circuits

SLEW RATE AND TRANSIENT RESPONSE TEST CIRCUIT



LARGE SIGNAL RESPONSE

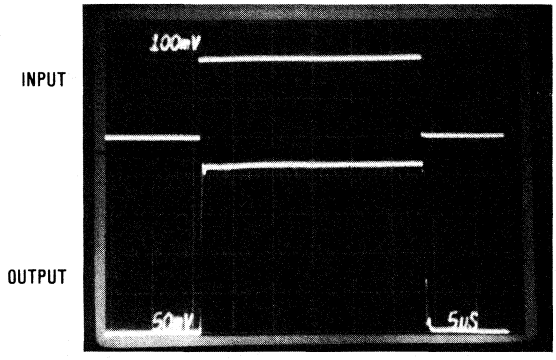
Vertical Scale: (Volts: Input = 5V/Div.)
(Volts: Output = 2/VDiv.)
Horizontal Scale: (Time: 5μs/Div.)



$+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V

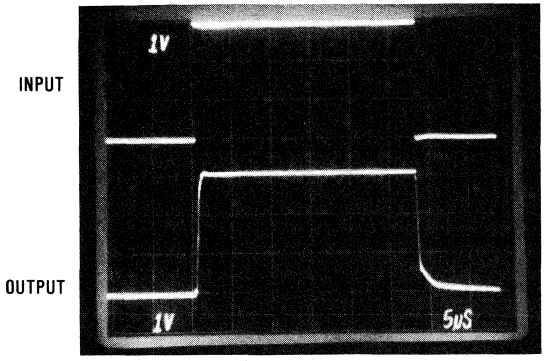
SMALL SIGNAL RESPONSE

Vertical Scale: (Volts: Input = 100mV/Div.)
(Volts: Output = 50mV/Div.)
Horizontal Scale: (Time: 5μs/Div.)



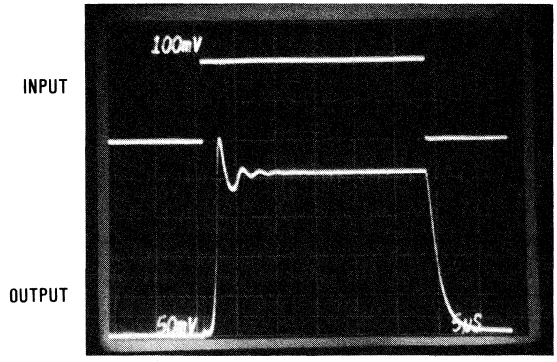
$+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V

Vertical Scale: (Volts: Input = 1V/Div.)
(Volts: Output = 1V/Div.)
Horizontal Scale: (Time: 5μs/Div.)



$+V_{SUPPLY}$ = +5V, $-V_{SUPPLY}$ = 0V

Vertical Scale: (Volts: Input = 100mV/Div.)
(Volts: Output = 50mV/Div.)
Horizontal Scale: (Time: 5μs/Div.)

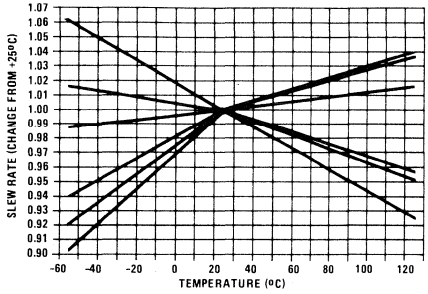


$+V_{SUPPLY}$ = +5V, $-V_{SUPPLY}$ = 0V

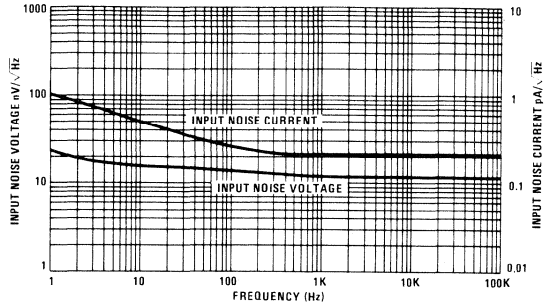
Typical Characteristics

SLEW RATE vs. TEMPERATURE

Normalized to Unity at +25°C, 6 Representative Units

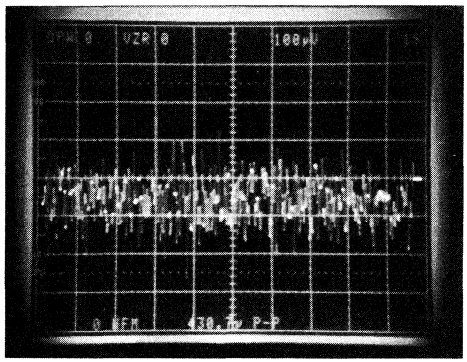


NOISE SPECTRAL DENSITY



PEAK-TO-PEAK NOISE 0.1Hz TO 10Hz

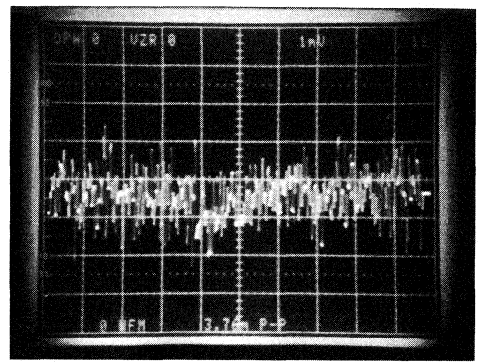
T_A = +25°C, A_V = 1000V/V



Horizontal Scale: (1sec/div)
Vertical Scale: (100μs/div)
430nV_{p-p} RTI

PEAK-TO-PEAK 0.1Hz TO 1MHz

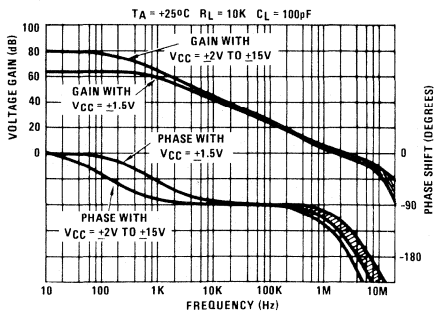
T_A = +25°C, A_V = 1000V/V



Horizontal Scale: (1sec/div)
Vertical Scale: (1mV/div)
3.70μV_{p-p} RTI

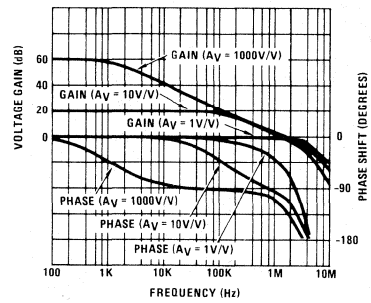
FREQUENCY RESPONSE vs. SUPPLY VOLTAGE

T_A = +25°C, R_L = 10k, C_L = 100pF



FREQUENCY RESPONSE AT VARIOUS GAINS

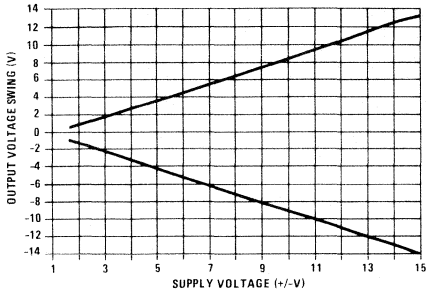
T_A = +25°C, V_{CC} = ±15V, R_L = 10k, C_L = 100pF



Typical Characteristics (Continued)

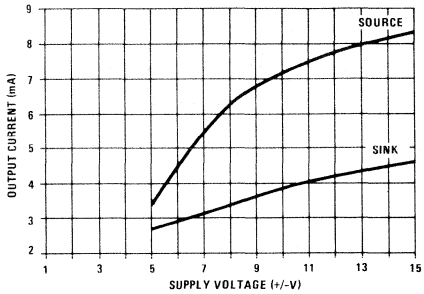
OUTPUT VOLTAGE SWING vs. SUPPLY VOLTAGE

(+25°C)



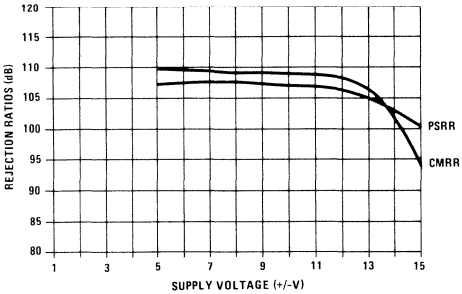
OUTPUT CURRENT vs. SUPPLY VOLTAGE

(+25°C)



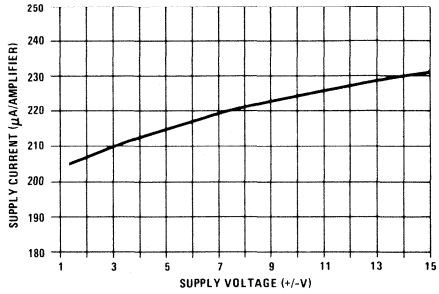
CMMR, PSRR vs. SUPPLY VOLTAGE

(+25°C)



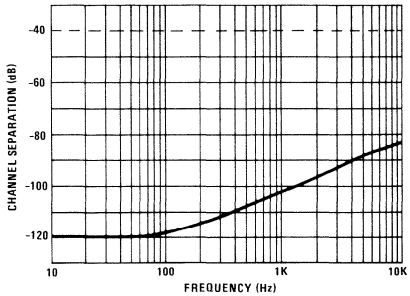
SUPPLY CURRENT vs. SUPPLY VOLTAGE

Per Amplifier (+25°C)



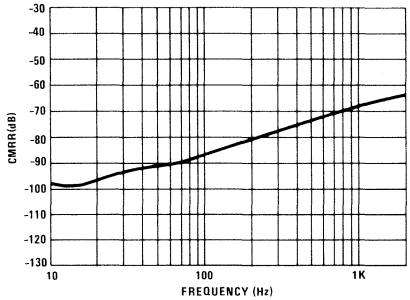
CHANNEL SEPARATION vs. FREQUENCY

V_{CC} = ±15V, T_A = +25°C



CMRR vs. FREQUENCY

T_A = +25°C, V_{CC} = ±15V



Applications Information

Independent Amplifiers

The HA-5152 dual op amp and the HA-5154 quad op amp consist of completely separate amplifier circuits. Unlike most duals and quads, these devices do not share a common bias network. Thus, one amplifier passing large, or noisy signals will have minimal effect on another channel carrying small, sensitive signals.

Loading

Although the standard load is 10kΩ, the HA-515X is capable of driving resistive loads down to 2kΩ and capacitive loads beyond 300pF.

Input Stage

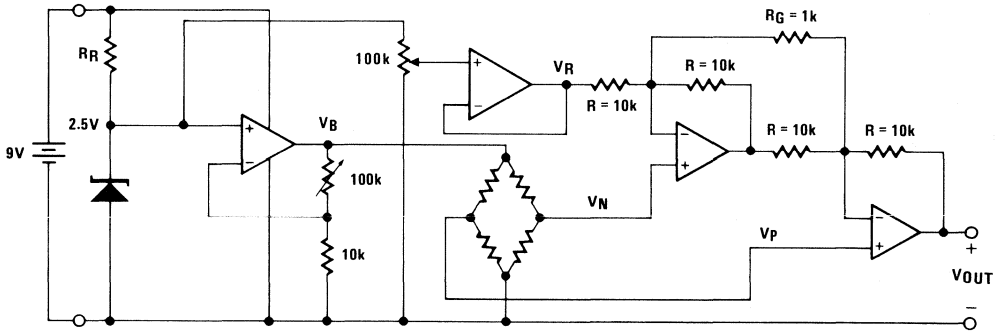
This amplifier uses a current amplifying input stage (see Application Note 544) and is not recommended for use in applications which involve large differential input voltages such as open-loop comparators. Most op amp applications use feedback and keep the input terminals at approximately the same voltage. The HA-515X will perform well in these circuits as long as the input terminals see less than 7 volts differential.

Typical Applications

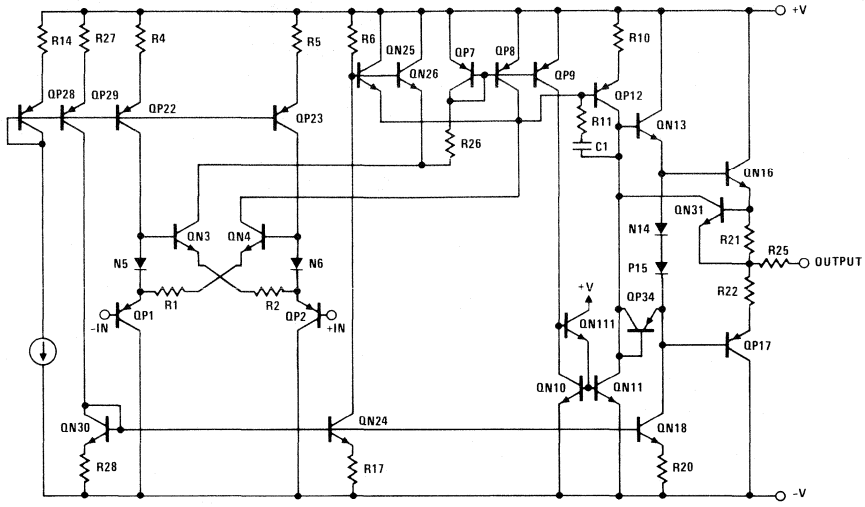
The low power consumption of the HA-5154 makes it ideal for applications like battery-powered instrumentation where the bridge amplifier circuit below would be used.

Choose a low-current zener voltage reference such as LM285Z-2.5 and select R_R accordingly. This circuit was evaluated using the resistor values shown and a laboratory voltage source for the 2.5V reference. With unmatched, off-the-shelf, 1% resistors, a gain accuracy of 1% to 2% can be expected. Temperature testing indicated a voltage offset tempco of less than 100μV/°C referred to output.

$$V_{OUT} = (V_P - V_N)\left[2\left(1 + \frac{R}{R_G}\right)\right] + V_R$$



Schematic



Die Characteristics

Transistor Count
- HA-5151 34
- HA-5152 68
- HA-5154 136

Substrate Potential* ..... V-

Process ..... Bipolar-DI

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
HA1-5154 (-2, -5, -7)	101	33
HA1-5154 (/883)	75	22
HA2-5151 (-2, -5, -7)	206	56
HA2-5151 (/883)	168	50
HA2-5152 (-2, -5, -7)	184	50
HA2-5152 (/883)	143	43
HA3-5151 (-5)	90	40
HA3-5152 (-5)	80	20
HA3-5154 (-5)	75	20
HA7-5151 (-2, -5, -7)	210	117
HA7-5151 (/883)	90	40
HA7-5152 (-2, -5, -7)	177	92
HA7-5152 (/883)	80	20

*The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.

NOTE: Consult Harris for LCC/PLCC information.

HARRIS

HA-5160/62

Wideband, JFET Input High Slew Rate, Uncompensated, Operational Amplifier

Features

- **Wide Gain Bandwidth (AV ≥10) 100MHz**
- **High Slew Rate 120V/μs**
- **Settling Time..... 280ns**
- **Power Bandwidth 1MHz**
- **Offset Voltage 1.0mV**
- **Bias Current 20pA**

Applications

- **Video and RF Amplifiers**
- **Data Acquisition**
- **Pulse Amplifiers**
- **Precision Signal Generation**

Description

The HA-5160 is a wideband, uncompensated, operational amplifier with FET/Bipolar technologies and Dielectric Isolation. This monolithic amplifier features superior high frequency capabilities further enhanced by precision laser trimming of the input stage to provide excellent input characteristics. This device has excellent phase margin at a closed loop gain of 10 without external compensation.

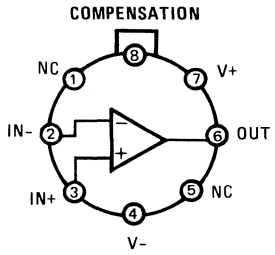
The HA-5160/5162 offers a number of important advantages over similiar FET input op amps from other manufacturers. In addition to superior bandwidth and settling characteristics, the HARRIS devices have nearly constant slew rate, bandwidth, and settling characteristics over the operating temperature range. This provides the user predictable performance in applications where settling time, full power bandwidth, closed loop bandwidth, or phase shift is critical. Note also that HARRIS specified all parameters at ambient (rather than junction) temperature to provide the designer meaningful data to predict actual operating performance.

Complementing the HA-5160/5162's predictable and excellent dynamic characteristics are very low input offset voltage, very low input bias current, and a very high input impedance. This ideal combination of features make these amplifiers most suitable for precision, high speed, data acquisition system designs and for a wide variety of signal conditioning applications. The HA-5160 provides excellent performance for applications which require both precision and high speed performance. The HA-5162 meets or exceeds the performance specifications of National's hybrid op amp, the LH0062.

The HA2-5160-2 denotes a temperature range of -55°C to +125° C and the HA2-5160/62-5 denotes a 0°C to +75°C range. Military version (/883) data sheets are available upon request.

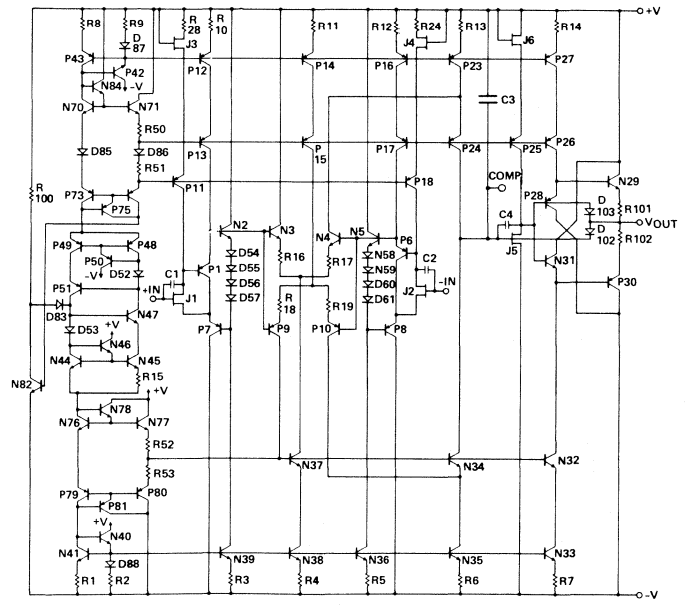
Pinout

HA2-5160/5162
(TO-99 METAL CAN)
TOP VIEW



Case Connected to V-

Schematic



CAUTION: These devices are sensitive to electric discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings

Voltage Between V+ and V- 40V
Differential Input Voltage ..... ±40V
Peak Output Current ..... Full Short Circuit Protection
Internal Power Dissipation (Note 2) 675mW

Operating Temperature Ranges:

HA-5160-2 ..... $-55^{o}C \leq TA \leq +125^{o}C$
HA-5160-5 ..... $0^{o}C \leq TA \leq +75^{o}C$
HA-5162-5 ..... $0^{o}C \leq TA \leq +75^{o}C$
Storage Temperature Range ..... $-65^{o}C \leq TA \leq +150^{o}C$
Maximum Junction Temperature (Note 2) ..... $+175^{o}C$

Electrical Specifications

V+ = +15V, V- = -15V, Unless Otherwise Specified.

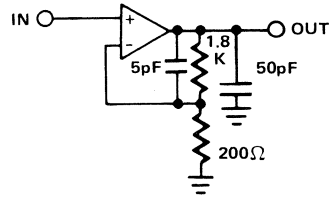
PARAMETER	TEMP	HA-5160-2 -55°C to 125°C			HA-5160-5 0°C to +75°C			HA-5162-5 0°C to +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS											
Offset Voltage	+25°C	-	1	3	-	1	3	-	3	15	mV
	Full	-	3	5	-	3	5	-	5	20	mV
Offset Voltage Average Drift	Full	-	10	-	-	20	-	-	20	35	µV/°C
Bias Current	+25°C	-	20	50	-	20	50	-	20	65	pA
	Full	-	5	10	-	5	10	-	5	10	nA
Offset Current	+25°C	-	2	10	-	2	10	-	2	10	pA
	Full	-	2	5	-	2	5	-	2	5	nA
Input Capacitance	+25°C	-	5	-	-	5	-	-	5	-	pF
Input Resistance	+25°C	-	10^{12}	-	-	10^{12}	-	-	10^{12}	-	Ω
Common Mode Range	Full	±10	±11	-	±10	±11	-	±10	±11	-	V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain	+25°C	75K	150K	-	75K	150K	-	25K	100K	-	V/V
(Note 3)	Full	60K	100K	-	60K	100K	-	25K	75K	-	V/V
Common Mode Rejection Ratio (Note 4)	Full	74	80	-	74	80	-	70	80	-	dB
Minimum Stable Gain	+25°C	10	-	-	10	-	-	10	-	-	V/V
Gain Bandwidth Product ($A_V \geq 10$)	Full	-	100	-	-	100	-	-	100	-	MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing	+25°C	±10	±11	-	±10	±11	-	±10	±11	-	V
(Note 5)	Full	±10	±11	-	±10	±11	-	±10	±11	-	V
Output Current (Note 6)	+25°C	±10	±20	-	±10	±20	-	±10	±20	-	mA
Output Short Circuit Current	+25°C	-	±35	-	-	±35	-	-	±35	-	mA
Full Power Bandwidth (Note 3, 7)	+25°C	1.6	1.9	-	1.6	1.9	-	0.8	1.1	-	MHz
Output Resistance (Note 8)	+25°C	-	50	-	-	50	-	-	50	-	Ω
TRANSIENT RESPONSE (Note 9)											
Rise Time	+25°C	-	20	-	-	20	-	-	20	-	ns
Slew Rate	+25°C	100	120	-	100	120	-	50	70	-	V/µs
Settling Time (Note 10)	+25°C	-	280	-	-	280	-	-	400	-	ns
POWER SUPPLY CHARACTERISTICS											
Supply Current	Full	-	8	10	-	8	10	-	8	12	mA
Power Supply Rejection Ratio (Note 11)	+25°C	74	86	-	74	86	-	70	86	-	dB

NOTES:

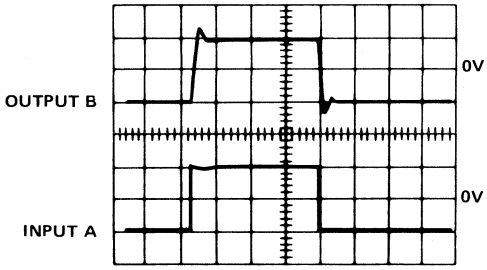
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Dearate at 6.8mW/^{o}C for operation at ambient temperatures above +75^{o}C.
3. V_{OUT} = ±10V, R_L = 2K
4. V_{CM} = ±10V DC
5. R_L = 2K
6. V_{OUT} = ±10V
7. Full Power Bandwidth guaranteed, based on slew rate measurement using FPWB = $\frac{\text{Slew Rate}}{2\pi V_{peak}}$
8. Output resistance measured under open loop conditions.
9. Refer to Test circuits section of the data sheet, where A_V = +10.
10. Settling Time is measured to 0.2% of final value for a 10 volt output step and A_V = 10.
11. V_{SUPP} = ±10V DC to ±20V DC

Test Circuits

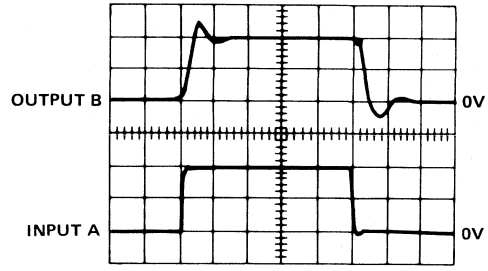
LARGE AND SMALL SIGNAL RESPONSE CIRCUIT



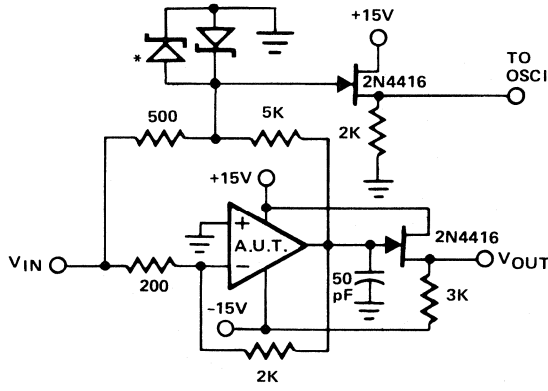
LARGE SIGNAL RESPONSE
Vertical Scale: A = 0.5V/Div., B = 5V/Div.
Horizontal Scale: Time = 500ns/Div.



SMALL SIGNAL RESPONSE
Vertical Scale: A = 10mV/Div., B = 100mV/Div.
Horizontal Scale: Time = 100ns/Div.



SETTLING TIME CIRCUIT

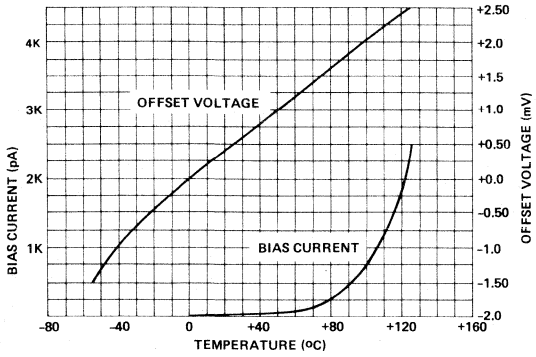


- A_V = -10
- Feedback and summing resistors should be 0.1% matched.

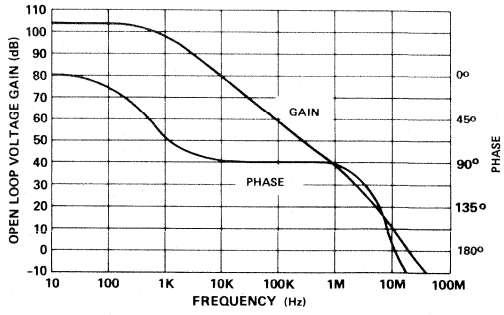
* Clipping Diodes are optional. HP5082-2810 recommended.

Typical Performance Curves

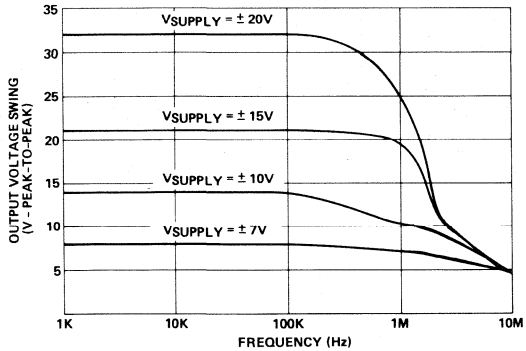
INPUT OFFSET VOLTAGE AND BIAS CURRENT vs. TEMPERATURE



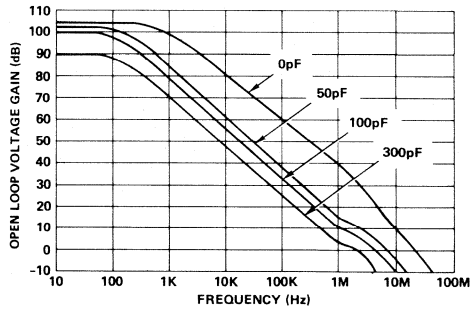
OPEN LOOP FREQUENCY RESPONSE



OUTPUT VOLTAGE SWING vs. FREQUENCY

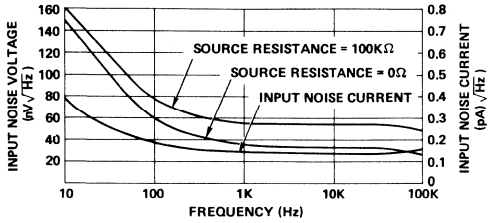


OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS BANDWIDTH CONTROL CAPACITANCES

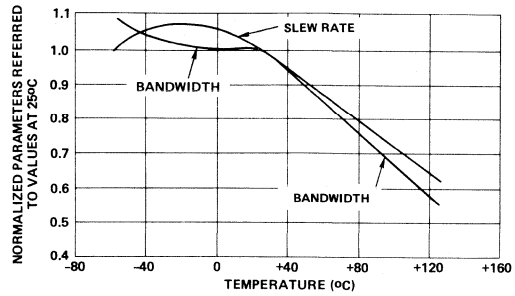


Typical Performance Curves (Continued)

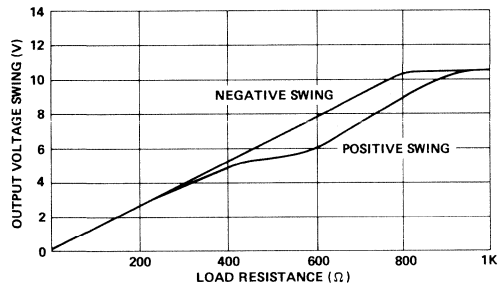
INPUT NOISE VOLTAGE AND NOISE CURRENT vs. FREQUENCY



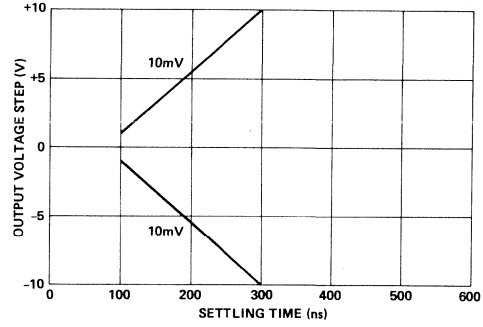
NORMALIZED AC PARAMETERS vs. TEMPERATURE



OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE

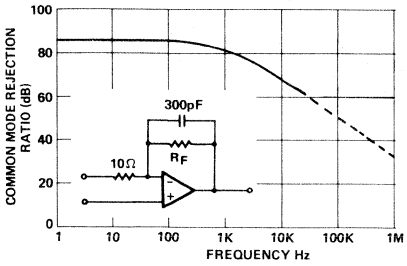


SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES

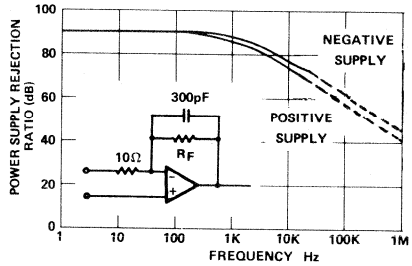


Typical Performance Curves (Continued)

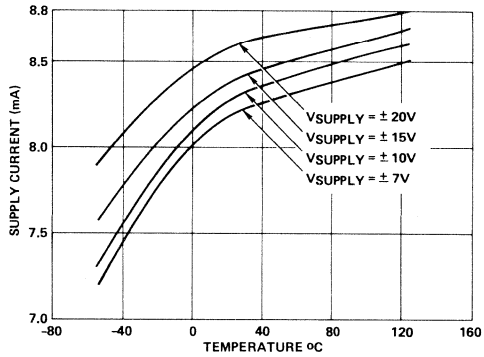
COMMON MODE REJECTION RATIO vs. FREQUENCY



POWER SUPPLY REJECTION RATIO vs. FREQUENCY



POWER SUPPLY CURRENT vs. TEMPERATURE



Die Characteristics

Transistor Count 82

Die Dimensions ..... 131 x 72 x 19 mils
(3330 x 1830 x 483µm)

Substrate Potential (Powered Up) ..... None

Process ..... Bipolar/JFET DI

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
HA2-5160 (-8, /883) (Gold Eutectic Die Attach)	103	31
HA2-5160/5162 (-2, -5, -7) (Glass Die Attach)	146	38

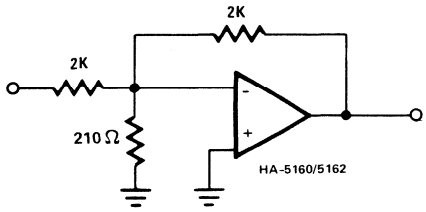
Applying the HA-5160/5162

1. POWER SUPPLY DECOUPLING: Although not absolutely necessary, it is recommended that all power supply lines be decoupled with 0.01μF ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.
2. STABILITY: The phase margin of the HA-5160/5162 will be improved by connecting a small capacitor (>10pF) between the output and the inverting input of the device This small capacitor compensated for the input capacitance of the FET.
3. CAPACITIVE LOADS: When driving large capacitive loads (>100pF), it is suggested that a small resistor (≈100Ω) be connected in series with the output of the device and inside the feedback loop.
4. POWER SUPPLY MINIMUM: The absolute supply minimum is ±6V and the safe level is ±7V.

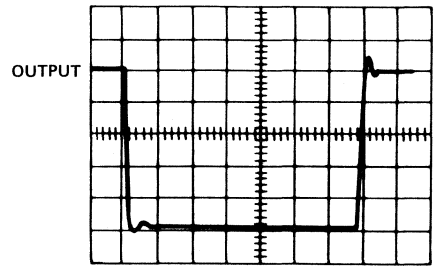
Applications

SUGGESTED COMPENSATION FOR UNITY GAIN STABILITY*

INVERTING UNITY GAIN CIRCUIT

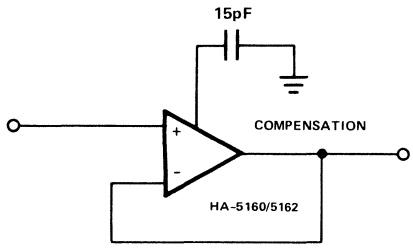


INVERTING UNITY GAIN PULSE RESPONSE

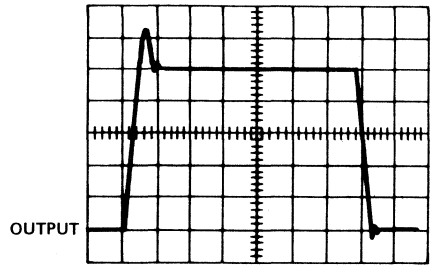


Vertical Scale: (Volts: 2V/Div.)
Horizontal Scale: (Time: 500ns/Div.)

NONINVERTING UNITY GAIN CIRCUIT



NONINVERTING UNITY GAIN PULSE RESPONSE



Vertical Scale: (Volts: 2V/Div.)
Horizontal Scale: (Time: 500ns/Div.)

*Values Were Determined Experimentally
For Optimum Speed and Settling Time.

HA-5170

Precision JFET Input Operational Amplifier

Features

- Low Offset Voltage 100μV
- Low Offset Voltage Drift ..... 2μV/°C
- Low Noise ..... 10nV/$\sqrt{Hz}$
- High Open Loop Gain ..... 600K V/V
- Wide Bandwidth 8MHz
- Unity Gain Stable

Applications

- High Gain Instrumentation Amplifiers
- Precision Data Acquisition
- Precision Integrators
- Precision Threshold Detectors
- For Further Design Ideas, Refer to App. Note 540.

Description

The Harris HA-5170 is a precision, JFET input, operational amplifier which features low noise, low offset voltage and low offset voltage drift. Constructed using FET/Bipolar technology, the Harris Dielectric Isolation (DI) process, and laser trimming this amplifier offers low input bias and offset currents. This operational amplifier design also completely eliminates the troublesome errors due to warm-up drift.

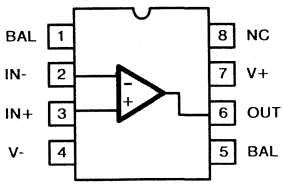
Complementing these excellent input characteristics are dynamic performance characteristics never before available from precision operational amplifiers. An 8V/μs slew rate and 8MHz bandwidth allow the designer to extend precision instrumentation applications in both speed and bandwidth. These characteristics make the HA-5170 well suited for precision integrator amplifier designs.

The superior input characteristics also make the HA-5170 ideally suited for transducer signal amplifiers, precision voltage followers and precision data acquisition systems. For application assistance , please refer to Application Note 540 addressing specifically this device.

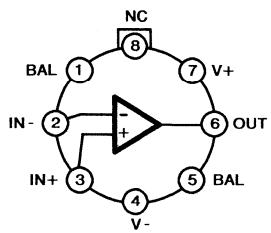
The HA-5170 is available in Metal Can (TO-99) and Ceramic Mini-DIP packages. HA-5170-2 denotes a -55°C to +125°C temperature range and HA-5170-5 denotes the 0°C to +75°C range. Military version (/883) product and data sheets available upon request.

Pinouts

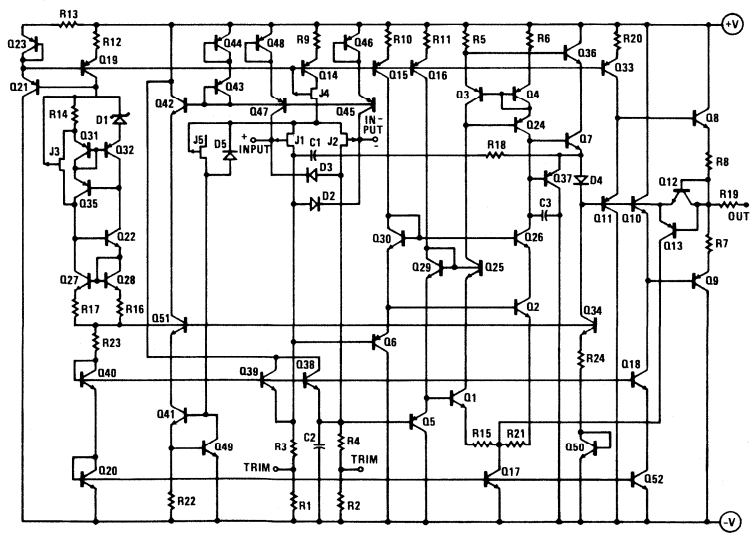
HA7-5170 (CERAMIC MINI-DIP)
TOP VIEW



HA2-5170 (TO-99 METAL CAN)
TOP VIEW



Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note)

T_A = +25°C, Unless Otherwise Specified.

- Voltage Between V+ and V- Terminals 44.0V
- Differential Input Voltage ..... ±30.0V
- Output Short Circuit Duration ..... Indefinite
- Power Dissipation (Note 2) 675mW
- Maximum Junction Temperature ..... +175°C

Operating Temperature Ranges

- HA-5170-2 ..... $-55°C \leq T_A \leq +125°C$
- HA-5170-5 ..... $0°C \leq T_A \leq +75°C$
- Storage Temperature Range ..... $-65°C \leq T_A \leq +150°C$

Electrical Specifications V+ = +15V, V- = -15V, Unless Otherwise Specified.

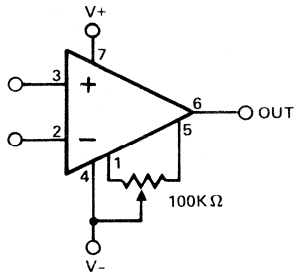
PARAMETER	TEMP	HA-5170-2 -55°C to +125°C MIN	HA-5170-2 -55°C to +125°C TYP	HA-5170-2 -55°C to +125°C MAX	HA-5170-5 0°C to +75°C MIN	HA-5170-5 0°C to +75°C TYP	HA-5170-5 0°C to +75°C MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C	-	0.1	0.3	-	0.1	0.3	mV
	Full	-	-	0.5	-	-	0.5	mV
Average Offset Voltage Drift (Note 3)	Full	-	2	5	-	2	5	µV/°C
Bias Current	+25°C	-	20	100	-	20	100	pA
	Full	-	3	30	-	0.1	2	nA
Bias Current Average Drift	Full	-	3	-	-	3	-	pA/°C
Offset Current	+25°C	-	3	30	-	3	60	pA
	Full	-	-	5	-	-	0.1	nA
Offset Current Average Drift (Note 3)	Full	-	0.3	1	-	0.3	1	pA/°C
Common Mode Range	Full	±10	+15.1 -12	-	±10	+15.1 -12	-	V V
Differential Input Capacitance	+25°C	-	80	100	-	80	100	pF
Differential Input Resistance (Note 3)	+25°C	$1x10^{10}$	$6x10^{10}$	-	$1x10^{10}$	$6x10^{10}$	-	Ω
Input Capacitance (Single Ended)	+25°C	-	12	-	-	12	-	pF
Input Noise Voltage 0.1Hz to10Hz (Note 3)	+25°C	-	0.5	5	-	0.5	5	μV_{p-p}
Input Noise Voltage Density (Note 3)								
f_O = 10Hz	+25°C	-	20	150	-	20	150	$nV/\sqrt{Hz}$
f_O = 100Hz	+25°C	-	12	50	-	12	50	$nV/\sqrt{Hz}$
f_O = 1000Hz	+25°C	-	10	25	-	10	25	$nV/\sqrt{Hz}$
Input Noise Voltage Density (Note 3)								
f_O = 10Hz	+25°C	-	0.05	-	-	0.05	-	$pA/\sqrt{Hz}$
f_O = 100Hz	+25°C	-	0.01	-	-	0.01	-	$pA/\sqrt{Hz}$
f_O = 1000Hz	+25°C	-	0.01	0.1	-	0.01	0.1	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Notes 4)	+25°C	300K	600K	-	300K	600K	-	V/V
	Full	200K	-	-	250K	-	-	V/V
Common Mode Rejection Ratio (Note 5)	Full	85	100	-	90	100	-	dB
Minimum Stable Gain	+25°C	1	-	-	1	-	-	V/V
Closed Loop Bandwidth (A_{VCL} = +1)	+25°C	4	8	-	4	8	-	MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 6)	+25°C	±10	±12	-	±10	±12	-	V
Full Power Bandwidth (Note 7)	+25°C	80	120	-	80	120	-	kHz
Output Current (Note 8)	+25°C	±10	±15	-	±10	±15	-	mA
Output Resistance (Note 3 & 9)	+25°C	-	45	100	-	45	100	Ω
TRANSIENT RESPONSE								
Rise Time	+25°C	-	45	100	-	45	100	ns
Slew Rate	+25°C	5	8	-	5	8	-	V/µs
Settling Time (Notes 3 & 10)	+25°C	-	1	5	-	1	5	µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	Full	-	1.9	2.5	-	1.9	2.5	mA
Power Supply Rejection Ratio (Note 11)	Full	85	105	-	90	105	-	dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate at 6.8 mW/°C for operation at ambient temperatures above +75°C.
3. Parameter is not 100% tested. 90% of all units meet or exceed these specifications.
4. V_{OUT} = ±10, R_L = 2kΩ.
5. ΔV_{CM} = ±10V D.C.
6. R_L = 2kΩ.
7. R_L = 2kΩ; Full power bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{SLEW\ RATE}{2\pi V_{PEAK}}$
8. V_{OUT} = ±10V. I_{SC} turns on at ≅ 23mA.
9. Output resistance measured under open loop conditions (f ≅ 100Hz).
10. Settling time is measured to 0.1% of final value for a 10V output step and A_V = -1.
11. ΔV_{SUPPLY} = ±10V D.C. to ±20V D.C.

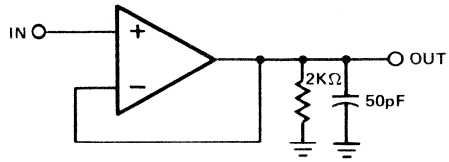
Test Circuits

V_{OS} ADJUSTMENT

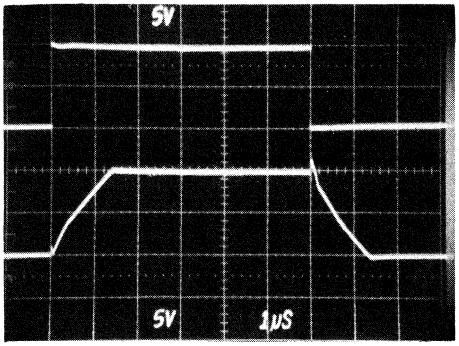


Tested Offset Adjustment Range is $|V_{OS} \pm 1mV|$ minimum referred to output.
Typical range is ±5mV with R_T = 1kΩ and ±15mV with R_T = 100kΩ.

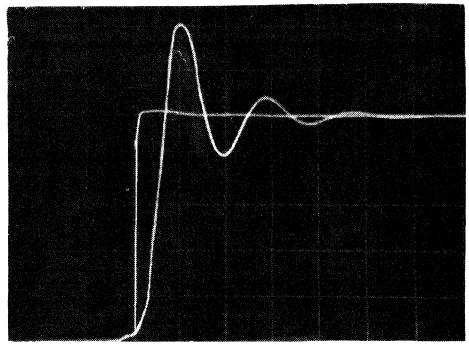
LARGE AND SMALL SIGNAL RESPONSE CIRCUIT



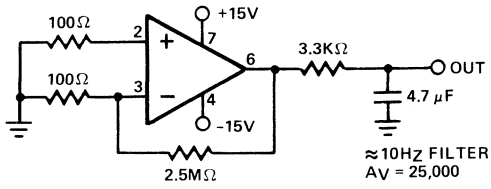
LARGE SIGNAL RESPONSE
Vertical Scale: 5V/Div.
Horizontal Scale: 500ns/Div.



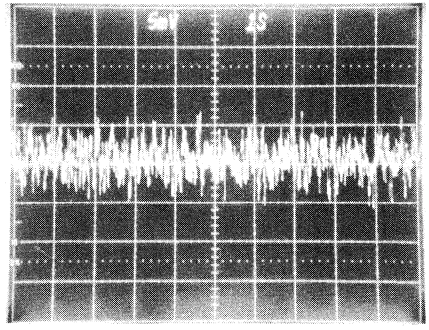
SMALL SIGNAL RESPONSE
Vertical Scale: 10mV/Div.
Horizontal Scale: 100ns/Div.



LOW FREQUENCY NOISE TEST CIRCUIT

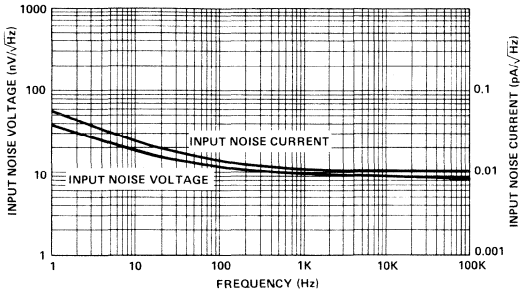


HA-5170 LOW FREQUENCY NOISE (0.1Hz TO 10Hz)
Vertical Scale: 200nV/Div. (Noise Referred to Input)
5mV Div.At Output, AVCL = 25,000.
Horizontal Scale: 1 Sec./Div.

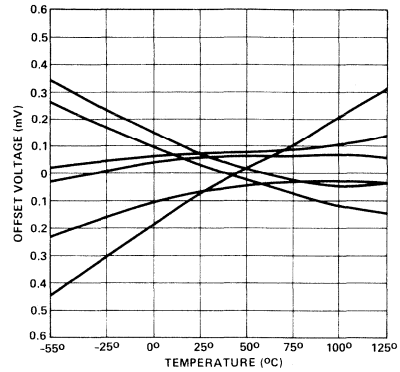


Typical Performance Curves

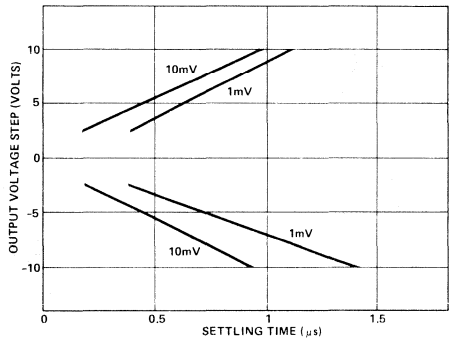
INIPUT VOLTAGE NOISE vs. FREQUENCY



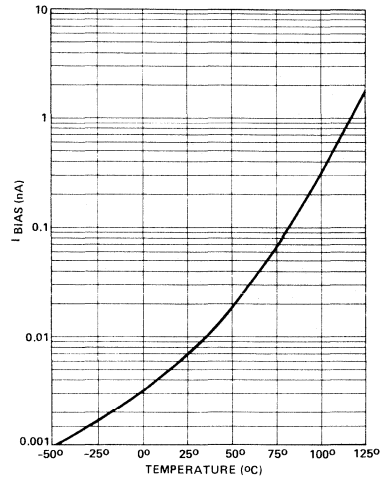
OFFSET VOLTAGE vs. TEMPERATURE DRIFT OF REPRESENTATIVE UNITS



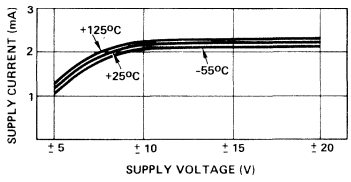
SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES



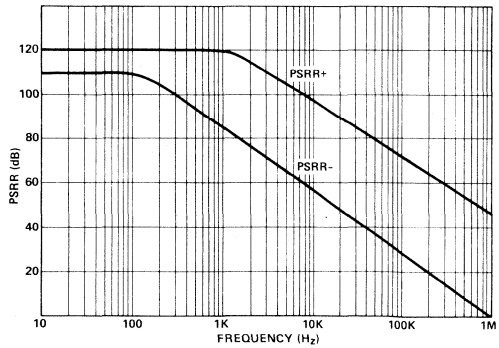
BIAS CURRENT vs. TEMPERATURE



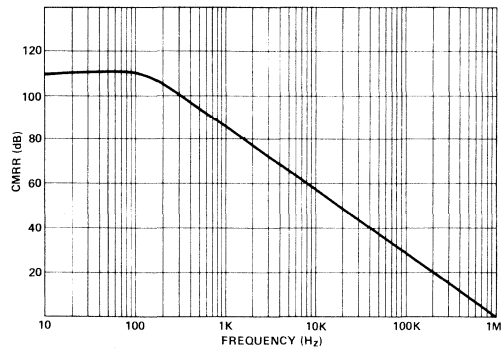
POWER SUPPLY CURRENT vs. SUPPLY VOLTAGE AND TEMPERATURE



POWER SUPPLY REJECTION RATIO vs. FREQUENCY

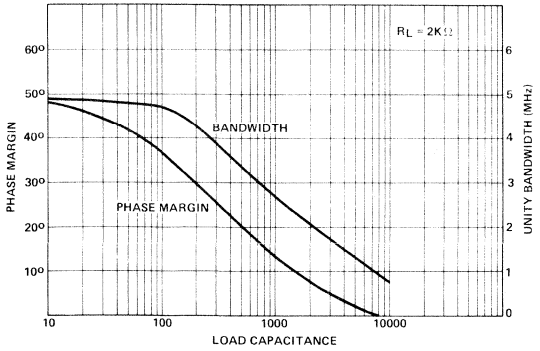


COMMON MODE REJECTION RATIO vs. FREQUENCY

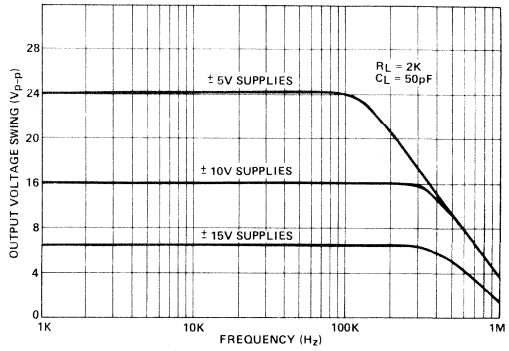


Typical Performance Curves (Continued)

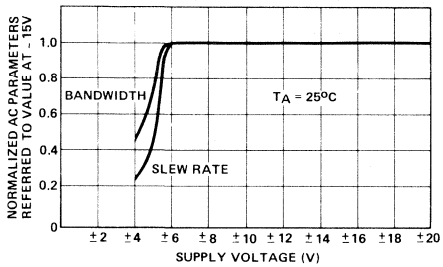
SMALL SIGNAL BANDWIDTH AND PHASE MARGIN vs. LOAD CAPACITANCE



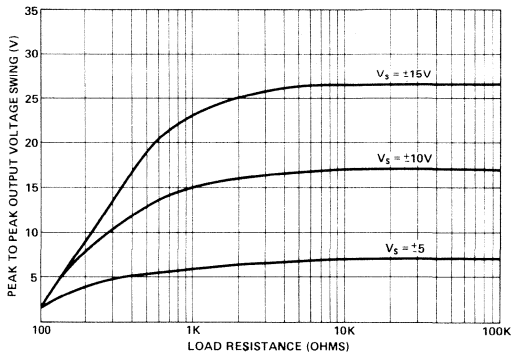
OUTPUT VOLTAGE SWING vs. FREQUENCY AND SUPPLY VOLTAGE



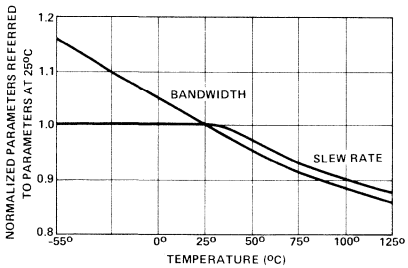
NORMALIZED AC PARAMETERS vs. SUPPLY VOLTAGE



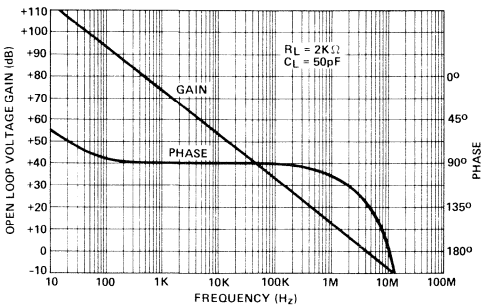
MAXIMUM OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE



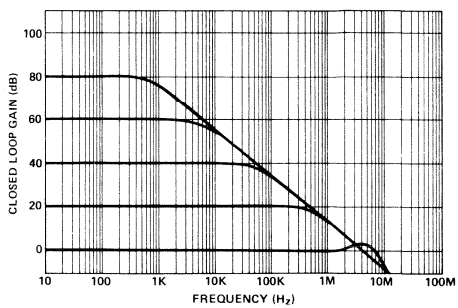
NORMALIZED AC PARAMETERS vs. TEMPERATURE



OPEN LOOP FREQUENCY RESPONSE



CLOSED LOOP FREQUENCY RESPONSE FOR VARIOUS CLOSED LOOP GAINS



HARRIS

HA-5177

PRELIMINARY

Ultra-Low Offset Voltage Operational Amplifier

Features

- Low Offset Voltage ..... 25μV Max.
- Low Offset Voltage Drift ..... 0.3μV/°C Max.
- High Voltage Gain ..... 134dB Min.
- High CMRR..... 120dB Min.
- High PSRR ..... 3μV/V Max.
- Low Noise ..... 9nV/$\sqrt{Hz}$ Typ.
- Low Power Consumption ..... 51mW Max.

Applications

- High Gain Instrumentation Amplifiers
- Precision Control Systems
- Precision Integrators
- High Resolution Data Converters
- Precision Threshold Detectors
- Low Level Transducer Amplifiers

Description

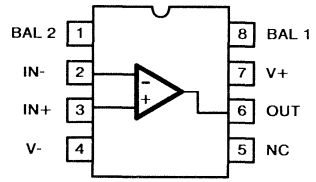
The HA-5177 is a monolithic, all bipolar, precision operational amplifier, utilizing Harris dielectric isolation and advance processing techniques. This design features a combination of precision input characteristics, wide bandwidth (1.4MHz) and high speed (0.8 V/μs).

The HA-5177 uses advanced matching techniques and laser trimming to produce low offset voltage (25μV) and low offset voltage drift (0.3μV/°C). This design also features low voltage noise (9.0nV/$\sqrt{Hz}$), low current noise (0.12pA/$\sqrt{Hz}$), nanoamp input currents, and 120dB minimum gain. These outstanding features along with high CMRR (140dB) and high PSRR (135dB) make this unity gain stable amplifier ideal for high resolution data acquisition systems, precision integrators, and low level transducer amplifiers.

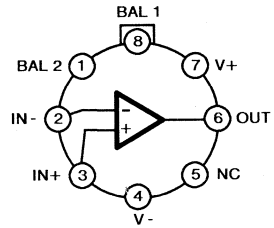
The HA-5177 can be used as a direct replacement for the OP05, OP07, and OP77 while offering higher bandwidth and slew rate. The HA-5177 is packaged in a 8 pin (TO-99) Metal Can and Ceramic 8 pin Mini-DIP and is pin compatible with many existing op amps. See the HA-5177/883 data sheet for military grade parts and LCC package.

Pinouts

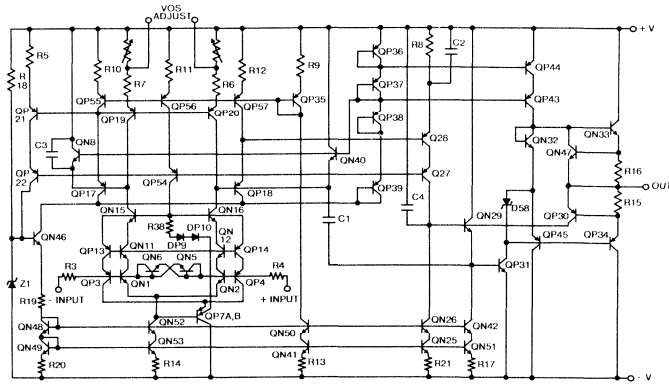
HA7-5177 (CERAMIC MINI-DIP)
TOP VIEW



HA2-5177 (TO-8 METAL CAN)
TOP VIEW



Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

T_A = +25°C Unless Otherwise Specified
Voltage Between V+ and V- Terminals 40V
Differential Input Voltage..... ±15V
Output Current ..... Short Circuit Protected
Power Dissipation 500mW
Maximum Junction Temperature..... +175°C

Operating Temperature Ranges

HA-5177A/5177-2 ..... $-55°C \leq T_A \leq +125°C$
HA-5177A/5177-5 ..... $0°C \leq T_A \leq +75°C$
Storage Temperature Range:..... $-65°C \leq T_A \leq +150°C$

Electrical Specifications V+ = +15V, V- = -15V

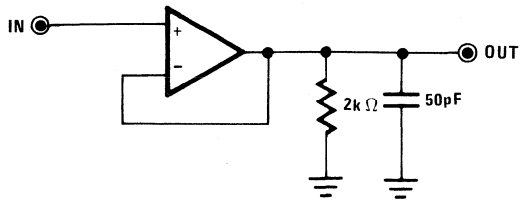
PARAMETER	TEMP	HA-5177A			HA-5177			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Offset Voltage	+25°C	-	10	25	-	20	60	µV
	Full	-	25	60	-	40	100	µV
Average Offset Voltage Drift	Full	-	0.1	0.3	-	0.2	0.6	µV/°C
Bias Current	+25°C	-	1.2	2	-	1.2	6	nA
	Full	-	2.4	4	-	2.4	8	nA
Bias Current Average Drift	Full	-	2.4	4	-	2.4	6	nA/°C
Offset Current	+25°C	-	0.6	2	-	0.6	6	nA
	Full	-	1.0	4	-	1.0	8	nA
Offset Current Average Drift	Full	-	1.5	25	-	1.5	50	pA/°C
Common Mode Range	Full	±12	-	-	±12	-	-	V
Differential Input Resistance	+25°C	-	47	-	-	47	-	MΩ
Input Noise Voltage 0.1Hz to 10Hz	+25°C	-	0.35	0.6	-	0.35	0.6	μV_{p-p}
Input Noise Voltage Density (Note 2)	+25°C	-	-	-	-	-	-	$nV/\sqrt{Hz}$
f_O = 10Hz		-	5.5	8	-	13	18	
f_O = 100Hz		-	4.5	5.6	-	10	13	
f_O = 1000Hz		-	3.8	4.5	-	9	11	
Input Noise Current 0.1Hz to 10Hz	+25°C	-	14	30	-	14	45	pA_{p-p}
Input Noise Current Density (Note 2)	+25°C	-	-	-	-	-	-	$pA/\sqrt{Hz}$
f_O = 10Hz		-	1.1	4	-	7.1	10	
f_O = 100Hz		-	0.55	2.3	-	3.3	5	
f_O = 1000Hz		-	0.32	1	-	1.2	2	
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 3)	+25°C	134	150	-	126	150	-	dB
	Full	126	140	-	120	140	-	dB
Common Mode Rejection Ratio (Note 4)	Full	120	140	-	110	140	-	dB
Closed Loop Bandwidth (A_{VCL} = +1)	+25°C	-	1.4	-	-	1.4	-	MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 5)	+25°C	±12	±13	-	±12	±13	-	V
	Full	±12	±12.5	-	±12	±12.5	-	V
Full Power Bandwidth (Note 6)	+25°C	8	10	-	8	10	-	kHz
Output Current (Note 7)	+25°C	15	20	-	15	20	-	mA
Output Resistance	+25°C	-	60	-	-	60	-	Ω
TRANSIENT RESPONSE								
Rise Time	+25°C	-	310	420	-	310	420	ns
Slew Rate	+25°C	0.5	0.8	-	0.5	0.8	-	V/µs
Settling Time (Note 9)	+25°C	-	14	-	-	14	-	µs
Overshoot	+25°C	-	10	40	-	10	40	%
POWER SUPPLY CHARACTERISTICS								
Supply Current	Full	-	1.2	1.7	-	1.2	1.7	mA
Power Supply Rejection Ratio (Note10)	Full	110	135	-	110	135	-	dB

NOTES:

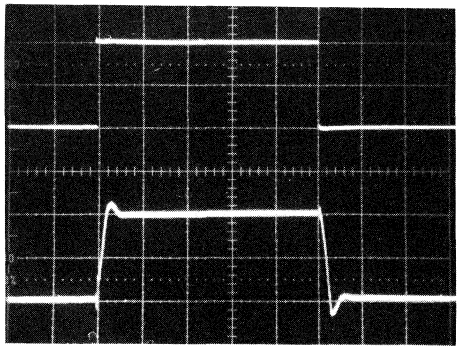
1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Sample Tested.
3. V_{OUT} = ±10V, R_L = 2kΩ
4. ΔV_{CM} = ±10V D.C.
5. R_L = 2K
6. Full power bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$, V_{PEAK} = 10V.
7. V_{OUT} = ±10.
8. Refer to test circuits section of the data sheet.
9. Settling time is measured to 0.1% of final value for a 10V output step and A_V = -1.
10. ΔV_{SUPPLY} = ±10V D.C. to ±20V D.C.

Test Circuits

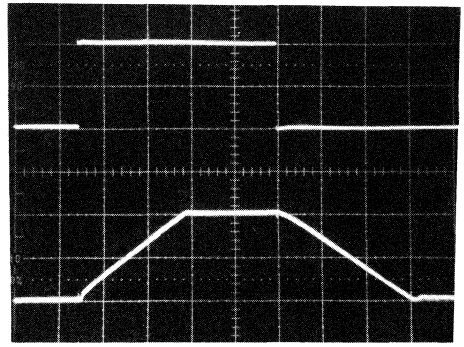
SLEW RATE AND TRANSIENT RESPONSE TEST CIRCUIT



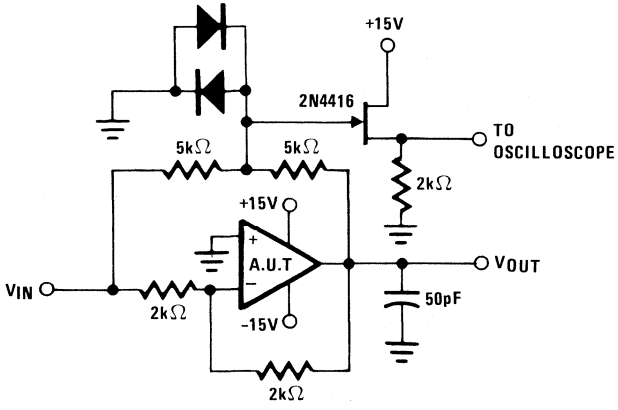
SMALL SIGNAL RESPONSE
Vertical Scale: (Volts: 100mV/Div.)
Horizontal Scale: (Time: 2μs/Div.)



LARGE SIGNAL RESPONSE
Vertical Scale: (Volts: 5V/Div.)
Horizontal Scale: (Time: 5μs/Div.)



SETTLING TIME CIRCUIT



- $A_V = -1$
- Feedback and summing resistors should be 0.1% matched.
- Clipping diodes are optional. HP5082-2810 recommended.

HA-5180

Low Bias Current, Low Power JFET Input Operational Amplifier

Features

- **Ultra Low Bias Current 250fA**
- **Low Power Supply Current 0.8mA**
- **Low Offset Voltage ..... 0.5mV Max.**
- **Unity Gain Bandwidth 2MHz**
- **Slew Rate 7V/μs**

Applications

- **Electrometer Amplifier Designs**
- **Photo Current Detectors**
- **Precision, Long-Term Integrators**
- **Low Drift Sample & Hold Circuits**
- **Very High Impedance Buffers**
- **High Impedance Biological Micro Probes**
- **Refer to Application Note 555**

Description

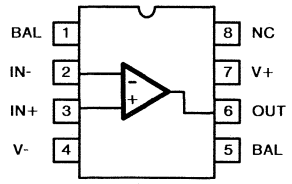
The Harris HA-5180 is an ultra low input bias current, JFET input, monolithic operational amplifier which also features low power, low offset voltage and excellent AC characteristics. Employing FET/Bipolar construction coupled with dielectric isolation this operational amplifier offers the lowest input bias currents (250fA typical) available in any monolithic operational amplifier. The HA-5180 has another unique feature in which the offset bias current may be nulled by externally adjusting the offset voltage.

The HA-5180 also offers excellent AC performance not previously available in similar hybrid or monolithic op amp designs. The 2MHz bandwidth and 7V/μs slew rate of the HA-5180 extends the bandwidth and speed for applications such as very low drift sample and hold amplifiers and photo-current detectors. Other applications include use in electrometer designs, pH/Ion sensitive electrodes, low current oxygen sensors, long term precision integrators and very high impedance buffer measurement designs.

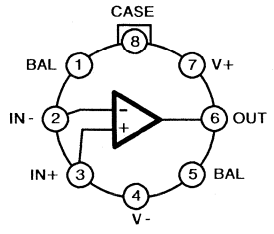
The HA-5180 is packaged in an 8 pin (TO-99) Metal Can and an 8 lead Mini-DIP and is pin compatible with most existing op amp configurations. The case of the TO-99 package is internally connected to pin 8 so that it may be connected to the same potential as the input. This feature helps minimize stray leakage to the case, helps shield the amplifier from external noise and reduces common mode input capacitance. For military grade product, refer to the HA-5180/883 data sheet.

Pinouts

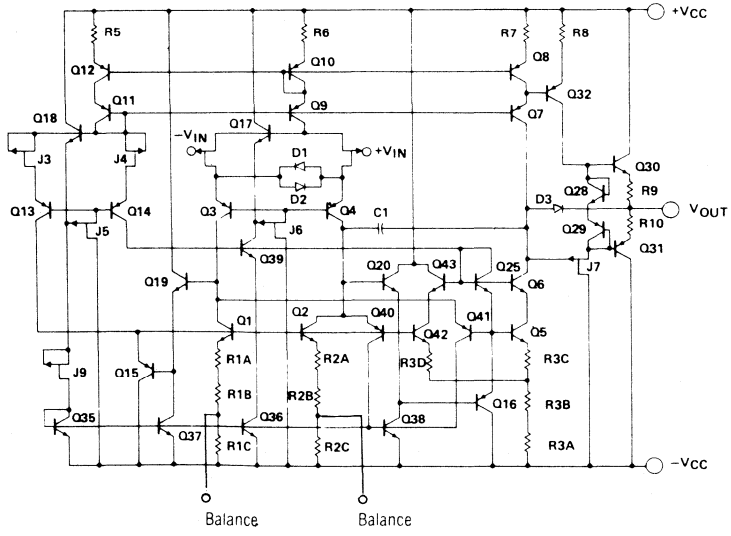
HA7-5180 (CERAMIC MINI-DIP)
TOP VIEW



HA2-5180 (TO-99 METAL CAN)
TOP VIEW



Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

T_A = +25°C Unless Otherwise Specified
Voltage Between V+ and V- Terminals 40V
Differential Input Voltage..... ±40V
Output Short Circuit Duration ..... Indefinite
Power Dissipation (Note 2)..... 300mW

Operating Temperature Ranges

HA-5180-2.....-55°C ≤ T_A ≤ +125°C
HA-5180-5..... 0°C ≤ T_A ≤ +75°C
Storage Temperature Range .....-65°C ≤ T_A ≤ +150°C

Electrical Specifications V+ = +15V, V- = -15V, Unless Otherwise Specified.

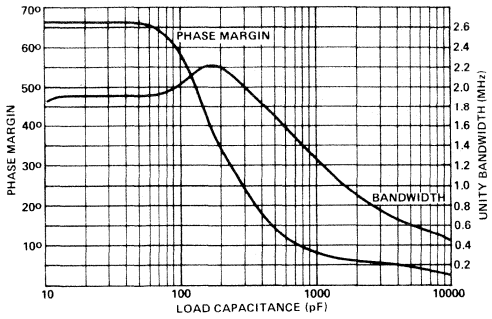
PARAMETER	TEMP	HA-5180-2 -55°C to +125°C			HA-5180-5 0°C to + 75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Offset Voltage	+25°C	-	1	3	-	1	3	mV
	Full	-	-	4	-	-	4	mV
Average Offset Voltage Drift	Full	-	5	-	-	5	-	µV/°C
Bias Current (Note 3)	+25°C	-	250	1000	-	250	1000	fA
	Full	-	100	500	-	6	30	pA
Offset Current (Note 3)	+25°C	-	30	200	-	30	200	fA
	Full	-	6	30	-	1	5	pA
Common Mode Range	Full	±10	±12	-	±10	±12	-	V
Differential Input Resistance	+25°C	-	10^{12}	-	-	10^{12}	-	Ω
Input Capacitance	+25°C	-	5	-	-	5	-	pF
Input Noise Voltage, 0.1Hz to 10Hz	+25°C	-	5	-	-	5	-	μV_{p-p}
Input Noise Voltage Density								
f_O = 10Hz	+25°C	-	200	-	-	200	-	$nV/\sqrt{Hz}$
f_O = 100Hz	+25°C	-	120	-	-	120	-	$nV/\sqrt{Hz}$
f_O = 1000Hz	+25°C	-	70	-	-	70	-	$nV/\sqrt{Hz}$
Input Noise Current (f = 1kHz)	+25°C	-	0.01	-	-	0.01	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Notes 4)	+25°C	200K	1M	-	200K	1M	-	V/V
	Full	150K	-	-	150K	-	-	V/V
Common Mode Rejection Ratio (Note 5)	Full	90	110	-	90	110	-	dB
Closed Loop Bandwidth (A_{VCL} = +1)	+25°C	-	2	-	-	2	-	MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 6)	+25°C	±10	±12	-	±10	±12	-	V
	Full	±10	-	-	±10	-	-	V
Full Power Bandwidth (Note 7)	+25°C	-	110	-	-	110	-	kHz
Output Current (Note 8)	+25°C	±10	±15	-	±10	±15	-	mA
Output Resistance (Note 9)	+25°C	-	25	-	-	25	-	Ω
TRANSIENT RESPONSE								
Overshoot	+25°C	-	30	50	-	30	50	%
Rise Time	+25°C	-	75	-	-	75	-	ns
Slew Rate	+25°C	4	7	-	4	7	-	V/µs
Settling Time (Note 10)	+25°C	-	2	-	-	2	-	µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	Full	-	0.7	1	-	0.8	1	mA
Power Supply Rejection Ratio (Note 11)	Full	85	105	-	85	105	-	dB

NOTES:

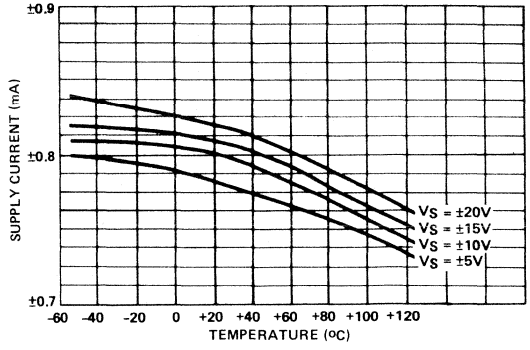
1. Absolute Maximum Ratings are limiting values applied individually beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Derate at 6.9 mW/°C for operation at ambient temperatures above +75°C.
3. This parameter is guaranteed by design and is not 100% tested.
4. V_{OUT} = ±10V; R_L = 2K. Gain dB = 20 $\log_{10} A_V$.
5. ΔV_{CM} = ±10V D.C.
6. R_L = 2K.
7. R_L = 2K, V_{PEAK} = 10V; Full power bandwidth guaranteed based on slew rate measurement using FPBW = $\frac{\text{SLEW RATE}}{2\pi V_{PEAK}}$
8. V_{OUT} = ±10V.
9. Output resistance specified under open loop conditions (f = 100Hz).
10. Settling time is speified to 0.1% of final value for a 10V output step and A_V = -1.
11. ΔV_{SUPPLY} = ±10V D.C. to ±20V D.C.

Typical Performance Curves

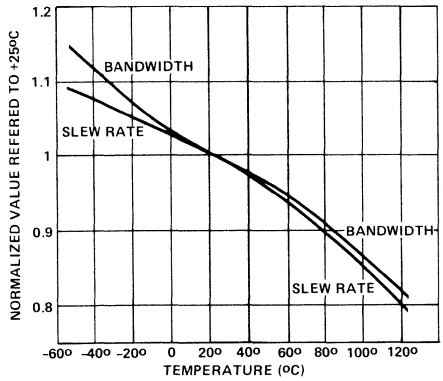
SMALL SIGNAL BANDWIDTH AND PHASE MARGIN vs. LOAD CAPACITANCE



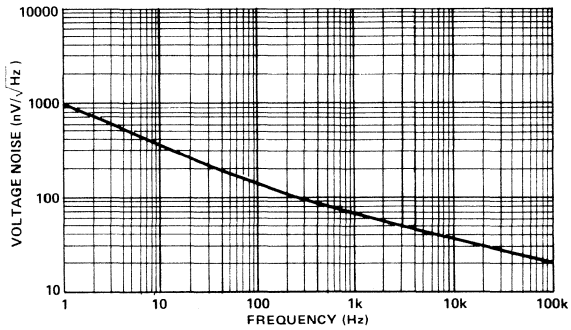
SUPPLY CURRENT vs. TEMPERATURE



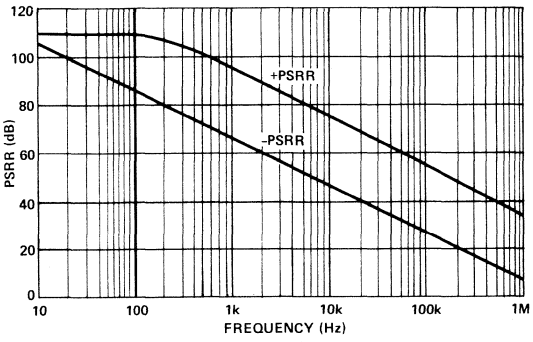
NORMALIZED AC PARAMETERS vs. TEMPERATURE



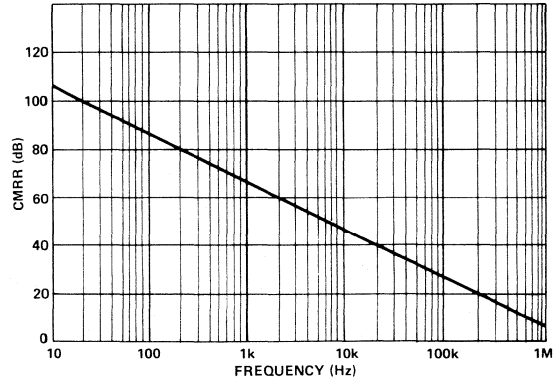
INPUT VOLTAGE NOISE vs. FREQUENCY



PSRR vs. FREQUENCY

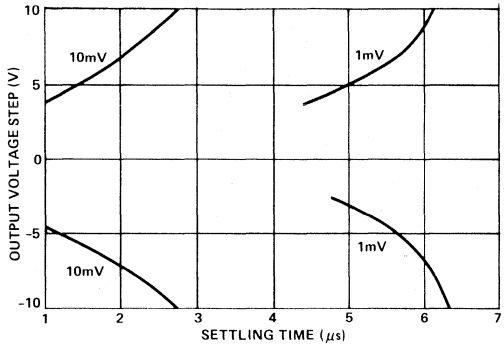


CMRR vs. FREQUENCY

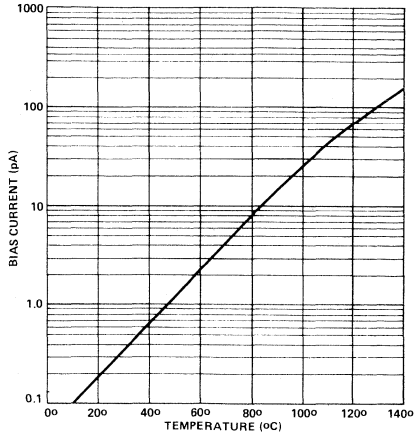


Typical Performance Curves (Continued)

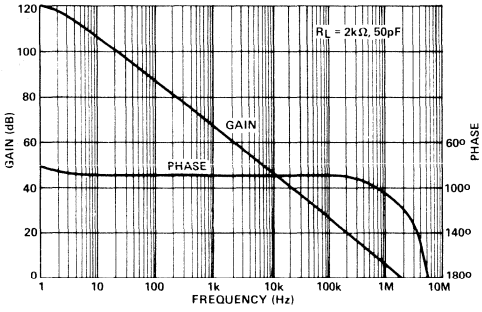
SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES



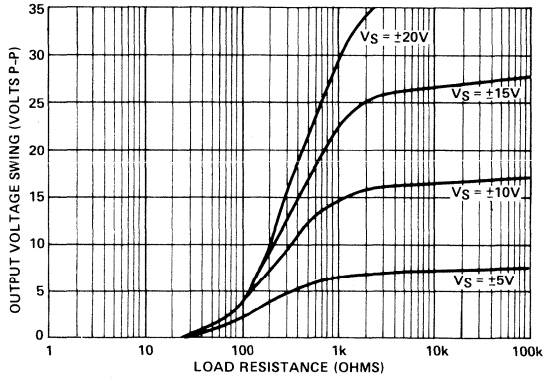
BIAS CURRENT vs. TEMPERATURE



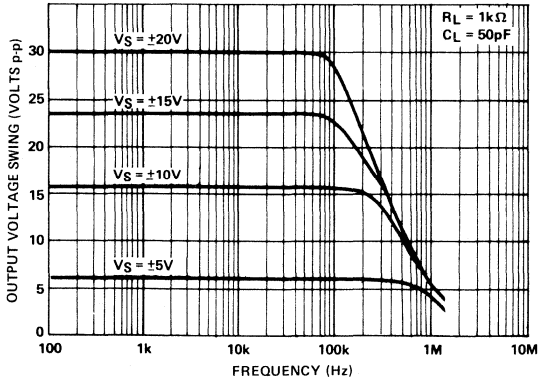
OPEN LOOP FREQUENCY RESPONSE



OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE



OUTPUT VOLTAGE SWING vs. FREQUENCY



Typical Applications

The HA-5180 offers one of the lowest input bias currents of any monolithic operational amplifier and is ideal for use in applications for measuring signals from very high impedance or very low current sources. To fully utilize the capabilities of the HA-5180, care should be taken to minimize noise pickup and current leakage paths with the use of shielding and guarding techniques and by placing the device as close as possible to the signal source. The small size and low quiesent current (possible battery operation) of the HA-5180 allows easy installation at the signal source or inside a probe. The HA-5180 is internally compensated and is capable of driving long signal cables which have several hundred pF capacitive loading.

If it is not possible to place the HA-5180 very close to the signal source, then the use of shielded coaxial cable will offer the best isolation of the high impedance signal line from external noise sources. However, the effects of leakage, capacitance and vibrational noise should be taken into account when using coaxial cables. Leakage can be minimized by using cables with very high insulation resistance (such as polyethylene or Virgin Teflon). For example, the current to voltage converter circuit (as shown in Figure 1) will eliminate leakage across the insulation of the cable by forcing the signal line to the same potential as the shield. This circuit also provides fast response to input signals because the cable capacitance is never forced to be charged or discharged. However, the cable capacitance directly increases the input capacitance of the circuit and could cause the circuit to become unstable; if so, adding capacitance across Rf will stabilize the circuit again. Leakage can also be reduced in the high-impedance non-inverting configuration (see Figure 2) by bootstrapping the shield to the same potential as the signal source instead of ground. If low closed-loop gains are used, the non-inverting configuration could also become unstable due to the positive feedback to the input through the cable capacitance. One method of compensating this circuit is to place a small (low leakage) capacitor from the input to ground. This technique will also reduce the effective capacitance presented to the signal source. When large closed-loop gains and/or long cable lengths are used, a buffer should be added to the circuit to drive the shield.

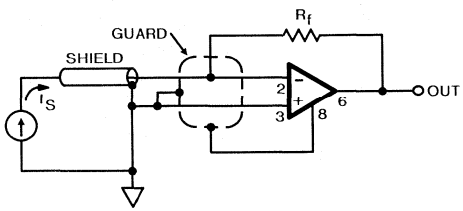


FIGURE 1. CURRENT TO VOLTAGE CONVERTER

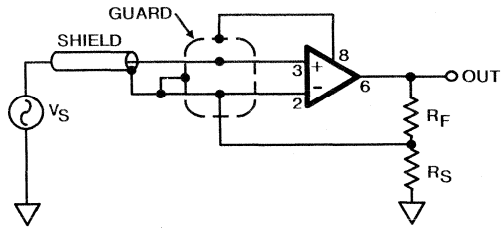


FIGURE 2. VERY HIGH IMPEDANCE NON-INVERTING AMPLIFIER

When using coaxial cable with the HA-5180 the cable should be kept as rigid and vibration free as possible. Frictional movement of the shield over the insulation can generate electrical charge which is picked up by the high impedance signal line as noise. Movement and bending of the cable can also cause charge movement due to small changes in cable capacitance and capacitance to surrounding objects. Another source of noise currents is that which is generated by the movement of a conductor in a magnetic field.

For lowest leakage at the device inputs either use a teflon IC socket or connect the signal line to the HA-5180 inputs using teflon standoffs. A guard ring, as shown in Figure 3, applied to both sides of the pc board and bootstrapped to the same potential as the input signal will minimize leakage paths across the pc board. Pin 8 of the TO-99 can, which is internally tied to the case, should also be tied to the bootstrap potential to help minimize noise pickup and leakage currents across the package insulation. This technique will also reduce common mode input capacitance.

Cleanliness of circuit boards and components is also important for achieving low leakage currents. Printed circuit boards and components should be thoroughly cleaned by using a low residue solvent such as TMC Freon , rinsed by deionized water and dried with nitrogen. The circuit board should be protected from high contamination and high humidity environments. A good quality conformal coating with low dielectric absorption provides the best protection from humidity and contamination.

Input protection is generally not necessary when designing with the HA-5180. Many electrometer type devices, especially CMOS, require elaborate zener protection schemes which may compromise overall performance. The Harris dielectric isolation process and JFET input design enables the HA-5180 to withstand input signals several volts beyond either supply and large differential signals equal to the rail-to-rail supply voltage without damage or degradation of performance.

For more information see Application Note 555.

Typical Applications (Continued)

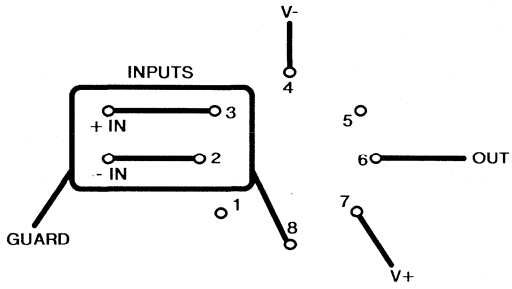


FIGURE 3. GUARD RING EXAMPLE

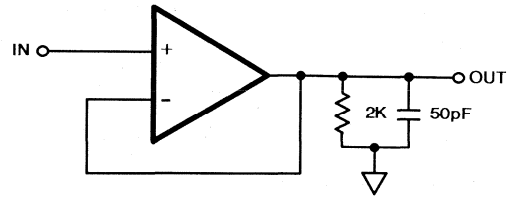


FIGURE 4. SLEW RATE AND TRANSIENT RESPONSE TEST CIRCUIT

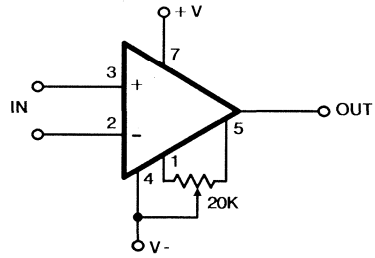
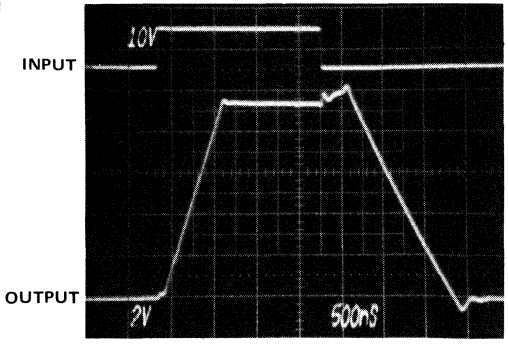


FIGURE 5. SUGGESTED OFFSET ADJUSTMENT CIRCUIT

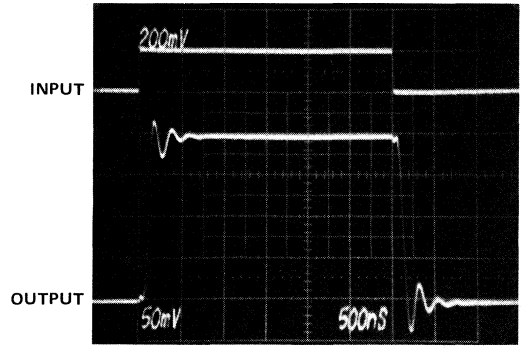
LARGE SIGNAL RESPONSE

Vertical Scale (Volts: 5V/Div. Input)
(Volts: 2V/Div. Output)
Horizontal Scale (Time: 500ns/Div.)



SMALL SIGNAL RESPONSE

Vertical Scale (Volts: 100mV/Div. Input)
(Volts: 50mV/Div. Output)
Horizontal Scale (Time: 500ns/Div.)



HARRIS HA-5190/95

Wideband, Fast Settling Operational Amplifier

Features

- Fast Settling Time (0.1%) 70ns
- Very High Slew Rate 200V/μs
- Wide Gain-Bandwidth ($A_V \geq 5$) 150MHz
- Power Bandwidth 6.5MHz
- Low Offset Voltage 3mV
- Input Noise Voltage ..... 6nV/$\sqrt{Hz}$
- Monolithic Bipolar D.I. Construction

Applications

- Fast, Precise D/A Converters
- High Speed Sample-Hold Circuits
- Pulse and Video Amplifiers
- WideBand Amplifiers
- Replace Costly Hybrids

Description

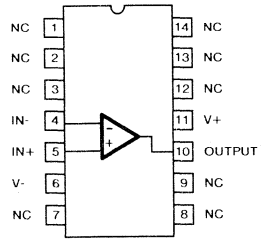
HA-5190/5195 are monolithic operational amplifiers featuring an ultimate combination of speed, precision, and bandwidth. Employing monolithic bipolar construction coupled with Dielectric Isolation, these devices are capable of delivering an unparalleled 200V/μs slew rate with a settling time of 70ns (0.1%, 5V output step). These truly differential amplifiers are designed to operate at gains ≥ 5 without the need for external compensation. Other oustanding HA-5190/5195 features are 150MHz gain-bandwidth-product and 6.5MHz full power bandwidth. In addition to these dynamic characteristics, these amplifiers also have excellent input characteristics such as 3mV offset voltage and 6.0nV/$\sqrt{Hz}$ input voltage noise at 1kHz.

With 200V/μs slew rate and 70ns settling time, these devices make ideal output amplifiers for accurate, high speed D/A converters or the main components in high speed sample/hold circuits. The 5190/5195 are also ideally suited for a variety of pulse and wideband video amplifiers. Please refer to Application Notes 525 and 526 for some of these application designs.

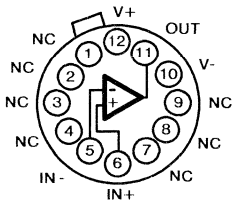
The HA-5190 is specified over the -55°C to +125°C range while the HA-5195 is specified from 0°C to +75°C. The HA-5190/5195 are available in 12 pin Metal Can (TO-8) and 14 pin Ceramic DIP packages. At temperatures above +75°C a heat sink is required for the HA-5190 (see Note 2 and Application Note 556). For military versions, please request the HA-5190/883 Data Sheet.

Pinouts

HA1-5190/5195 (CERAMIC DIP)
TOP VIEW

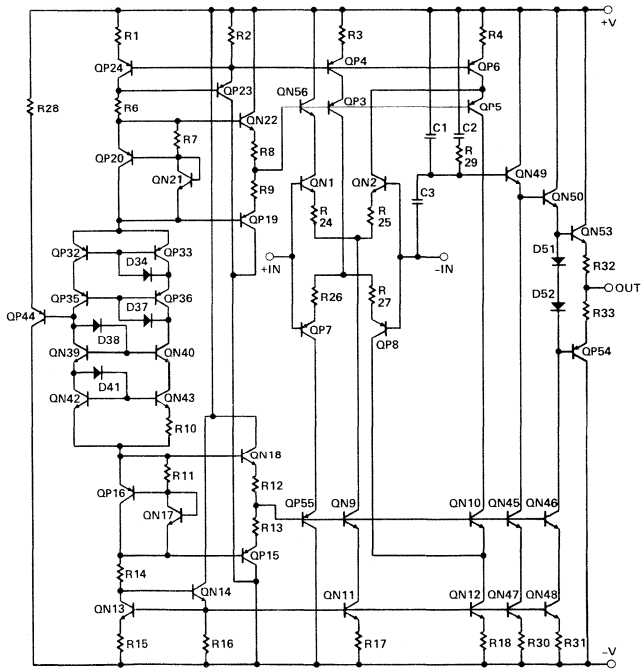


HA2-5190/5195 (TO-8 METAL CAN)
TOP VIEW



Case Tied To V-

Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Terminals 35V
Differential Input Voltage ..... ±6V
Output Current ..... 50mA (Peak)
Internal Power Dissipation (Note 2) ..... 870mW (Cerdip); 1W (TO-8) Free Air
Maximum Junction Temperature (Note 2) ..... +175°C

Operating Temperature Ranges

HA-5190-2 ..... $-55^{o}C \leq T_A \leq +125^{o}C$
HA-5190-5 ..... $0^{o}C \leq T_A \leq +75^{o}C$
Storage Temperature Range ..... $-65^{o}C \leq T_A \leq +150^{o}C$

Electrical Specifications

$V_{SUPPLY} = \pm 15V$; $R_L = 200\Omega$, Unless Otherwise Specified.

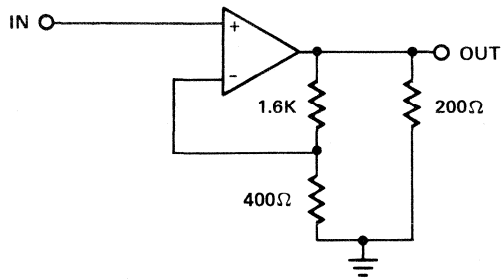
PARAMETER	TEMP	HA-5190-2 -55°C to +125°C			HA-5190-5 0°C to +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Offset Voltage	+25°C	-	3	5	-	3	6	mV
	Full	-	-	10	-	-	10	mV
Average Offset Voltage Drift	Full	-	20	-	-	20	-	µV/°C
Bias Current	+25°C	-	5	15	-	5	15	µA
	Full	-	-	20	-	-	20	µA
Offset Current	+25°C	-	1	4	-	1	4	µA
	Full	-	-	6	-	-	6	µA
Input Resistance	+25°C	-	10	-	-	10	-	kΩ
Input Capacitance	+25°C	-	1	-	-	1	-	pF
Common Mode Range	Full	±5	-	-	±5	-	-	V
Input Noise Current (f = 1kHz, Rg = 0Ω)	+25°C	-	5	-	-	5	-	$pA/\sqrt{Hz}$
Input Noise Voltage (f = 1kHz, Rg = 0Ω)	+25°C	-	6	-	-	6	-	$nV/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Notes 3)	+25°C	15K	30K	-	10K	30K	-	V/V
	Full	5K	-	-	5K	-	-	V/V
Common Mode Rejection Ratio (Note 4)	Full	74	95	-	74	95	-	dB
Minimum Stable Gain	+25°C	5	-	-	5	-	-	V/V
Gain-Bandwidth-Product (Notes 5 & 6)	+25°C	-	150	-	-	150	-	MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 3)	Full	±5	±8	-	±5	±8	-	V
Output Current (Note 3)	+25°C	±25	±30	-	±25	±30	-	mA
Output Resistance	+25°C	-	30	-	-	30	-	Ω
Full Power Bandwidth (Note 3 & 7)	+25°C	5	6.5	-	5	6.5	-	MHz
TRANSIENT RESPONSE (Note 8)								
Rise Time	+25°C	-	13	18	-	13	18	ns
Overshoot	+25°C	-	8	-	-	8	-	%
Slew Rate	+25°C	160	200	-	160	200	-	V/µs
Settling Time:								
5V Step to 0.1%	+25°C	-	70	-	-	70	-	ns
5V Step to 0.01%	+25°C	-	100	-	-	100	-	ns
2.5V Step to 0.1%	+25°C	-	50	-	-	50	-	ns
2.5V Step to 0.01%	+25°C	-	80	-	-	80	-	ns
POWER SUPPLY CHARACTERISTICS								
Supply Current	Full	-	19	28	-	19	28	mA
Power Supply Rejection Ratio (Note 9)	Full	70	90	-	70	90	-	dB

NOTES:

1. Absolute Maximum Ratings are limiting values applied individually beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Recommended heat sinks: For TO-8 Metal Can, Thermalloy #2240A ($\theta_{SA} = 27^{o}C/W$) or #2268B ($\theta_{SA} = 24^{o}C/W$). For 14 pin Ceramic DIP: AAVID #5602B ($\theta_{SA} = 16^{o}C/W$). See Die Characteristics Section for θ_{ja}/θ_{jc} values.
3. $R_L = 200\Omega$, $C_L < 10pF$, $V_{OUT} = \pm 5V$.
4. $\Delta V_{CM} = \pm 5V$.
5. $V_{OUT} = 90mV$.
6. $A_V = 10$.
7. Full power bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$.
8. Refer to Test Circuits section of data sheet.
9. $\Delta V_{SUPPLY} = \pm 10V$ D.C. to $\pm 20V$ D.C.

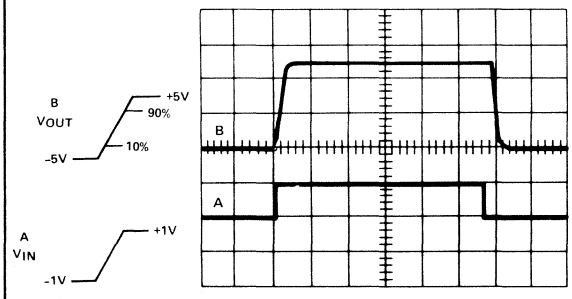
Test Circuits

LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT*

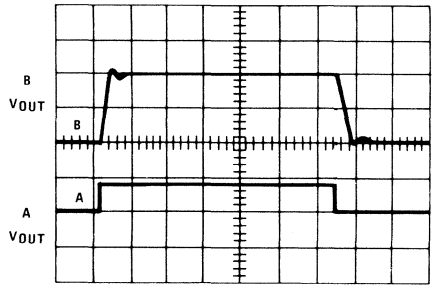


$A_V = 5$
* $C_L < 10pF$

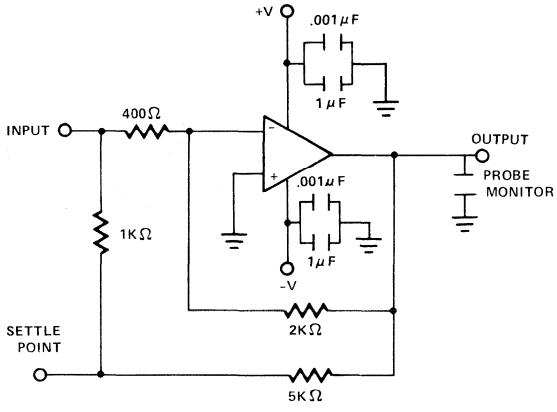
LARGE SIGNAL RESPONSE
Vertical Scale: (Volts: A = 2.0V/Div., B = 4.0/Div.)
Horizontal Scale: (Time: 100ns/Div.)



SMALL SIGNAL RESPONSE
Vertical Scale: (Volts: A = 50mV/Div., B = 100mV/Div.)
Horizontal Scale: (Time: 100ns/Div.)



SETTLING TIME TEST CIRCUIT

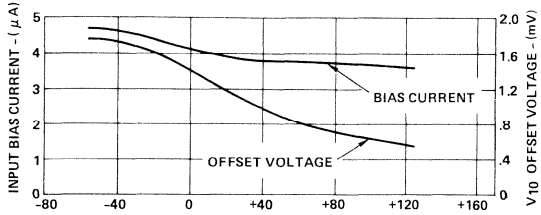


- $A_V = -5$
- Load Capacitance should be less than 10pF.
- It is recommended that resistors be carbon composition and that feedback and summing network ratios be matched to 0.1%.
- Settle Point (Summing Node) capacitance should be less than 10pF. For optimum settling time results, it is recommended that the test circuit be constructed directly onto the device pins. A Tektronix 568 Sampling Oscilloscope with S-3A sampling heads is recommended as a settle point monitor.

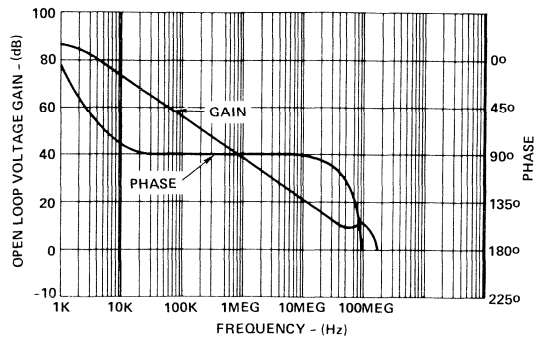
Typical Performance Curves

V+ = +15V, V- = -15V, T_A = +25°C, Unless Otherwise Specified.

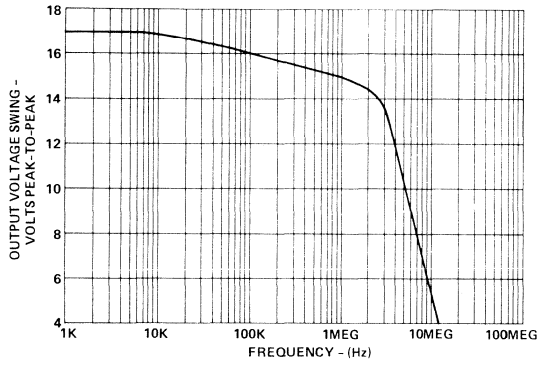
INPUT OFFSET VOLTAGE AND BIAS CURRENT vs. TEMPERATURE



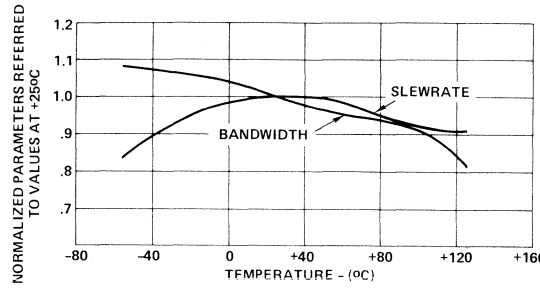
OPEN LOOP FREQUENCY RESPONSE



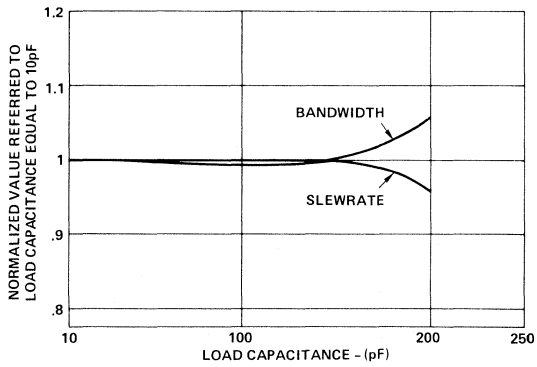
OUTPUT VOLTAGE SWING vs. FREQUENCY



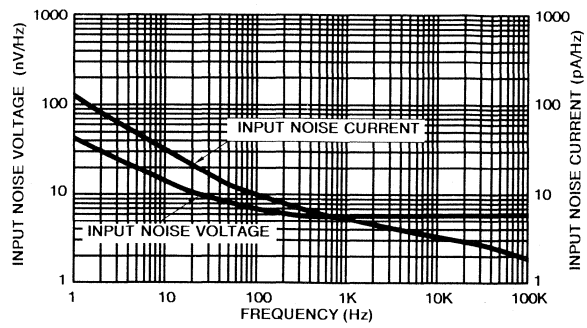
NORMALIZED AC PARAMETERS vs. TEMPERATURE



NORMALIZED AC PARAMETERS vs. LOAD CAPACITANCE

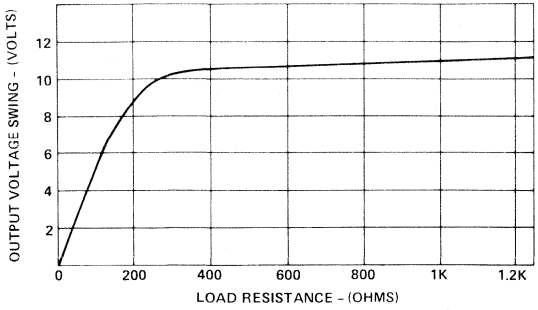


INPUT NOISE VOLTAGE AND NOISE CURRENT vs. FREQUENCY

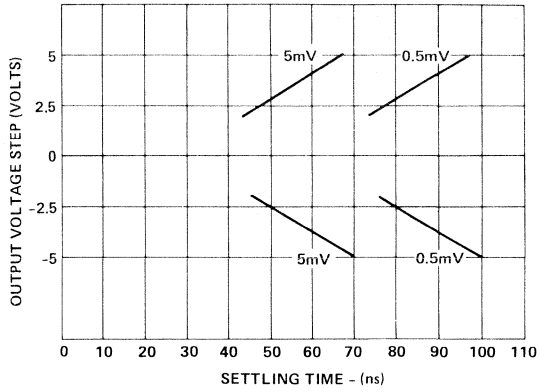


Typical Performance Curves (Continued)

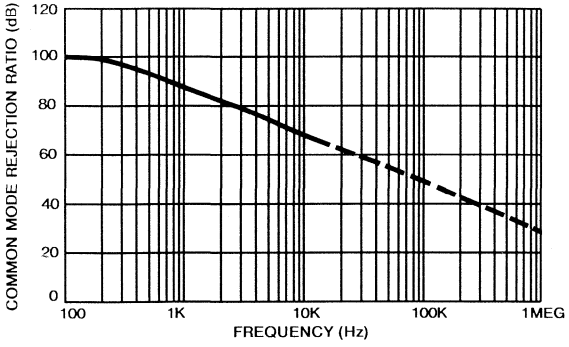
OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE



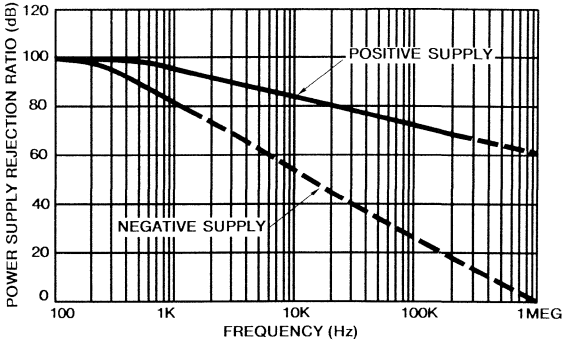
SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES



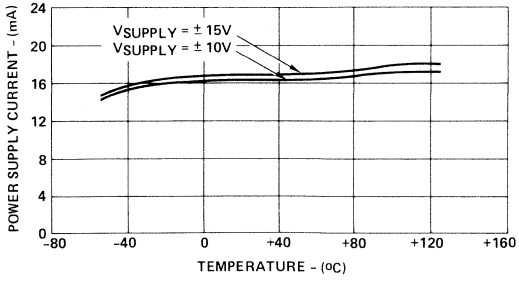
COMMON MODE REJECTION RATIO vs. FREQUENCY



POWER SUPPLY REJECTION RATIO vs. FREQUENCY



POWER SUPPLY CURRENT vs. TEMPERATURE



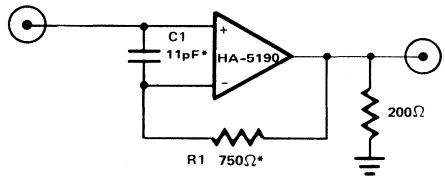
Applying the HA-5190/5195

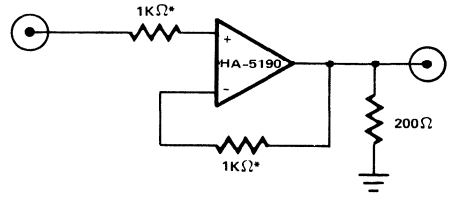
1. POWER SUPPLY DECOUPLING: Although not absolutely necessary, it is recommended that all power supply lines be decoupled with 0.01μF ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.
2. STABILITY CONSIDERATIONS: HA-5190/5195 is stable at gains ≥ 5. Gains < 5 are covered elsewhere in this data sheet. Feedback resistors should be of carbon composition located as near to the input terminals as possible.
3. WIRING CONSIDERATIONS: Video pulse circuits should be built on a ground plane. Minimum point to point connections directly to the amplifier terminals should be used. When ground planes cannot be used, good single point grounding techniques should be applied.
4. OUTPUT SHORT CIRCUIT: HA-5190/5195 does not have output short circuit protection. Short circuits to ground can be tolerated for approximately 10 seconds. Short circuits to either supply will result in immediate destruction of the device.
5. HEAVY CAPACITIVE LOADS: When driving heavy capacitive loads (≥ 100pF) a small resistor (≈100Ω) should be connected in series with the output and inside the feedback loop.

Typical Applications (Also see Application Notes 525 and 526)

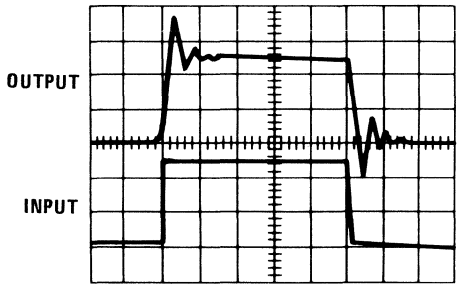
SUGGESTED COMPENSATION FOR UNITY GAIN STABILITY:

NONINVERTING

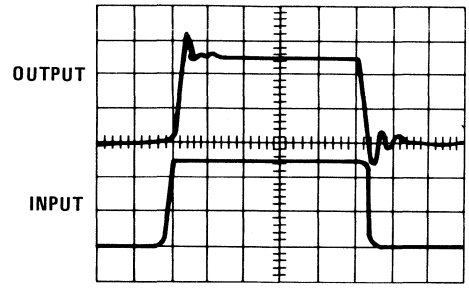




Vertical Scale: (Volts: 2V/Div.)
Horizontal Scale: (Time: 100ns/Div.)



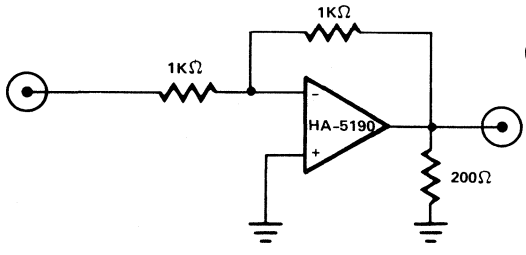
Vertical Scale: (Volts: 2V/Div.)
Horizontal Scale: (Time: 100ns/Div.)

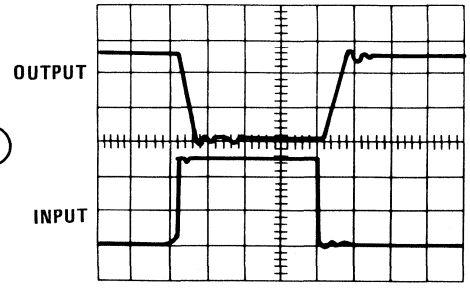


* Values were determined experimentally for optimum speed and settling time. R1 and C1 should be optimized for each particular application to ensure best overall frequency response.

INVERTING

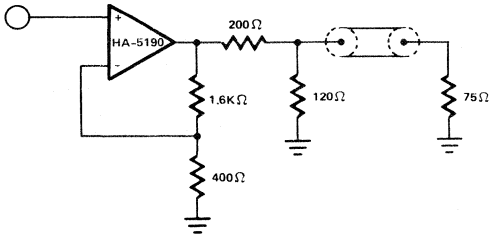
Vertical Scale: (Volts: 2V/Div.)
Horizontal Scale: (50ns/Div.)



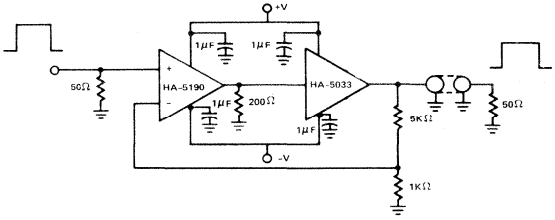


Typical Applications (Continued)

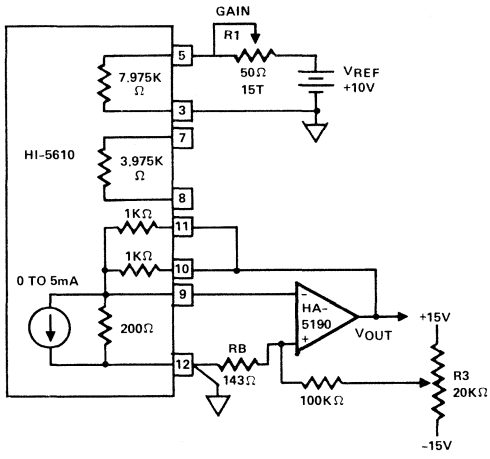
VIDEO PULSE AMPLIFIER/75Ω COAXIAL DRIVER



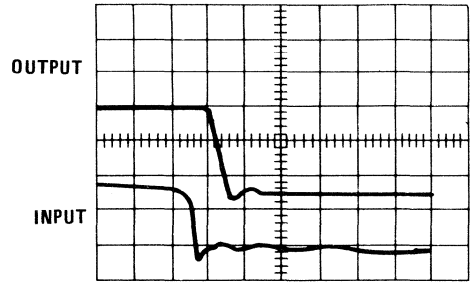
VIDEO PULSE AMPLIFIER COAXIAL LINE DRIVER



FAST DAC OUTPUT BUFFER



Vertical Scale: (Volts: 2V/Div.)
Horizontal Scale: (Time: 50ns/Div.)
B = V_{OUT} C = Digital Input



* Time delay between B and C represents total time delay for 0V to +5V full scale coded change.

Die Characteristics

Transistor Count 49

Die Dimensions ..... 0.087 x 0.052 x 0.019 inches (2210 x 1320 x 483 μm)

Substrate Potential (Powered Up)* ..... V-

Process ..... High Frequency Bipolar Dielectric Isolation

Passivation ..... Nitride

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
Ceramic DIP	104	48
Metal Can	87	32

*The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.

ANALOG

CMOS Analog Switches

3

ABSOLUTE MAXIMUM RATINGS

As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Specifications" are the only conditions recommended for satisfactory operation.

Ordering Information

HARRIS PRODUCT CODE EXAMPLE

H I 7 — 201HS — 5

PREFIX:
H (HARRIS)

FAMILY:
A : Analog
C : Communications
D : Digital
I : Interface
M : Memory
V : Analog High Voltage

PACKAGE:
1 : Dual-In-Line Ceramic
2 : Metal Can
3 : Dual-In-Line Plastic
7 : Mini-DIP, Ceramic
0 : Chip Form

PART NUMBER

TEMPERATURE:
2 : -55°C to +125°C
4 : -25°C to +85°C
5 : 0°C to +75°C
7 : Dash-7 High Reliability Commercial Product 0°C to +75°C Includes 96 Hour Burn-In

These products are available fully screened to Mil-Std-883C. Contact a Harris Sales Office for a copy of the /883 data sheet.

Standard Products Packaging Availability†

PACKAGE	PLASTIC DIP 3-	CERAMIC DIP 1-				CERAMIC MINI-DIP 7-			METAL CAN 2-		
TEMPERATURE	**-5**	**-2**	**-4**	**-5**	**-7**	**-2**	**-4**	**-5**	**-2**	**-4**	**-5**
DEVICE NUMBER											
HI-200	N	B1	B1	B1	B1				X	X	X
HI-201	O	C1	C1	C1	C1						
HI-201HS	O	C1	C1	C1	C1						
HI-300	N	B1		B1	B1				X		X
HI-301	N	B1		B1	B1				X		X
HI-302	N	B1		B1	B1						
HI-303	N	B1		B1	B1						
HI-304	N	B1		B1	B1				X		X
HI-305	N	B1		B1	B1				X		X
HI-306	N	B1		B1	B1						
HI-307	N	B1		B1	B1						
HI-381	N	B1		B1	B1				X		X
HI-384	N	B1		B1	B1						
HI-387	N	B1		B1	B1				X		X
HI-390	N	B1		B1	B1						
HI-5040	O	C1		C1	C1						
HI-5041	O	C1		C1	C1						
HI-5042	O	C1		C1	C1						
HI-5043	O	C1		C1	C1						
HI-5044	O	C1		C1	C1						
HI-5045	O	C1		C1	C1						
HI-5046	O	C1		C1	C1						
HI-5046A	O	C1		C1	C1						
HI-5047	O	C1		C1	C1						
HI-5047A	O	C1		C1	C1						
HI-5048	O	C1		C1	C1						
HI-5049	O	C1		C1	C1						
HI-5050	O	C1		C1	C1						
HI-5051	O	C1		C1	C1						

† Letter codes in this chart indicate available packages as shown in Packaging Section 11.

Analog Switches Glossary

ANALOG SIGNAL RANGE ($\pm V_S$) - The maximum safe input voltage range.

BREAK-BEFORE-MAKE-DELAY (t_{OPEN}) - The elapsed time between the turn-off of one switch and the corresponding turn-on of another switch for a common change in logic state. This delay is measured between the 50% points of the output transitions.

CHANNEL INPUT CAPACITANCE (C_{SOFF}) - The capacitance between the analog input and ground with the channel "OFF". This capacitance consists primarily of the source-body capacitance.

CHANNEL OUTPUT CAPACITANCE (C_{DOFF}) - The capacitance between the analog output and ground with the channel "OFF". This capacitance consists of the sum of the drain-body capacitances.

CHANNEL OUTPUT CAPACITANCE (C_{DON}) - The capacitance between the analog output and ground with the channel "ON".

CHARGE INJECTION - The amount of charge transferred to a specified load capacitance due to the switch changing state.

CROSSTALK - The amount of cross coupling from an "OFF" analog input to the output of another "ON" channel output.

DIGITAL INPUT CAPACITANCE - The capacitance between a digital input and ground.

INPUT LOW LEAKAGE CURRENT (I_{AL}) - The current measured at the digital input with a logic low applied.

INPUT LOW THRESHOLD (V_{AL}) - The maximum allowable voltage that can be applied to the digital inputs and still be recognized by the device as a low input.

INPUT HIGH LEAKAGE CURRENT (I_{AH}) - The current measured at the digital input with a logic high applied.

INPUT HIGH THRESHOLD (V_{AH}) - The minimum voltage that can be applied to the digital inputs and still be recognized by the device as a high input.

INPUT TO OUTPUT CAPACITANCE (CD_{SOFF}) - The capacitance between the analog input and output when the channel is "OFF".

"OFF" INPUT LEAKAGE CURRENT (I_{SOFF}) - The current measured at the input of an "OFF" channel with a specified voltage applied to both input and output. This current consists largely of the diode leakage current of the source-body junctions.

OFF ISOLATION - The feedthrough of an applied signal through an "OFF" switch to the output. This feedthrough occurs through the source-body and drain-body capacitances and has a greater effect at high frequencies.

"OFF" OUTPUT LEAKAGE CURRENT (I_{DOFF}) - The current measured at the output of an "OFF" channel with a specified voltage applied to both input and output. This current is due largely to the diode leakages of the drain-body junctions.

"ON" CHANNEL LEAKAGE CURRENT (I_{DON}) - The current flowing through the source-body and drain-body junctions of the "ON" channel. This current is measured with a specified voltage applied to both the input and output.

"ON" RESISTANCE (R_{ON}) - The series "ON" channel resistance measured between the input and output terminals under a specified range of input voltages.

SUPPLY CURRENT (I_S) - The current required from the power supply to operate the switch in a no load condition.

SWITCH TURN "OFF" TIME (t_{OFF}) - The time required to deactivate an "ON" switch to an "OFF" state. This time is measured from the 50% point of the logic input change to the time the output reaches 10% of the initial value.

SWITCH TURN "ON" TIME (t_{ON}) - The time required to activate an "OFF" switch to an "ON" state. This time is measured for the 50% point of the logic input to the time the output reaches 90% of the final value.

Selection Guide

CMOS SWITCHES

FUNCTION	DEVICE	R_{ON} (Ω) (TYPICAL)	$I_{D(OFF)}$ (nA) (TYPICAL)	$t_{(ON)}$ (ns) (TYPICAL)	$t_{(OFF)}$ (ns) (TYPICAL)	P_D (mW) (TYPICAL)
SPST	HI-5040	50	0.5	370	280	1.5
2 x SPST	HI-200	55	1	240	180	15
	HI-300	35	0.04	210	160	1
	HI-304	35	0.04	210	160	0.3
	HI-381	35	0.04	210	160	1
	HI-5048	25	0.5	370	280	1.5
	HI-5041	50	0.5	370	280	1.5
4 x SPST	HI-201	55	1	180	155	15
	HI-201HS	30	0.3	30	40	120
SPDT	HI-301	35	0.04	210	160	1
	HI-305	35	0.04	210	160	0.3
	HI-387	35	0.04	210	160	1
	HI-5050	25	0.5	370	280	1.5
	HI-5042	50	0.5	370	280	1.5
2 x SPDT	HI-303	35	0.04	210	160	1
	HI-307	35	0.04	210	160	0.3
	HI-390	35	0.04	210	160	1
	HI-5051	25	0.5	370	280	1.5
	HI-5043	50	0.5	370	280	1.5
DPST	HI-5044	50	0.5	370	280	1.5
2 x DPST	HI-302	35	0.04	210	160	1
	HI-306	35	0.04	210	160	0.3
	HI-384	35	0.04	210	160	1
	HI-5049	25	0.5	370	280	1.5
	HI-5045	50	0.5	370	280	1.5
DPDT	HI-5046A	25	0.5	370	280	1.5
	HI-5046	50	0.5	370	280	1.5
4PST	HI-5047A	25	0.5	370	280	1.5
	HI-5047	50	0.5	370	280	1.5

NOTE: All data represents typical room temperature specifications at ±15V supplies. For guaranteed and tested specifications, consult the device data sheet.

Dual SPST CMOS Analog Switch

Features

- **Analog Voltage Range** ..... **±15V**
- **Analog Current Range** **80mA**
- **Turn-On Time** **240ns**
- **Low R_{ON}** **55Ω**
- **Low Power Dissipation** **15mW**
- **TTL/CMOS Compatible**

Applications

- **High Frequency Analog Switching**
- **Sample and Hold Circuits**
- **Digital Filters**
- **Operational Amplifier Gain Switching Networks**

Description

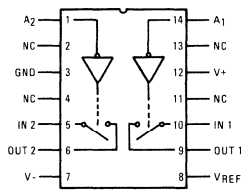
HI-200 is a monolithic device comprising two independently selectable SPST switches which feature fast switching speeds (240ns) combined with low power dissipation (15mW at +25°C). Each switch provides low "ON" resistance operation for input signal voltages up to the supply rails and for signal currents up to 80mA. Employing Dielectric Isolation and CMOS processing, HI-200 operates without any applications problems induced by latch-up or SCR mode phenomena.

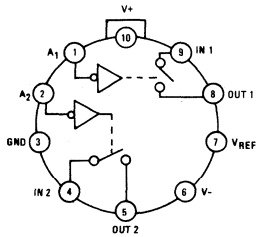
All devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. HI-200 is an ideal component for use in high frequency analog switching. Typical applications include signal path switching, sample and hold circuit, digital filters, and op amp gain switching networks.

HI-200 is available in DIP and (TO-99) Metal Cans. HI-200-2 is specified from -55°C to +125°C while HI-200-5 operates from 0°C to +75°C. HI-200 is functionally and pin compatible with other available "200 series" switches.

Pinouts

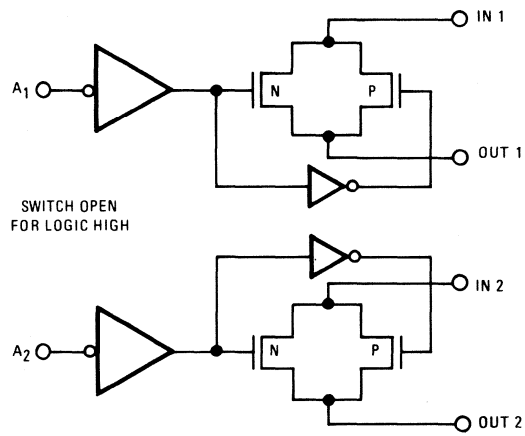
TOP VIEWS





CASE TIED TO V-

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings

Supply Voltage ..... 44V (±22)
V_{REF} to Ground ..... +20V, -5V
Digital Input Voltage ..... $+V_{SUPPLY}$ +4V
$-V_{SUPPLY}$ -4V
Analog Input Voltage (One Switch) ..... $+V_{SUPPLY}$ +2.0V
$-V_{SUPPLY}$ -2.0V
Total Power Dissipation* 450mW

Operating Temperature Range

HI-200-2 ..... -55°C to +125°C
HI-200-4 ..... -25°C to +85°C
HI-200-5 ..... 0°C to +75°C
Storage Temperature ..... -65°C to +150°C

*Derate 6mW/°C Above T_A = +75°C

Electrical Specifications

Unless Otherwise Specified: Supplies = +15V, -15V; V_{REF} = Open; V_{AH} (Logic Level High) = 2.4V, V_{AL} (Logic Level Low) = +0.8V

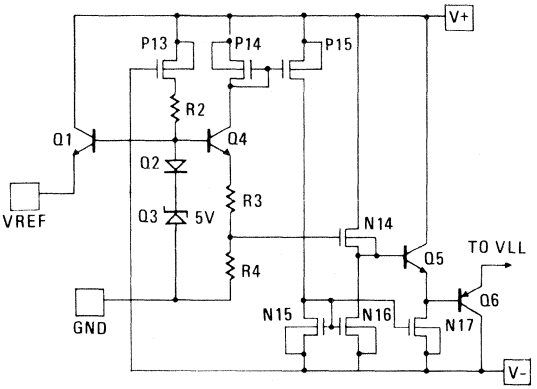
PARAMETER	TEMP	HI-200-2 -55°C to +125°C MIN	HI-200-2 -55°C to +125°C TYP	HI-200-2 -55°C to +125°C MAX	HI-200-5** 0°C to +75°C MIN	HI-200-5** 0°C to +75°C TYP	HI-200-5** 0°C to +75°C MAX	UNITS
ANALOG SWITCH CHARACTERISTICS								
V_S, Analog Signal Range	Full	-15	-	+15	-15	-	+15	V
R_{ON}, On Resistance (Note 1)	+25°C	-	55	70	-	55	80	Ω
	Full	-	80	100	-	72	100	Ω
$I_{S(OFF)}$, Off Input Leakage Current (Note 6)	+25°C	-	1	5	-	1	50	nA
	Full	-	100	500	-	10	500	nA
$I_{D(OFF)}$, Off Output Leakage Current (Note 6)	+25°C	-	1	5	-	1	50	nA
	Full	-	100	500	-	10	500	nA
$I_{D(ON)}$, On Leakage Current (Note 6)	+25°C	-	1	5	-	1	50	nA
	Full	-	100	500	-	10	500	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full	-	-	0.8	-	-	0.8	V
V_{AH}, Input High Threshold	Full	2.4	-	-	2.4	-	-	V
I_A, Input Leakage Current (High or Low) (Note 2)	Full	-	-	1.0	-	-	1.0	µA
SWITCHING CHARACTERISTICS								
t_{OPEN}, Break-Before Make Delay (Note 3)	+25°C	-	60	-	-	60	-	ns
t_{ON}, Switch On Time	+25°C	-	240	500	-	240	-	ns
t_{OFF}, Switch Off Time	+25°C	-	330	500	-	500	-	ns
"Off Isolation" (Note 4)	+25°C	-	70	-	-	70	-	dB
$C_{S(OFF)}$, Input Switch Capacitance	+25°C	-	5.5	-	-	5.5	-	pF
$C_{D(OFF)}$, Output Switch Capacitance	+25°C	-	5.5	-	-	5.5	-	pF
$C_{D(ON)}$, Output Switch Capacitance	+25°C	-	11	-	-	11	-	pF
C_A, Digital Input Capacitance	+25°C	-	5	-	-	5	-	pF
$C_{DS(OFF)}$, Drain-To-Source Capacitance	+25°C	-	0.5	-	-	0.5	-	pF
POWER REQUIREMENTS (Note 5)								
P_D, Power Dissipation	+25°C	-	15	-	-	15	-	mW
	Full	-	-	60	-	-	60	mW
I^+, Current	+25°C	-	0.5	-	-	0.5	-	mA
	Full	-	-	2.0	-	-	2.0	mA
I^-, Current	+25°C	-	0.5	-	-	0.5	-	mA
	Full	-	-	2.0	-	-	2.0	mA

NOTES:
1. V_{OUT} = ±10V, I_{OUT} = 1mA
2. Digital Inputs are MOS gates — Typical Leakage is Less Than 1nA.
3. V_{AH} = 4.0V.
4. V_A = 5V, R_L = 1kΩ, C_L = 10pF, V_S = $3V_{RMS}$, f = 100kHz.
5. V_A = +3V or V_A = 0V for Both Switches.
6. Refer to Leakage Current Measurement Diagram on Page 3-8.

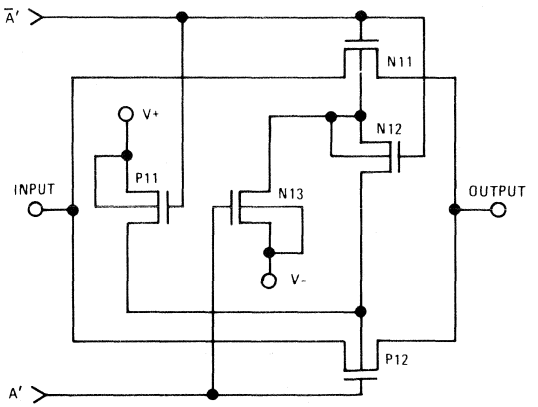
**NOTE: HI-200-4 Has Same Specifications as HI-200-5 Over the Temperature Range -20°C to +85°C.

Schematic Diagrams

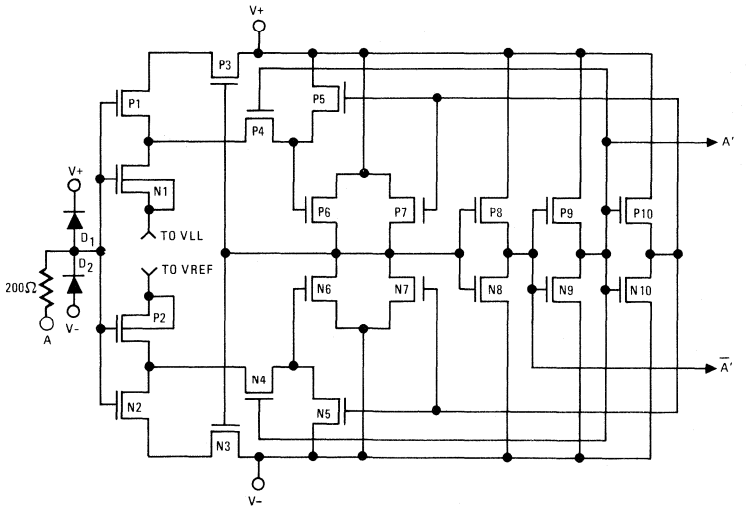
TTL/CMOS REFERENCE CIRCUIT
V-REF CELL



SWITCH CELL



DIGITAL INPUT BUFFER
AND LEVEL SHIFTER

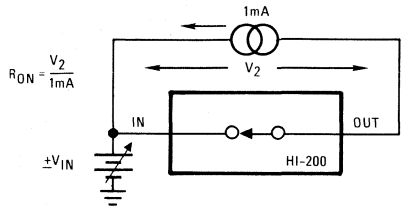


ALL N-CHANNEL BODIES TO V-
ALL P-CHANNEL BODIES TO V+
EXCEPT AS SHOWN.

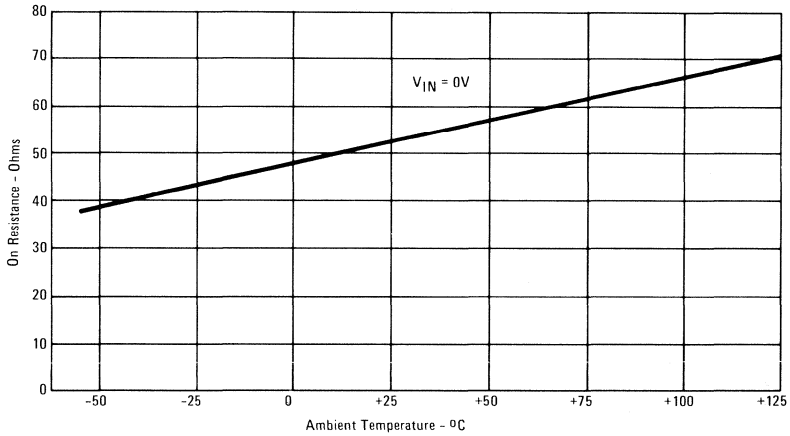
Performance Characteristics and Test Circuits

Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm 15V$, $V_{AH} = 2.4V$, $V_{AL} = 0.8V$ and V_{REF} = Open

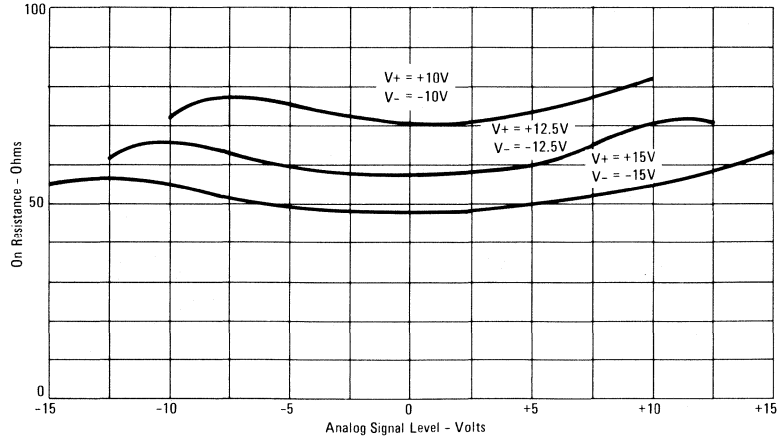
ON RESISTANCE vs. ANALOG SIGNAL LEVEL, SUPPLY VOLTAGE AND TEMPERATURE



ON RESISTANCE vs. TEMPERATURE

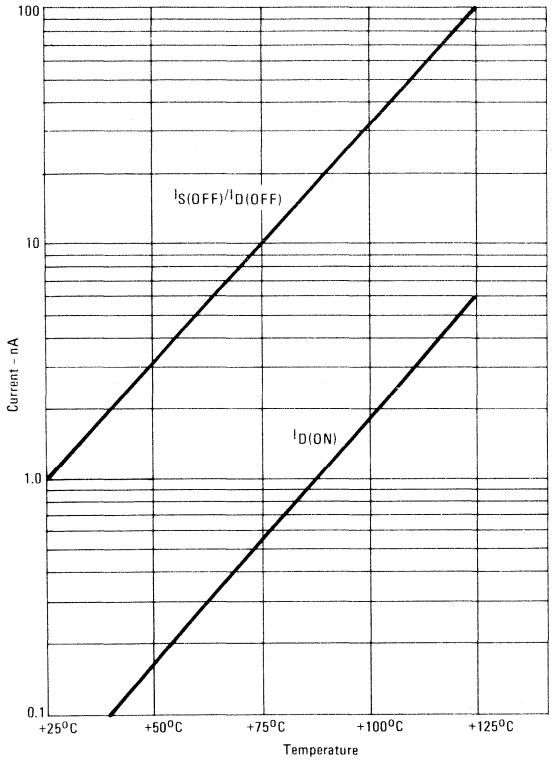


(HI-200)
ON RESISTANCE vs. ANALOG SIGNAL LEVEL AND POWER SUPPLY VOLTAGE

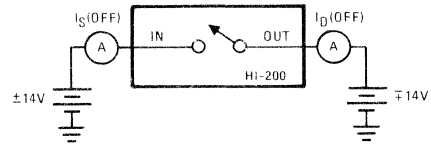


Performance Characteristics and Test Circuits (Continued)

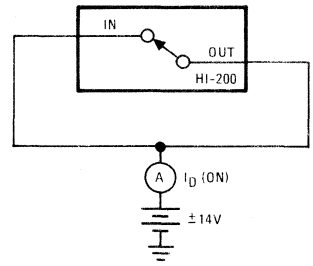
SWITCH LEAKAGE CURRENT vs. TEMPERATURE (HI-200)



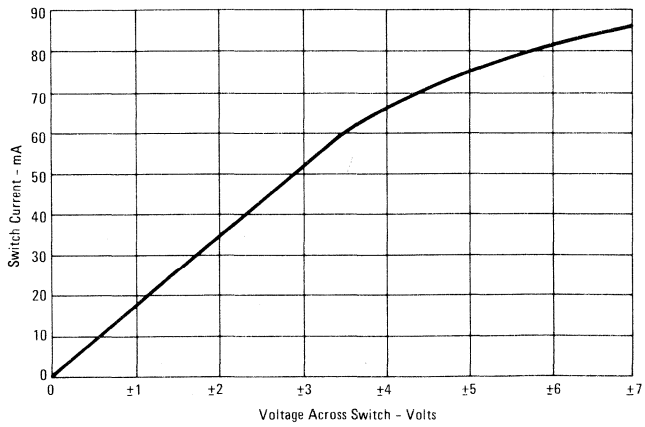
OFF LEAKAGE CURRENT vs. TEMPERATURE



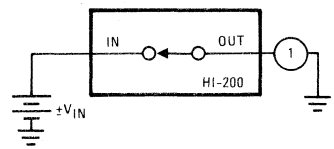
ON LEAKAGE CURRENT vs. TEMPERATURE



SWITCH CURRENT vs. VOLTAGE

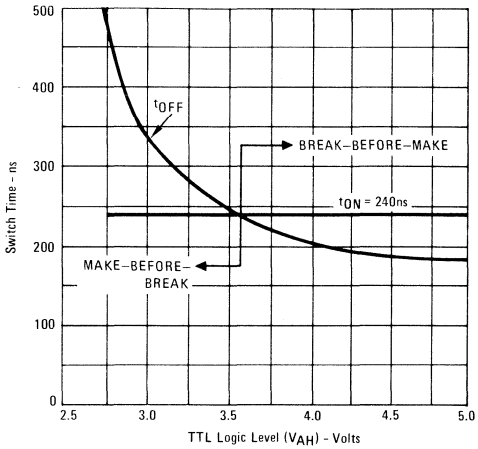


SWITCH CURRENT vs. VOLTAGE

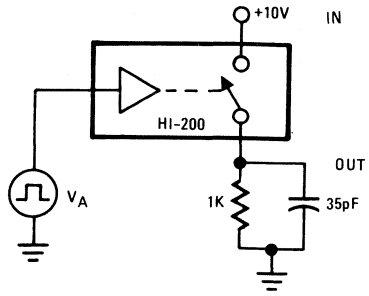


Performance Characteristics and Test Circuits (Continued)

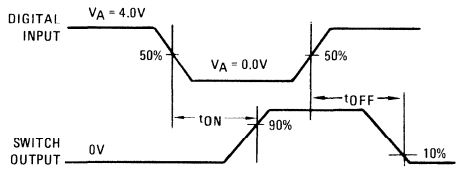
(HI-200)
SWITCH TIME vs. TTL LOGIC LEVEL



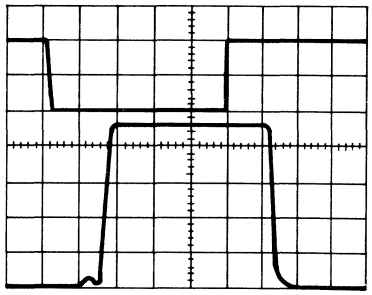
ON/OFF SWITCH TIME vs. LOGIC LEVEL



Switching Waveforms

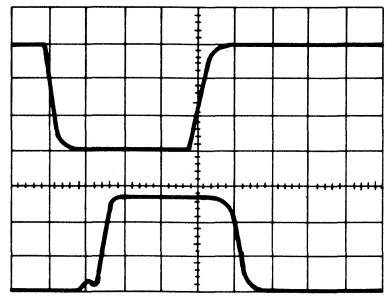


t_{ON}, t_{OFF} (TTL INPUT)
V_{AH} = +4.0V



TOP: TTL Input VERTICAL: 2V/Div.
BOTTOM: Output HORIZONTAL: 200ns/Div.

t_{ON}, t_{OFF} (CMOS INPUT)
V_{REF} = OPEN, V_{AH} = +15V



TOP: CMOS Input VERTICAL: 5V/Div.
BOTTOM: Output HORIZONTAL: 200ns/Div.

Quad SPST CMOS Analog Switch

Features

- **Analog Voltage Range** ..... **±15V**
- **Analog Current Range** **80mA**
- **Turn-On Time** **185ns**
- **Low R_{ON}** **55Ω**
- **Low Power Dissipation** **15mW**
- **TTL/CMOS Compatible**

Applications

- **High Frequency Analog Switching**
- **Sample and Hold Circuits**
- **Digital Filters**
- **Operational Amplifier Gain Switching Networks**

Description

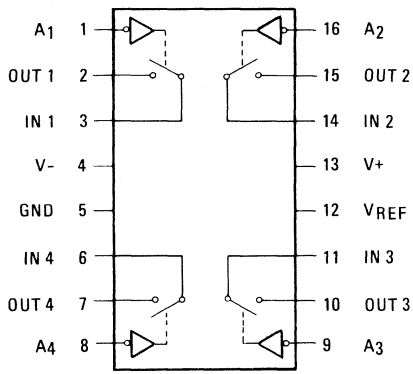
HI-201 is a monolithic device comprising four independently selectable SPST switches which feature fast switching speeds (185ns) combined with low power dissipation (15mW at +25°C). Each switch provides low "ON" resistance operation for input signal voltages up to the supply rails and for signal currents up to 80mA. Employing Dielectric Isolation and CMOS processing, HI-201 operates without any applications problems induced by latch-up or SCR mode phenomena.

All devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. HI-201 is an ideal component for use in high frequency analog switching. Typical applications include signal path switching, sample and hold circuit, digital filters, and op amp gain switching networks.

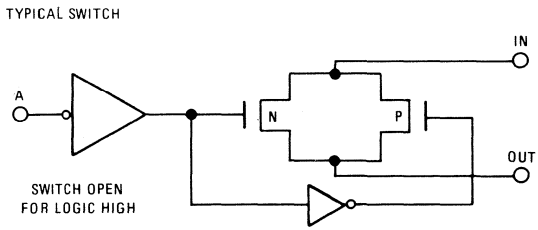
HI-201 is available in a 16 lead Dual-In-Line package. HI-201-2 is specified from -55°C to +125°C while HI-201-5 operates from 0°C to +75°C. HI-201 is functionally and pin compatible with other available "200 series" switches.

Pinout

HI1-201-X
TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings

Supply Voltage Between Pins 4 and 13 ..... 44V (±22)
V_{REF} to Ground ..... +20V, -5V
Digital Input Voltage ..... $+V_{SUPPLY}$ +4V
$-V_{SUPPLY}$ -4V
Analog Input Voltage (One Switch) ..... $+V_{SUPPLY}$ +2.0V
$-V_{SUPPLY}$ -2.0V
Analog Current — Continuous, Peak 30mA, 80mA
Total Dissipation* 750mW

Operating Temperature Range

HI-201-2 ..... -55°C to +125°C
HI-201-4 ..... -25°C to +85°C
HI-201-5 ..... 0°C to +75°C
Storage Temperature ..... -65°C to +150°C

*Derate 8mW/°C Above T_A = +75°C

Electrical Specifications

Unless Otherwise Specified: Supplies = +15V, -15V; V_{REF} = Open; V_{AH} (Logic Level High) = 2.4V, V_{AL} (Logic Level Low) = +0.8V
For Test Conditions Consult Peformance Characteristics

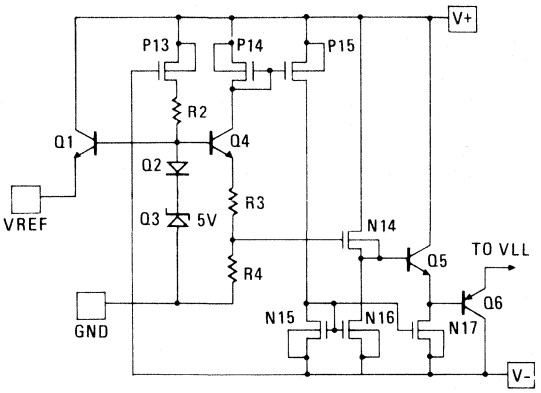
PARAMETER	TEMP	HI-201-2 -55°C to +125°C MIN	TYP	MAX	HI-201-5** 0°C to +75°C MIN	TYP	MAX	UNITS
ANALOG SWITCH CHARACTERISTICS								
V_S, Analog Signal Range	Full	-15	-	+15	-15	-	+15	V
R_{ON}, On Resistance (Note 1)	+25°C	-	55	70	-	55	80	Ω
	Full	-	80	100	-	75	100	Ω
$I_{S(OFF)}$, Off Input Leakage Current (Note 6)	+25°C	-	2	5	-	2	50	nA
	Full	-	-	500	-	-	250	nA
$I_{D(OFF)}$, Off Output Leakage Current (Note 6)	+25°C	-	2	5	-	2	50	nA
	Full	-	35	500	-	35	250	nA
$I_{D(ON)}$, On Leakage Current (Note 6)	+25°C	-	2	5	-	2	50	nA
	Full	-	-	500	-	-	250	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full	-	-	0.8	-	-	0.8	V
V_{AH}, Input High Threshold	Full	2.4	-	-	2.4	-	-	V
I_A, Input Leakage Current (High or Low) (Note 2)	Full	-	-	1.0	-	-	1.0	µA
SWITCHING CHARACTERISTICS								
t_{OPEN}, Break-Before Make Delay (Note 3)	+25°C	-	30	-	-	30	-	ns
t_{ON}, Switch On Time	+25°C	-	185	500	-	185	-	ns
	Full	-	1000	-	-	1000	-	ns
t_{OFF}, Switch Off Time	+25°C	-	220	500	-	220	-	ns
	Full	-	1000	-	-	1000	-	ns
"Off Isolation" (Note 4)	+25°C	-	80	-	-	80	-	dB
$C_{S(OFF)}$, Input Switch Capacitance	+25°C	-	5.5	-	-	5.5	-	pF
$C_{D(OFF)}$, Output Switch Capacitance	+25°C	-	5.5	-	-	5.5	-	pF
$C_{D(ON)}$, Output Switch Capacitance	+25°C	-	11	-	-	11	-	pF
C_A, Digital Input Capacitance	+25°C	-	5	-	-	5	-	pF
$C_{DS(OFF)}$, Drain-To-Source Capacitance	+25°C	-	0.5	-	-	0.5	-	pF
POWER REQUIREMENTS (Note 5)								
P_D, Power Dissipation	+25°C	-	15	-	-	15	-	mW
	Full	-	-	60	-	-	60	mW
I^+, Current (Pin 13)	+25°C	-	0.5	-	-	0.5	-	mA
	Full	-	-	2.0	-	-	2.0	mA
I^-, Current (Pin 4)	+25°C	-	0.5	-	-	0.5	-	mA
	Full	-	-	2.0	-	-	2.0	mA

NOTES:
1. V_{OUT} = ±10V, I_{OUT} = 1mA
2. Digital Inputs are MOS gates — Typical Leakage is Less Than 1nA.
3. V_{AH} = 4.0V.
4. V_A = 5V, R_L = 1kΩ, C_L = 10pF, V_S = $3V_{RMS}$, f = 100kHz.
5. V_A = +3V or V_A = 0V for All Switches.
6. Refer to Leakage Current Measurement Diagram on Page 3-8.

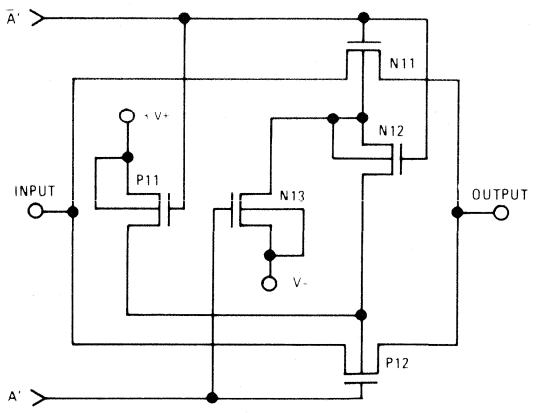
**NOTE: HI-201-4 Has Same Specifications as HI-201-5 Over the Temperature Range -25°C to +85°C.

Schematic Diagrams

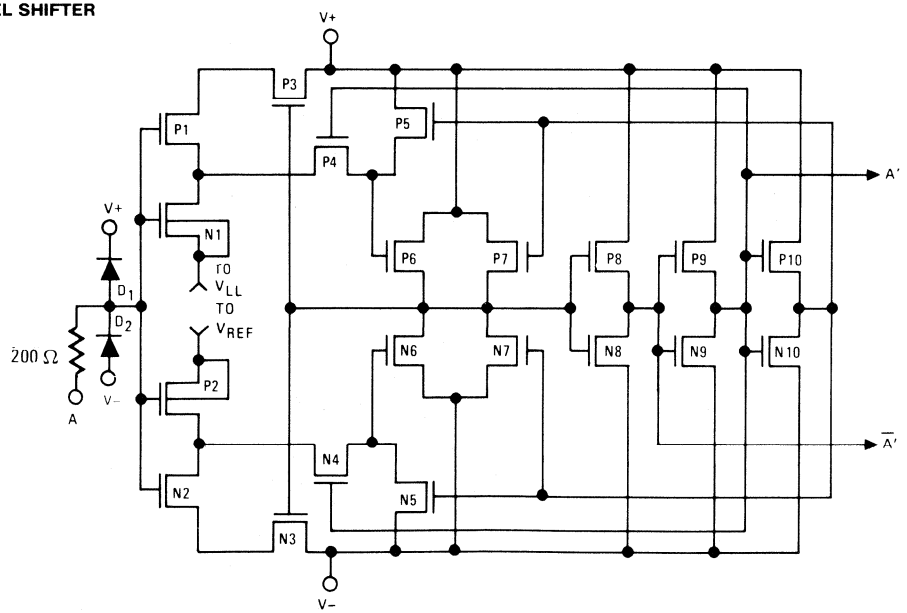
TTL/CMOS REFERENCE CIRCUIT V-REF CELL



SWITCH CELL



DIGITAL INPUT BUFFER AND LEVEL SHIFTER

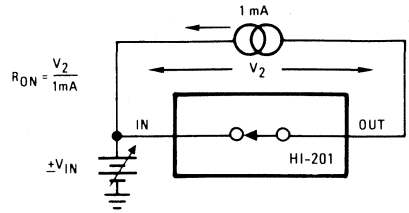


ALL N-CHANNEL BODIES TO V-
ALL P-CHANNEL BODIES TO V+
EXCEPT AS SHOWN.

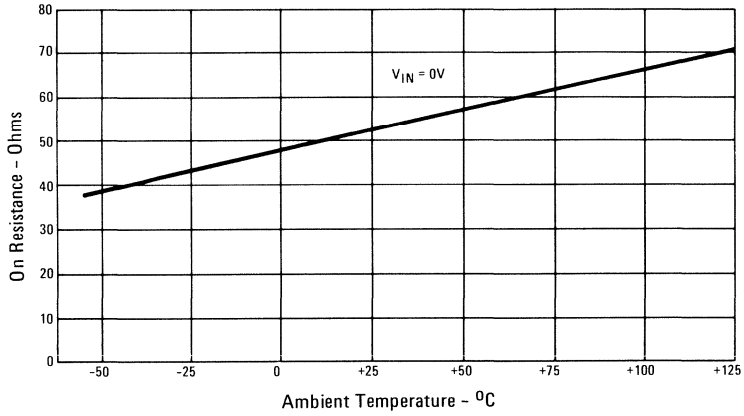
Performance Characteristics and Test Circuits

Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm 15V$, $V_{AH} = 2.4V$, $V_{AL} = 0.8V$ and V_{REF} = Open

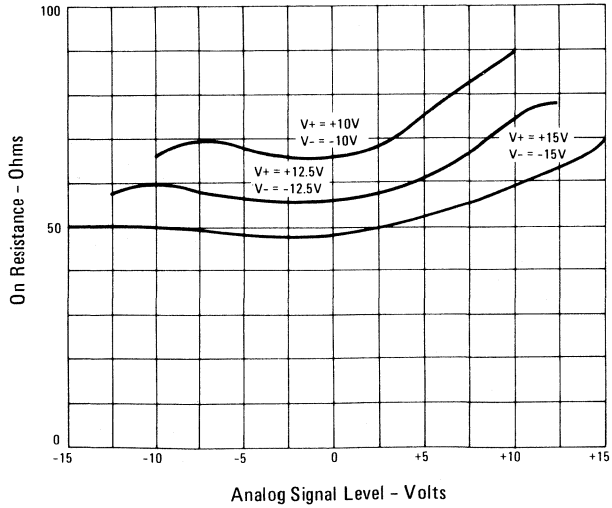
ON RESISTANCE vs. ANALOG SIGNAL LEVEL, SUPPLY VOLTAGE AND TEMPERATURE



ON RESISTANCE vs. TEMPERATURE

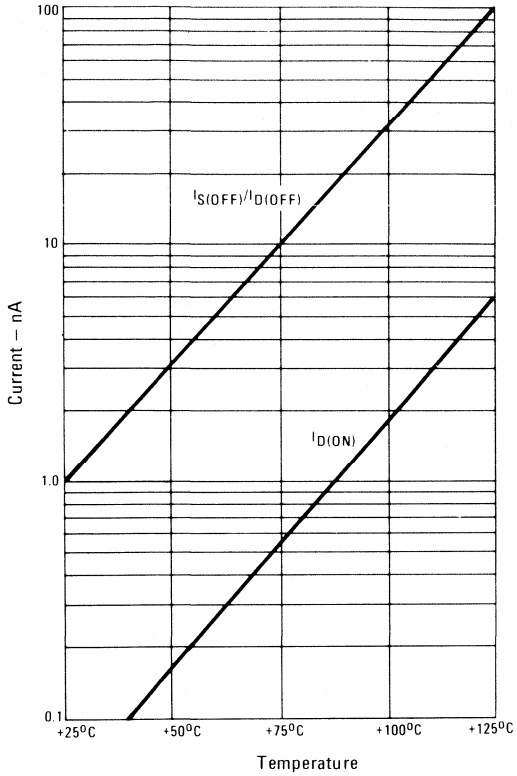


(HI-201)
ON RESISTANCE vs. ANALOG SIGNAL LEVEL AND POWER SUPPLY VOLTAGE

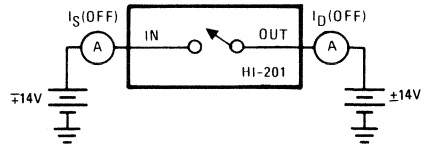


Performance Characteristics and Test Circuits (Continued)

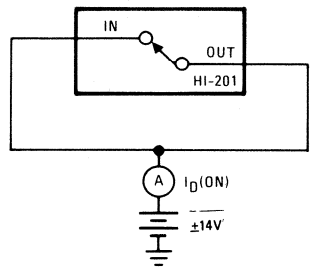
SWITCH LEAKAGE CURRENT vs. TEMPERATURE (HI-201)



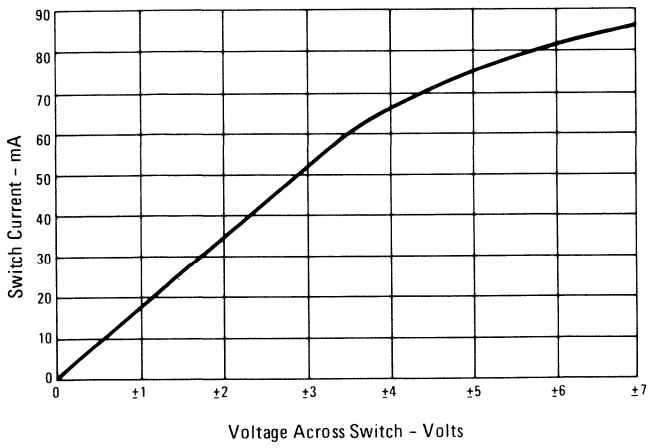
OFF LEAKAGE CURRENT vs. TEMPERATURE



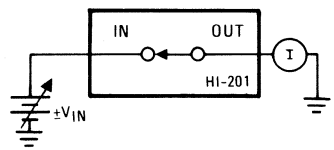
ON LEAKAGE CURRENT vs. TEMPERATURE



SWITCH CURRENT vs. VOLTAGE

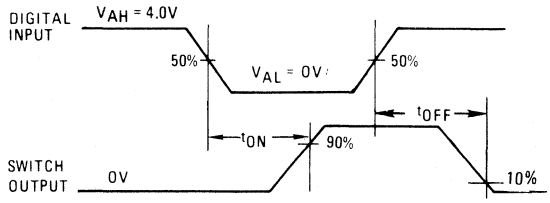


SWITCH CURRENT vs. VOLTAGE

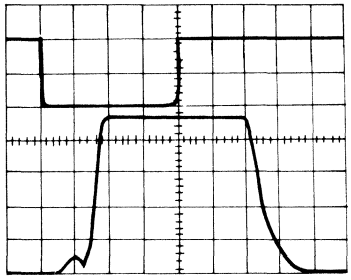


Switching Waveforms

LOGIC "0" = SWITCH ON

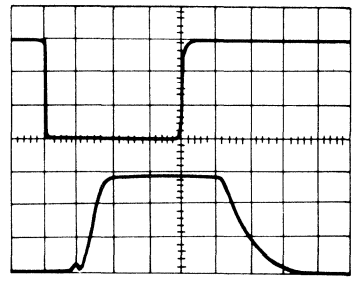


t_{ON}, t_{OFF} (TTL INPUT)
V_{IN} = +4.0V



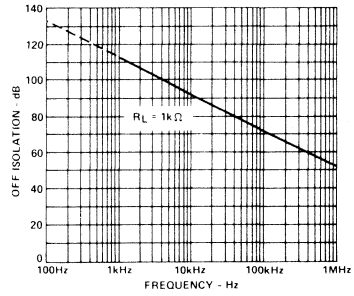
TOP: TTL Input VERTICAL: 2V/Div.
BOTTOM: Output HORIZONTAL: 100ns/Div.

t_{ON}, t_{OFF} (CMOS INPUT)
V_{REF} = OPEN, V_{IN} = +15V



TOP: CMOS Input VERTICAL: 5V/Div.
BOTTOM: Output HORIZONTAL: 100ns/Div.

OFF ISOLATION vs. FREQUENCY



For More Information See Application Notes 520, 521, 531, 532 and 557 in Section 10 of Data Book.

HI-201HS

High Speed Quad SPST CMOS Analog Switch

Features

- Fast Switching Times ..... t_{ON} = 30ns, t_{OFF} = 40ns
- Low "ON" Resistance 30Ω
- Pin Compatible with Standard HI-201
- Wide Analog Voltage Range (±15V Supplies) .. ±15V
- Low Charge Injection (±15V Supplies) 10pC
- TTL Compatible
- Symmetrical Switching Analog Current Range 80mA

Applications

- High Speed Multiplexing
- High Frequency Analog Switching
- Sample and Hold Circuits
- Digital Filters
- Operational Amplifier Gain Switching Networks
- Integrator Reset Circuits

Description

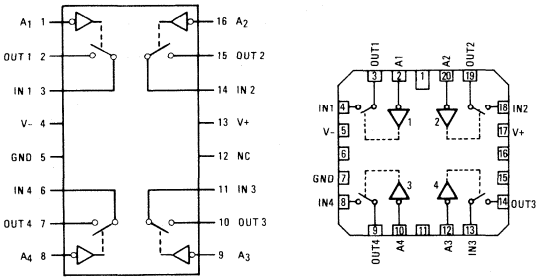
The HI-201HS is a monolithic CMOS Analog Switch featuring very fast switching speeds and low ON resistance. This integrated circuit consists of four independently selectable SPST switches and is pin compatible with the industry standard HI-201 switch.

Fabricated using silicon-gate technology and the Harris Dielectric Isolation process, this TTL compatible device offers improved performance over previously available CMOS analog switches. Featuring maximum switching times of 50ns, low ON resistance of 50Ω maximum, and a wide analog signal range, the HI-201HS is designed for any application where improved switching performance, particularly switching speed, is required. (A more detailed discussion on the design and application of the HI-201HS can be found in Application Note 543).

The HI-201HS is available in a 16 pin Ceramic DIP package. The HI-201HS-2 is specified over the temperature range from -55°C to +125°C and the HI-201HS-5 version from 0°C to +75°C. HI-201HS-4 is also offered from -25°C to +85°C.

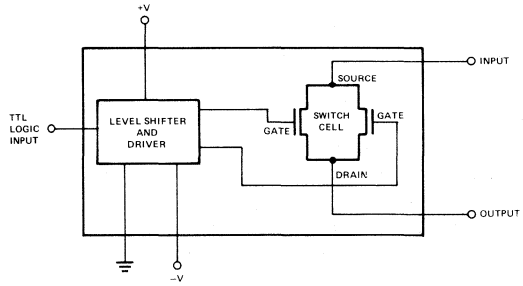
Pinout

TOP VIEW



LOGIC	SWITCH
0	ON
1	OFF

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings

Supply Voltage (Between Pins 4 and 13) 36V
Digital Input Voltage (Pins 1, 8, 9, 16) ..... $+V_{SUPPLY}$ +4V
$-V_{SUPPLY}$ -4V
Analog Input Voltage (One Switch) ..... $+V_{SUPPLY}$ +2.0V
Pins 2, 3, 6, 7, 10, 11, 14, 15 $-V_{SUPPLY}$ -2.0V
Analog Current — Continuous Peak 30mA, 80mA
Total Power Dissipation (Note 2) 750mW
Maximum Junction Temperature ..... +175°C

Operating Temperature Range

HI-201HS-2 ..... -55°C to +125°C
HI-201HS-4 ..... -25°C to +85°C
HI-201HS-5 ..... 0°C to +75°C
Storage Temperature ..... -65°C to +150°C

Electrical Specifications

Unless Otherwise Specified: Supplies = +15V, -15V; V_{AH} (Logic Level High) = 3.0V, V_{AL} (Logic Level Low) = +0.8V, GND = 0V

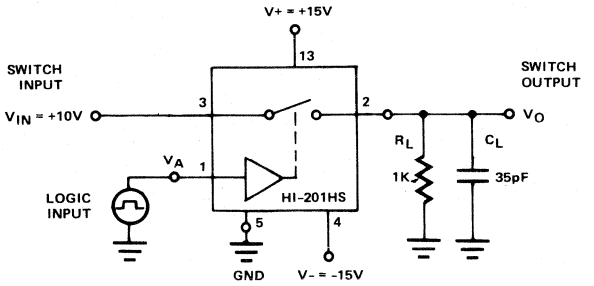
PARAMETER	TEMP	HI-201HS-2 MIN	HI-201HS-2 TYP	HI-201HS-2 MAX	HI-201HS-5/-4 MIN	HI-201HS-5/-4 TYP	HI-201HS-5/-4 MAX	UNITS
ANALOG SWITCH CHARACTERISTICS								
V_S, Analog Signal Range	Full	-15	-	+15	-15	-	+15	V
R_{ON}, On Resistance (Note 3)	+25°C	-	30	50	-	30	50	Ω
	Full	-	-	75	-	-	75	Ω
R_{ON} Match	+25°C	-	3	-	-	3	-	%
$I_{S(OFF)}$, Off Input Leakage Current	+25°C	-	0.3	1	-	0.3	1	nA
	Full	-	-	100	-	-	50	nA
$I_{D(OFF)}$, Off Output Leakage Current	+25°C	-	0.3	1	-	0.3	1	nA
	Full	-	-	100	-	-	50	nA
$I_{D(ON)}$, On Leakage Current	+25°C	-	0.1	1	-	0.1	1	nA
	Full	-	-	100	-	-	50	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full	-	-	0.8	-	-	0.8	V
V_{AH}, Input High Threshold	+25°C	2.0	-	-	2.0	-	-	V
	Full	2.4	-	-	2.4	-	-	V
I_{AL}, Input Leakage Current (Low)	+25°C	-	200	-	-	200	-	µA
	Full	-	-	-500	-	-	-500	µA
I_{AH}, Input Leakage Current (High)	+25°C	-	20	-	-	20	-	µA
	Full	-	-	+40	-	-	+40	µA
SWITCHING CHARACTERISTICS								
t_{ON}, Switch On Time (Note 4)	+25°C	-	30	50	-	30	50	ns
t_{OFF1}, Switch Off Time (Note 4)	+25°C	-	40	50	-	40	50	ns
t_{OFF2}, Switch Off Time (Note 4)	+25°C	-	150	-	-	150	-	ns
Output Settling Time 0.1%	+25°C	-	180	-	-	180	-	ns
"Off Isolation" (Note 5)	+25°C	-	72	-	-	72	-	dB
Crosstalk (Note 6)	+25°C	-	86	-	-	86	-	dB
Charge Injection (Note 7)	+25°C	-	10	-	-	10	-	pC
$C_{S(OFF)}$, Input Switch Capacitance	+25°C	-	10	-	-	10	-	pF
$C_{D(OFF)}$, Output Switch Capacitance	+25°C	-	10	-	-	10	-	pF
$C_{D(ON)}$, Output Switch Capacitance	+25°C	-	30	-	-	30	-	pF
C_A, Digital Input Capacitance	+25°C	-	18	-	-	18	-	pF
$C_{DS(OFF)}$, Drain-To-Source Capacitance	+25°C	-	0.5	-	-	0.5	-	pF
POWER REQUIREMENTS (Note 8)								
P_D, Power Dissipation	+25°C	-	120	-	-	120	-	mW
	Full	-	-	240	-	-	240	mW
I^+, Current (Pin 13)	+25°C	-	4.5	-	-	4.5	-	mA
	Full	-	-	10.0	-	-	10.0	mA
I^-, Current (Pin 4)	+25°C	-	3.5	-	-	3.5	-	mA
	Full	-	-	6	-	-	6	mA

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate 8mW/°C above T_A = +75°C, θ_{ja} = 100°C/W, θ_{jc} = 32°C/W.
3. V_{OUT} = ±10V, I_{OUT} = 1mA.
4. R_L = 1kΩ, C_L = 35pF, V_{IN} = +10V, V_A = +3V. (See Switching Waveforms).
5. V_A = 3V, R_L = 1kΩ, C_L = 10pF, V_{IN} = $3V_{RMS}$, f = 100kHz.
6. V_A = 3V, R_L = 1kΩ, V_{IN} = $3V_{RMS}$, f = 100kHz.
7. C_L = 1000pF, V_{IN} = 0V, R_{IN} = 0Ω, $\Delta Q = C_L \times \Delta V_O$.
8. V_A = 3V or V_A = 0 for all switches.
9. V_A = 4V.

Test Circuit

SWITCHING TEST CIRCUIT (t_{ON}, t_{OFF1}, t_{OFF2})

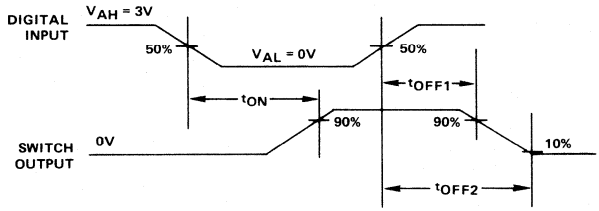


$$V_O = V_{IN} \frac{R_L}{R_L + R_{ON}}$$

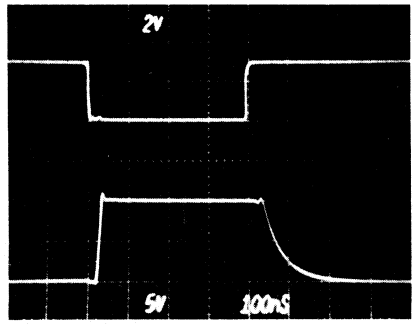
C_L INCLUDES $C_{FIXTURE} + C_{PROBE}$

Switching Waveforms

LOGIC "0" = SWITCH ON



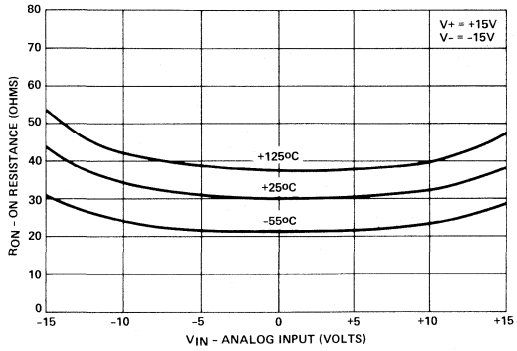
t_{ON}, t_{OFF}(TTL INPUT)
V_{AH} = +3.0V



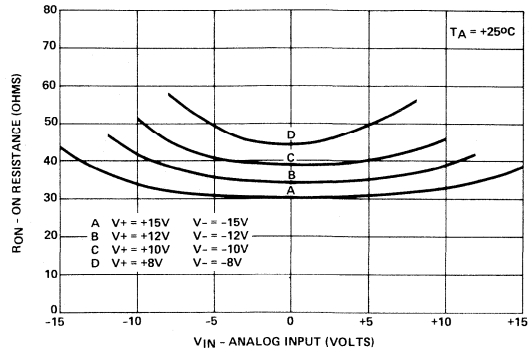
TOP: TTL Input (2V/Div.)
BOTTOM: Output (5V/Div.) HORIZONTAL: 100ns/Div.

Typical Performance Curves

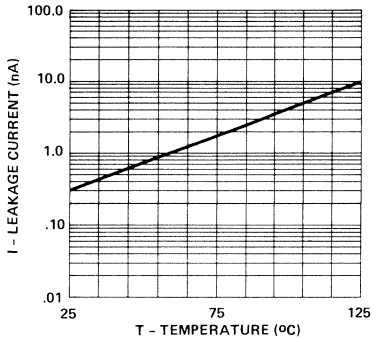
"ON" RESISTANCE vs. ANALOG SIGNAL LEVEL AND TEMPERATURE



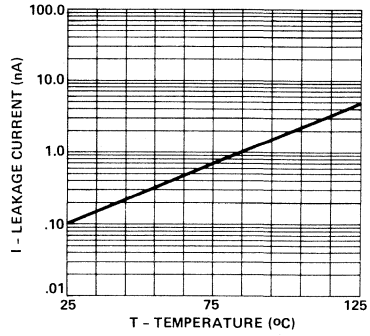
"ON" RESISTANCE vs. ANALOG SIGNAL LEVEL AND POWER SUPPLY VOLTAGE



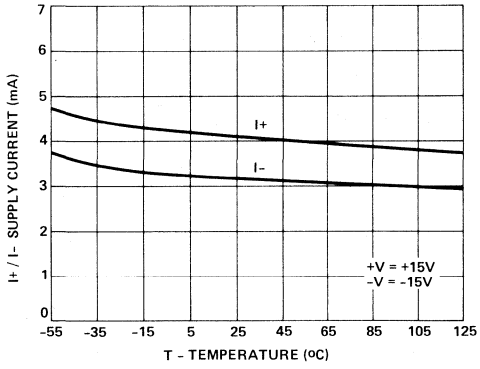
$I_{S(OFF)}$ OR $I_{D(OFF)}$ vs. TEMPERATURE*



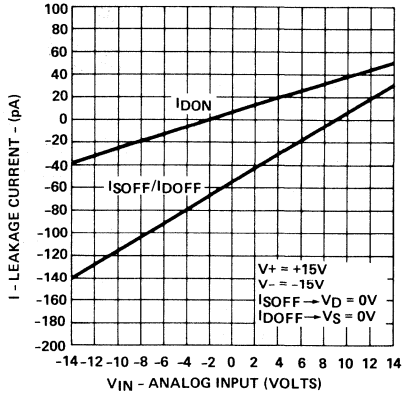
$I_{D(ON)}$ vs. TEMPERATURE*



SUPPLY CURRENT vs. TEMPERATURE



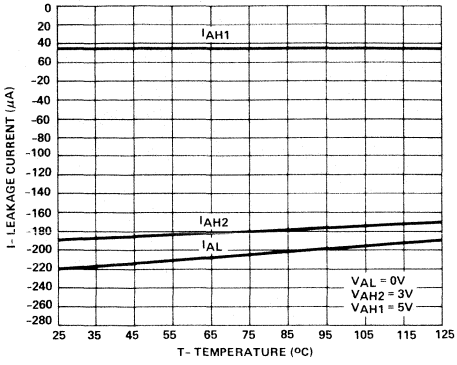
LEAKAGE CURRENT vs. ANALOG INPUT VOLTAGE



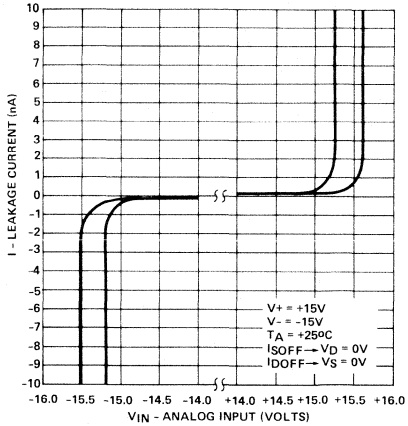
* THEORETICALLY, LEAKAGE CURRENT WILL CONTINUE TO DECREASE BELOW +25°C. BUT DUE TO ENVIRONMENTAL CONDITIONS, LEAKAGE MEASUREMENTS BELOW THIS TEMPERATURE ARE NOT REPRESENTATIVE OF ACTUAL SWITCH PERFORMANCE.

Typical Performance Curves (Continued)

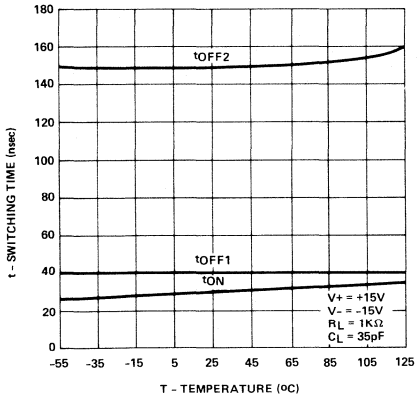
DIGITAL INPUT LEAKAGE CURRENT vs. TEMPERATURE*



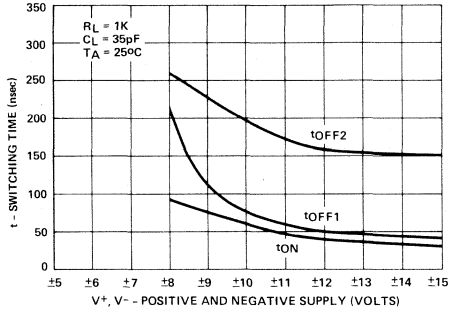
LEAKAGE CURRENT vs. ANALOG INPUT VOLTAGE
(V_{IN} > +14V, V_{IN} < -14V)



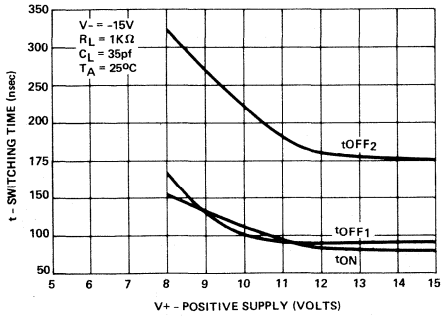
SWITCHING TIME vs. TEMPERATURE



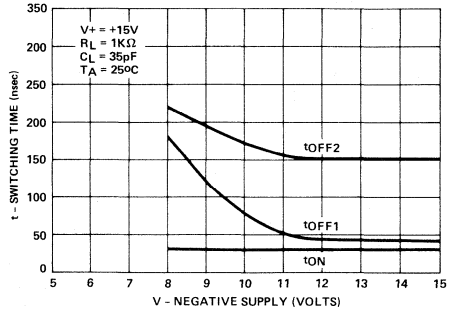
SWITCHING TIME vs. POSITIVE AND NEGATIVE SUPPLY VOLTAGE



SWITCHING TIME vs. POSITIVE SUPPLY VOLTAGE



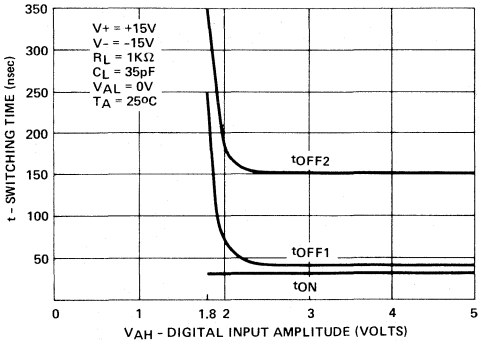
SWITCHING TIME vs. NEGATIVE SUPPLY VOLTAGE



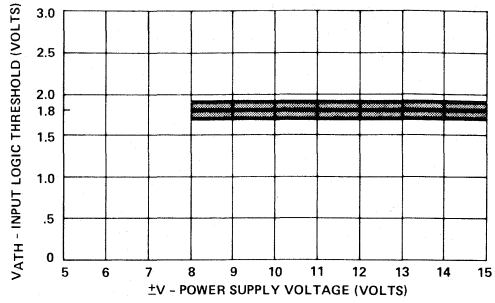
* THEORETICALLY, LEAKAGE CURRENT WILL CONTINUE TO DECREASE BELOW +25°C. BUT DUE TO ENVIRONMENTAL CONDITIONS, LEAKAGE MEASUREMENTS BELOW THIS TEMPERATURE ARE NOT REPRESENTATIVE OF ACTUAL SWITCH PERFORMANCE.

Typical Performance Curves (Continued)

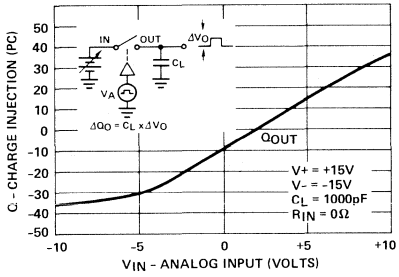
SWITCHING TIME vs. INPUT LOGIC AMPLITUDE



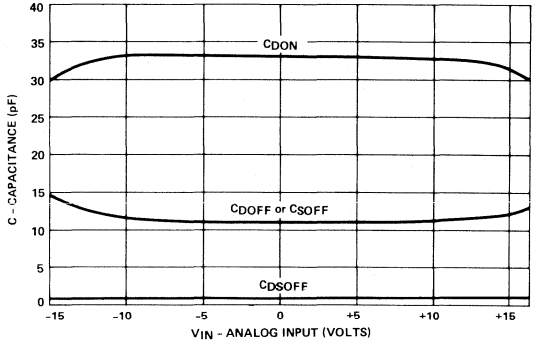
INPUT SWITCHING THRESHOLD vs. POSITIVE AND NEGATIVE SUPPLY VOLTAGES



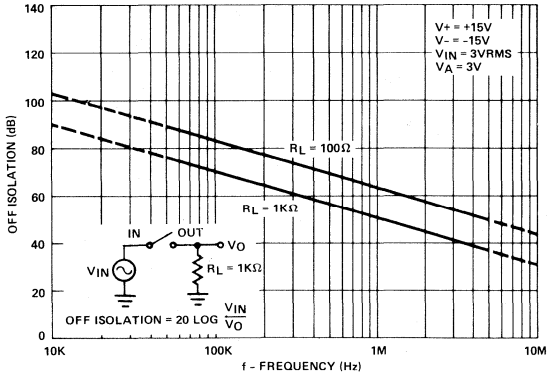
CHARGE INJECTION vs. ANALOG INPUT



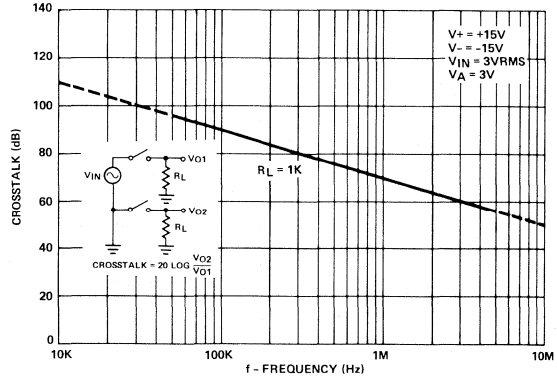
CAPACITANCE vs. ANALOG INPUT



OFF ISOLATION vs. FREQUENCY



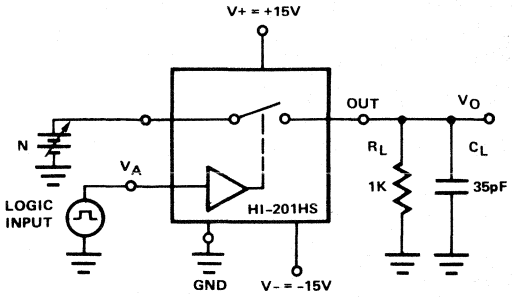
CROSSTALK vs. FREQUENCY



Switching Characteristics

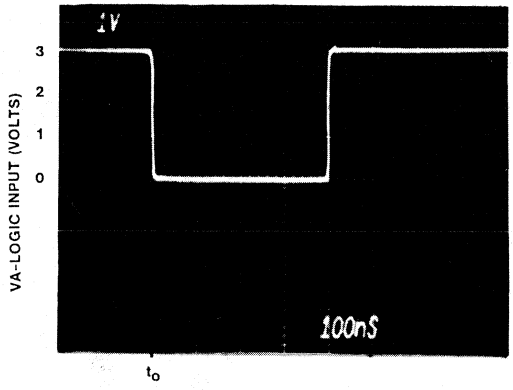
SWITCHING CHARACTERISTICS vs. INPUT VOLTAGE

Typical delay, t_{ON}, t_{OFF}, settling time and switching transients in this circuit.

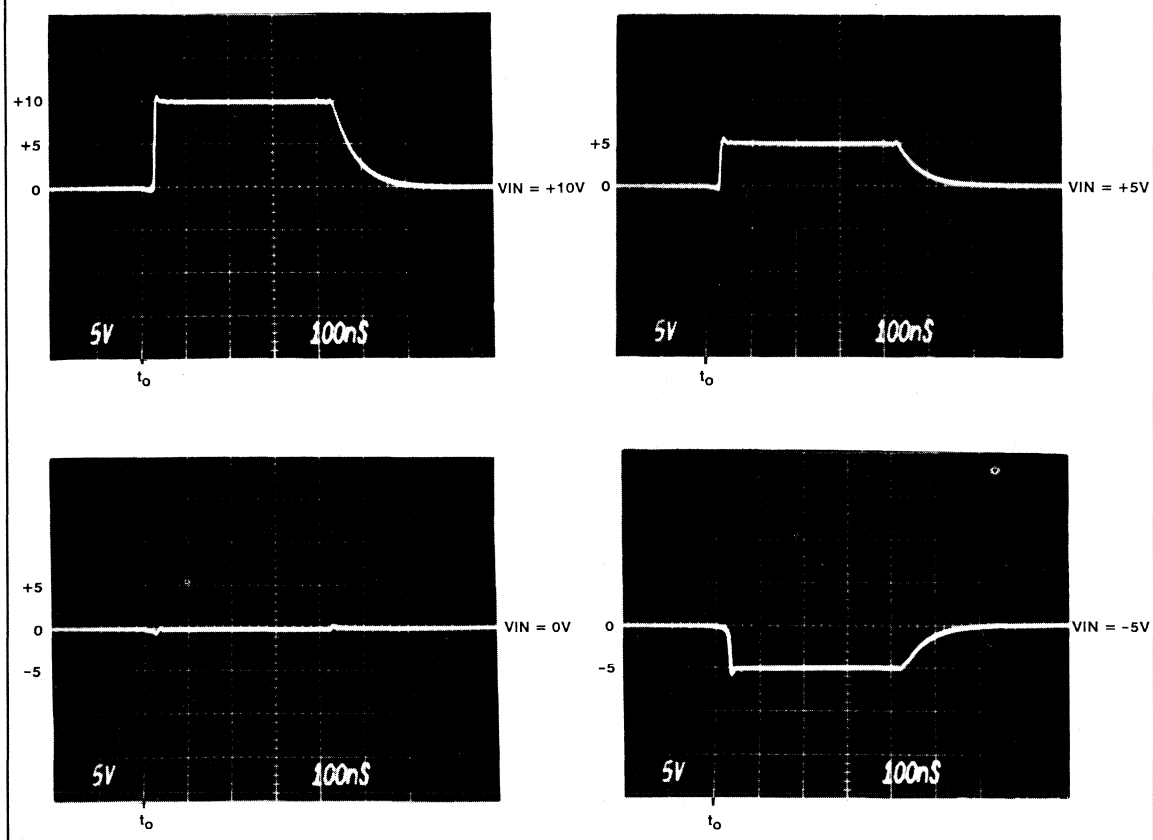


If R_L or C_L is increased, there will be corresponding increases in rise and/or fall RC times.

LOGIC INPUT

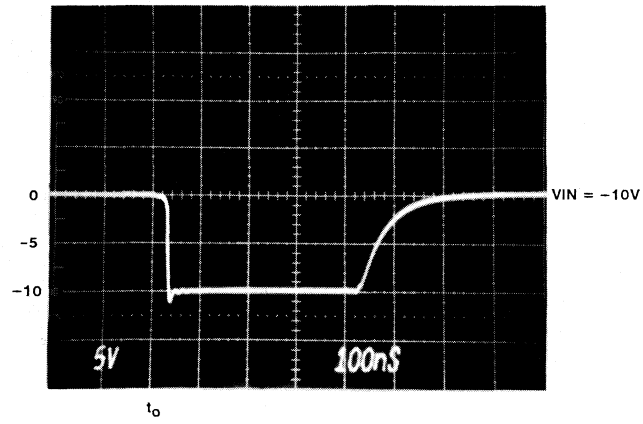


V_O - OUTPUT SWITCHING WAVEFORMS



Switching Characteristics (Continued)

V_O - OUTPUT SWITCHING WAVEFORMS



Application Information

LOGIC COMPATIBILITY

The HI-201HS is TTL compatible. Its logic inputs (Pins 1, 8, 9, 16) are designed to react to digital inputs which exceed a fixed, internally generated TTL switching threshold. The HI-201HS can also be driven with CMOS logic (0-15V), although the switch performance with CMOS logic will be inferior to that with TTL logic (0-5V).

The logic input design of the HI-201HS is largely responsible for its fast switching speed. It is a design which features a unique input stage consisting of complementary vertical PNP and NPN bipolar transistors. This design differs from that of the standard HI-201 product where the logic inputs are MOS transistors.

Although the new logic design enhances the switching speed performance, it also increases the logic input leakage currents. Therefore, the HI-201HS will exhibit larger digital input leakage currents in comparison to the standard HI-201 product.

CHARGE INJECTION

Charge injection is the charge transferred, through the internal gate-to-channel capacitances, from the digital logic input to the analog output. To optimize charge injection performance for the HI-201HS, it is advisable to provide a TTL logic input with fast rise and fall times.

If the power supplies are reduced from ±15V, charge injection will become increasingly dependent upon the digital input frequency. Increased logic input frequency will result in larger output error due to charge injection.

POWER SUPPLY CONSIDERATIONS

The electrical characteristics specified in this data sheet are guaranteed for power supplies $\pm V_S = \pm 15V$. Power supply voltages less than ±15V will result in reduced switch performance. The following information is intended as a design aid only:

POWER SUPPLY VOLTAGES	SWITCH PERFORMANCE
$\pm 12 < \pm V_S \pm 15V$	Minimal Variation
$\pm V_S < \pm 12V$	Parametric Variation becomes Increasingly Large (Increased ON Resistance, Longer Switching Times).
$\pm V_S < \pm 10V$	Not Recommended.
$\pm V_S > \pm 16V$	Not Recommended.

SINGLE SUPPLY

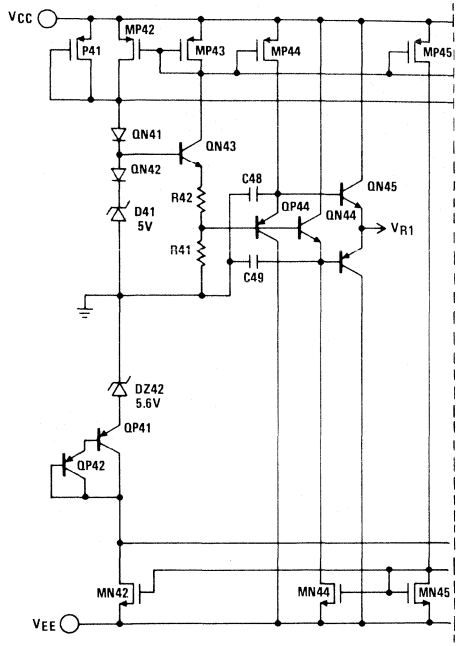
The switch operation of the HI-201HS is dependent upon an internally generated switching threshold voltage optimized for ±15V power supplies. The HI-201HS does not provide the necessary internal switching threshold in a single supply system. Therefore, if single supply operation is required, the HI-300 series of switches is recommended. The HI-300 series will remain operational to a minimum +5V single supply.

Switch performance will degrade as power supply voltage is reduced from optimum levels (±15V). So it is recommended that a single supply design be thoroughly evaluated to ensure that the switch will meet the requirements of the application.

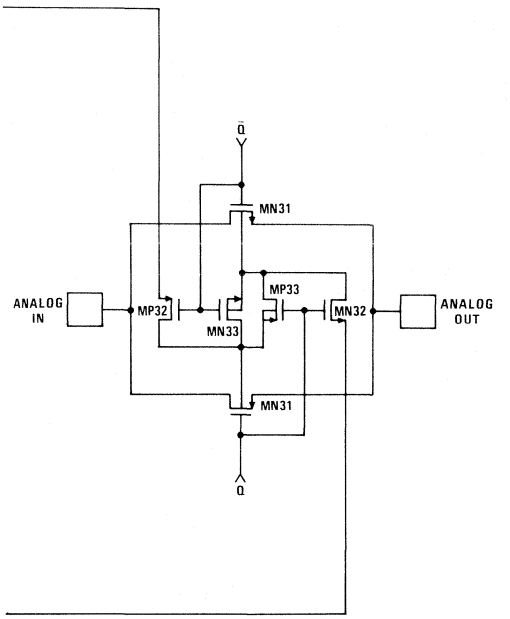
For Further Information See Application Notes 520, 521, 531, 532, 543 and 557 in Section 10 of Data Book.

Schematic Diagrams

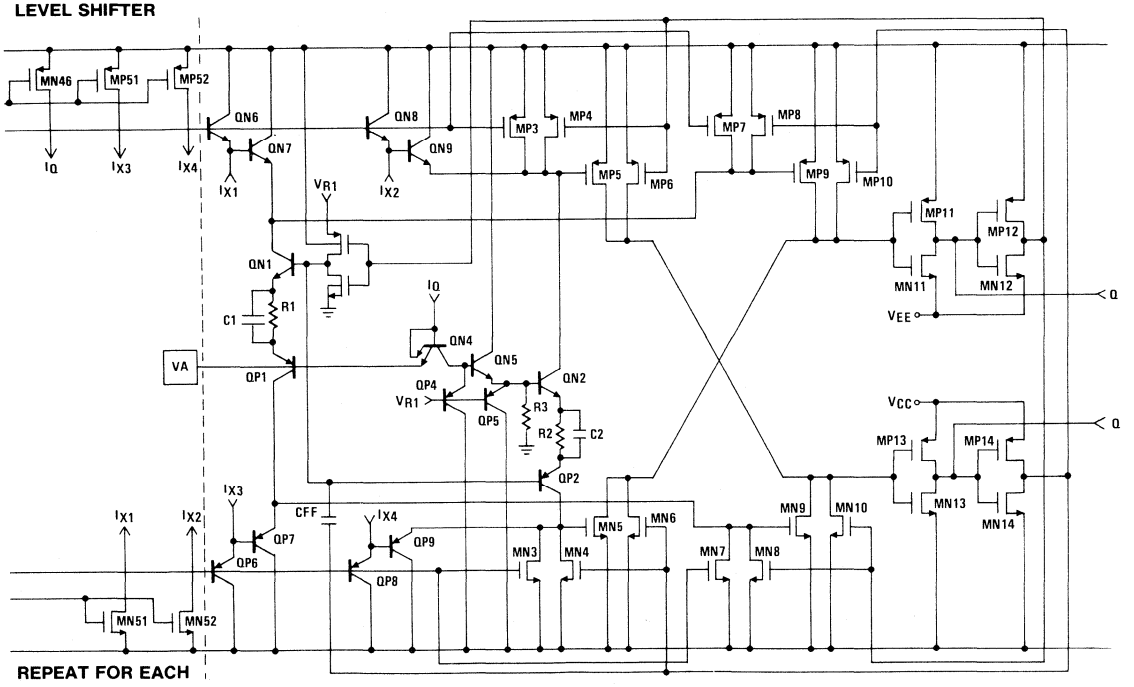
TTL/CMOS REFERENCE CIRCUIT



SWITCH CELL



DIGITAL INPUT AND LEVEL SHIFTER



REPEAT FOR EACH LEVEL SHIFTER

HARRIS

HI-300 thru HI-307

CMOS Analog Switches

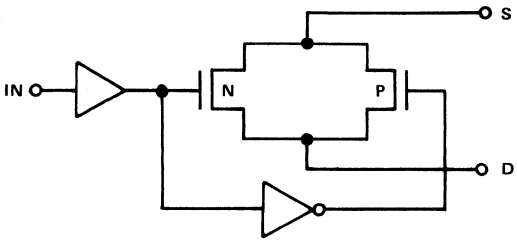
Features

- Analog Signal Range (±15V Supplies) ..... ±15V
- Low Leakage (Typical @ +25°C) 40pA
- Low Leakage (Typical @ +125°C) 1nA
- Low On Resistance (Typical @ +25°C) 35Ω
- Break-Before-Make Delay (Typical) 60ns
- Charge Injection 30pC
- TTL, CMOS Compatible
- Symetrical Switch Elements
- Low Operating Power ..... 1.0mW (Typical for HI-300 - 303)

Applications

- Sample and Hold i.e. Low Leakage Switching
- Op Amp Gain Switching i.e. Low On Resistance
- Portable, Battery Operated Circuits
- Low Level Switching Circuits
- Dual or Single Supply Systems

Functional Diagram



TYPICAL SWITCH 300 SERIES

Description

The HI-300 through HI-307 series of switches are monolithic devices fabricated using CMOS technology and the Harris dielectric isolation process. These switches feature break-before-make switching, (HI-301, 303, 305 & 307 only), low and nearly constant ON resistance over the full analog signal range, and low power dissipation, (a few milliwatts for the HI-300 - 303, a few hundred microwatts for the HI-304 - 307).

The HI-300 - 303 are TTL compatible and have a logic "0" condition with an input less than 0.8V and a logic "1" condition with an input greater than 4.0V. The HI-304 - 307 switches are CMOS compatible and have a low state with an input less than 3.5V and a high state with an input greater than 11V. (See pinouts for switch conditions with a logic "1" input.)

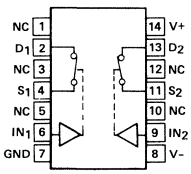
All the devices are available in a 14 pin Epoxy or Ceramic DIP. The HI-300, 301, 304 and 305 are also available in a 10 pin Metal Can. Each of the switch types are available in either the -55°C to +125°C or 0°C to +75°C operating ranges.

Pinouts (SWITCH STATES ARE FOR A LOGIC "1" INPUT)

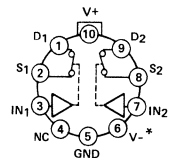
DUAL SPST HI-300 & HI-304

TOP VIEWS

DIP



METAL CAN



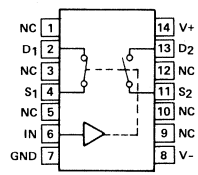
LOGIC	SWITCH
0	OFF
1	ON

* The substrate and case are internally tied to V-. (The case should not be used as the V- connection, however.)

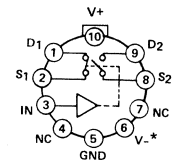
SPDT HI-301 & HI-305

TOP VIEWS

DIP



METAL CAN



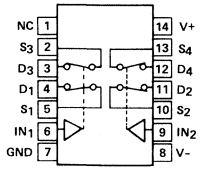
LOGIC	SW 1	SW 2
0	OFF	ON
1	ON	OFF

* The substrate and case are internally tied to V-. (The case should not be used as the V- connection, however.)

DUAL DPST HI-302 & HI-306

TOP VIEW

DIP

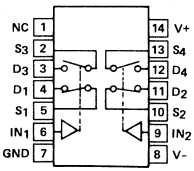


LOGIC	SWITCH
0	OFF
1	ON

DUAL SPDT HI-303 & HI-307

TOP VIEW

DIP



LOGIC	SW 1 SW 2	SW 3 SW 4
0	OFF	ON
1	ON	OFF

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

Voltage Between Supplies ..... 44V (±22)
Digital Input Voltage ..... $+V_{SUPPLY}$ +4V
$-V_{SUPPLY}$ -4V
Analog Input Voltage ..... $+V_{SUPPLY}$ +1.5V
$-V_{SUPPLY}$ -1.5V
Total Power Dissipation* 14 Pin Epoxy DIP 526mW
14 Pin Ceramic DIP 588mW
10 Pin Metal Can* 435mW

Operating Temperature Range

HI-3XX-2 ..... -55°C to +125°C
HI-3XX-5 ..... 0°C to +75°C
Storage Temperature ..... -65°C to +150°C

*Derate 6.9mW/0°C Above T_A = +70°C

Electrical Specifications

Unless Otherwise Specified: Supplies = +15V, -15V; V_{IN} = Logic Input.
HI-300-303: V_{IN} - for Logic "1" = 4V, for Logic "0" = 0.8V
HI-304-307: V_{IN} - for Logic "1" = 11V, for Logic "0" = 3.5V

PARAMETER	TEMP	-55°C To +125°C			0°C To +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG SWITCH CHARACTERISTICS								
Analog Signal Range	Full	-15	-	+15	-15	-	+15	V
R_{ON}, On Resistance (Note 2)	+25°C	-	35	50	-	35	50	Ω
	Full	-	40	75	-	40	75	Ω
$I_{S(OFF)}$, Off Input Leakage Current (Note 3)	+25°C	-	0.04	1	-	0.04	5	nA
	Full	-	1	100	-	0.2	100	nA
$I_{D(OFF)}$, Off Output Leakage Current (Note 3)	+25°C	-	0.04	1	-	0.04	5	nA
	Full	-	1	100	-	0.2	100	nA
$I_{D(ON)}$, On Leakage Current (Note 4)	+25°C	-	0.03	1	-	0.03	5	nA
	Full	-	0.5	100	-	0.2	100	nA
DIGITAL INPUT CHARACTERISTICS								
V_{INL}, Input Low Level*	Full	-	-	0.8	-	-	0.8	V
V_{INH}, Input High Level*	Full	4	-	-	4	-	-	V
V_{INL}, Input Low Level**	Full	-	-	3.5	-	-	3.5	V
V_{INH}, Input High Level**	Full	11	-	-	11	-	-	V
I_{INL}, Input Leakage Current (Low) (Note 5)	Full	-	-	1	-	-	1	µA
I_{INH}, Input Leakage Current (High) (Note 5)	Full	-	-	1	-	-	1	µA
SWITCHING CHARACTERISTICS								
t_{OPEN}, Break-Before Make Delay***	+25°C	-	60	-	-	60	-	ns
t_{ON}, Switch On Time*	+25°C	-	210	300	-	210	300	ns
t_{OFF}, Switch Off Time*	+25°C	-	160	250	-	160	250	ns
t_{ON}, Switch Off Time**	+25°C	-	160	250	-	160	250	ns
t_{OFF}, Switch Off Time**	+25°C	-	100	150	-	100	150	ns
"Off Isolation" (Note 6)	+25°C	-	60	-	-	60	-	dB
Charge Injection (Note 7)	+25°C	-	3	-	-	3	-	mV
$C_{S(OFF)}$, Input Switch Capacitance	+25°C	-	16	-	-	16	-	pF
$C_{D(OFF)}$, Output Switch Capacitance	+25°C	-	14	-	-	14	-	pF
$C_{D(ON)}$, Output Switch Capacitance	+25°C	-	35	-	-	35	-	pF
C_{IN}, (High) Digital Input Capacitance	+25°C	-	5	-	-	5	-	pF
C_{IN}, (Low) Digital Input Capacitance	+25°C	-	5	-	-	5	-	pF
POWER REQUIREMENTS								
I^+, Current* (Note 8)	+25°C	-	0.09	0.5	-	0.09	0.5	mA
	Full	-	-	1	-	-	1	mA
I^-, Current* (Note 8)	+25°C	-	0.01	10	-	0.01	100	µA
	Full	-	-	100	-	-	-	µA
I^+, Current* (Note 9)	+25°C	-	0.01	10	-	0.01	100	µA
	Full	-	-	100	-	-	-	µA
I^-, Current* (Note 9)	+25°C	-	0.01	10	-	0.01	100	µA
	Full	-	-	100	-	-	-	µA
I^+, Current** (Note 10)	+25°C	-	0.01	10	-	0.01	100	µA
	Full	-	-	100	-	-	-	µA
I^-, Current** (Note 10)	+25°C	-	0.01	10	-	0.01	100	µA
	Full	-	-	100	-	-	-	µA
I^+, Current** (Note 11)	+25°C	-	0.01	10	-	0.01	100	µA
	Full	-	-	100	-	-	-	µA
I^-, Current** (Note 11)	+25°C	-	0.01	10	-	0.01	100	µA
	Full	-	-	100	-	-	-	µA

*HI-300 Thru HI-303 Only; **HI-304 Thru HI-307 Only; ***HI-301, HI-303, HI-305, HI-307 Only

Electrical Specifications Notes:

1. As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Specifications" are the only conditions recommended for satisfactory operation.
2. V_S = ±10V, I_{OUT} = -10mA. On resistance derived from the voltage measured across the switch under the above conditions.
3. V_S = ±14V, V_D = ±14V.
4. $V_S = V_D$ = ±14V.
5. The digital inputs are diode protected MOS gates and typical leakages of 1nA or less can be expected.
6. $V_S = 1V_{RMS}$, f = 500kHz, C_L = 15pF, R_L = 1k.
7. V_S = 0V, C_L = 10,000pF, Logic Drive = 5V pulse. (HI-300 - 303) Switches are symmetrical; S and D may be interchanged. Logic Drive = 15V (HI-304 - 307).
8. V_{IN} = 4V (One Input) (All Other Inputs = 0V).
9. V_{IN} = 0.8V (All Inputs).
10. V_{IN} = 15V (All Inputs).
11. V_{IN} = 0V (All Inputs).
12. To drive from DTL/TTL circuits, pull-up resistors to +5V supply are recommended.

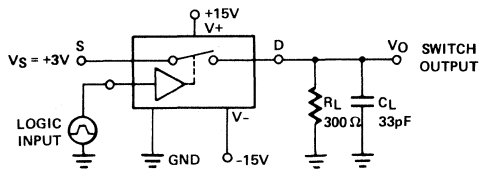
Test Circuits

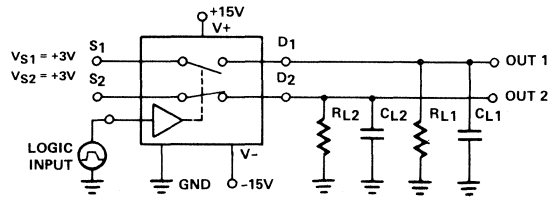
SWITCHING TEST CIRCUIT (t_{ON}, t_{OFF})

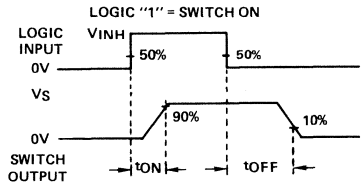
SWITCH TYPE	V_{INH}
HI-300 thru HI-303	4V
HI-304 thru HI-307	15V

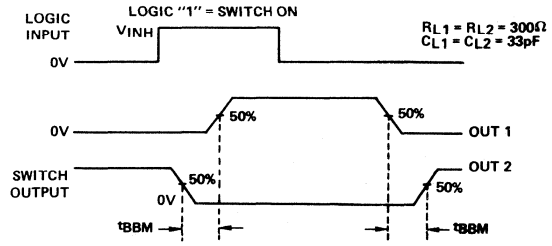
BREAK-BEFORE-MAKE TEST CIRCUIT (t_{BBM})

SWITCH TYPE	V_{INH}
HI-301, HI-303	5V
HI-305, HI-307	15V



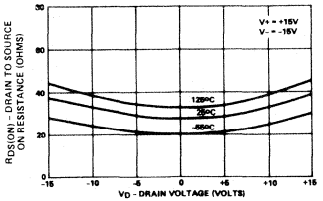




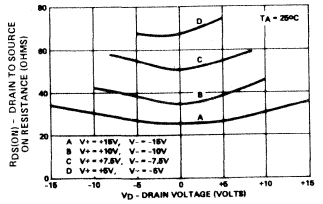


Typical Performance Curves

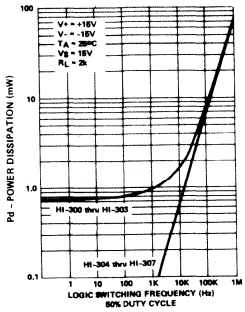
$R_{DS(ON)}$ VS. V_D AND TEMPERATURE



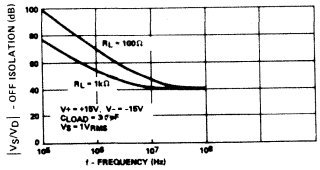
$R_{DS(ON)}$ VS. V_D AND POWER SUPPLY VOLTAGE



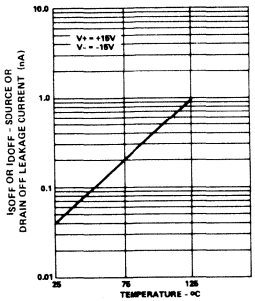
DEVICE POWER DISSIPATION VS. SWITCHING FREQUENCY SINGLE LOGIC INPUT



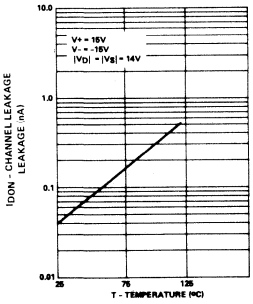
OFF ISOLATION VS. FREQUENCY



$I_{S(OFF)}$ OR $I_{D(OFF)}$ VS. TEMPERATURE *

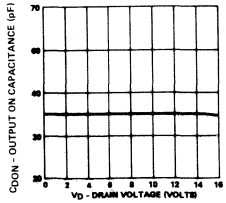


$I_{D(ON)}$ VS. TEMPERATURE *

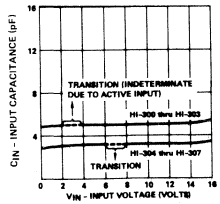


* The net leakage into the source or drain is the n-channel leakage minus the p-channel leakage. This difference can be positive, negative, or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

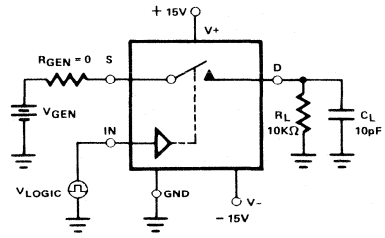
OUTPUT ON CAPACITANCE VS. DRAIN VOLTAGE



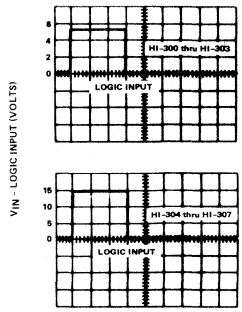
DIGITAL INPUT CAPACITANCE VS. INPUT VOLTAGE

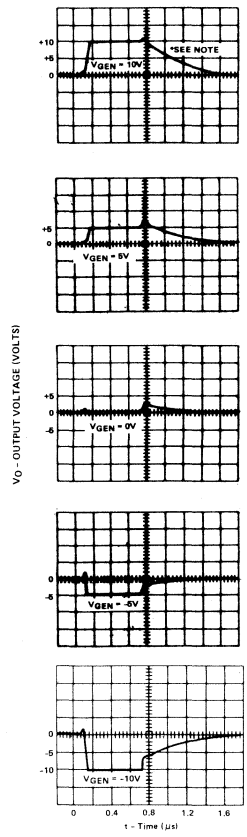


Typical delay, rise, fall, settling times, and switching transients in this circuit.



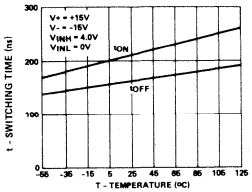
If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.



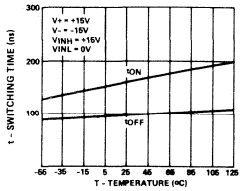


Typical Performance Curves (Continued)

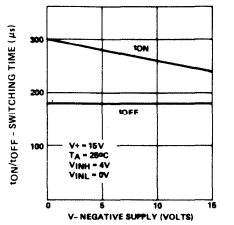
SWITCHING TIME VS. TEMPERATURE HI-300 thru HI-303



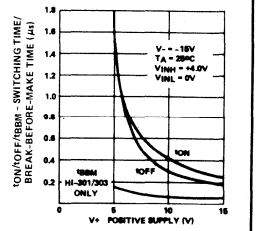
SWITCHING TIME VS. TEMPERATURE HI-304 thru HI-307



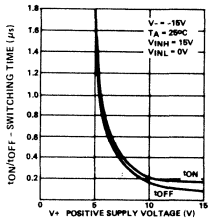
SWITCHING TIME VS. NEGATIVE SUPPLY VOLTAGE HI-300 thru HI-303



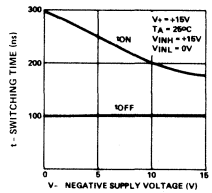
SWITCHING TIME AND BREAK BEFORE MAKE TIME VS. POSITIVE SUPPLY VOLTAGE HI-300 thru HI-303



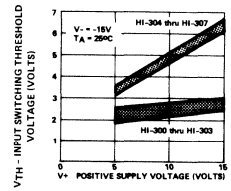
SWITCHING TIME VS. POSITIVE SUPPLY VOLTAGE HI-304 thru HI-307



SWITCHING TIME VS. NEGATIVE SUPPLY VOLTAGE HI-304 thru HI-307

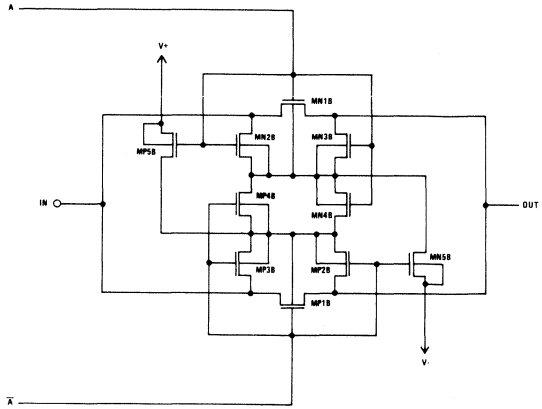


INPUT SWITCHING THRESHOLD VS. POSITIVE SUPPLY VOLTAGE HI-300 thru HI-307

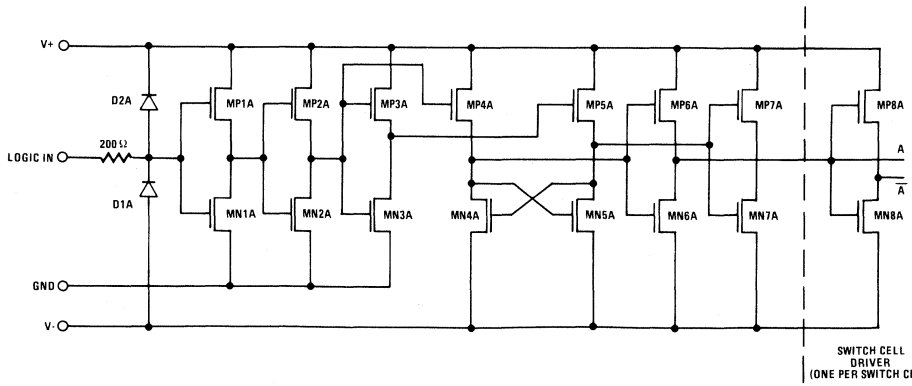


Schematic Diagrams

SWITCH CELL



DIGITAL INPUT BUFFER AND LEVEL SHIFTER



HI-381/384/387/390

CMOS Analog Switches

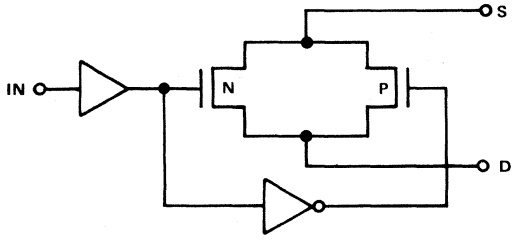
Features

- Analog Signal Range (±15V Supplies) ..... ±15V
- Low Leakage (Typical @ +25°C) 40pA
- Low Leakage (Typical @ +125°C) 1nA
- Low On Resistance (Typical @ +25°C) 35Ω
- Break-Before-Make Delay (Typical) 60ns
- Charge Injection 30pC
- TTL Compatible
- Symetrical Switch Elements
- Low Operating Power 1.0mW

Applications

- Sample and Hold i.e. Low Leakage Switching
- Op Amp Gain Switching i.e. Low On Resistance
- Portable Battery Operated Circuits
- Low Level Switching Circuits
- Dual or Single Supply Systems

Functional Diagram



TYPICAL SWITCH 300 SERIES

Description

The HI-381 through HI-390 series of switches are monolithic devices fabricated using CMOS technology and the Harris dielectric isolation process. These devices are TTL compatible and are available in four switching configurations. (See device pinout for particular switching function with a logic "1" input.)

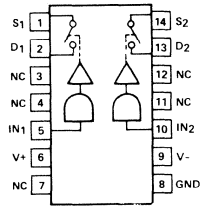
These switches feature low leakage and supply currents, low and nearly constant ON resistance over the analog signal range, break-before-make switching and low power dissipation.

The HI-381 and HI-387 switches are available in a 14 pin Epoxy or Ceramic DIP or 10 pin Metal Can. The HI-384 and HI-390 are available in a 16 pin Epoxy or Ceramic DIP. Each of the individual switch types are available in the -55°C to +125°C and 0°C to +75°C operating ranges.

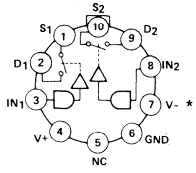
Pinouts (SWITCH STATES ARE FOR A LOGIC "1" INPUT)

DUAL SPST HI-381
TOP VIEWS

DIP



METAL CAN

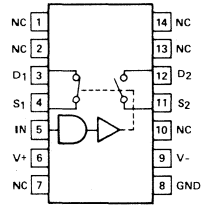


LOGIC	SW 1-2
0	OFF
1	ON

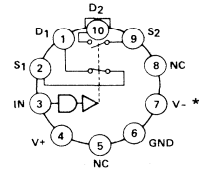
* The substrate and case are internally tied to V-. (The case should not be used as the V- connection, however.)

SPDT HI-387
TOP VIEWS

DIP



METAL CAN

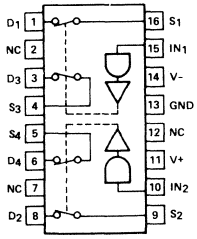


LOGIC	SW 1	SW 2
0	OFF	ON
1	ON	OFF

* The substrate and case are internally tied to V-. (The case should not be used as the V- connection, however.)

DUAL DPST HI-384
TOP VIEW

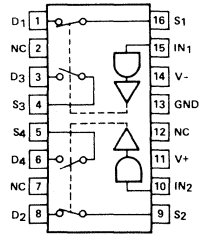
DIP



LOGIC	SW 1-4
0	OFF
1	ON

DUAL SPDT HI-390
TOP VIEW

DIP



LOGIC	SW 1 SW 2	SW 3 SW 4
0	OFF	ON
1	ON	OFF

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

Voltage Between Supplies ..... 44V (±22)
Digital Input Voltage ..... $+V_{SUPPLY}$ +4V
$-V_{SUPPLY}$ -4V
Analog Input Voltage ..... $+V_{SUPPLY}$ +1.5V
$-V_{SUPPLY}$ -1.5V
Total Power Dissipation* 14 Pin Epoxy DIP 526mW
14 Pin Ceramic DIP 588mW
16 Pin Epoxy DIP 625mW
16 Pin Ceramic DIP 685mW
10 Pin Metal Can* 435mW

Operating Temperature Range

HI-3XX-2 ..... -55°C to +125°C
HI-3XX-5 ..... 0°C to +75°C
Storage Temperature ..... -65°C to +150°C

*Derate 6.9mW/°C Above T_A = +70°C

Electrical Specifications

Unless Otherwise Specified: Supplies = +15V, -15V; V_{IN} = Logic Input. V_{IN} for Logic "1" = 4V, for Logic "0" = 0.8V

PARAMETER	TEMP	-55°C to +125°C			0°C to +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG SWITCH CHARACTERISTICS								
Analog Signal Range	Full	-15	-	+15	-15	-	+15	V
R_{ON}, On Resistance (Note 2)	+25°C	-	35	50	-	35	50	Ω
	Full	-	40	75	-	40	75	Ω
$I_{S(OFF)}$, Off Input Leakage Current (Note 3)	+25°C	-	0.04	1	-	0.04	5	nA
	Full	-	1	100	-	0.2	100	nA
$I_{D(OFF)}$, Off Output Leakage Current (Note 3)	+25°C	-	0.04	1	-	0.04	5	nA
	Full	-	1	100	-	0.2	100	nA
$I_{D(ON)}$, On Leakage Current (Note 4)	+25°C	-	0.03	1	-	0.03	5	nA
	Full	-	0.5	100	-	0.2	100	nA
DIGITAL INPUT CHARACTERISTICS								
V_{INL}, Input Low Level	Full	-	-	0.8	-	-	0.8	V
V_{INH}, Input High Level	Full	4	-	-	4	-	-	V
I_{INL}, Input Leakage Current (Low) (Note 5)	Full	-	-	1	-	-	1	µA
I_{INH}, Input Leakage Current (High) (Note 5)	Full	-	-	1	-	-	1	µA
SWITCHING CHARACTERISTICS								
t_{OPEN}, Break-Before Make Delay (HI-387/390 Only)	+25°C	-	60	-	-	60	-	ns
t_{ON}, Switch On Time	+25°C	-	210	300	-	210	300	ns
t_{OFF}, Switch Off Time	+25°C	-	160	250	-	160	250	ns
"Off Isolation" (Note 6)	+25°C	-	60	-	-	60	-	dB
Charge Injection (Note 7)	+25°C	-	3	-	-	3	-	mV
$C_{S(OFF)}$, Input Switch Capacitance	+25°C	-	16	-	-	16	-	pF
$C_{D(OFF)}$, Output Switch Capacitance	+25°C	-	14	-	-	14	-	pF
$C_{D(ON)}$, Output Switch Capacitance	+25°C	-	35	-	-	35	-	pF
C_{IN}, (High) Digital Input Capacitance	+25°C	-	5	-	-	5	-	pF
C_{IN}, (Low) Digital Input Capacitance	+25°C	-	5	-	-	5	-	pF
POWER REQUIREMENTS								
I^+, Current (Note 8)	+25°C	-	0.09	0.5	-	0.09	0.5	mA
	Full	-	-	1	-	-	1	mA
I^-, Current (Note 8)	+25°C	-	0.01	10	-	0.01	100	µA
	Full	-	-	100	-	-	-	µA
I^+, Current (Note 9)	+25°C	-	0.01	10	-	0.01	100	µA
	Full	-	-	100	-	-	-	µA
I^-, Current (Note 9)	+25°C	-	0.01	10	-	0.01	100	µA
	Full	-	-	100	-	-	-	µA

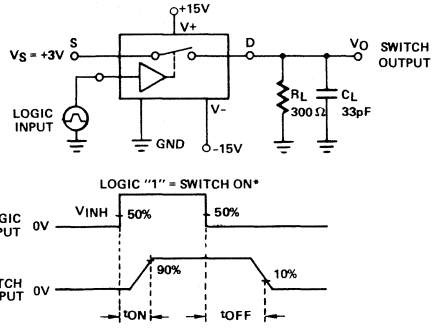
Electrical Specifications Notes:

1. As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Specifications" are the only conditions recommended for satisfactory operation.
2. V_S = ±10V, I_{OUT} = -10mA. On resistance derived from the voltage measured across the switch under the above conditions.
3. V_S = ±14V, V_D = ±14V.
4. V_S = V_D = ±14V.
5. The digital inputs are diode protected MOS gates and typical leakages of 1nA or less can be expected.
6. V_S = $1V_{RMS}$, f = 500kHz, C_L = 15pF, R_L = 1k, C_L = $C_{FIXTURE}$ + C_{PROBE}, "off isolation" = 20_{Log} V_S/V_D.
7. V_S = 0V, C_L = 10,000pF, Logic Drive = 5V pulse. Switches are symmetrical; S and D may be interchanged.
8. V_{IN} = 4V (One Input) (All Other Inputs = 0V).
9. V_{IN} = 0.8V (All Inputs).
10. To drive from DTL/TTL circuits, pull-up resistors to +5V supply are recommended.

Test Circuits

SWITCHING TEST CIRCUIT (t_{ON}, t_{OFF})

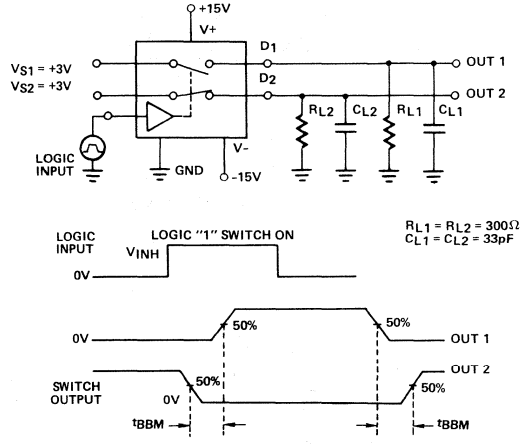
SWITCH TYPE	V_{INH}
HI-381 thru HI-390	5V



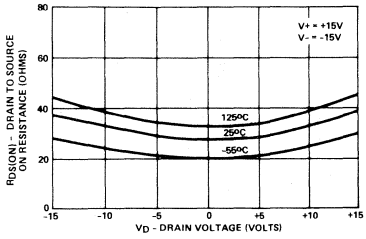
*INVERTED LOGIC FOR HI-381

BREAK-BEFORE-MAKE TEST CIRCUIT (t_{BBM})

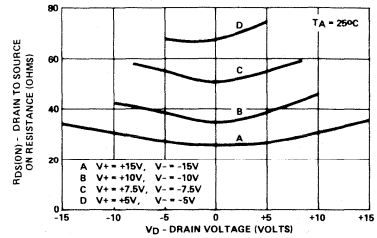
SWITCH TYPE	V_{INH}
HI-387, HI-390	5V



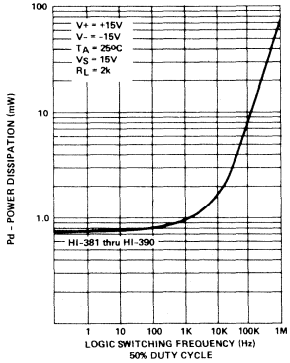
$R_{DS(ON)}$ VS. V_D AND TEMPERATURE



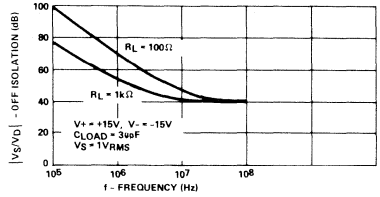
$R_{DS(ON)}$ VS. V_D AND POWER SUPPLY VOLTAGE



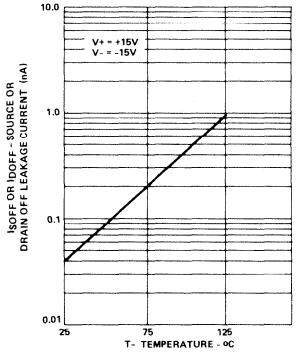
DEVICE POWER DISSIPATION VS. SWITCHING FREQUENCY SINGLE LOGIC INPUT



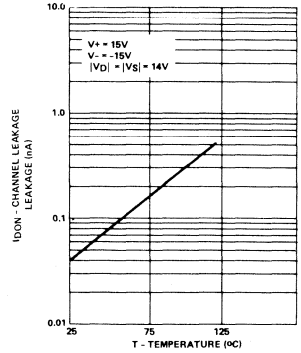
OFF ISOLATION VS. FREQUENCY



$I_{S(OFF)}$ OR $I_{D(OFF)}$ VS. TEMPERATURE*.

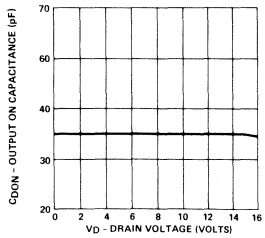


$I_{D(ON)}$ VS. TEMPERATURE*

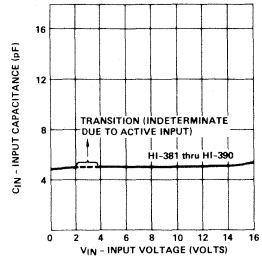


* The net leakage into the source or drain is the n-channel leakage minus the p-channel leakage. This difference can be positive, negative, or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

OUTPUT ON CAPACITANCE VS. DRAIN VOLTAGE

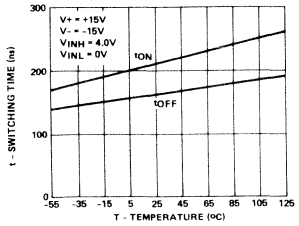


DIGITAL INPUT CAPACITANCE VS. INPUT VOLTAGE

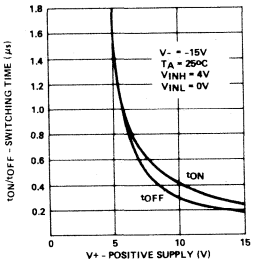


HI-381/384/387/390 Typical Performance Curves (Continued)

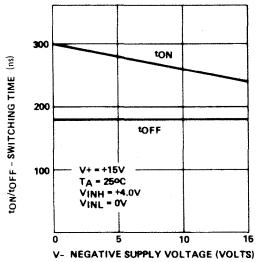
SWITCHING TIME vs. TEMPERATURE HI-381 THRU HII-390



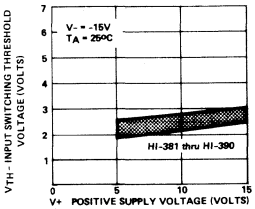
SWITCHING TIME vs. POSITIVE SUPPLY VOLTAGE HI-381 THRU HI-390



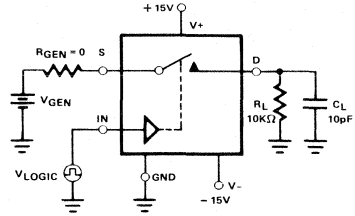
SWITCHING TIME vs. NEGATIVE SUPPLY VOLTAGE HI-381 THRU HI-390



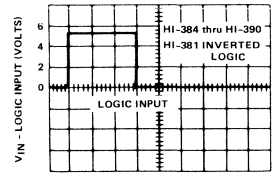
INPUT SWITCHING THRESHOLD vs. POSITIVE SUPPLY VOLTAGE HI-381 THRU HI-390

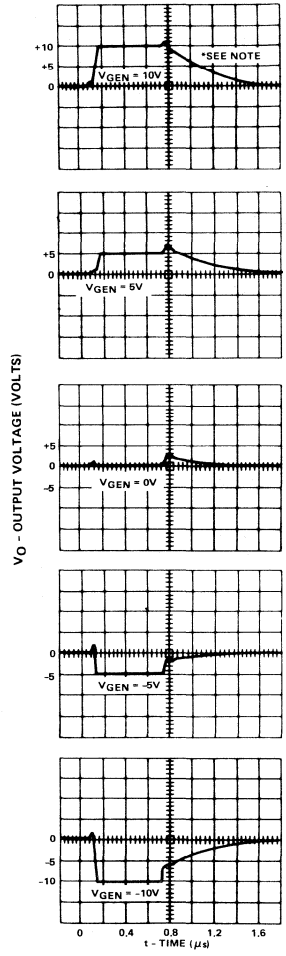


Typical delay, rise, fall, settling times, and switching transients in this circuit.



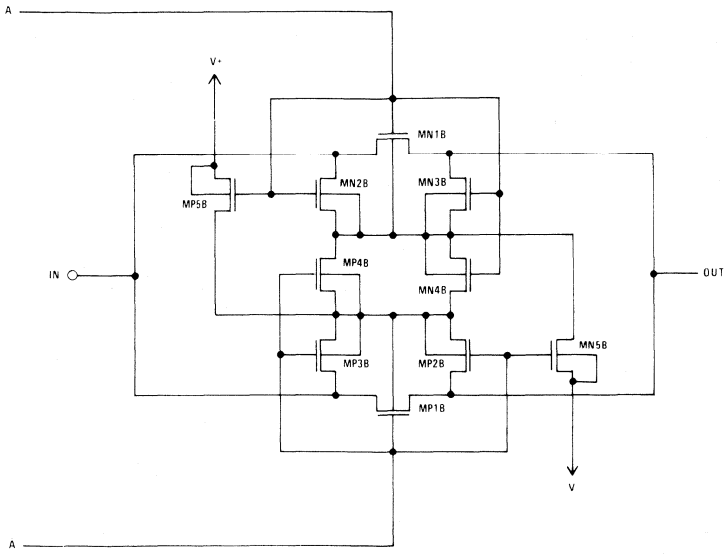
If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.



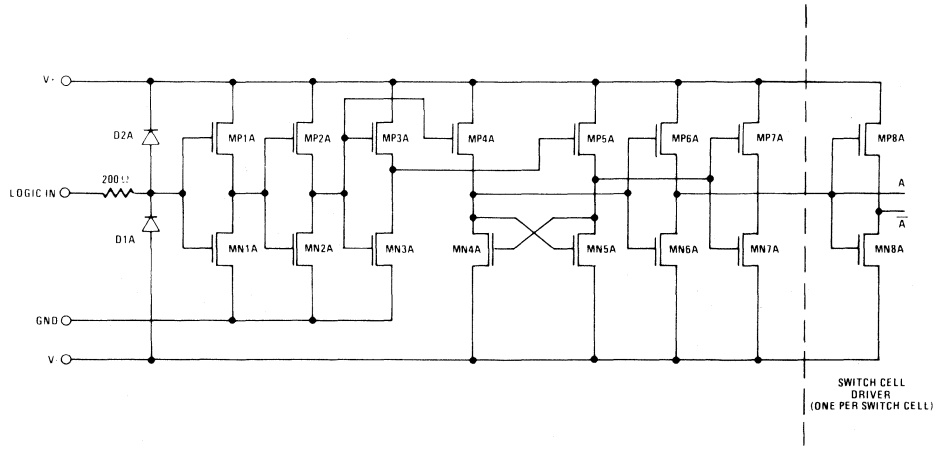


* NOTE: The turn-off time is primarily limited here by the RC time constant (100ns) of the load.

Schematic Diagrams



DIGITAL INPUT BUFFER AND LEVEL SHIFTER



HARRIS HI-5040 thru HI-5051 HI-5046A and HI-5047A

CMOS Analog Switches

Features

- Wide Analog Signal Range ..... ±15V
- Low "ON" Resistance (Typical) 25Ω
- High Current Capability (Typical) 80mA
- Break-Before-Make Switching
  - ▸ Turn-On Time (Typical) 370ns
  - ▸ Turn-Off Time (Typical) 280ns
- No Latch-Up
- Input MOS Gates Are Protected From Electrostatic Discharge
- DTL, TTL, CMOS, PMOS Compatible

Applications

- High Frequency Switching
- Sample and Hold
- Digital Filters
- Operational Amplifier Gain Switching

Description

This family of CMOS analog switches offers low-resistance switching performance for analog voltages up to the supply rails and for signal currents up to 80mA. "ON" resistance is low and stays reasonably constant over the full range of operating signal voltage and current. R_{ON} remains exceptionally constant for input voltages between +5V and -5V and currents up to 50mA. Switch impedance also changes very little over temperature, particularly between 0°C and +75°C. R_{ON} is nominally 25Ω for HI-5048 through HI-5051 and HI-5046A/5047A and 50Ω for HI-5040 through HI-5047.

All devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. Performance is further enhanced by Dielectric Isolation processing which insures latch-free operation with very low input and output leakage currents (0.8nA at +25°C). This family of switches also features very low power operation (1.5mW at +25°C).

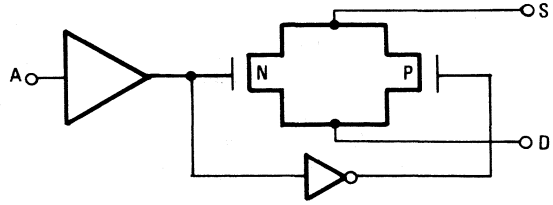
There are 14 devices in this switch series which are differentiated by type of switch action and value of R_{ON} (see Functional Diagram). All devices are available in 16 pin DIP packages. the HI-5040/5050 switches can directly replace HI-5040 series devices and are functionally compatible with the DG 180/190 family. Each switch type is available in the -55°C to +125°C and 0°C to +75°C performance grades.

Functional Description

PART NUMBER	TYPE	R_{ON}
HI-5040	SPST	75Ω
HI-5041	DUAL SPST	75Ω
HI-5042	SPDT	75Ω
HI-5043	DUAL SPST	75Ω
HI-5044	DPST	75Ω
HI-5045	DUAL DPST	75Ω
HI-5046	DPDT	75Ω
HI-5046A	DPDT	25Ω
HI-5047	4PST	75Ω
HI-5047A	4PST	25Ω
HI-5048	DUAL SPST	25Ω
HI-5049	DUAL DPST	25Ω
HI-5050	SPDT	25Ω
HI-5051	DUAL SPDT	25Ω

Functional Diagram

TYPICAL DIAGRAM



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings

Supply Voltage (V+, V-) 36V
V_R to Ground ..... V+, V-
Digital and Analog Input Voltage ..... $+V_{SUPPLY}$ +4V
$-V_{SUPPLY}$ -4V
Analog Current (S to D) Continous 30mA
Analog Current (S to D) Peak 80mA
Total Power Dissipation* 450mW

Operating Temperature Range

HI-50XX-2 ..... -55°C to +125°C
HI-50XX-5 ..... 0°C to +75°C
Storage Temperature ..... -65°C to +150°C

*Derate 6mW/°C Above T_A = +75°C

Electrical Specifications Unless Otherwise Specified Supplies = +15V, -15V; V_R = 0V; V_{AH} (Logic Level High) = 3.0V, V_{AL} (Logic Level Low) = +0.8V, V_L = +5V For Test Conditions, Consult Performance Characteristics, Unused Pins are Grounded.

PARAMETER	TEMP	-55°C To +125°C			0°C To +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG SWITCH CHARACTERISTICS								
Analog Signal Range	Full	-15	-	+15	-15	-	+15	V
R_{ON}, On Resistance (Note 1a)	+25°C	-	50	-	-	50	-	Ω
	Full	-	-	75	-	-	75	Ω
R_{ON}, On Resistance (Note 1b)	+25°C	-	25	-	-	25	-	Ω
	Full	-	-	50	-	-	50	Ω
R_{ON}, Channel-to-Channel Match (Note 1a)	+25°C	-	2	10	-	2	10	Ω
R_{ON}, Channel-to-Channel Match (Note 1b)	+25°C	-	1	5	-	1	5	Ω
$I_{S(OFF)} = I_{D(OFF)}$, Off Input or Output Leakage Current	+25°C	-	0.8	-	-	0.8	-	nA
	Full	-	100	500	-	100	500	nA
$I_{D(ON)}$, On Leakage Current	+25°C	-	0.01	-	-	0.01	-	nA
	Full	-	2	500	-	2	500	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full	-	-	0.8	-	-	0.8	V
V_{AH}, Input High Threshold	Full	3.0	-	-	3.0	-	-	V
I_A, Input Leakage Current (High or Low)	Full	-	0.01	1.0	-	0.01	1.0	µA
SWITCHING CHARACTERISTICS								
t_{ON}, Switch On Time	+25°C	-	370	1000	-	370	1000	ns
t_{OFF}, Switch Off Time	+25°C	-	280	500	-	280	500	ns
Charge Injection (Note 2)	+25°C	-	5	20	-	5	-	mV
"Off Isolation" (Note 3)	+25°C	75	80	-	-	80	-	dB
"Crosstalk" (Note 3)	+25°C	80	88	-	-	88	-	dB
$C_{S(OFF)}$, Input Switch Capacitance	+25°C	-	11	-	-	11	-	pF
$C_{D(OFF)}$, Output Switch Capacitance	+25°C	-	11	-	-	11	-	pF
$C_{D(ON)}$, Output Switch Capacitance	+25°C	-	22	-	-	22	-	pF
C_A, Digital Input Capacitance	+25°C	-	5	-	-	5	-	pF
$C_{DS(OFF)}$, Drain-To-Source Capacitance	+25°C	-	0.5	-	-	0.5	-	pF
POWER REQUIREMENTS								
P_D, Quiescent Power Dissipation	+25°C	-	1.5	-	-	1.5	-	mW
I^+, +15V Quiescent Current	Full	-	-	0.3	-	-	0.5	mA
I^-, -15V Quiescent Current	Full	-	-	0.3	-	-	0.5	mA
I_L, +5V Quiescent Current	Full	-	-	0.3	-	-	0.5	mA
I_R, Ground Quiescent Current	Full	-	-	0.3	-	-	0.5	mA

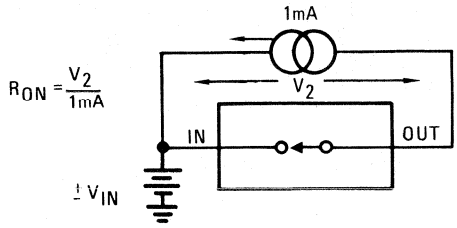
NOTES:

1. V_{OUT} = ±10V, I_{OUT} = 1mA
   a). For HI-5040 thru HI-5047
   b). For HI-5048 thru HI-5051, HI-5046A/5047A.
2. V_{IN} = 0V, C_L = 10,000pF.
3. R_L = 100Ω, f = 100kHz, $V_{IN} = V_{p-p}$, C_L = 5pF.

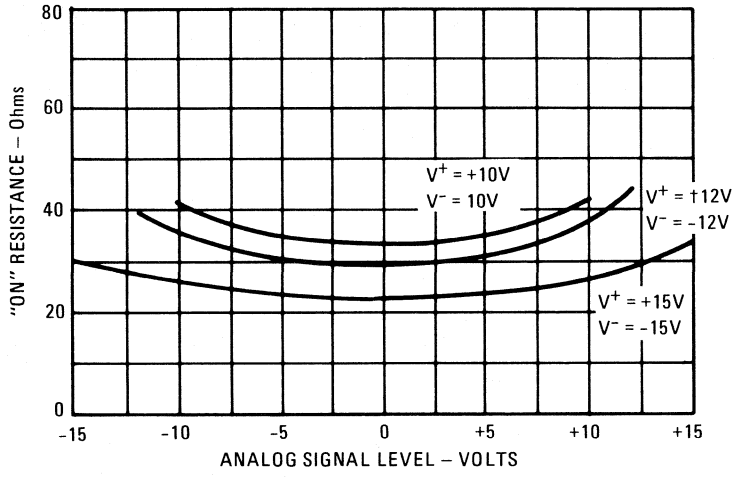
Performance Characteristics and Test Circuits

Unless Otherwise Specified: $T_A = +25^oC$, V+ = +15V, V- = -15V, $V_L = +5V$, $V_R = 0V$, $V_{AH} = 3.0V$ and $V_{AL} = 0.8V$

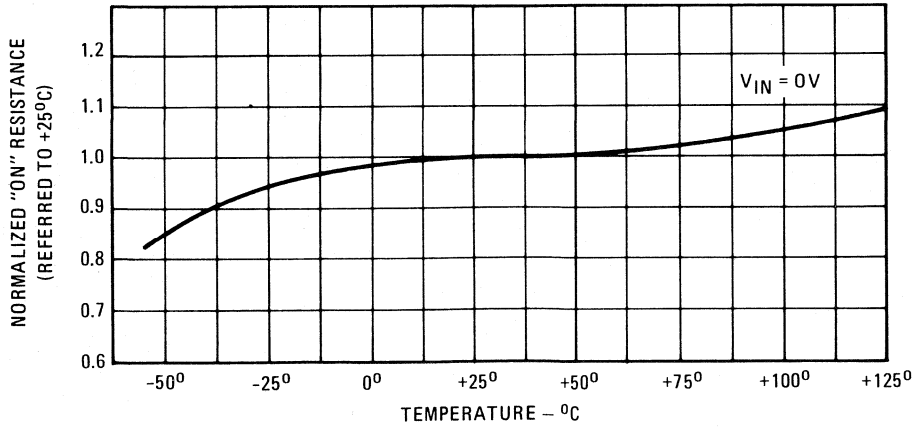
"ON" RESISTANCE vs. ANALOG SIGNAL LEVEL, SUPPLY VOLTAGE AND TEMPERATURE



"ON" RESISTANCE vs. ANALOG SIGNAL LEVEL AND POWER SUPPLY VOLTAGE

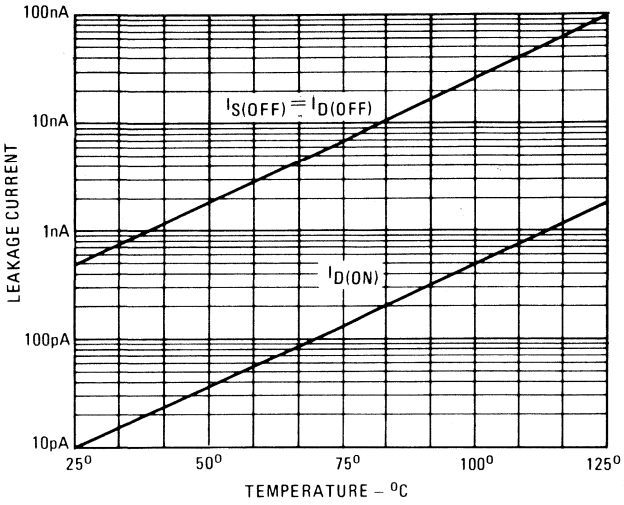


NORMALIZED "ON" RESISTANCE vs. TEMPERATURE

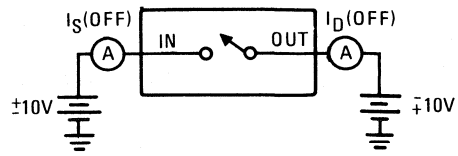


Performance Characteristics and Test Circuits (Continued)

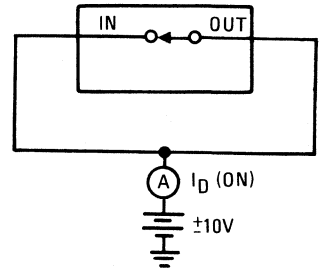
ON/OFF LEAKAGE CURRENT vs. TEMPERATURE



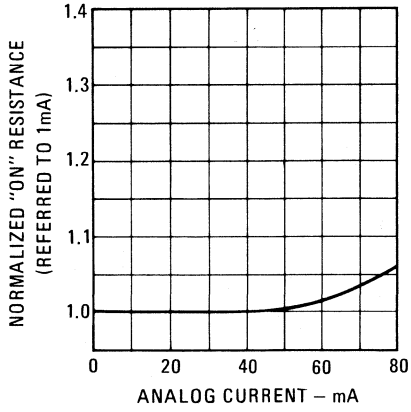
OFF LEAKAGE CURRENT vs. TEMPERATURE



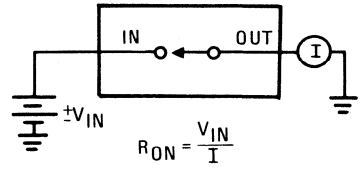
ON LEAKAGE CURRERT vs. TEMPERATURE



NORMALIZED "ON" RESISTANCE vs. ANALOG CURRENT

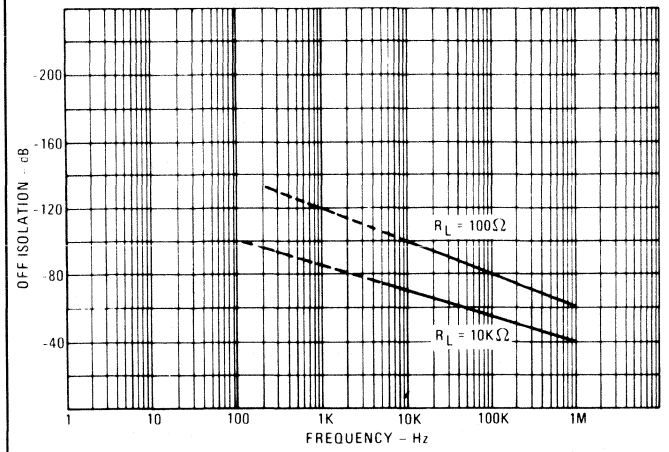


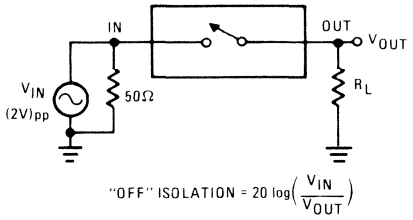
"ON" RESISTANCE vs. ANALOG CURRENT



Performance Characteristics and Test Circuits (Continued)

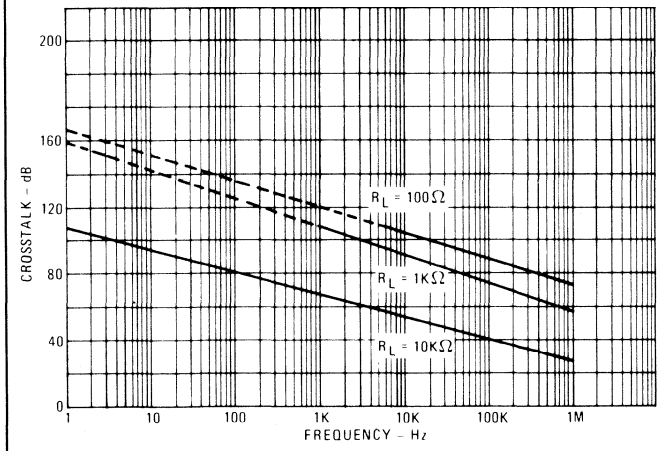
"OFF" ISOLATION vs. FREQUENCY

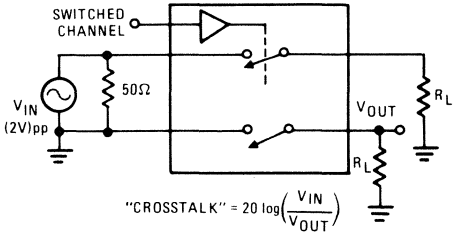




"OFF" ISOLATION = $20 \log\left(\frac{V_{IN}}{V_{OUT}}\right)$

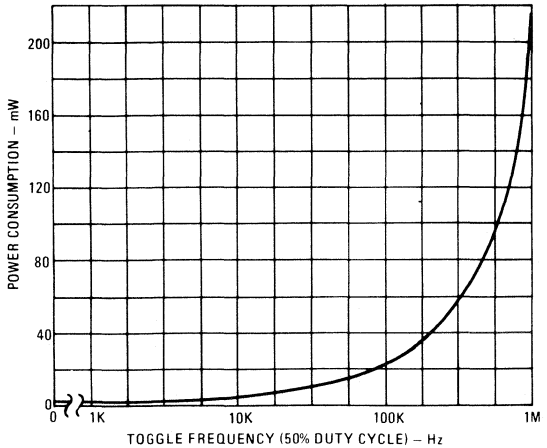
CROSSTALK vs. FREQUENCY

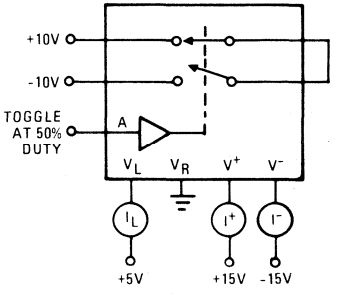




"CROSSTALK" = $20 \log\left(\frac{V_{IN}}{V_{OUT}}\right)$

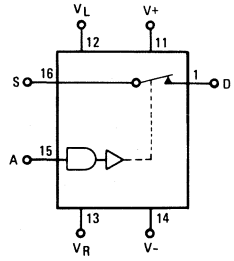
POWER CONSUMPTION vs. FREQUENCY



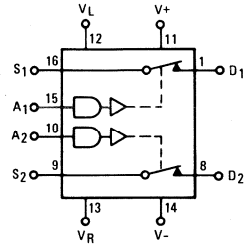


Switch Functions SWITCH STATES ARE FOR LOGIC "1" INPUT

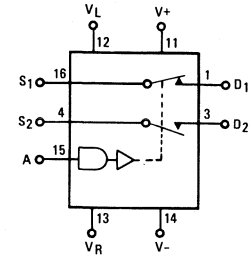
SPST
HI-5040 (75Ω)



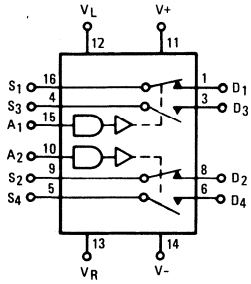
DUAL SPST
HI-5041 (75Ω)



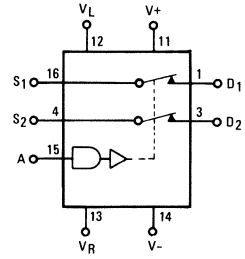
SPDT
HI-5042 (75Ω)



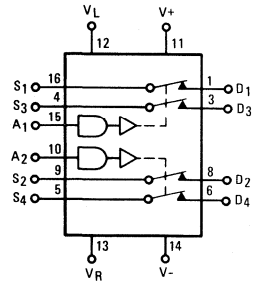
DUAL SPST
HI-5043 (75Ω)



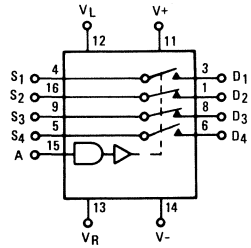
DPST
HI-5044 (75Ω)



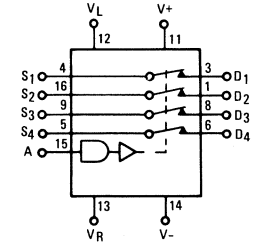
DUAL DPST
HI-5045 (75Ω)



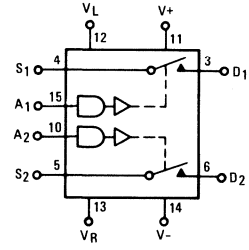
DPDT
HI-5046 (75Ω)
HI-5046A (25Ω)



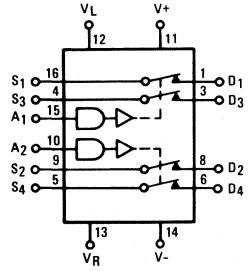
4PST
HI-5047 (75Ω)
HI-5047A (25Ω)



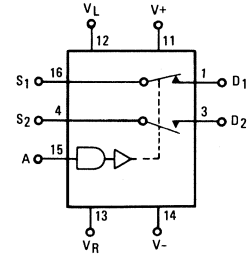
DUAL SPDT
HI-5048 (25Ω)



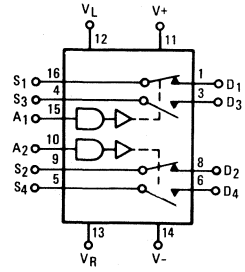
DUAL DPST
HI-5049 (25Ω)



SPDT
HI-5050 (25Ω)



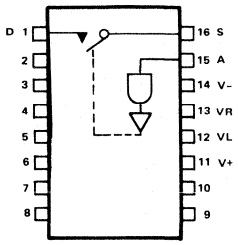
DUAL SPDT
HI-5051 (25Ω)



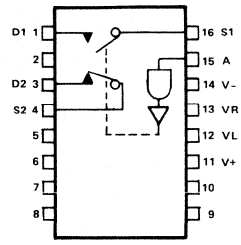
Pin Configurations SWITCH STATES ARE FOR LOGIC "0" INPUT

SINGLE CONTROL

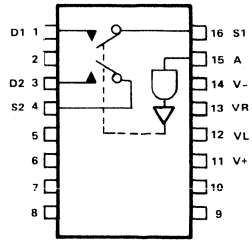
SPST
HI-5040 (75Ω)



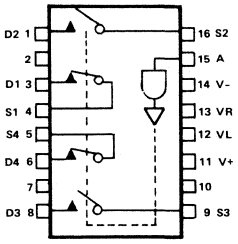
SPDT
HI-5042 (75Ω)
HI-5050 (25Ω)



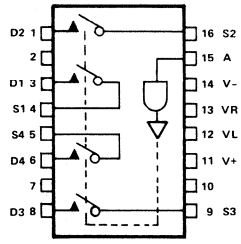
DPST
HI-5044 (75Ω)



DPDT
HI-5046 (75Ω)
HI-5046A (25Ω)

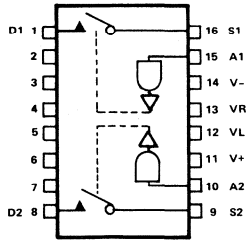


4 SPDT
HI-5047 (75Ω)
HI-5047A(25Ω)

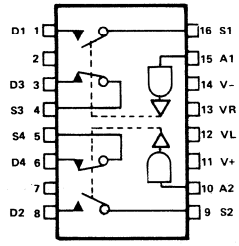


DUAL CONTROL

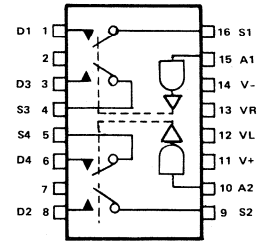
DUAL SPST
HI-5041 (75Ω)



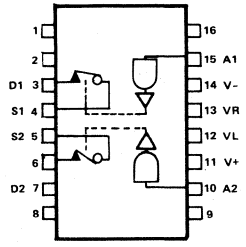
DUAL SPDT
HI-5043 (75Ω)
HI-5051 (25Ω)



DUAL DPST
HI-5045 (75Ω)
HI-5049 (25Ω)



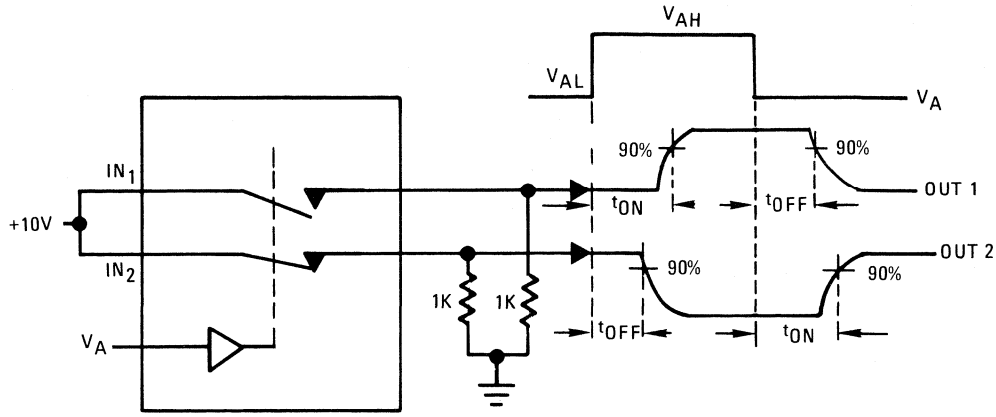
DUAL SPST
HI-5048 (25Ω)



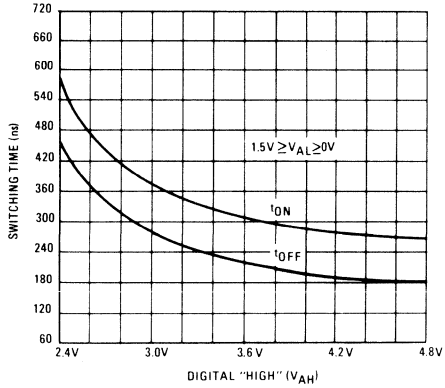
NOTE: Unused pins may be internally connected.
Ground all unused pins.

Switching Characteristics

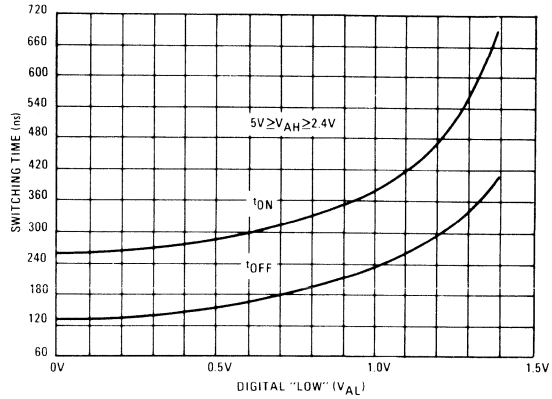
ON/OFF SWITCH TIME vs. LOGIC LEVEL



SWITCHING TIMES FOR POSITIVE DIGITAL TRANSITION

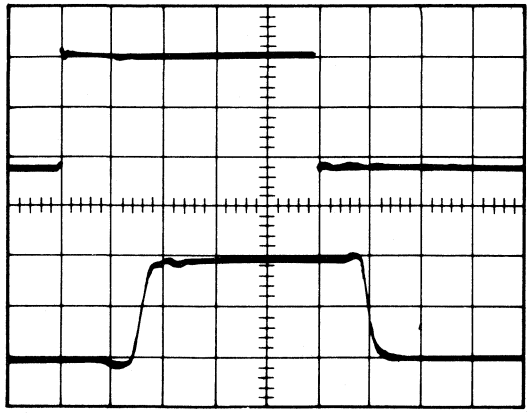


SWITCHING TIMES FOR NEGATIVE DIGITAL TRANSITION



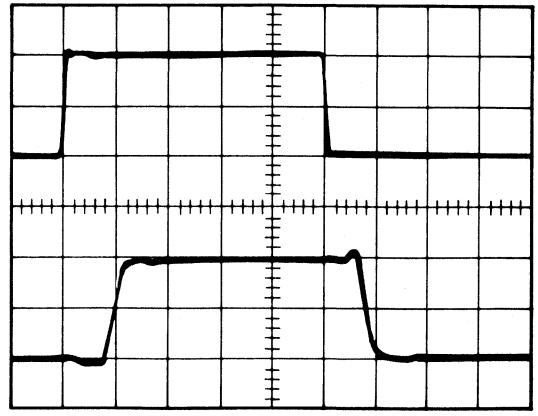
Switching Waveforms

Top: TTL Input (1V/Div.)
V_{AH} = 3V, V_{AL} = 0.8V
Bottom: Output (5V/Div.)
Horizontal: 200ns/Div.



200ns/DIV

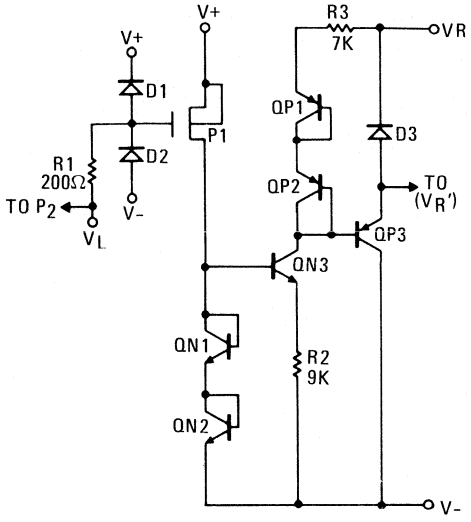
Top: CMOS Input (5V/Div.)
V_{AH} = 10V, V_{AL} = 0V
Bottom: Output (5V/Div.)
Horizontal: 200ns/Div.



200ns/DIV

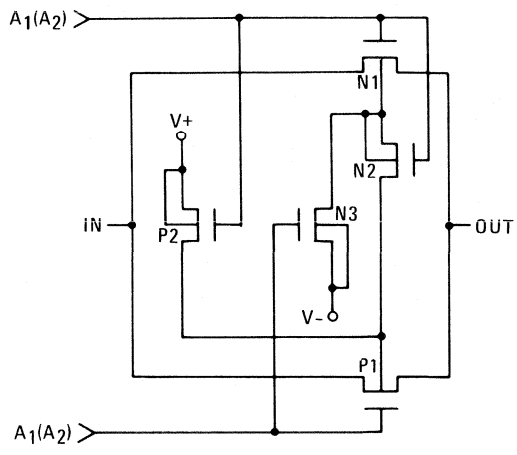
Switching Characteristics

TTL/CMOS REFERENCE CIRCUIT*

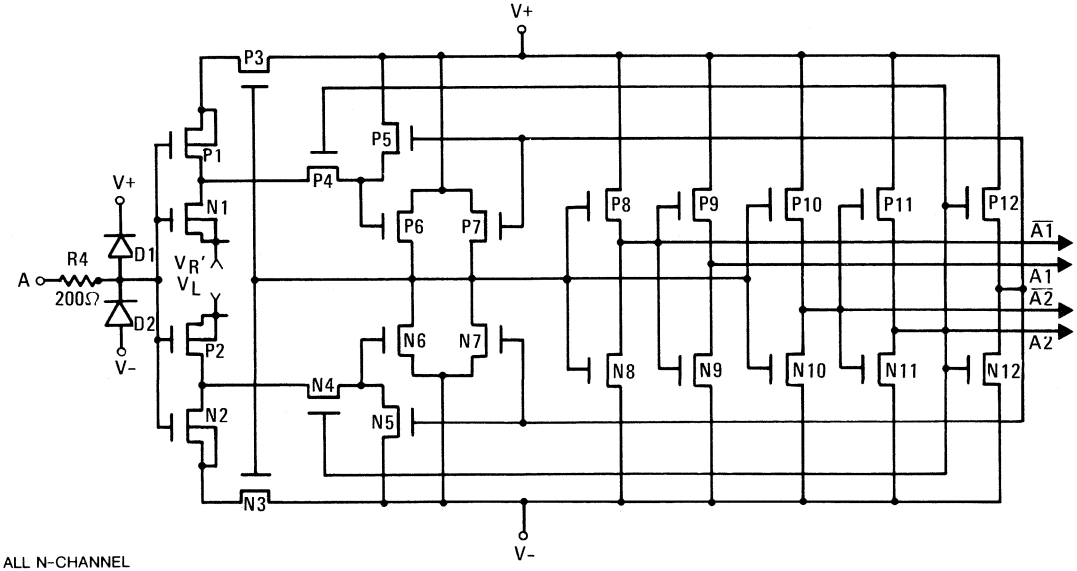


*Connect V+ to V_L for minimizing power consumption when driving from CMOS circuits

SWITCH CELL



DIGITAL INPUT BUFFER AND LEVEL SHIFTER



ALL N-CHANNEL BODIES TO V-

ALL P-CHANNEL BODIES TO V+

EXCEPT AS SHOWN

For Further Information Refer to Application Notes 520, 521, 531, 532, and 557 in Section 10 of Data Book.

ANALOG

Multiplexers

4

ABSOLUTE MAXIMUM RATINGS

As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Specifications" are the only conditions recommended for satisfactory operation.

Ordering Information

HARRIS PRODUCT CODE EXAMPLE

H I 1 — 0506 — 5

PREFIX:
H (HARRIS)

FAMILY:
- A : Analog
- C : Communications
- D : Digital
- F : Filters
- I : Interface
- M : Memory
- V : Analog High Voltage
- Y : Analog Hybrids

PACKAGE:
- 1 : Dual-In-Line Ceramic
- 3 : Dual-In-Line Plastic
- 4 : Leadless Chip Carriers (LCC)
- 4P : Plastic Leaded Chip Carriers (PLCC)
- 5 : LCC Hybrid
- 7 : Mini-DIP, Ceramic
- 0 : Chip Form

PART NUMBER

TEMPERATURE:
- 1 : 0°C to +200°C *
- 2 : -55°C to +125°C
- 4 : -25°C to +85°C
- 5 : 0°C to +75°C
- 6 : 100% +25°C Probe (Dice Only)
- 7 : Dash-7 High Reliability Commercial Product 0°C to +75°C
- 8 : Dash-8 Program
- 9 : -40°C to +85°C

* Special High Temperature Testing Available on Certain Product Types. Consult Factory for Availability.

Standard Products Packaging Availability †

PACKAGE	PLASTIC DIP	CERAMIC DIP					SURFACE MOUNT LCC	SURFACE MOUNT PLCC
TEMPERATURE	-5	-2	-4	-5	-7	-8	-8	-5
DEVICE NUMBER								
MULTIPLEXERS								
HI-0506	S	H	H	H	H	H	U	AB
HI-0506A	S	H		H	H	H	U	
HI-0507	S	H	H	H	H	H	U	AB
HI-0507A	S	H		H	H	H	U	
HI-0508	O	C1	C1	C1	C1	C1	T	AA
HI-0508A	O	C1		C1	C1	C1	T	
HI-0509	O	C1	C1	C1	C1	C1	T	AA
HI-0509A	O	C1		C1	C1	C1	T	
HI-0516	S	H		H		H	U	AB
HI-0518	P	D		D		D	T	AA
HI-0524	P	D		D		D	T	AA
HI-0539	O	C1	C1	C1		C1		AA
HI-1818A	O	C1		C1	C1	C1		AA
HI-1828A	O	C1		C1	C1	C1		AA
HI-0546	S	H	H	H		*	*	AB
HI-0547	S	H	H	H		*	*	AB
HI-0548	O	C1	C1	C1		*	*	AA
HI-0549	O	C1	C1	C1		*	*	AA

* Available as MIL-STD-883 Only.
† Letter codes in this chart indicate available packages as shown in Packaging Section 11.

Selection Guide

CMOS MULTIPLEXERS

FUNCTION	DEVICE	FEATURE	TTL 'HIGH' MIN(V)	R_{ON} (Ω) (TYP)	$I_{D(OFF)}$ (nA) (TYP)	$t_{(ON)}$ (ns) (TYP)	$t_{(OFF)}$ (ns) (TYP)	P_D (mW) (TYP)	ΔR_{ON} (TYP)	PAGE
4-Channel Differential	HI-1828A	Low R_{ON} Low Leakage	4.0	250	0.05	300	300	28 Max	N/A	4-65
	HI-509	Low R_{ON}	2.4	180	0.3	250	250	28	5%	4-16
	HI-509A	Analog Input Overvoltage Protection	4.0	1.2K	0.1	300	300	7.5	N/A	4-23
	HI-549	Analog Input Overvoltage Protection With Low ΔR_{ON}	4.0	1.2K	0.1	300	300	7.5	7% Max	4-59
8-Channel	HI-1818A	Low R_{ON} Low Leakage	4.0	250	0.1	300	300	28 Max	N/A	4-65
	HI-508	Low R_{ON}	2.4	180	0.3	250	250	28	5%	4-16
	HI-508A	Analog Input Overvoltage Protection	4.0	1.2K	0.1	300	300	7.5	N/A	4-23
	HI-548	Analog Input Overvoltage Protection With Low ΔR_{ON}	4.0	1.2K	0.1	300	300	7.5	7% Max	4-59
8-Channel Differential	HI-507	Low R_{ON}	2.4	180	0.3	250	250	30	5%	4-4
	HI-507A	Analog Input Overvoltage Protection	4.0	1.2K	0.1	300	300	7.5	N/A	4-10
	HI-547	Analog Input Overvoltage Protection With Low ΔR_{ON}	4.0	1.2K	0.1	300	300	7.5	7% Max	4-53
16-Channel	HI-506	Low R_{ON}	2.4	180	0.3	250	250	30	5%	4-4
	HI-506A	Analog Input Overvoltage Protection	4.0	1.2K	0.1	300	300	7.5	N/A	4-10
	HI-546	Analog Input Overvoltage Protection With Low ΔR_{ON}	4.0	1.2K	0.1	300	300	7.5	7% Max	4-53
8-Channel 4-Differential	HI-518 Low Leakage	High Speed	2.4	480	0.02	120	140	450 Max	N/A	4-34
16-Channel 8-Differential	HI-516 Low Leakage	High Speed	2.4	620	0.03	120	140	750 Max	N/A	4-29
4-Channel	HI-524	Video Bandwidth	2.4	700	0.02	180	180	750 Max	N/A	4-39
4-Channel Differential	HI-539	Low Level Signals	4.0	650	0.03 $\Delta I_{D(OFF)}$ = .003	250	160	2.3	4Ω	4-44

HARRIS

HI-506/507

Single 16/Differential 8 Channel CMOS Analog Multiplexers

Features

- **Low On Resistance (Typ.) 180Ω**
- **Wide Analog Signal Range ..... ±15V**
- **TTL/CMOS Compatible ... 2.4V (Logic "1")**
- **Access Time (Typ) 250ns**
- **44V Maximum Power Supply**
- **Break-Before-Make Switching**
- **No Latch-up**
- **Replaces DG506A/DG506AA and DG507A/DG507AA**

Applications

- **Data Acquisition Systems**
- **Precision Instrumentation**
- **Demultiplexing**
- **Selector Switch**

Description

These monolithic CMOS multiplexers each include an array of sixteen analog switches, a digital decode circuit for channel selection, a voltage reference for logic thresholds, and an ENABLE input for device selection when several multiplexers are present.

The Dielectric Isolation (DI) process used in fabrication of these devices eliminates the problem of latch-up. Also, DI offers much lower substrate leakage and parasitic capacitance than conventional junction-isolated CMOS (See Application Note 521). With the low ON resistance (180Ω typical), this allows low static error, fast channel switching rates, and fast settling.

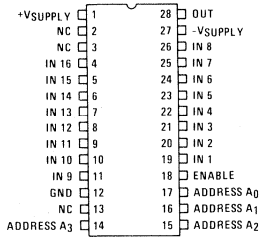
The switching threshold for each digital input is established by an internal +5V reference, providing a guaranteed minimum 2.4V for "1" and maximum 0.8V for "0". This allows direct interface without pull-up resistors to signals from most logic families: CMOS, TTL, DTL and some PMOS. For protection against transient overvoltage, the digital inputs include a series 200Ω resistor and diode clamp to each supply.

The HI-506 is a sixteen channel single-ended multiplexer, and the HI-507 is an eight channel differential version. Each device is available in a 28 pin Ceramic or Plastic DIP, 28 pad Leadless Chip Carrier (LCC), and 28 pin Plastic Leaded Chip Carrier (PLCC) packages. If input overvoltage protection is needed, the HI-546/547 multiplexers are recommended. For further information see Application Notes 520 and 521.

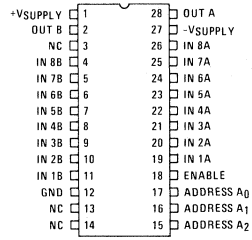
The HI-506/507 is offered in both commercial and military grades. For additional Hi-Rel screening including 160 hour burn-in specify the "-8" suffix. For MIL-STD-883 compliant parts, request the HI-506/883 or HI-507/883 data sheet.

Pinouts

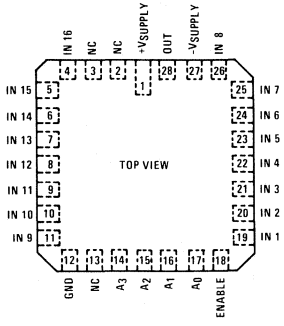
HI1-506 (CERAMIC DIP)
HI3-506 (PLASTIC DIP)
TOP VIEW



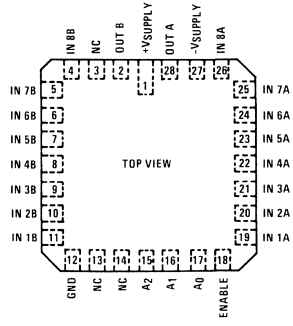
HI1-507 (CERAMIC DIP)
HI3-507 (PLASTIC DIP)
TOP VIEW



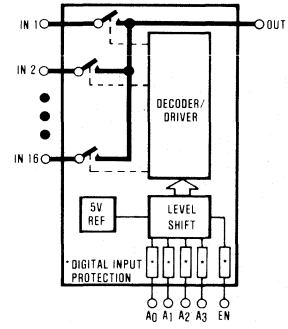
HI4-506 (CERAMIC LCC)
HI4P506 (PLCC)
TOP VIEW



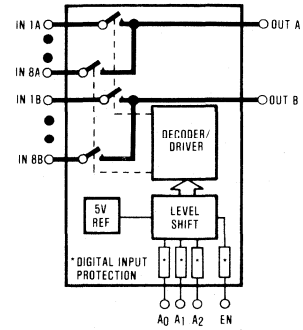
HI4-507 (CERAMIC LCC)
HI4P507 (PLCC)
TOP VIEW



Functional Diagrams



HI-506



HI-507

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

$V_{SUPPLY(+)}$ to $V_{SUPPLY(-)}$ 44V
$V_{SUPPLY(+)}$ to GND 22V
$V_{SUPPLY(-)}$ to GND 25V
Digital Input Overvoltage
$+V_{EN}$, $+V_A$ ..... $+V_{SUPPLY}$ +4V
$-V_{EN}$, $-V_A$ ..... $-V_{SUPPLY}$ -4V
or 20mA, whichever occurs first
Analog Signal Overvoltage (Note 7)
$+V_S$ ..... $+V_{SUPPLY}$ +2V
$-V_S$ ..... $-V_{SUPPLY}$ -2V
Continuous Current, S or D: 20mA
Peak Current, S or D
(Pulsed at 1ms, 10% duty cycle max): 40mA
Junction Temperature ..... +175°C
Operating Temperature Ranges:
HI-506/507-2, -8 ..... -55°C to +125°C
HI-506/507-4 ..... -25°C to +85°C
HI-506/507-5 ..... 0°C to +75°C
Storage Temperature Range ..... -65°C to +150°C

Electrical Specifications Unless Otherwise Specified:

Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V;
V_{AL} (Logic Level Low) = +0.8V. For Test Conditions, consult Performance Characteristics Section.

PARAMETER	TEMP.	HI-506/HI-507 -2, -8 MIN.	HI-506/HI-507 -2, -8 TYP.	HI-506/HI-507 -2, -8 MAX.	HI-506/507 -4, -5 MIN.	HI-506/507 -4, -5 TYP.	HI-506/507 -4, -5 MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS								
*V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
*R_{ON}, On Resistance (Note 2)	+25°C		180	300		180	400	Ω
	Full			400			500	Ω
△R_{ON}, (Any Two Channels)	+25°C		5			5		%
*I_S (OFF), Off Input Leakage Current (Note 3)	+25°C		0.03			0.03		nA
	Full			50			50	nA
*I_D (OFF), Off Output Leakage Current (Note 3)	+25°C		0.3			0.3		nA
HI-506	Full			300			300	nA
HI-507	Full			200			200	nA
*I_D (ON), On Channel Leakage Current (Note 3)	+25°C		0.3			0.3		nA
HI-506	Full			300			300	nA
HI-507	Full			200			200	nA
*I_{DIFF}, Differential Off Output Leakage Current (HI-507 Only)	Full			50			50	nA
DIGITAL INPUT CHARACTERISTICS								
*V_{AL}, Input Low Threshold	Full			+0.8			+0.8	V
*V_{AH}, Input High Threshold	Full	+2.4			+2.4			V
*I_A, Input Leakage Current (High or Low) (Note 4)	Full			1.0			1.0	μA
SWITCHING CHARACTERISTICS								
*t_A, Access Time	+25°C		250	500		250		ns
	Full			1000			1000	ns
*t_{OPEN}, Break-Before-Make Delay	+25°C	25	80		25	80		ns
*t_{ON} (EN), Enable Delay (ON)	+25°C		250	500		250		ns
	Full			1000			1000	ns
*t_{OFF} (EN), Enable Delay (OFF)	+25°C		250	500		250		ns
	Full			1000			1000	ns
Settling Time (0.1%)	+25°C		1.2			1.2		μs
(0.01%)	+25°C		2.4			2.4		μs
"Off Isolation" (Note 5)	+25°C	50	68		50	68		dB
C_S (OFF), Channel Input Capacitance	+25°C		5			5		pF
C_D (OFF), Channel Output Capacitance HI-506	+25°C		44			44		pF
HI-507	+25°C		22			22		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
C_{DS} (OFF), Input to Output Capacitance	+25°C		0.08			0.08		pF
POWER REQUIREMENTS								
*I+, Current, Pin 1 (Note 6)	Full		1.5	3.0		1.5	3.0	mA
*I−, Current Pin 27 (Note 6)	Full		0.4	1.0		0.4	1.0	mA

*100% tested for Dash 8. Leakage currents not tested at −55°C.

TRUTH TABLES

HI-506

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	NONE
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

HI-507

A_2	A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

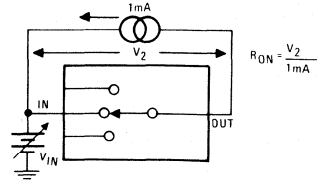
NOTES:
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. V_{OUT} = ±10V, I_{OUT} = -1mA.
3. Ten nanoamps is the practical lower limit for high speed measurement in the production test environment.
4. Digital input leakage is primarily due to the clamp diodes (see Schematic). Typical leakage is less than 1nA at 25°C.
5. V_{EN} = 0.8V, R_L = 1K, C_L = 15pF, V_S = $7V_{RMS}$, f = 100kHz.
6. V_{EN}, V_A = 0V or 2.4V.
7. Signal voltage at any analog input or output (S or D) will be clamped to the supply rail by internal diodes. Limit the resulting current as shown under absolute maximum ratings. If an overvoltage condition is anticipated (analog input exceeds either power supply voltage), the Harris HI-546/547 multiplexers are recommended.

Performance Characteristics and Test Circuits

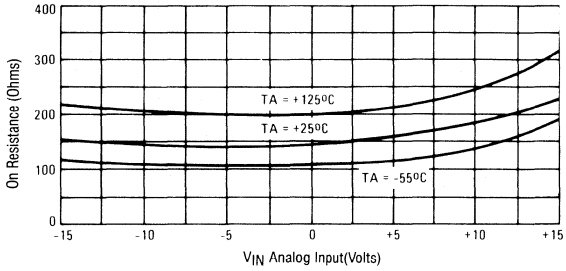
Unless Otherwise Specified; T_A = 25°C, V_{Supply} = ±15 V, V_{AH} = 2.4 V, V_{AL} = 0.8 V.

TEST CIRCUIT NO. 1

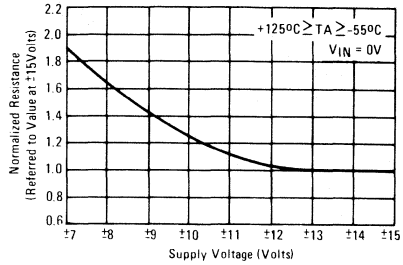
ON RESISTANCE vs. INPUT SIGNAL LEVEL, SUPPLY VOLTAGE



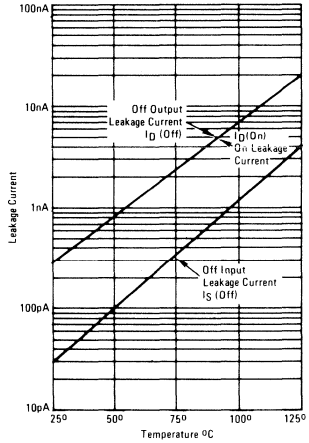
ON RESISTANCE vs. ANALOG INPUT VOLTAGE, TEMPERATURE



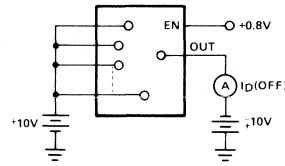
NORMALIZED ON RESISTANCE vs. SUPPLY VOLTAGE



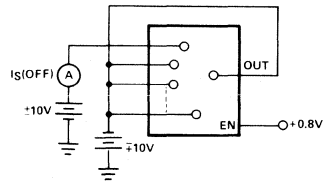
LEAKAGE CURRENT VS. TEMPERATURE



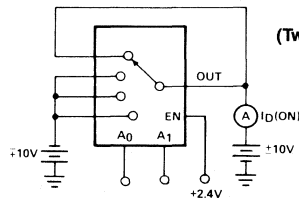
TEST CIRCUIT NO. 2*



TEST CIRCUIT NO. 3*

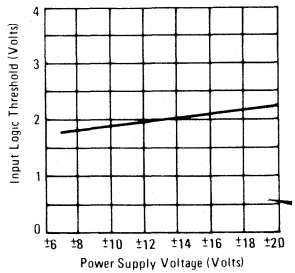


TEST CIRCUIT NO. 4*

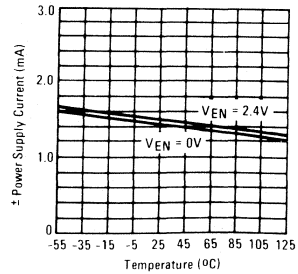


***Two measurements per channel: +10 V/−10 V and −10 V/+10 V. (Two measurements per device for $I_{D(OFF)}$ +10 V/−10 V and −10 V/+10 V.)**

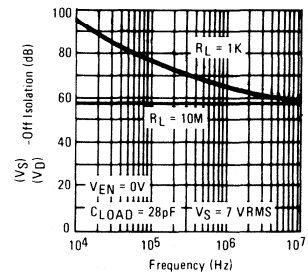
LOGIC THRESHOLD vs. POWER SUPPLY VOLTAGE



POWER SUPPLY CURRENT vs. TEMPERATURE

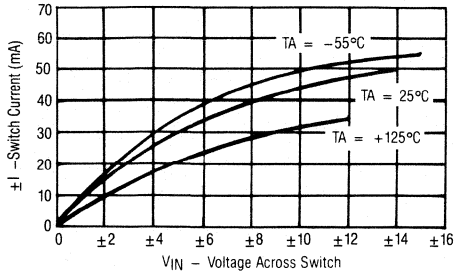


OFF ISOLATION vs. FREQUENCY



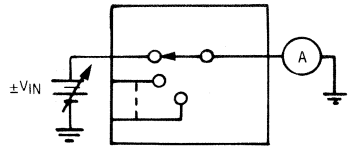
Performance Characteristics and Test Circuits (continued)

ON CHANNEL CURRENT vs. VOLTAGE



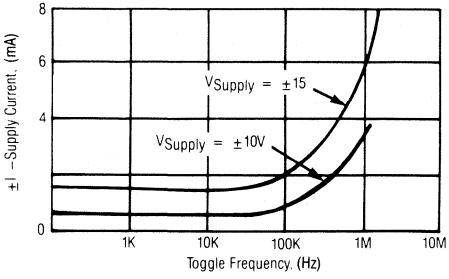
TEST CIRCUIT NO. 5

ON CHANNEL CURRENT vs. VOLTAGE

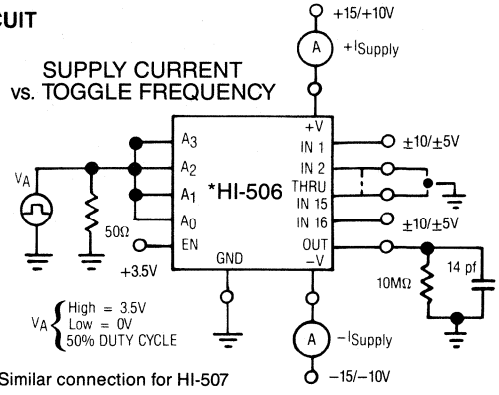


TEST CIRCUIT NO. 6

SUPPLY CURRENT vs. TOGGLE FREQUENCY



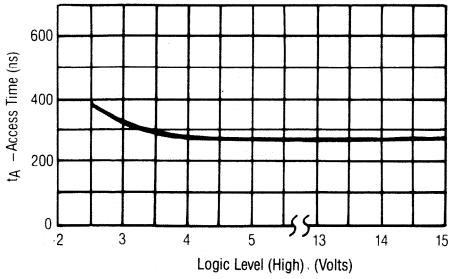
SUPPLY CURRENT vs. TOGGLE FREQUENCY



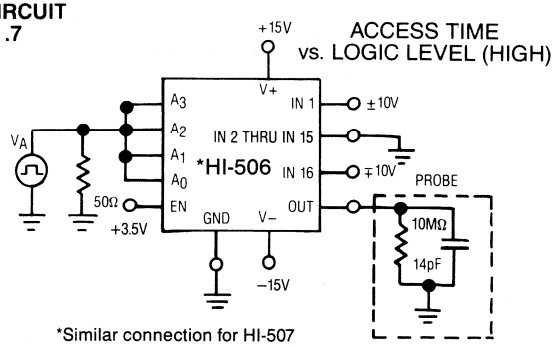
*Similar connection for HI-507

TEST CIRCUIT NO .7

ACCESS TIME VS. LOGIC LEVEL (HIGH)

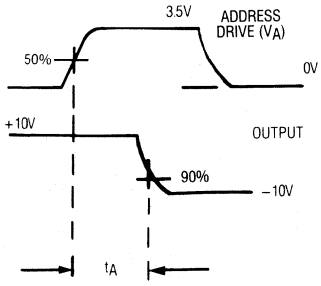


ACCESS TIME vs. LOGIC LEVEL (HIGH)

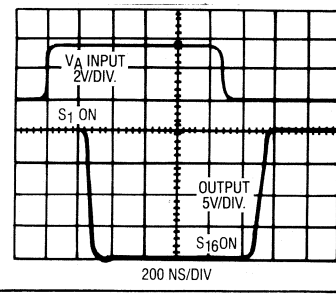


*Similar connection for HI-507

Switching Waveforms



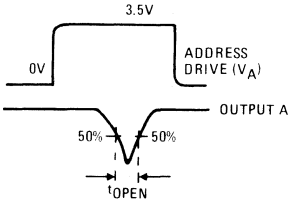
ACCESS TIME

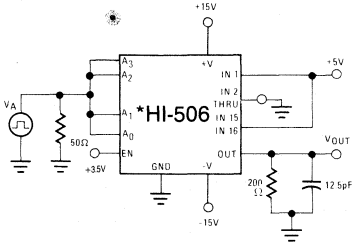


Switching Waveforms (continued)

TEST CIRCUIT NO. 8

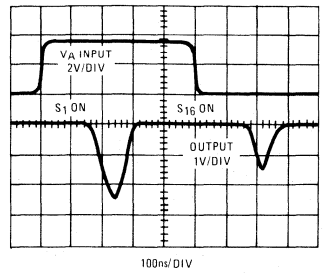
BREAK-BEFORE-MAKE DELAY (t_{OPEN})





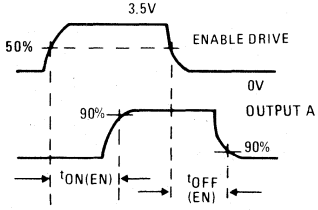
*Similar connection for HI-507

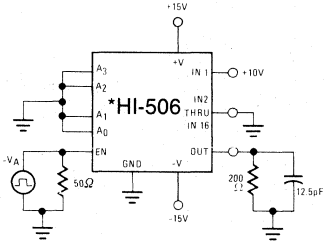
BREAK-BEFORE-MAKE DELAY(t_{OPEN})



TEST CIRCUIT NO. 9

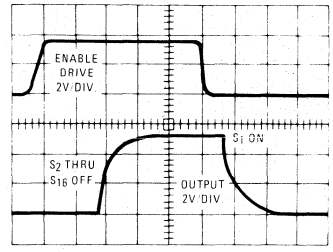
ENABLE DELAY $t_{ON(EN)}$,$t_{OFF(EN)}$





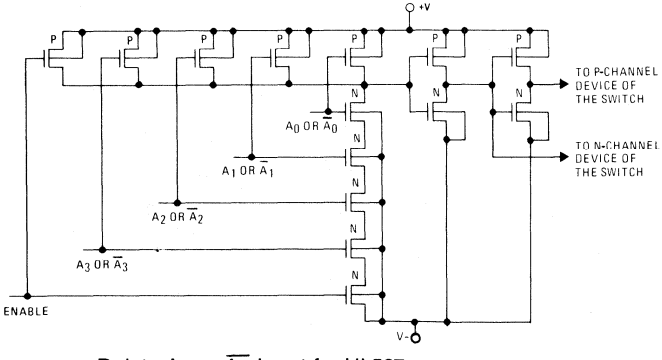
*Similar connection for HI-507

ENABLE DELAY $t_{ON(EN)}$,$t_{OFF(EN)}$



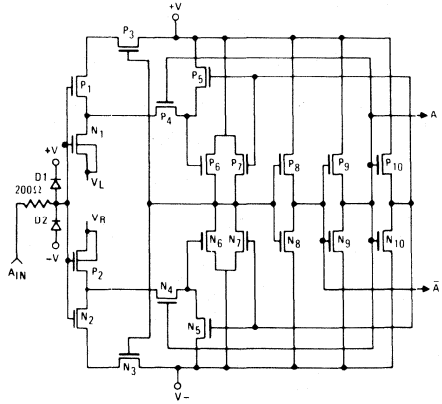
Schematic Diagrams

ADDRESS DECODER



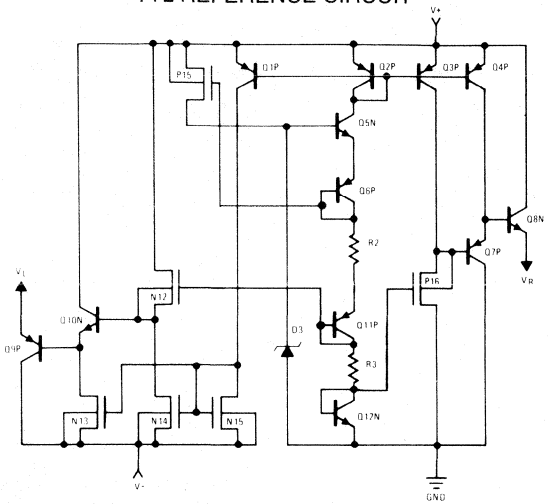
Delete A_3 or $\overline{A_3}$ Input for HI-507

ADDRESS INPUT BUFFER LEVER SHIFTER

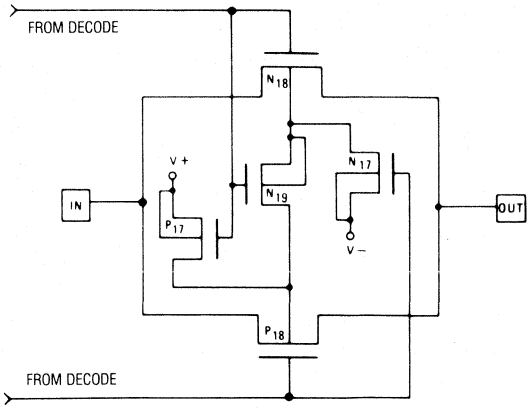


All N-Channel Bodies to V–
All P-Channel Bodies to V+
Unless Otherwise Indicated

TTL REFERENCE CIRCUIT



MULTIPLEX SWITCH



Die Characteristics

Transistor Count		421
Die Dimensions		129 x 82 mils
Substrate Potential*		$-V_{SUPPLY}$
Process		CMOS-DI
Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
Ceramic DIP	51	20
Ceramic LCC	81	40

*The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential.

HARRIS HI-506A/507A

Single 16/Differential 8 Channel CMOS Analog Multiplexers with Active Overvoltage Protection

Features

- **Analog Overvoltage Protection ... $70V_{p-p}$**
- **No Channel Interaction During Overvoltage**
- **ESD Resistant ..... >4,000V**
- **44V Maximum Power Supply**
- **Fail Safe with Power Loss (No Latch-Up)**
- **Break-Before-Make Switching**
- **Analog Signal Range ..... ±15V**
- **Access Time (Typical) 500ns**
- **Standby Power (Typical) 7.5mW**

Applications

- **Data Acquisition**
- **Industrial Controls**
- **Telemetry**

Description

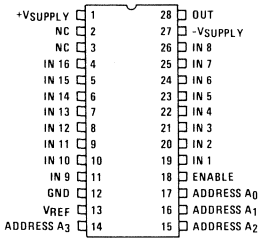
The HI-506A and HI-507A are analog multiplexers with Active Overvoltage Protection. Analog input levels may greatly exceed either power supply without damaging the device or disturbing the signal path of other channels. Active protection circuitry assures that signal fidelity is maintained even under fault conditions that would destroy other multiplexers. Analog inputs can withstand constant 70 volt peak-to-peak levels and typically survive static discharges beyond 4,000 volts. Digital inputs will also sustain continuous faults up to 4 volts greater than either supply. In addition, signal sources are protected from short circuiting should multiplexer supply loss occur; each input presents 1kΩ of resistance under this condition. These features make the HI-506A and HI-507A ideal for use in systems where the analog inputs originate from external equipment or separately powered circuitry. Both devices are fabricated with 44 volt dielectrically isolated CMOS technology. The HI-506A is a 16 channel device and the HI-507A is an 8 channel differential version. If input overvoltage protection is not needed, the HI-506 and HI-507 multiplexers are recommended. For further information see Application Notes 520 and 521.

Each device is available in a 28 pin Plastic or Ceramic DIP and a 28 pad Ceramic LCC package.

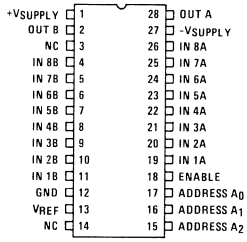
The HI-506A/507A are offered in both commercial and military grades. Additional Hi-Rel screening including 160 hour burn-in is specified by the "-8" suffix. For MIL-STD-883 compliant parts, request the HI-546/883 or HI-547/883 data sheets.

Pinouts

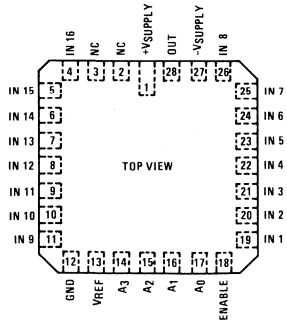
HI1-506A (CERAMIC DIP)
HI3-506A (PLASTIC DIP)
TOP VIEW



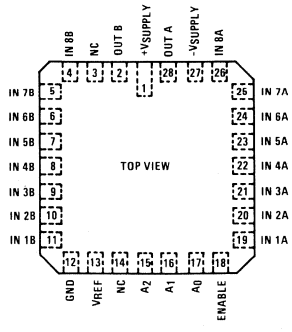
HI1-507A (CERAMIC DIP)
HI3-507A (PLASTIC DIP)
TOP VIEW



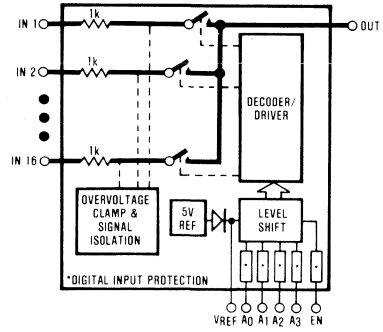
HI4-506A (CERAMIC LCC)
TOP VIEW



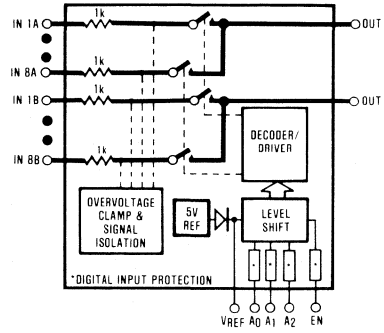
HI4-507A (CERAMIC LCC)
TOP VIEW



Functional Diagrams



HI-506A



HI-507A

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

$V_{SUPPLY(+)}$ to $V_{SUPPLY(-)}$ 44V
$V_{SUPPLY(+)}$ to GND 22V
$V_{SUPPLY(-)}$ to GND 25V
Digital Input Overvoltage
$+V_{EN}$, $+V_A$ ..... $+V_{SUPPLY}$ +4V
$-V_{EN}$, $-V_A$ ..... $-V_{SUPPLY}$ -4V
or 20mA, whichever occurs first
Analog Signal Overvoltage
$+V_S$ ..... $+V_{SUPPLY}$ +20V
$-V_S$ ..... $-V_{SUPPLY}$ -20V

Continuous Current, S or D: 20mA
Peak Current, S or D
(Pulsed at 1ms, 10% duty cycle max): 40mA
Junction Temperature ..... +175°C
Operating Temperature Ranges:
HI-506A/507A-2, -8 ..... -55°C to +125°C
HI-506A/507A-4 ..... -25°C to +85°C
HI-506A/507A-5 ..... 0°C to +75°C
Storage Temperature Range ..... -65°C to +150°C

Electrical Specifications Unless Otherwise Specified:

Supplies = +15V, -15V; V_{REF} pin = Open; V_{AH} (Logic Level High) = +4.0V;
V_{AL} (Logic Level Low) = +0.8V. For Test Conditions, consult Performance Characteristics Section.

PARAMETER	TEMP.	HI-506A/HI-507A -2, -8 MIN.	TYP.	MAX.	HI-506A/507A -4, -5 MIN.	TYP.	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS								
*V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
*R_{ON}, On Resistance (Note 2)	+25°C		1.2	1.5		1.5	1.8	kΩ
	Full		1.5	1.8		1.8	2.0	kΩ
*I_S (OFF), Off Input Leakage Current (Note 3)	+25°C		0.03			0.03		nA
	Full			50			50	nA
*I_D (OFF), Off Output Leakage Current (Note 3)	+25°C		0.1			0.1		nA
HI-506A	Full			300			300	nA
HI-507A	Full			200			200	nA
*I_D (OFF), with Input Overvoltage Applied (Note 4)	+25°C		4.0			4.0		nA
	Full			2.0				μA
*I_D (ON), On Channel Leakage Current (Note 3)	+25°C		0.1			0.1		nA
HI-506A	Full			300			300	nA
HI-507A	Full			200			200	nA
I_{DIFF}, Differential Off Output Leakage Current (HI-507A Only)	Full			50			50	nA
DIGITAL INPUT CHARACTERISTICS								
*V_{AL}, Input Low Threshold TTL Drive	Full			0.8			0.8	V
*V_{AH}, Input High Threshold (Note 8)	Full	4.0			4.0			V
V_{AL} MOS Drive (Note 9)	+25°C			0.8			0.8	V
V_{AH} MOS Drive (Note 9)	+25°C	6.0			6.0			V
*I_A, Input Leakage Current (High or Low) (Note 5)	Full			1.0			1.0	μA
SWITCHING CHARACTERISTICS								
*t_A, Access Time	+25°C		0.5			0.5		μs
	Full			1.0			1.0	μs
*t_{OPEN}, Break-Before-Make Delay	+25°C	25	80		25	80		ns
*t_{ON} (EN), Enable Delay (ON)	+25°C		300	500		300		ns
	Full			1000			1000	ns
*t_{OFF} (EN), Enable Delay (OFF)	+25°C		300	500		300		ns
	Full			1000			1000	ns
Settling Time (0.1%)	+25°C		1.2			1.2		μs
(0.01%)	+25°C		3.5			3.5		μs
"Off Isolation" (Note 6)	+25°C	50	68		50	68		dB
C_S (OFF), Channel Input Capacitance	+25°C		5			5		pF
C_D (OFF), Channel Output Capacitance HI-506A	+25°C		50			50		pF
HI-507A	+25°C		25			25		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
C_{DS} (OFF), Input to Output Capacitance	+25°C		0.1			0.1		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full		75			75		mW
*I+, Current Pin 1 (Note 7)	Full		0.5	2.0		0.5	2.0	mA
*I-, Current Pin 27 (Note 7)	Full		0.02	1.0		0.02	1.0	mA

*100% tested for Dash 8. Leakage currents not tested at -55°C.

TRUTH TABLES

HI-506A

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	NONE
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

HI-507A

A_2	A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

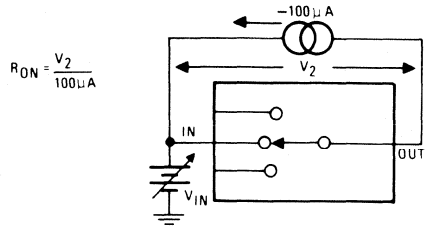
NOTES:
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. V_{OUT} = ±10V, I_{OUT} = -100 μA.
3. Ten nanoamps is the practical lower limit for high speed measurement in the production test environment.
4. Analog Overvoltage = ±33 V.
5. Digital input leakage is primarily due to the clamp diodes (see Schematic). Typical leakage is less than 1 nA at 25°C.
6. V_{EN} = 0.8 V, R_L = 1 K, C_L = 15 pF, V_S = 7 V_{RMS}, f = 100 kHz.
7. V_{EN}, V_A = 0 V or 4.0 V.
8. To drive from DTL/TTL Circuits, 1 kΩ pull-up resistors to +5.0 V supply are recommended.
9. V_{REF} = +10 V.

Performance Characteristics and Test Circuits

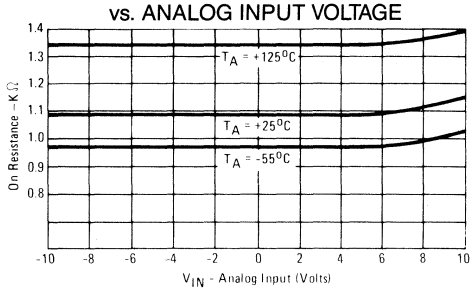
Unless Otherwise Specified: T_A = 25°C, V_{Supply} = ±15 V, V_{AH} = +4 V, V_{AL} = 0.8 V And V_{Ref} = Open.

ON RESISTANCE vs. INPUT SIGNAL LEVEL, SUPPLY VOLTAGE

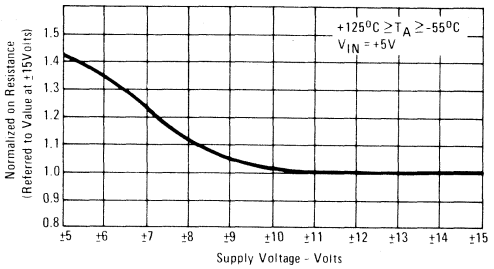
TEST CIRCUIT NO. 1



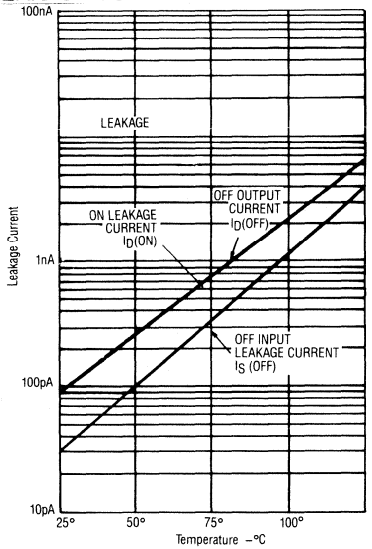
ON RESISTANCE vs. ANALOG INPUT VOLTAGE



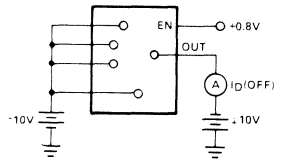
NORMALIZED ON RESISTANCE vs. SUPPLY VOLTAGE



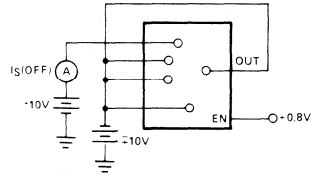
LEAKAGE CURRENT VS. TEMPERATURE



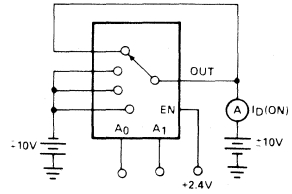
TEST CIRCUIT NO. 2*



TEST CIRCUIT NO. 3*

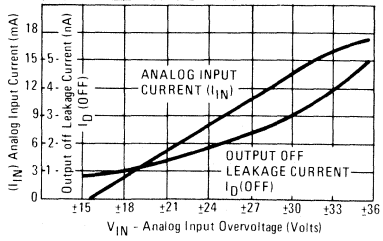


TEST CIRCUIT NO. 4*



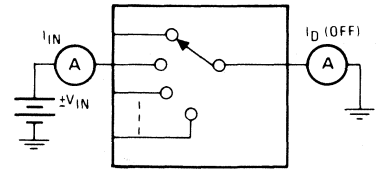
***Two measurements per channel: +10 V/−10 V and −10 V/+10 V. (Two measurements per device for $I_{D(OFF)}$: +10 V/−10 V and −10 V/+10 V.)**

ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



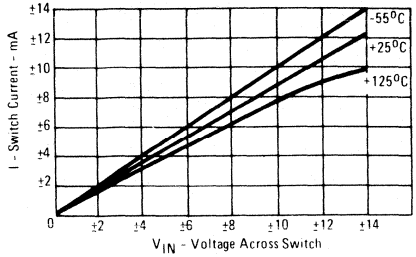
TEST CIRCUIT NO. 5

ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



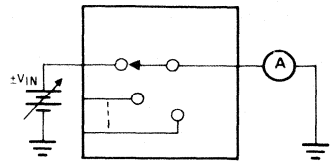
Performance Characteristics and Test Circuits (continued)

ON CHANNEL CURRENT vs. VOLTAGE

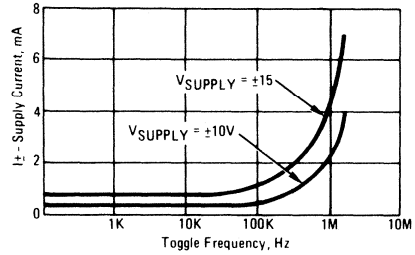


TEST CIRCUIT NO. 6

ON CHANNEL CURRENT vs. VOLTAGE

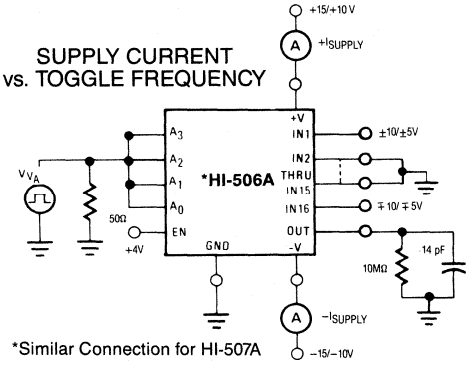


SUPPLY CURRENT vs. TOGGLE FREQUENCY



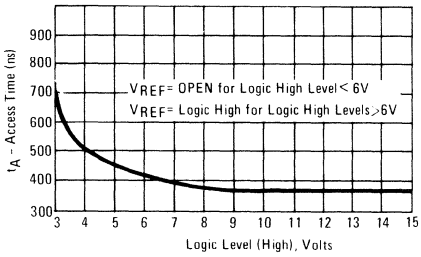
TEST CIRCUIT NO. 7

SUPPLY CURRENT vs. TOGGLE FREQUENCY



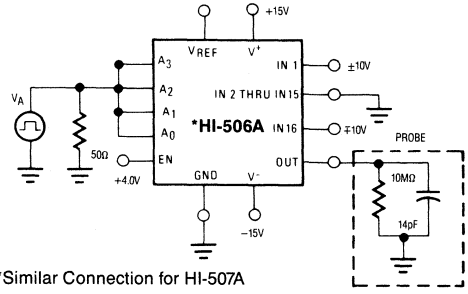
*Similar Connection for HI-507A

ACCESS TIME VS. LOGIC LEVEL (HIGH)



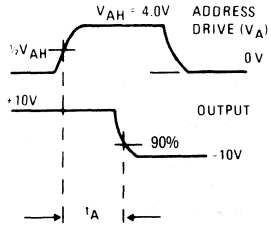
TEST CIRCUIT NO. 8

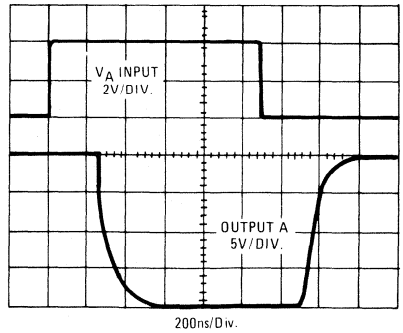
ACCESS TIME vs. LOGIC LEVEL (HIGH)



*Similar Connection for HI-507A

Switching Waveforms

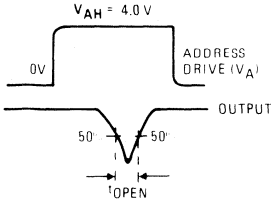


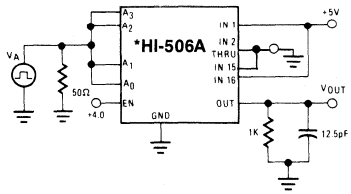


Switching Waveforms (continued)

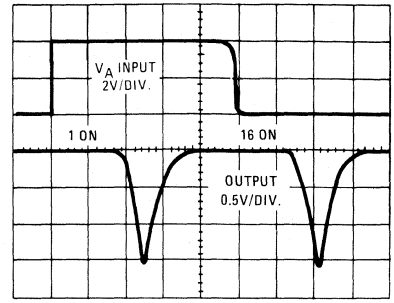
TEST CIRCUIT NO. 9

BREAK-BEFORE-MAKE DELAY (tOPEN)





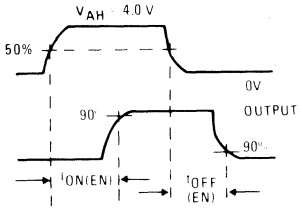
BREAK-BEFORE-MAKE DELAY(tOPEN)



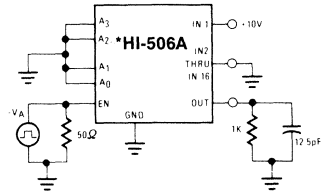
*Similar Connection for HI-507A

TEST CIRCUIT NO. 10

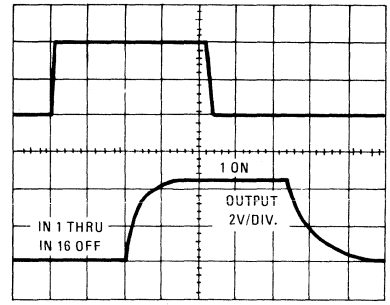
ENABLE DRIVE



ENABLE DELAY (tON(EN),tOFF(EN))

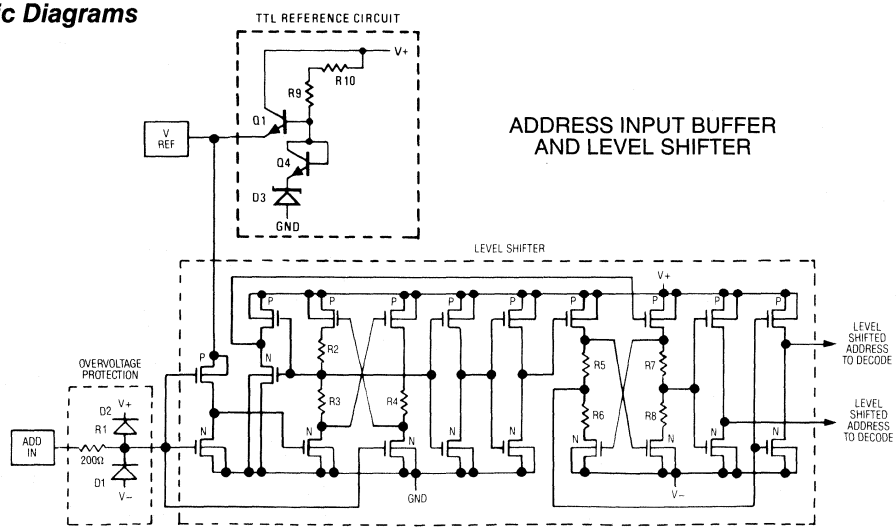


ENABLE DELAY (tON(EN),tOFF(EN))

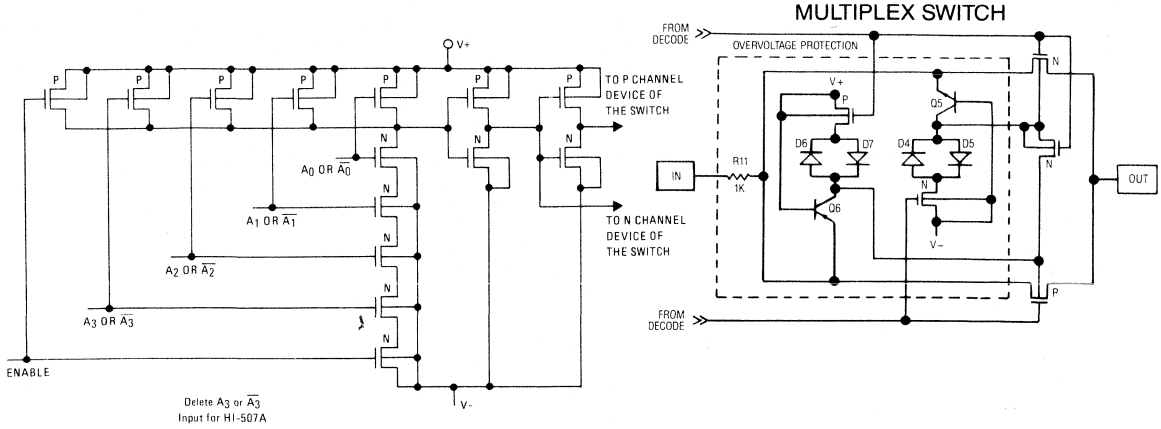


*Similar Connection for HI-507A

Schematic Diagrams



Schematic Diagrams (continued)



Die Characteristics

Transistor Count	485
Die Dimensions	159 x 84 mils
Substrate Potential*	$-V_{SUPPLY}$
Process	CMOS-DI

Thermal Constants ($^oC/W$)	θ_{ja}	θ_{jc}
Ceramic DIP	50	18
Ceramic LCC	81	40

*The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential.

HARRIS

HI-508/509

Single 8/Differential 4 Channel CMOS Analog Multiplexers

Features

- Low On Resistance (Typ) 180Ω
- Wide Analog Signal Range ..... ±15V
- TTL/CMOS Compatible ..... 2.4V (Logic "1")
- Fast Access 250ns
- Fast Settling (0.01%) 600ns
- 44V Maximum Power Supply
- Break-Before-Make Switching
- No Latch-Up
- Replaces DG508A/DG508AA and DG509A/DG509AA

Applications

- Data Acquisition Systems
- Precision Instrumentation
- Demultiplexing
- Selector Switch

Description

These monolithic CMOS multiplexers each include an array of eight analog switches, a digital decode circuit for channel selection, a voltage reference for logic thresholds, and an ENABLE input for device selection when several multiplexers are present.

The Dielectric Isolation (DI) process used in fabrication of these devices eliminates the problem of latch-up. Also, DI offers much lower substrate leakage and parasitic capacitance than conventional junction-isolated CMOS (see Application Note 521). Combined with the low ON resistance (180Ω typical), these benefits allow low static error, fast channel switching rates, and fast settling.

Switches are guaranteed to break-before-make, so that two channels are never shorted together.

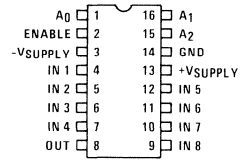
The switching threshold for each digital input is established by an internal +5V reference, providing a guaranteed minimum 2.4V for "1" and maximum 0.8V for "0". This allows direct interface without pull-up resistors to signals from most logic families: CMOS, TTL, DTL and some PMOS. For protection against transient overvoltage, the digital inputs include a series 200Ω resistor and a diode clamp to each supply.

The HI-508 is an eight channel single-ended multiplexer, and the HI-509 is a four channel differential version. Each device is available in a 16 pin Plastic or Ceramic DIP, a 20 pin Plastic Leaded Chip Carrier (PLCC) or 20 pad Ceramic Leadless Chip Carrier (LCC). If input overvoltage protection is needed, the HI-548/549 multiplexers are recommended.

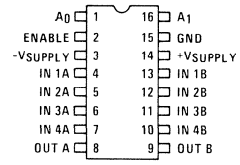
The HI-508/509 is offered in both commercial and military grades, suitable for spacecraft/military applications. For additional Hi-Rel screening including 160 hour burn-in, specify the "-8" suffix. For further information see Application Notes 520 and 521. For MIL-STD-883 compliant parts, request the HI-508/883 or HI-509/883 data sheets.

Pinouts

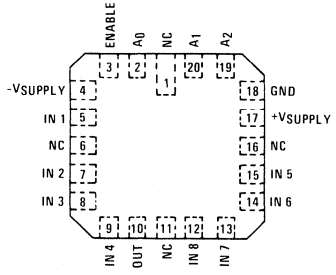
HI1-508 (CERAMIC DIP)
HI3-508 (PLASTIC DIP)
TOP VIEW



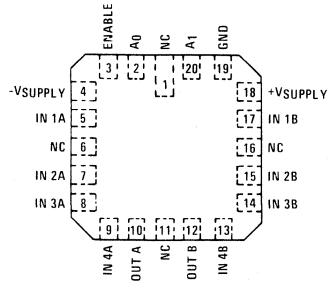
HI1-509 (CERAMIC DIP)
HI3-509 (PLASTIC DIP)
TOP VIEW



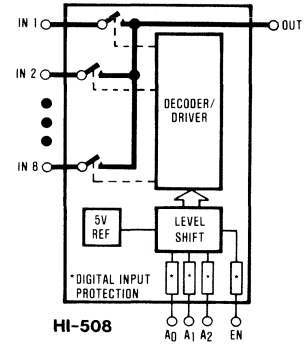
HI4-508 (CERAMIC LCC)
HI4P508 (PLCC)
TOP VIEW



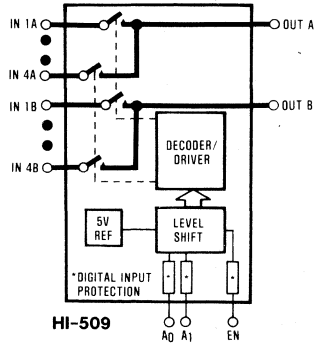
HI4-509 (CERAMIC LCC)
HI4P509 (PLCC)
TOP VIEW



Functional Diagrams



HI-508



HI-509

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

$V_{SUPPLY(+)}$ to $V_{SUPPLY(-)}$ 44V
$V_{SUPPLY(+)}$ to GND 22V
$V_{SUPPLY(-)}$ to GND 25V
Digital Input Overvoltage
$+V_{EN}$, $+V_A$ ..... $+V_{SUPPLY}$ +4V
$-V_{EN}$, $-V_A$ ..... $-V_{SUPPLY}$ -4V
or 20mA, whichever occurs first
Analog Signal Overvoltage (Note 7)
$+V_S$ ..... $+V_{SUPPLY}$ +2V
$-V_S$ ..... $-V_{SUPPLY}$ -2V
Continuous Current, S or D: 20mA
Peak Current, S or D
(Pulsed at 1ms, 10% duty cycle max): 40mA
Junction Temperature ..... +175°C
Operating Temperature Ranges:
HI-508/509-2, -8 ..... -55°C to +125°C
HI-508/509-4 ..... -25°C to +85°C
HI-508/509-5 ..... 0°C to +75°C
Storage Temperature Range ..... -65°C to +150°C

Electrical Specifications Unless Otherwise Specified:

Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V;
V_{AL} (Logic Level Low) = +0.8V. For Test Conditions, consult Performance Characteristics Section.

PARAMETER	TEMP.	HI-508/HI-509 -2, -8 MIN.	TYP.	MAX.	HI-508/509 -4, -5 MIN.	TYP.	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS								
*V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
*R_{ON}, On Resistance (Note 2)	+25°C		180	300		180	400	Ω
	Full			400			500	Ω
$\triangle R_{ON}$, Any Two Channels	+25°C		5			5		%
*I_S (OFF), Off Input Leakage Current (Note 3)	+25°C		0.03			0.03		nA
	Full			50			50	nA
*I_D (OFF), Off Output Leakage Current (Note 3)	+25°C		0.3			0.3		nA
HI-508	Full			200			200	nA
HI-509	Full			100			100	nA
*I_D (ON), On Channel Leakage Current (Note 3)	+25°C		0.3			0.3		nA
HI-508	Full			200			200	nA
HI-509	Full			100			100	nA
*I_{DIFF}, Differential Off Output Leakage Current (HI-509 Only)	Full			50			50	nA
DIGITAL INPUT CHARACTERISTICS								
*V_{AL}, Input Low Threshold	Full			0.8			0.8	V
*V_{AH}, Input High Threshold	Full	2.4			2.4			V
*I_A, Input Leakage Current (High or Low) (Note 4)	Full			1.0			1.0	μA
SWITCHING CHARACTERISTICS								
*t_A, Access Time	+25°C		250	500		250		ns
	Full			1000			1000	ns
*t_{OPEN}, Break-Before-Make Interval	+25°C	25	80		25	80		ns
*t_{ON} (EN), Enable Turn-On	+25°C		250	500		250		ns
	Full			1000			1000	ns
*t_{OFF} (EN), Enable Turn-Off	+25°C		250	500		250		ns
	Full			1000			1000	ns
t_S, Settling Time to 0.1%	+25°C		360			360		ns
to 0.01%	+25°C		600			600		ns
"Off Isolation" (Note 5)	+25°C	50	68		50	68		dB
C_S (OFF), Channel Input Capacitance	+25°C		5			5		pF
C_D (OFF), Channel Output Capacitance HI-508	+25°C		22			22		pF
HI-509	+25°C		11			11		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
C_{DS} (OFF), Input to Output Capacitance	+25°C		.08			.08		pF
POWER REQUIREMENTS								
*I_+, Positive Supply Current (Note 6)	Full		1.5	2.4		1.5	2.4	mA
*I_-, Negative Supply Current (Note 6))	Full		0.4	1		0.4	1	mA
P_D, Power Dissipation	Full			51			51	mW

*100% tested for Dash 8. Leakage currents not tested at -55°C.

TRUTH TABLES

HI-508

A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-509

A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	L	NONE
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

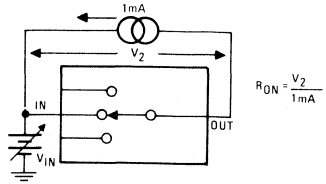
NOTES:
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. V_{OUT} = ±10V, I_{OUT} = -1mA.
3. Ten nanoamps is the practical lower limit for high speed measurement in the production test environment.
4. Digital input leakage is primarily due to the clamp diodes (see Schematic). Typical leakage is less than 1nA at 25°C.
5. V_{EN} = 0.8V, R_L = 1K, C_L = 15pF, V_S = $7V_{RMS}$, f = 100kHz. Worst case isolation occurs on channel 4 due to proximity of the output pins.
6. V_{EN}, V_A = 0V or 2.4V.
7. Signal voltage at any analog input or output (S or D) will be clamped to the supply rail by internal diodes. Limit the resulting current as shown under absolute maximum ratings. If an overvoltage condition is anticipated (analog input exceeds either power supply voltage), the Harris HI-548/549 multiplexers are recommended.

Performance Characteristics and Test Circuits

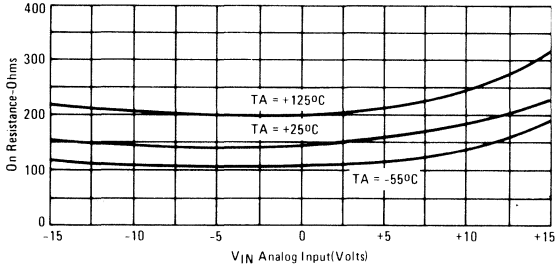
Unless Otherwise Specified; T_A = 25°C, V_{Supply} = ±15 V, V_{AH} = 2.4 V, V_{AL} = 0.8 V.

ON RESISTANCE vs. INPUT SIGNAL LEVEL, SUPPLY VOLTAGE

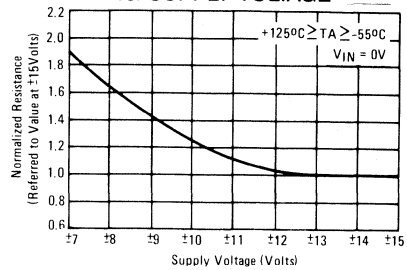
TEST CIRCUIT NO. 1



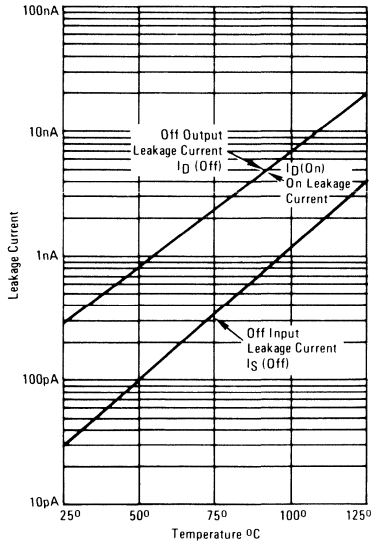
ON RESISTANCE vs. ANALOG INPUT VOLTAGE, TEMPERATURE



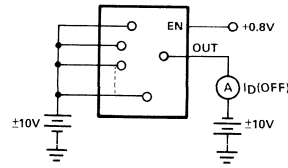
NORMALIZED ON RESISTANCE vs. SUPPLY VOLTAGE



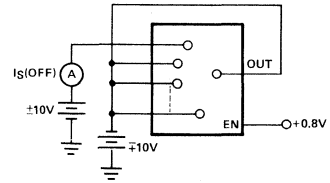
LEAKAGE CURRENT VS. TEMPERATURE



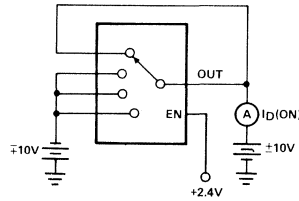
TEST CIRCUIT NO. 2*



TEST CIRCUIT NO. 4*

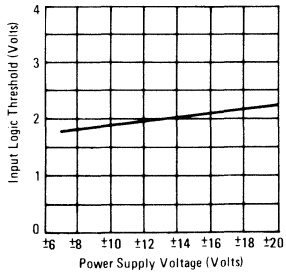


TEST CIRCUIT NO. 3*

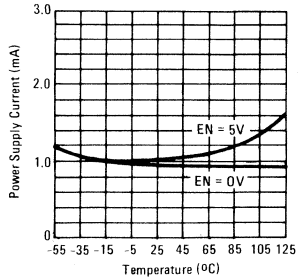


***Two measurements per channel: +10 V/−10 V and −10 V/+10 V. (Two measurements per device for $I_{D(OFF)}$: +10 V/−10 V and −10 V/+10 V.)**

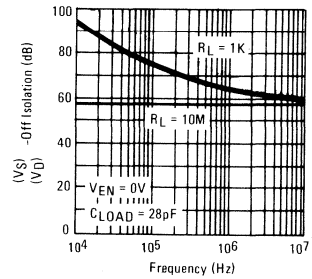
LOGIC THRESHOLD vs. POWER SUPPLY VOLTAGE



POWER SUPPLY CURRENT vs. TEMPERATURE

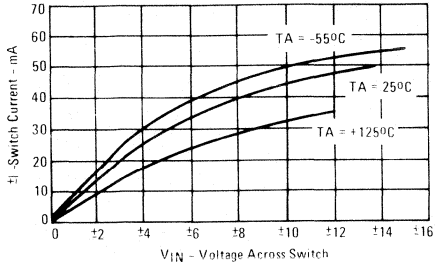


OFF ISOLATION vs. FREQUENCY



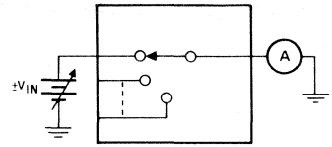
Performance Characteristics and Test Circuits (continued)

ON CHANNEL CURRENT vs. VOLTAGE

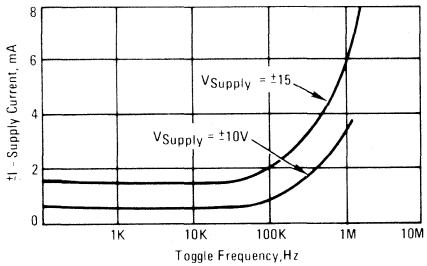


TEST CIRCUIT NO. 5

ON CHANNEL CURRENT vs. VOLTAGE

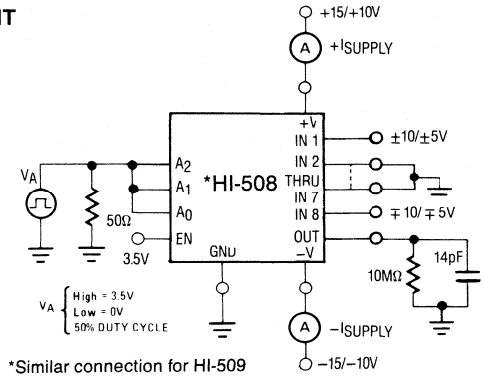


SUPPLY CURRENT vs. TOGGLE FREQUENCY



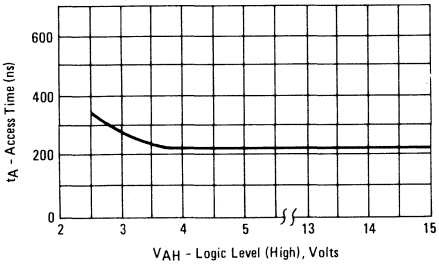
TEST CIRCUIT NO. 6

SUPPLY CURRENT vs. TOGGLE FREQUENCY



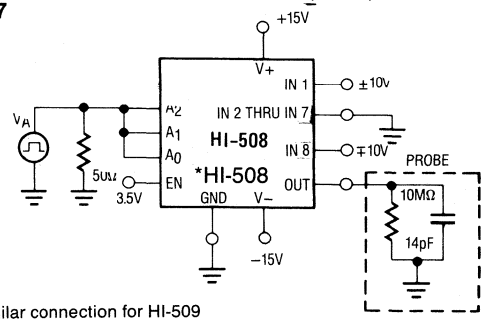
*Similar connection for HI-509

ACCESS TIME vs. LOGIC LEVEL (HIGH)



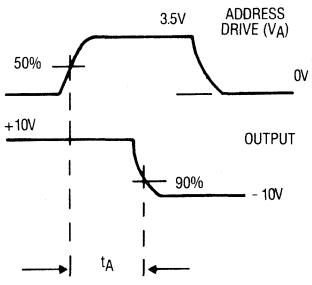
TEST CIRCUIT NO. 7

ACCESS TIME vs. LOGIC LEVEL (HIGH)

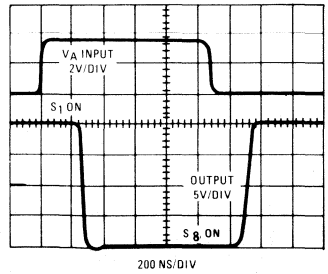


*Similar connection for HI-509

Switching Wav



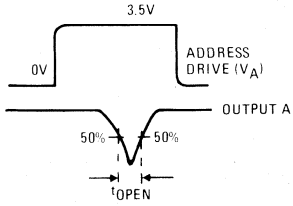
ACCESS TIME



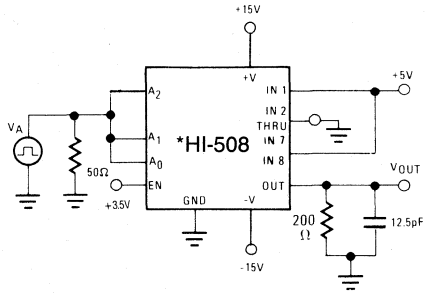
Switching Waveforms (continued)

TEST CIRCUIT NO. 8

ADDRESS DRIVE

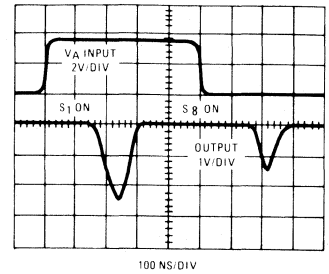


BREAK-BEFORE-MAKE DELAY (t_{OPEN})



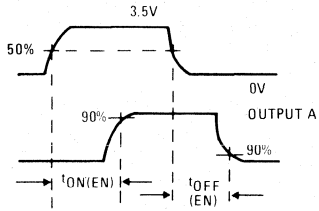
*Similar connection for HI-509

BREAK-BEFORE-MAKE DELAY(t_{OPEN})

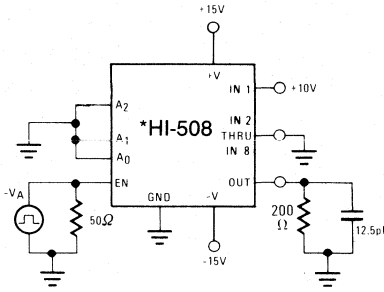


TEST CIRCUIT NO. 9

ENABLE DRIVE

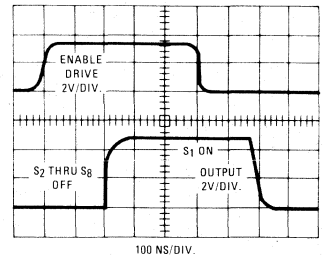


ENABLE DELAY ($t_{ON(EN)}$,$t_{OFF(EN)}$)



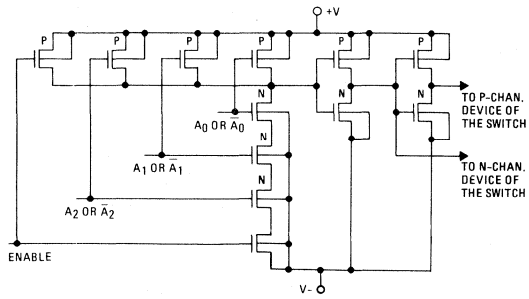
*Similar connection for HI-509

ENABLE DELAY ($t_{ON(EN)}$,$t_{OFF(EN)}$)

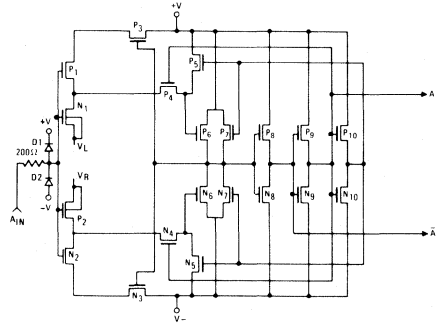


Schematic Diagrams

ADDRESS DECODER



ADDRESS INPUT BUFFER LEVER SHIFTER

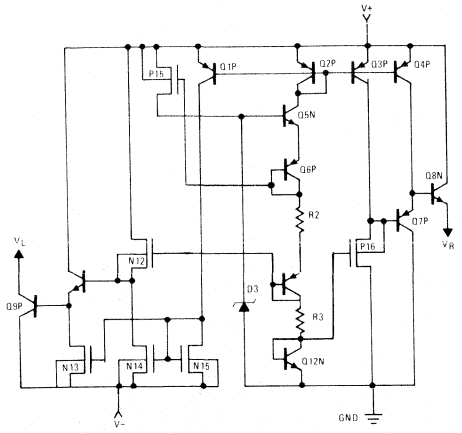


Delete A_2 or $\overline{A_2}$ Input for HI-509

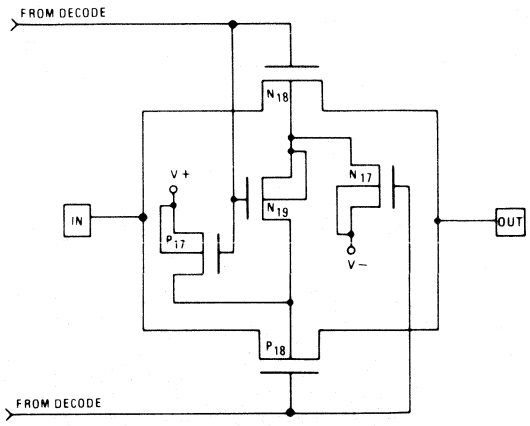
All N-Channel Bodies to V–
All P-Channel Bodies to V+ Unless Otherwise Indicated

Schematic Diagrams (continued)

TTL REFERENCE CIRCUIT

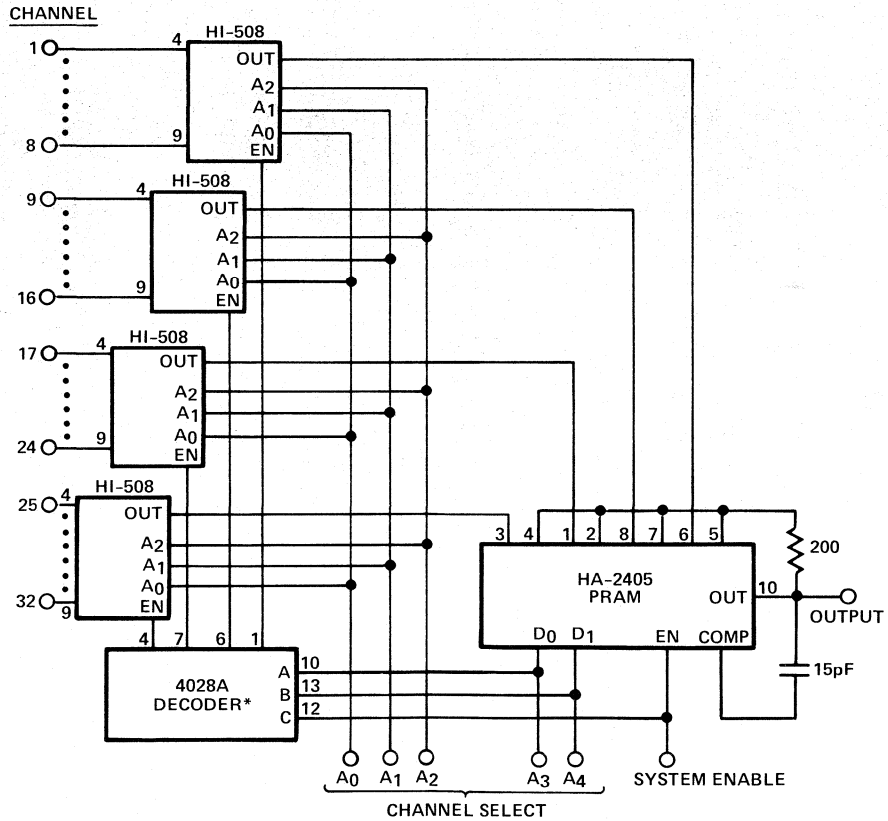


MULTIPLEX SWITCH



Applications

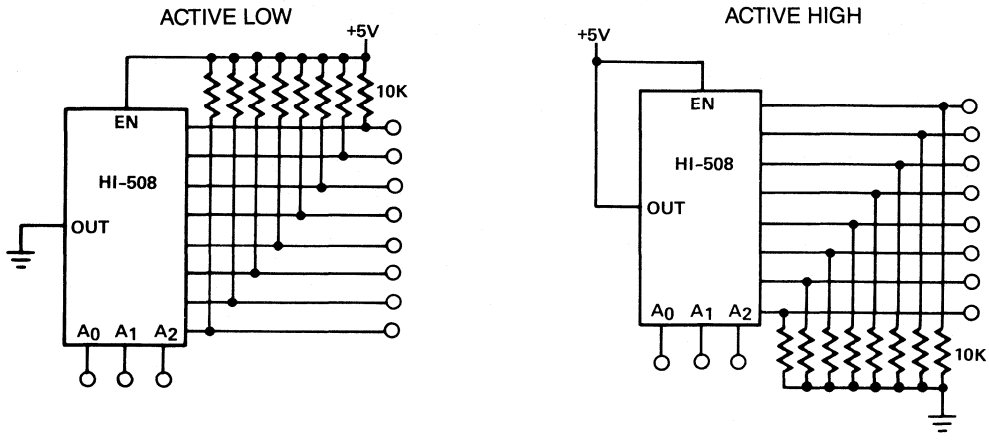
32 CHANNEL BUFFERED MULTIPLEXER



*Optional; Provides Greater Isolation for AC Signals.

Applications (continued)

ONE OF 8 DECODER



Die Characteristics

Transistor Count		243
Die Dimensions		81.9 x 90.2 mils
Substrate Potential*		$-V_{SUPPLY}$
Process		CMOS-DI
Thermal Constants ($^oC/W$)	θ_{ja}	θ_{jc}
Ceramic DIP	110	41
Plastic DIP	80	31
Ceramic LCC	82	24

*The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential.

HI-508A/509A

Single 8/Differential 4 Channel CMOS Analog Multiplexers with Active Overvoltage Protection

Features

- Analog Overvoltage Protection ... $70V_{p-p}$
- No Channel Interaction During Overvoltage
- ESD Resistant ..... > 4,000V
- 44V Maximum Power Supply
- Fail Safe with Power Loss (No Latch-Up)
- Break-Before-Make Switching
- Analog Signal Range ..... ±15V
- Access Time (Typical) 500ns
- Standby Power (Typical) 7.5mW

Applications

- Data Acquisition
- Industrial Controls
- Telemetry

Description

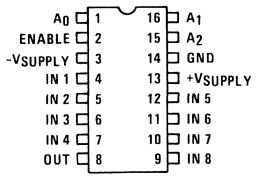
The HI-508A and HI-509A are analog multiplexers with Active Overvoltage Protection. Analog input levels may greatly exceed either power supply without damaging the device or disturbing the signal path of other channels. Active protection circuitry assures that signal fidelity is maintained even under fault conditions that would destroy other multiplexers. Analog inputs can withstand constant 70 volt peak-to-peak levels and typically survive static discharges beyond 4,000 volts. Digital inputs will also sustain continuous faults up to 4 volts greater than either supply. In addition, signal sources are protected from short circuiting should multiplexer supply loss occur; each input presents 1kΩ of resistance under this condition. These features make the HI-508A and HI-509A ideal for use in systems where the analog inputs originate from external equipment or separately powered circuitry. Both devices are fabricated with 44 volt dielectrically isolated CMOS technology. The HI-508A is an 8 channel device and the HI-509 is a 4 channel differential version. If input overvoltage protection is not needed, the HI-508 and HI-509 multiplexers are recommended. For further information see Application Notes 520 and 521.

Each device is available in a 16 pin Plastic or Ceramic DIP and a 20 pad Ceramic LCC package.

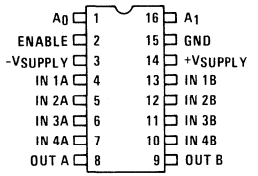
The HI-508A/509A are offered in both commercial and military grades. Additional Hi-Rel screening including 160 hour burn-in is specified by the "-8" suffix. For MIL-STD-883 compliant parts, request the HI-548/883 or HI-549/883 data sheets.

Pinouts

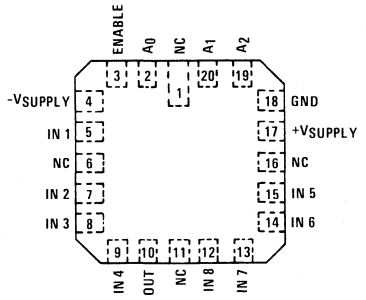
HI1-508A (CERAMIC DIP)
HI3-508A (PLASTIC DIP)
TOP VIEW



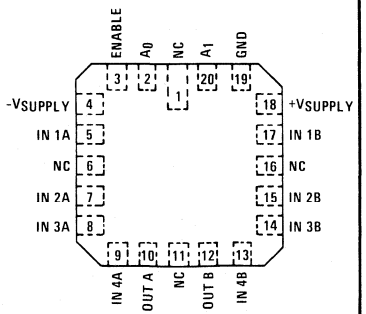
HI1-509A (CERAMIC DIP)
HI3-509A (PLASTIC DIP)
TOP VIEW



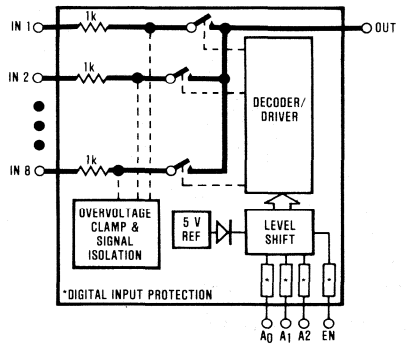
HI4-508A (CERAMIC LCC)
TOP VIEW



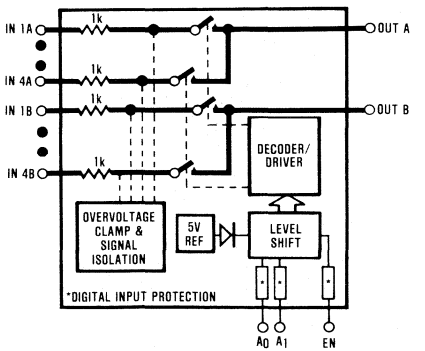
HI4-509A (CERAMIC LCC)
TOP VIEW



Functional Diagrams



HI-508A



HI-509A

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

$V_{SUPPLY(+)}$ to $V_{SUPPLY(-)}$ 44V
$V_{SUPPLY(+)}$ to GND 22V
$V_{SUPPLY(-)}$ to GND 25V
Digital Input Overvoltage
$+V_{EN}$, $+V_A$ ..... $+V_{SUPPLY}$ +4V
$-V_{EN}$, $-V_A$ ..... $-V_{SUPPLY}$ -4V
or 20mA, whichever occurs first
Analog Signal Overvoltage (Note 7)
$+V_S$ ..... $+V_{SUPPLY}$ +20V
$-V_S$ ..... $-V_{SUPPLY}$ -20V
Continuous Current, S or D: 20mA
Peak Current, S or D
(Pulsed at 1ms, 10% duty cycle max): 40mA
Junction Temperature ..... +175°C
Operating Temperature Ranges:
HI-508A/509A-2, -8 ..... -55°C to +125°C
HI-508A/509A-4 ..... -25°C to +85°C
HI-508A/509A-5 ..... 0°C to +75°C
Storage Temperature Range ..... -65°C to +150°C

Electrical Specifications Unless Otherwise Specified:

Supplies = +15V, -15V; V_{AH} (Logic Level High) = +4.0V;
V_{AL} (Logic Level Low) = +0.8V. For Test Conditions, consult Performance Characteristics Section.

PARAMETER	TEMP.	HI-508A/HI-509A -2, -8 MIN.	TYP.	MAX.	HI-508A/509A -5 MIN.	TYP.	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS								
*V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
*R_{ON}, On Resistance (Note 2)	+25°C		1.2	1.5		1.5	1.8	kΩ
	Full		1.5	1.8		1.8	2.0	kΩ
*I_S (OFF), Off Input Leakage Current (Note 3)	+25°C		0.03			0.03		nA
	Full			50			50	nA
*I_D (OFF), Off Output Leakage Current (Note 3)	+25°C		0.1			0.1		nA
HI-508A	Full			200			200	nA
HI-509A	Full			100			100	nA
*$I_{D(OFF)}$ with Input Overvoltage Applied (Note 4)	+25°C		4.0			4.0		nA
	Full			2.0				μA
*I_D (ON), On Channel Leakage Current (Note 3)	+25°C		0.1			0.1		nA
HI-508A	Full			200			200	nA
HI-509A	Full			100			100	nA
I_{DIFF}, Differential Off Output Leakage Current (HI-509A Only)	Full			50			50	nA
DIGITAL INPUT CHARACTERISTICS								
*V_{AL}, Input Low Threshold (Note 8)	Full			0.8			0.8	V
*V_{AH}, Input High Threshold	Full	4.0			4.0			V
*I_A, Input Leakage Current (High or Low) (Note 5)	Full			1.0			1.0	μA
SWITCHING CHARACTERISTICS								
*t_A, Access Time	+25°C		0.5			0.5		μs
	Full			1.0			1.0	μs
*t_{OPEN}, Break-Before-Make Delay	+25°C	25	80		25	80		ns
*$t_{ON (EN)}$, Enable Delay (ON)	+25°C		300	500		300		ns
	Full			1000			1000	ns
*$t_{OFF (EN)}$, Enable Delay (OFF)	+25°C		300	500		300		ns
	Full			1000			1000	ns
Settling Time (0.1%)	+25°C		1.2			1.2		μs
(0.01%)	+25°C		3.5			3.5		μs
"OFF Isolation" (Note 6)	+25°C	50	68		50	68		dB
C_S (OFF), Channel Input Capacitance	+25°C		5			5		pF
C_D (OFF), Channel Output Capacitance HI-508A	+25°C		25			25		pF
HI-509A	+25°C		12			12		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
$C_{DS (OFF)}$, Input to Output Capacitance	+25°C		0.1			0.1		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full		7.5			7.5		mW
*I+, Current (Note 7)	Full		0.5	2.0		0.5	2.0	mA
*I−, Current (Note 7)	Full		0.02	1.0		0.02	1.0	mA

*100% tested for Dash 8. Leakage currents not tested at -55°C.

TRUTH TABLES

HI-508A

A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-509A

A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	L	NONE
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

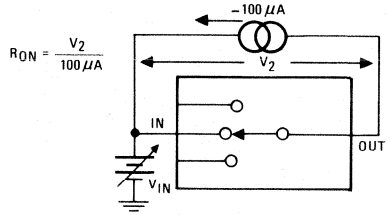
NOTES:
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. V_{OUT} = ±10V, I_{OUT} = -100μA.
3. Ten nanoamps is the practical lower limit for high speed measurement in the production test environment.
4. Analog Overvoltage = ±33V.
5. Digital input leakage is primarily due to the clamp diodes (see Schematic). Typical leakage is less than 1nA at 25°C.
6. V_{EN} = 0.8V, R_L = 1K, C_L = 15pF, V_S = $7V_{RMS}$, f = 100kHz. Worst Case isolation occurs on channel 4 due to proximity of the output pins.
7. V_{EN}, V_A = 0V or 4.0V.
8. To drive from DTL/TTL Circuits, 1kΩ pull-up resistors to +5.0V supply are recommended.

Performance Characteristics and Test Circuits

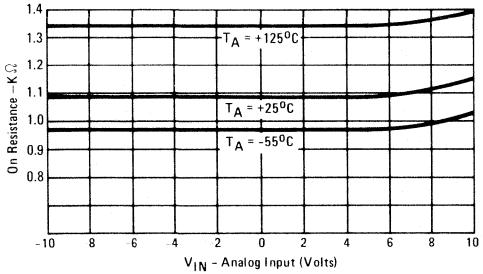
Unless Otherwise Specified T_A = 25°C, V_{Supply} = ±15 V, V_{AH} = +4 V, V_{AL} = 0.8 V

ON RESISTANCE vs. INPUT SIGNAL LEVEL, SUPPLY VOLTAGE

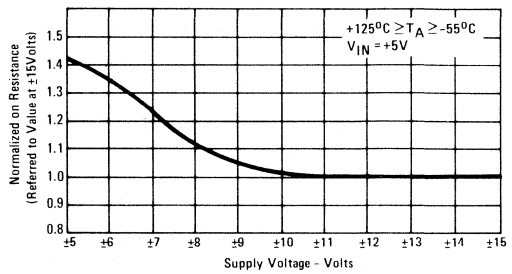
TEST CIRCUIT NO. 1



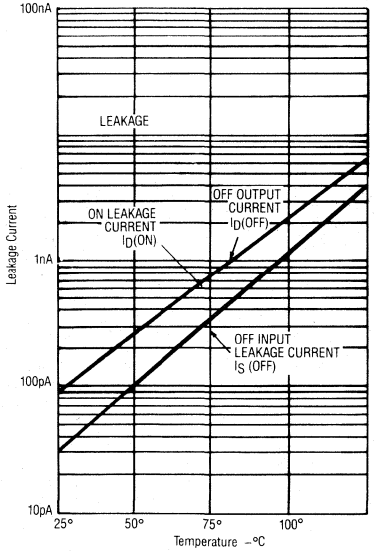
ON RESISTANCE vs. ANALOG INPUT VOLTAGE



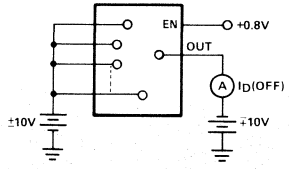
NORMALIZED ON RESISTANCE vs. SUPPLY VOLTAGE



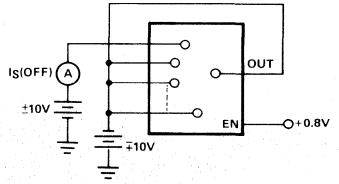
LEAKAGE CURRENT VS. TEMPERATURE



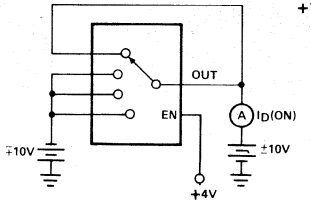
TEST CIRCUIT NO. 2*



TEST CIRCUIT NO. 3*

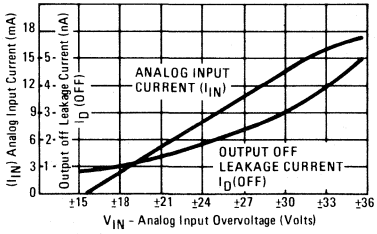


TEST CIRCUIT NO. 4*



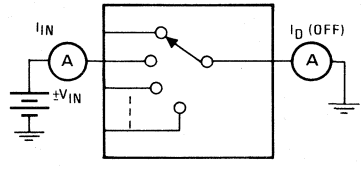
***Two measurements per channel: +10 V/−10 V and −10 V/+10 V. (Two measurements per device for $I_{D(OFF)}$: +10 V/−10 V and −10 V/+10 V.)**

ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



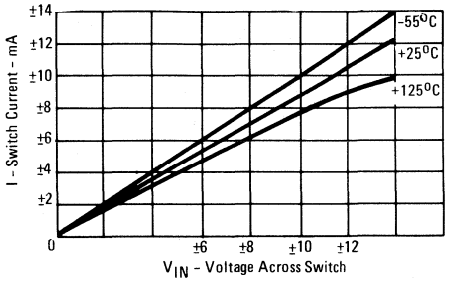
TEST CIRCUIT NO. 5

ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



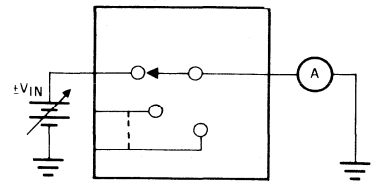
Performance Characteristics and Test Circuits (continued)

ON CHANNEL CURRENT vs. VOLTAGE

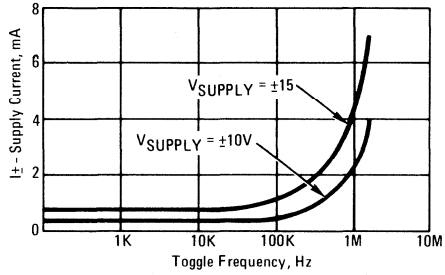


TEST CIRCUIT NO. 6

ON CHANNEL CURRENT vs. VOLTAGE

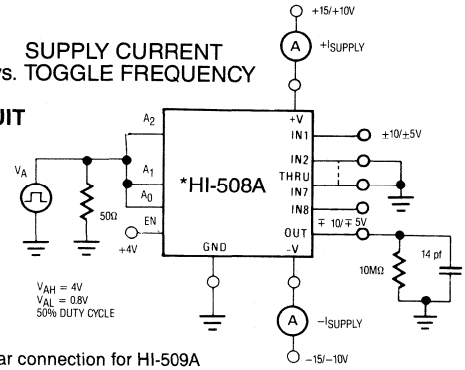


SUPPLY CURRENT vs. TOGGLE FREQUENCY



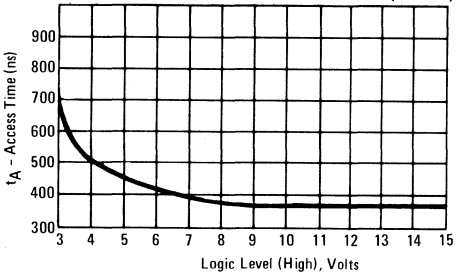
TEST CIRCUIT NO. 7

SUPPLY CURRENT vs. TOGGLE FREQUENCY



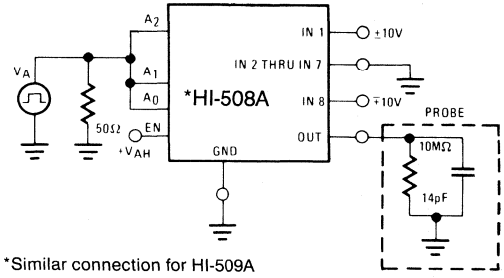
*Similar connection for HI-509A

ACCESS TIME VS. LOGIC LEVEL (HIGH)



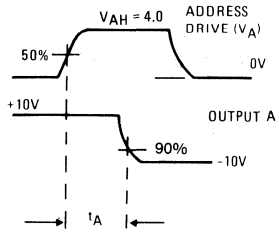
TEST CIRCUIT NO. 8

ACCESS TIME vs. LOGIC LEVEL (HIGH)

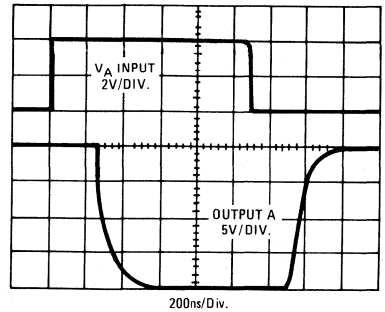


*Similar connection for HI-509A

Switching Waveforms



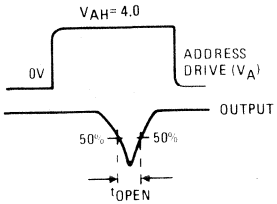
ACCESS TIME

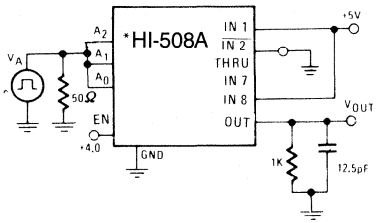


Switching Waveforms (continued)

TEST CIRCUIT NO. 9

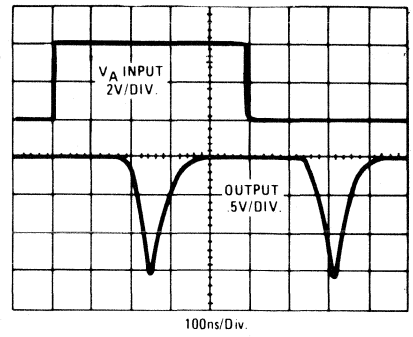
BREAK-BEFORE-MAKE DELAY(tOPEN)





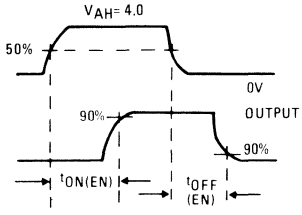
*Similar connection for HI-509A

BREAK-BEFORE-MAKE DELAY (tOPEN)

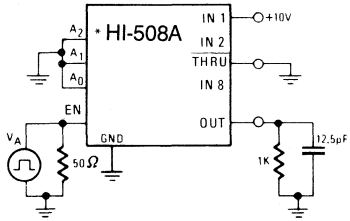


TEST CIRCUIT NO. 10

ENABLE DRIVE

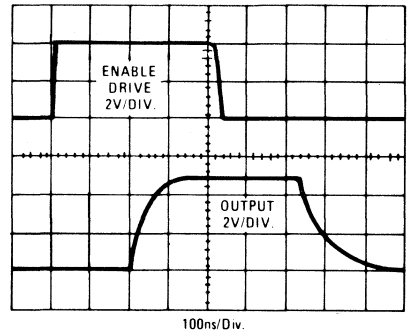


ENABLE DELAY (tON(EN),tOFF(EN))

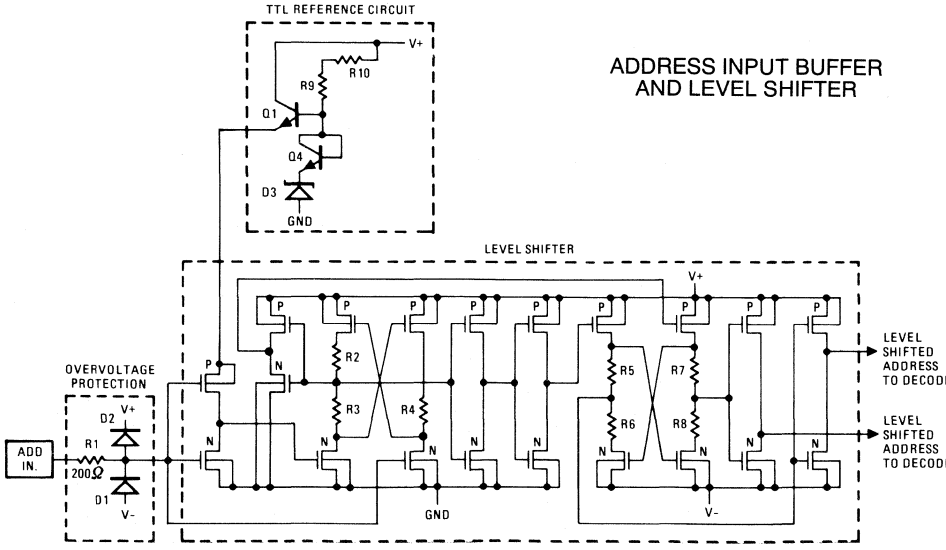


*Similar connection for HI-509A

ENABLE DELAY (tON(EN),tOFF(EN))

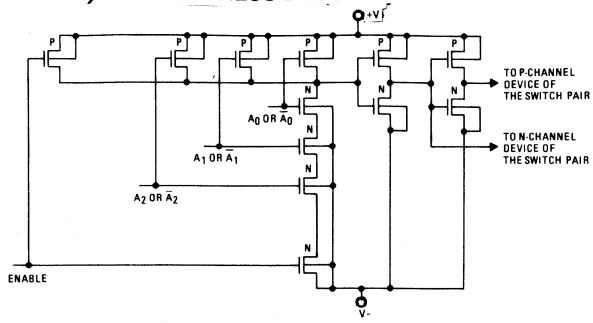


Schematic Diagrams

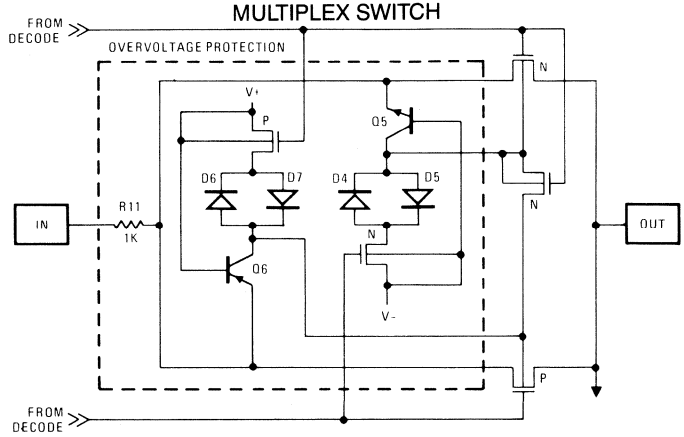


Schematic Diagrams (continued)

ADDRESS DECODER



MULTIPLEX SWITCH



Die Characteristics

Transistor Count	253
Die Dimensions	108 x 83 mils
Substrate Potential*	$-V_{SUPPLY}$
Process	CMOS-DI

Thermal Constants ($^oC/W$)	θ_{ja}	θ_{jc}
Ceramic DIP	104	35
Plastic DIP	75	23
Ceramic LCC	76	19

*The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential.

HI-516

16 Channel/Differential 8 Channel CMOS High Speed Analog Multiplexer

Features

- **Access Time (Typical) 130ns**
- **Settling Time (0.1%) 250ns**
- **Low Leakage (Typical)**
  - **I_S(OFF) 10pA**
  - **I_D(OFF) 30pA**
- Low Capacitance (Max)
  - C_S(OFF) 10pF
  - C_D(OFF) 25pF
- **High Off Isolation at 500kHz (Min) 55dB**
- **Low Charge Injection Error 20mV**
- **Single Ended to Differential Selectable (SDS)**
- **Logic Level Selectable (LLS)**

Applications

- **Data Acquisition Systems**
- **Precision Instrumentation**
- **Industrial Control**

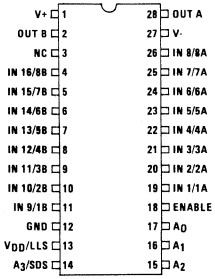
Description

The HI-516 is a monolithic dielectrically isolated, high speed, high performance CMOS analog multiplexer. It offers unique built-in channel selection decoding plus an inhibit input for disabling all channels. The dual function of address input A3 enables the HI-516 to be user programmed either as a single ended 16-channel multiplexer by connecting 'out A' to 'out B' and using A3 as a digital address input, or as an 8-channel differential multiplexer by connecting A3 to the V- supply. The substrate leakages and parasitic capacitances are reduced substantially by using the Harris Dielectric Isolation process to achieve optimum performance in both high and low level signal applications. The low output leakage current (I_DOFF < 100pA at 25°C) and fast settling (t_{SETTLE} = 800ns to 0.01%) characteristics of the device make it an ideal choice for high speed data acquisition systems, precision instrumentation, and industrial process control.

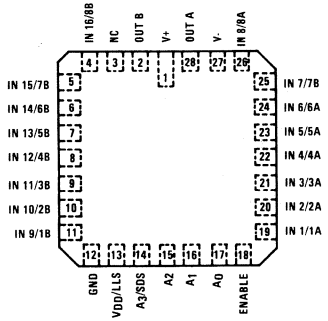
The HI-516 is available in 28 pin Ceramic or Plastic DIPs or in 28 pin Ceramic LCC or PLCC packages. For Mil-Std-883 compliant parts, request the HI-516/883 data sheet.

Pinouts

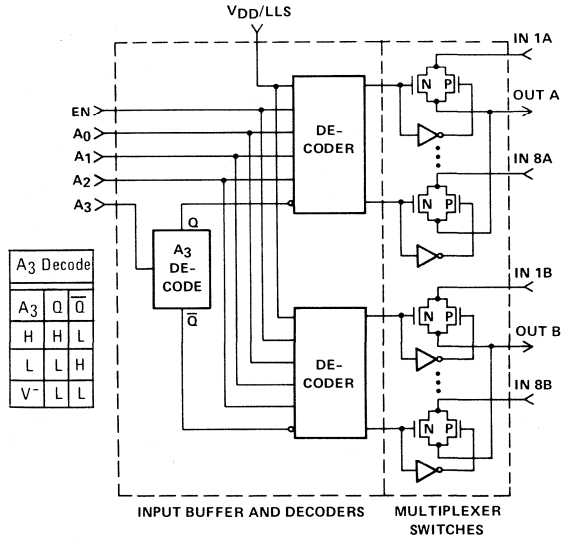
CERAMIC/PLASTIC DIP
TOP VIEW



LCC/PLCC
TOP VIEW



Functional Diagram



A3 Decode		
A3	Q	$\overline{Q}$
H	H	L
L	L	H
V⁻	L	L

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

Voltage Between Supply Pins 33V
Analog Input Voltage
- $+V_{IN}$ ..... $+V_{SUPPLY}$ +2V
- $-V_{IN}$ ..... $-V_{SUPPLY}$ -2V

Digital Input Voltage
- TTL Levels Selected (V_{DD}/LLS Pin = GND or Open)
- $+V_A$ ..... +6V
- $-V_A$ ..... -6V
- $+A_3$/SDS ..... $+V_{SUPPLY}$ +2V
- $-A_3$/SDS ..... $-V_{SUPPLY}$ -2V

CMOS Levels Selected (V_{DD}/LLS Pin = V_{DD})
- $+V_A$ ..... $+V_{SUPPLY}$ +2V
- $-V_A$ ..... -2V

Junction Temperature (Max) ..... 175°C
Operating Temperature Ranges:
- HI-516-2, -8 ..... -55°C to +125°C
- HI-516-5 ..... 0°C to +75°C

Storage Temperature Range ..... -65°C to +150°C

Electrical Specifications

(Unless otherwise specified) Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V, V_{AL} (Logic Level Low) = +0.8V; V_{DD}/LLS = GND. (Note 2)

PARAMETER	TEMP	HI-516-2, -8 MIN	HI-516-2, -8 TYP	HI-516-2, -8 MAX	HI-516-5 MIN	HI-516-5 TYP	HI-516-5 MAX	UNITS
ANALOG CHANNEL CHARACTERISTICS								
V_{IN}, Analog Signal Range (Note 3)	Full	-14		+14	-15		+15	V
R_{ON}, On Resistance (Note 4)	+25°C		620	750		620	750	Ω
	Full			1,000			1,000	Ω
I_S (OFF), Off Input Leakage Current	+25°C		0.01			0.01		nA
	Full			50			50	nA
I_D(OFF), Off Output Leakage Current	+25°C		0.03			0.03		nA
	Full			100			100	nA
I_D(ON), On Channel Leakage Current	+25°C		0.04			0.04		nA
	Full			100			100	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL} Input Low Threshold (TTL)	Full			0.8			0.8	V
V_{AH} Input High Threshold (TTL)	Full	2.4			2.4			V
V_{AL} Input Low Threshold (CMOS)	Full			$0.3V_{DD}$			$0.3V_{DD}$	V
V_{AH} Input High Threshold (CMOS)	Full	$0.7V_{DD}$			$0.7V_{DD}$			V
I_{AH} Input Leakage Current (High)	Full			1			1	μA
I_{AL} Current (Low)	Full			25			25	μA
SWITCHING CHARACTERISTICS								
t_A, Access Time	+25°C		130	175		130	175	ns
	Full			225			225	ns
t_{OPEN}, Break before make delay	+25°C	10	20		10	20		ns
t_{ON}(EN), Enable Delay (ON)	+25°C		120	175		120	175	ns
t_{OFF}(EN), Enable Delay (OFF)	+25°C		140	175		140	175	ns
Settling Time (0.1%)	+25°C		250			250		ns
(0.01%)	+25°C		800			800		ns
Charge Injection Error (Note 5)	+25°C			20			20	mV
Off Isolation (Note 6)	+25°C	55			55			dB
C_S(OFF), Channel Input Capacitance	+25°C			10			10	pF
C_D(OFF), Channel Output Capacitance	+25°C			25			25	pF
C_A, Digital Input Capacitance	+25°C			10			10	pF
C_{DS}(OFF), Input to Output Capacitance	+25°C		0.02			0.02		pF
POWER REQUIREMENTS								
PD, Power Dissipation	Full			750			900	mW
I^+, Current (Note 7)	Full			25			30	mA
I^-, Current (Note 7)	Full			25			30	mA

NOTES:
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. V_{DD}/LLS pin = open or grounded for TTL compatibility. V_{DD}/LLS pin = V_{DD} for CMOS Compatibility
3. At temperatures above 90°C, care must be taken to fassure V_{IN} remains at least 1.0V below the V_{SUPPLY} for proper operation.
4. V_{IN} = ±10V, I_{OUT} = -100μA
5. V_{IN} = 0V, C_L = 100pF, Enable input pulse = 3V, f = 500kHz.
6. V_{EN} = 0.8V, V_S = $3V_{RMS}$, f = 500kHz, C_L = 40pF, R_L = 1K, Pin 3 grounded.
7. V_{EN} = +2.4V

TRUTH TABLES

HI-516 USED AS A 16-CHANNEL MULTIPLEXER OR 8 CHANNEL DIFFERENTIAL MULTIPLEXER *

USE A_3 AS DIGITAL ADDRESS INPUT					ON CHANNEL TO	
ENABLE	A_3	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	X	NONE	NONE
H	L	L	L	L	1A	NONE
H	L	L	L	H	2A	NONE
H	L	L	H	L	3A	NONE
H	L	L	H	H	4A	NONE
H	L	H	L	L	5A	NONE
H	L	H	L	H	6A	NONE
H	L	H	H	L	7A	NONE
H	L	H	H	H	8A	NONE
H	H	L	L	L	NONE	1B
H	H	L	L	H	NONE	2B
H	H	L	H	L	NONE	3B
H	H	L	H	H	NONE	4B
H	H	H	L	L	NONE	5B
H	H	H	L	H	NONE	6B
H	H	H	H	L	NONE	7B
H	H	H	H	H	NONE	8B

* For 16-Channel single-ended function, tie 'out A' to 'out B', for dual 8-channel function use the A_3 address pin to select between MUX A and MUX B, where MUX A is selected with A_3 low.

HI-516 USED AS A DIFFERENTIAL 8-CHANNEL MULTIPLEXER

A_3 CONNECT TO V^- SUPPLY				ON CHANNEL TO	
ENABLE	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	NONE	NONE
H	L	L	L	1A	1B
H	L	L	H	2A	2B
H	L	H	L	3A	3B
H	L	H	H	4A	4B
H	H	L	L	5A	5B
H	H	L	H	6A	6B
H	H	H	L	7A	7B
H	H	H	H	8A	8B

Die Characteristics

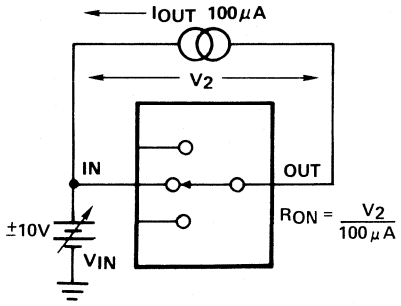
Transistor Count 647
Die Dimension ..... 89 x 146 mils
Substrate Potential* ..... $-V_{SUPPLY}$
Process: ..... CMOS-DI

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
Ceramic DIP	50	18
Ceramic LCC	81	40

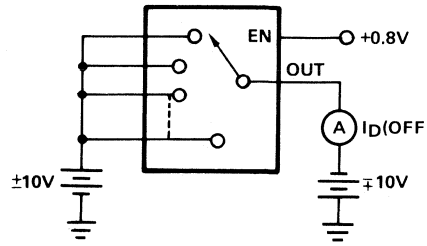
*The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential.

Performance Characteristics and Test Circuits

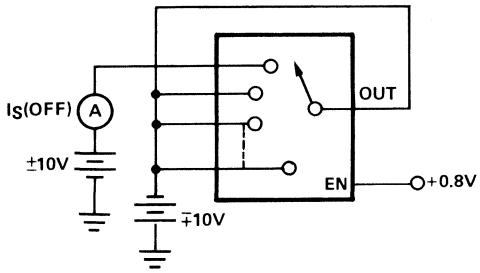
TEST CIRCUIT NO. 1
ON RESISTANCE vs. INPUT SIGNAL LEVEL



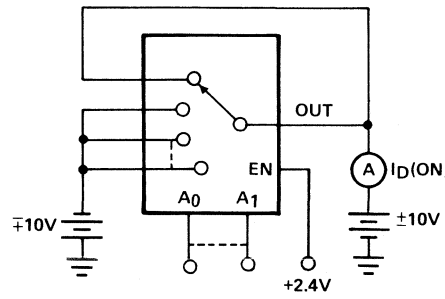
TEST CIRCUIT NO. 2*



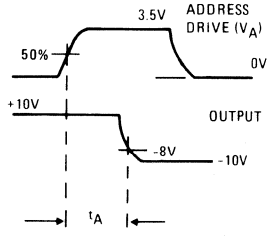
TEST CIRCUIT NO. 3*

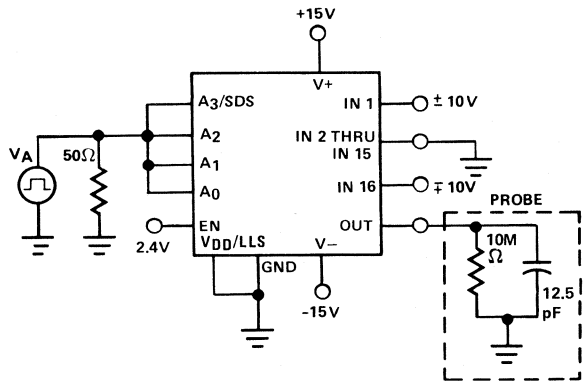


TEST CIRCUIT NO. 4*



TEST CIRCUIT NO. 5
ACCESS TIME



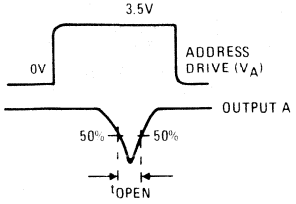


*Two measurements per channel: +10V/-10V and -10V/+10V.
(Two measurements per device for $I_{D(OFF)}$: +10V/-10V and -10V/+10V)

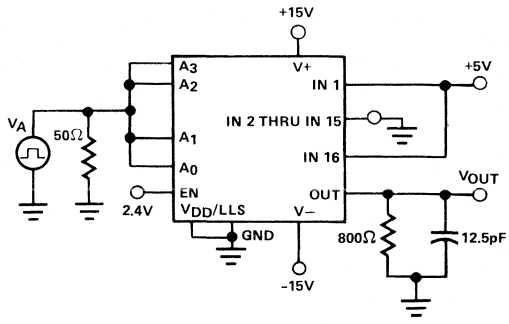
Performance Characteristics and Test Circuits (Continued)

TEST CIRCUIT NO. 6

ENABLE DRIVE

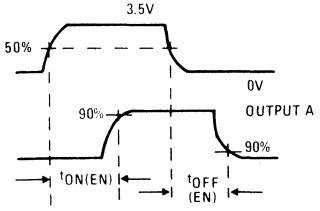


BREAK-BEFORE MAKE DELAY (t_{OPEN})

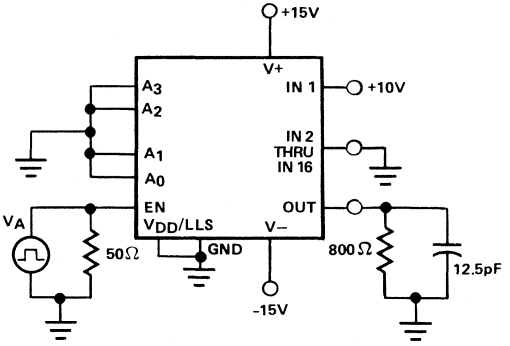


TEST CIRCUIT NO. 7

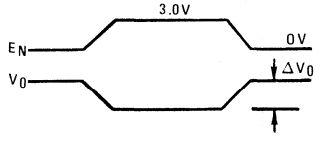
ENABLE DRIVE



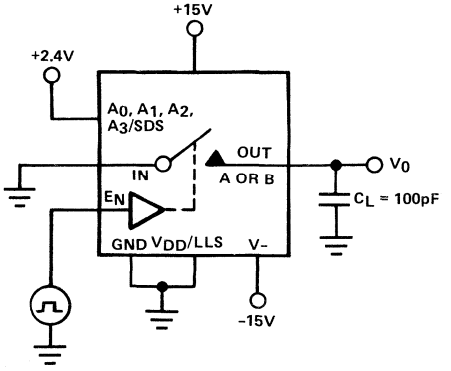
ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)



TEST CIRCUIT NO. 8
CHARGE INJECTION TEST CIRCUIT



ΔV_0 IS THE MEASURED VOLTAGE ERROR DUE TO CHARGE INJECTION. THE ERROR VOLTAGE IN COULOMBS IS $Q = C_L \times \Delta V_0$.



HARRIS

HI-518

8 Channel/Differential
4 Channel CMOS High Speed Analog Multiplexer

Features

- Access Time (Typical) 130ns
- Settling Time (0.1%) 250ns
- Low Leakage (Typical)
  - I_S(OFF) 5pA
  - I_D(OFF) 15pA
- Low Capacitance (Max)
  - C_S(OFF) 5pF
  - C_D(OFF) 10pF
- High Off Isolation at 500kHz (Min) 45dB
- Low Charge Injection Error 25mV
- Single Ended to Differential Selectable (SDS)
- Logic Level Selectable (LLS)

Applications

- Data Acquisition Systems
- Precision Instrumentation
- Industrial Control

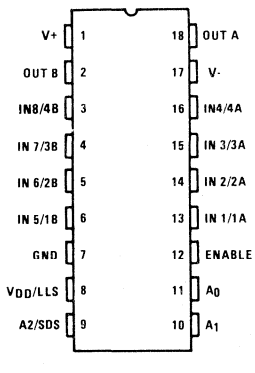
Description

The HI-518 is a monolithic dielectrically isolated, high speed, high performance CMOS analog multiplexer. It offers unique built-in channel selection decoding plus an inhibit input for disabling all channels. The dual function of address input A_2 enables the HI-518 to be user programmed either as a single ended 8-channel multiplexer by connection 'out A' to 'out B' and using A_2 as a digital address input, or as a 4-channel differential multiplexer by connecting A_2 to V- supply. The substrate leakages and parasitic capacitances are reduced substantially by using the Harris dielectric isolation process to achieve optimum performance in both high and low level signal applications. The low output leakage current (I_DOFF < 100pA @ +25°C) and fast settling (t_{SETTLE} = 800ns to 0.01%) characteristics of the device make it an ideal choice for high speed data acquisition systems, precision instrumentation, and industrial process control.

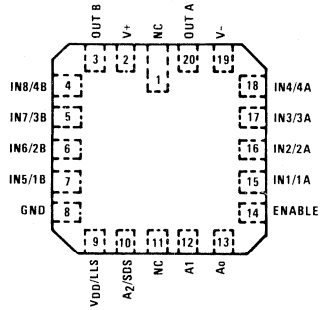
The HI-518 is available in an 18 lead Ceramic or Plastic dual-in-line package and a 20 pin LCC or PLCC package. It is offered in two operating ranges: -55°C to +125°C and 0°C to +75°C. For MIL-STD-883 compliant parts, request the HI-518/883 data sheet.

Pinouts

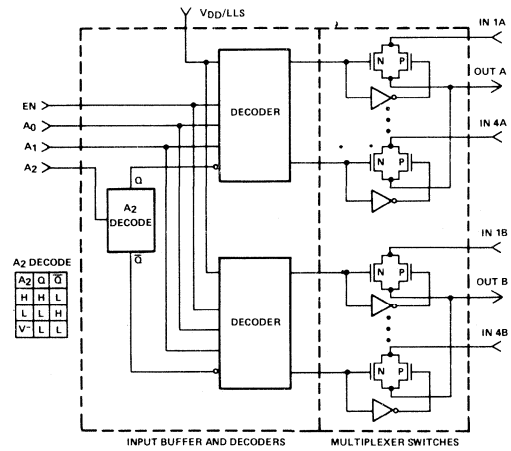
CERAMIC/PLASTIC DIP
TOP VIEW



LCC/PLCC
TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

Analog Input Voltage
- $+V_{IN}$ ..... $+V_{SUPPLY}$ +2V
- $-V_{IN}$ ..... $-V_{SUPPLY}$ -2V

Digital Input Voltage

TTL Levels Selected (V_{DD}/LLS Pin = GND or Open)
- $+V_A$ ..... +6V
- $-V_A$ ..... -6V
- A2/SDS ..... $+V_{SUPPLY}$ +2V
- A2/SDS ..... $-V_{SUPPLY}$ -2V

Voltage Between Supply Pins 33V

CMOS Levels Selected (V_{DD}/LLS Pin = V_{DD})
- $+V_A$ ..... $+V_{SUPPLY}$ +2V
- $-V_A$ ..... -2V

Operating Temperature Ranges
- HI-518-2/-8 ..... -55°C to +125°C
- HI-518-5 ..... 0°C to +75°C

Storage Temperature Range ..... -65°C to +150°C

Junction Temperature (Max) ..... 175°C

Electrical Specifications

(Unless Otherwise Specified) Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V, V_{AL} (Logic Level Low) = +0.8V; V_{DD}/LLS = GND (Note 2)

PARAMETER	TEMP	HI-518-2, -8 MIN	HI-518-2, -8 TYP	HI-518-2, -8 MAX	HI-518-5 MIN	HI-518-5 TYP	HI-518-5 MAX	UNITS
ANALOG CHANNEL CHARACTERISTICS								
V_{IN} Analog Signal Range (Note 3)	Full	-14		+14	-15		+15	V
R_{ON} On Resistance (Note 4)	+25°C		480	750		480	750	Ω
	Full			1000			1000	Ω
I_S (OFF) Off Input	+25°C		0.01			0.01		nA
Leakage Current	Full			50			50	nA
I_D (OFF) Off Output	+25°C		0.015			0.015		nA
Leakage Current	Full			50			50	nA
I_D (ON) On Channel	+25°C		0.015			0.015		nA
Leakage Current	Full			50			50	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL} Input Low Threshold (TTL)	Full			0.8			0.8	V
V_{AH} Input High Threshold (TTL)	Full	2.4			2.4			V
V_{AL} Input Low Threshold (CMOS)	Full			$0.3V_{DD}$			$0.3V_{DD}$	V
V_{AH} Input High Threshold (CMOS)	Full	$0.7V_{DD}$			$0.7V_{DD}$			V
I_{AH} Input Leakage Current (High)	Full			1			1	μA
I_{AL} Input Leakage Current (Low)	Full			20			20	μA
SWITCHING CHARACTERISTICS								
t_A, Access Time	+25°C		130	175		130	175	ns
	Full			225			225	ns
t_{OPEN}, Break before make Delay	+25°C	10	20		10	20		ns
t_{ON} (EN), Enable Delay (ON)	+25°C		120	175		120	175	ns
t_{OFF} (EN), Enable Delay (OFF)	+25°C		140	175		140	175	ns
Settling Time (0.1%)	+25°C		250			250		ns
(0.01%)	+25°C		800			800		ns
Charge Injection Error (Note 5)	+25°C			25			25	mV
Off Isolation (Note 6)	+25°C	45			45			dB
C_S (OFF) Channel Input Capacitance	+25°C			5			5	pF
C_D (OFF) Channel Output Capacitance	+25°C			10			10	pF
C_A, Digital Input Capacitance	+25°C			5			5	pF
CDS (OFF) Input to Output Capacitance	+25°C		0.02			0.02		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full			450			540	mW
I+, Current (Note 7)	Full			15			18	mA
I⁻, Current (Note 7)	Full			15			18	mA

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. V_{DD}/LLS Pin = Open or Grounded for TTL compatibility. V_{DD}/LLS pin = V_{DD} for CMOS compatibility.
3. At temperatures above +90°C, care must be taken to assure V_{IN} remains at least 1.0V below the V_{SUPPLY}.
4. V_{IN} = ±10V, I_{OUT} = -100μA.
5. V_{IN} = 0V, C_L = 100pF, Enable Input Pulse = 3V, f = 500kHz.
6. C_L = 40pF, R_L = 1k. Due to the pin to pin capacitance between IN 8/4B and OUT B channel 8/4B exhibits 60dB of OFF Isolation under the above test conditions.
7. V_{EN} = 2.4V.

Truth Tables

HI-518 USED AS A 8 CHANNEL MULTIPLEXER OR 4 CHANNEL DIFFERENTIAL MULTIPLEXER

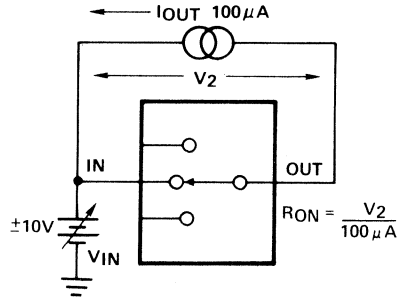
USE A_2 AS DIGITAL ADDRESS INPUT				ON CHANNEL TO	
ENABLE	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	NONE	NONE
H	L	L	L	1A	NONE
H	L	L	H	2A	NONE
H	L	H	L	3A	NONE
H	L	H	H	4A	NONE
H	H	L	L	NONE	1B
H	H	L	H	NONE	2B
H	H	H	L	NONE	3B
H	H	H	H	NONE	4B

HI-518 USED AS DIFFERENTIAL 4 CHANNEL MULTIPLEXER

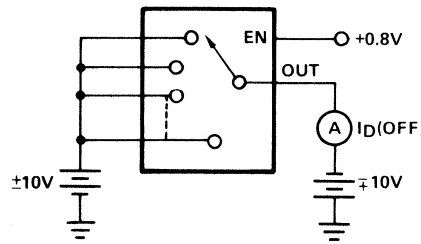
A_2 CONNECT TO V^- SUPPLY			ON CHANNEL TO	
ENABLE	A_1	A_0	OUT A	OUT B
L	X	X	NONE	NONE
H	L	L	1A	1B
H	L	H	2A	2B
H	H	L	3A	3B
H	H	H	4A	4B

Performance Characteristics and Test Circuits

TEST CIRCUIT NO. 1
ON RESISTANCE vs. INPUT SIGNAL LEVEL



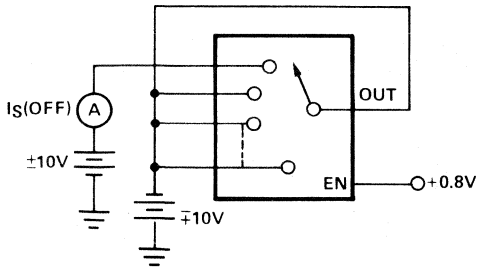
TEST CIRCUIT NO. 2*



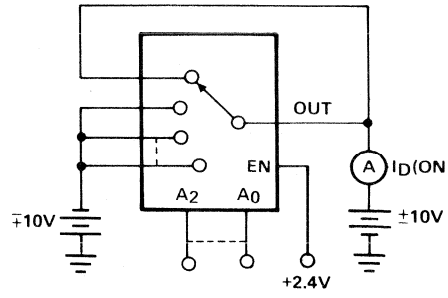
*Two measurements per channel: +10V/-10V and -10V/+10V. (Two measurements per device for I_D(OFF): +10V/-10V and -10V/+10V)

Performance Characteristics and Test Circuits (Continued)

TEST CIRCUIT NO. 3*



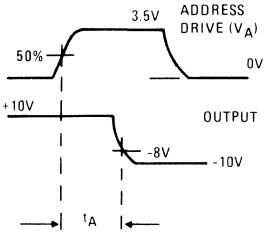
TEST CIRCUIT NO. 4*

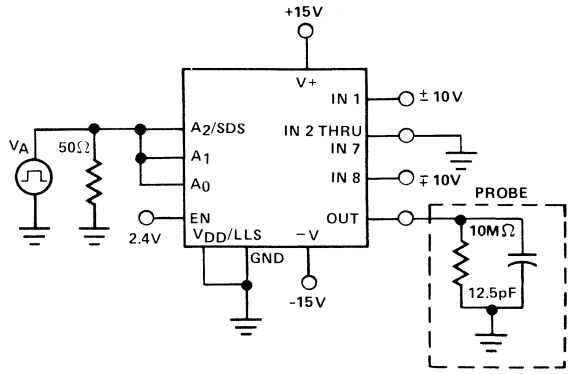


*Two measurements per channel: +10V/-10V and -10V/+10V. (Two measurements per device for I_D(OFF): +10V/-10V and -10V/+10V)

TEST CIRCUIT NO. 5

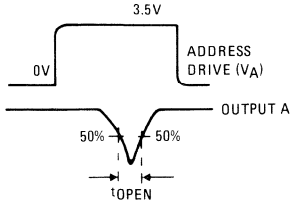
ACCESS TIME



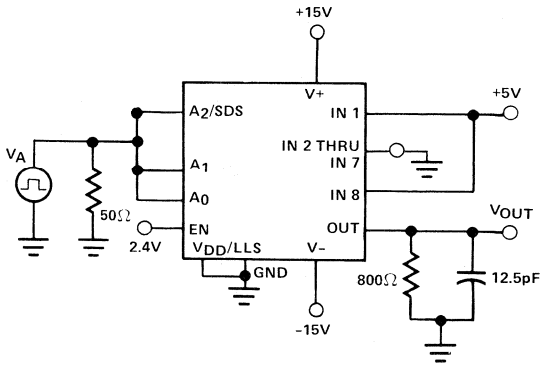


TEST CIRCUIT NO. 6

ENABLE DRIVE



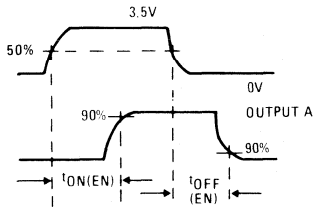
BREAK-BEFORE MAKE DELAY (t_{OPEN})



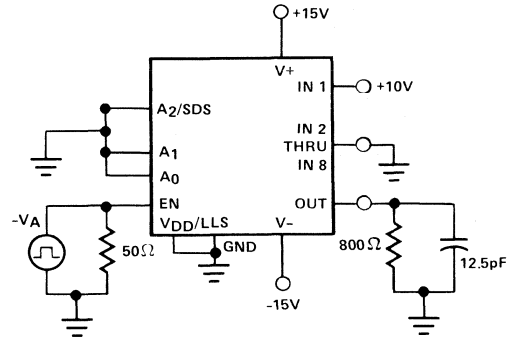
Performance Characteristics and Test Circuits (Continued)

TEST CIRCUIT NO. 7

ENABLE DRIVE

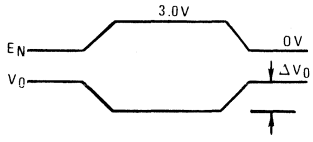


ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)

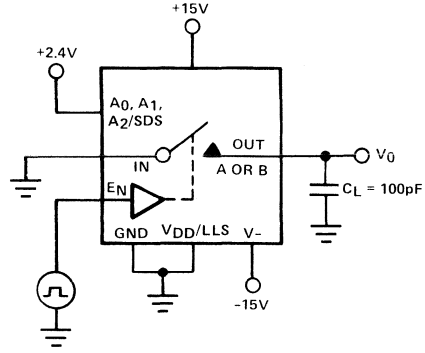


TEST CIRCUIT NO. 8

CHARGE INJECTION TEST CIRCUIT



ΔV_O IS THE MEASURED VOLTAGE ERROR DUE TO CHARGE INJECTION. THE ERROR VOLTAGE IN COULOMBS IS $Q = C_L \times \Delta V_O$.



Die Characteristics

Transistor Count 356

Die Dimensions ..... 89 x 93 mils

Substrate Potential* ..... $-V_{SUPPLY}$

Process: ..... CMOS-DI

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
Ceramic DIP	84	25
Plastic DIP	81	33
Ceramic LCC	78	21

*The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential.

HI-524

4 Channel Wideband and Video Multiplexer

Features

- Crosstalk (10MHz)..... < -60dB
- Fast Access Time 150ns
- Fast Settling Time 200ns
- TTL Compatible

Applications

- Wideband Switching
- Radar
- TV Video
- ECM

Description

The HI-524 is a four channel CMOS analog multiplexer designed to process single-ended signals with bandwidths up to 10MHz. The chip includes a 1 of 4 decoder for channel selection and an enable input to inhibit all channels (chip select).

Three CMOS transmission gates are used in each channel, as compared to the single gate in more conventional CMOS multiplexers. This provides a double barrier to the unwanted coupling of signals from each input to the output. In addition, Dielectric Isolation (DI) processing helps to insure the Crosstalk is less than -60dB at 10MHz.

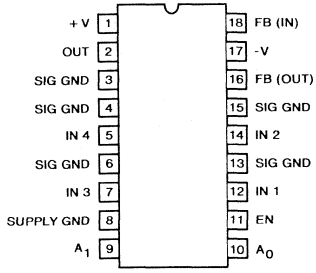
The HI-524 is designed to operate into a wideband buffer amplifier such as the Harris HA-2541. The multiplexer chip includes two "ON" switches in series, for use as a feedback element with the amplifier. This feedback resistance matches and tracks the channel R_{ON} resistance, to minimize the amplifier V_{OS} and its variation with temperature.

The HI-524 is well suited to the rapid switching of video and other wideband signals in telemetry, instrumentation, radar and video systems. It is packaged in an 18 pin ceramic or plastic DIP and a 20 pin plastic leaded chip carrier or a 20 pin ceramic leadless chip carrier and operates on ±15V supplies.

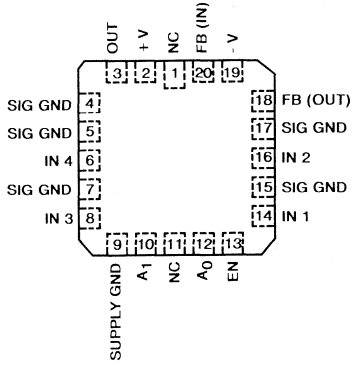
For MIL-STD-883 compliant parts, request the HI-524/883 data sheet.

Pinouts

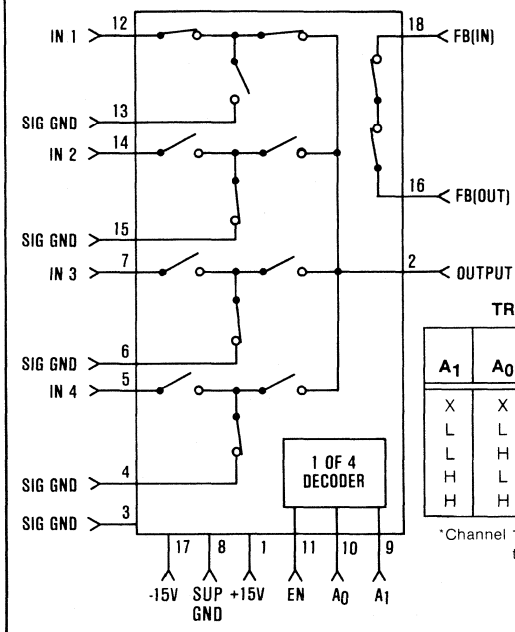
CERAMIC/PLASTIC DIP
TOP VIEW



LCC/PLCC
TOP VIEW



Functional Diagram



TRUTH TABLE

A_1	A_0	EN	ON CHANNEL
X	X	L	NONE
L	L	H	1*
L	H	H	2
H	L	H	3
H	H	H	4

*Channel 1 is shown selected in the diagram

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

Voltage Between Supply 33V
Digital Input Voltage:
$+V_A$ ..... +6V
$-V_A$ ..... -6V
Analog Input Voltage
$+V_{IN}$ ..... $+V_{SUPPLY}$ +2V
$-V_{IN}$ ..... $-V_{SUPPLY}$ -2V
Either Supply to Ground 16.5V
Junction Temperature (Max) ..... 175°C

Operating Temperature Range

HI-524-2/-8 ..... -55°C to +125°C
HI-524-5 ..... 0°C to +75°C
Storage Temperature Range ..... -65°C to +150°C

Electrical Specifications (Unless otherwise specified) Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V, V_{AL} = (Logic Level Low) = +0.8V; V_{EN} = +2.4V

PARAMETER	TEMP	HI-524 -2/-8 MIN	HI-524 -2/-8 TYP	HI-524 -2/-8 MAX	HI-524 -5 MIN	HI-524 -5 TYP	HI-524 -5 MAX	UNITS
ANALOG CHANNEL SPECIFICATIONS								
V_{IN}, Analog Signal Range	Full	-10		+10	-10		+10	V
R_{ON}, On Resistance (Note 2)	+25°C		700			700		Ω
	Full			1.5K			1.5K	Ω
I_S (OFF), Off Input Leakage Current (Note 3)	+25°C		0.2			0.2		nA
	Full			50			50	nA
I_D (OFF), Off Output Leakage Current (Note 3)	+25°C		0.2			0.2		nA
	Full			50			50	nA
I_D (ON), On Channel Leakage Current (Note 3)	+25°C		0.7			0.7		nA
	Full			50			50	nA
3dB Bandwidth: (Note 4)	+25°C		8			8		MHz
DIGITAL INPUT SPECIFICATIONS								
V_{AL} Input Low Threshold (TTL)	Full			0.8			0.8	V
V_{AH} Input High Threshold (TTL)	Full	2.4			2.4			V
I_{AH} Input Leakage Current (High)	Full		0.05	1		0.05	1	μA
A_L Current (Low)	Full			25			25	μA
SWITCHING SPECIFICATIONS								
t_A, Access Time (Note 5)	+25°C		150	300		150	300	ns
t_{OPEN}, Break-Before-Make Delay (Note 5)	+25°C		20			20		ns
t_{ON} (EN), Enable Delay (ON), R_L = 500Ω	+25°C		180	300		180		ns
t_{OFF} (EN), Enable Delay (OFF), R_L = 500Ω	+25°C		180	250		180		ns
Settling Time (0.1%) (Note 5)	+25°C		200			200		ns
(0.01%)	+25°C		600			600		ns
Crosstalk (Note 6)	+25°C		-65			-65		dB
C_S(OFF), Channel Input Capacitance	+25°C		4			4		pF
C_D(OFF), Channel Output Capacitance	+25°C		10			10		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full			750			750	mW
I+, Current (Note 7)	Full			25			25	mA
I-, Current (Note 7)	Full			25			25	mA

NOTES:

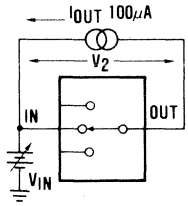
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. V_{IN} = ±10V; I_{OUT} = 100μA (See Test Circuits #1)
3. V_O = ±10V; V_{IN} = ±10V (See Test Circuits #2, 3, 4,)
4. MUX output is buffered with HA-5033 amplifier.
5. See Test Circuit #5.
6. V_{IN} = 10MHz, $3V_{p-p}$ on one channel, with any other channel selected. (Worst case is channel 3 selected with input on channel 4). MUX output is buffered with HA-2541 as shown in Applications section. Terminate all channels with 75Ω.
7. Supply currents vary less than 0.5mA for switching rates from DC to 2MHz.

Performance Characteristics and Test Circuits

Unless otherwise specified T_A = +25°C, V_{SUPPLY} = ±15V, V_{AH} = 2.4V, V_{AL} = 0.8V

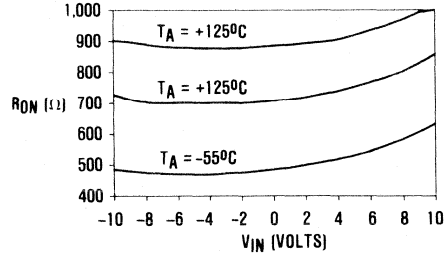
ON RESISTANCE

TEST CIRCUIT NO. 1

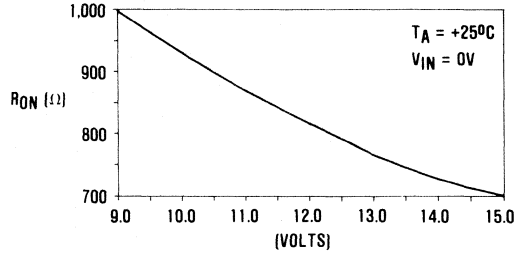


$$R_{ON} = \frac{V2}{100\mu A}$$

ON RESISTANCE vs. ANALOG INPUT VOLTAGE

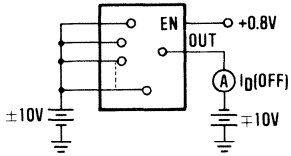


ON RESISTANCE vs. SUPPLY VOLTAGE

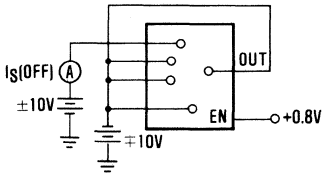


LEAKAGE CURRENT

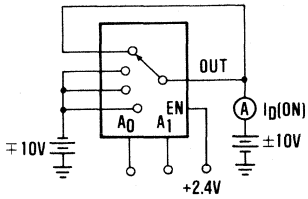
TEST CIRCUIT NO. 2*



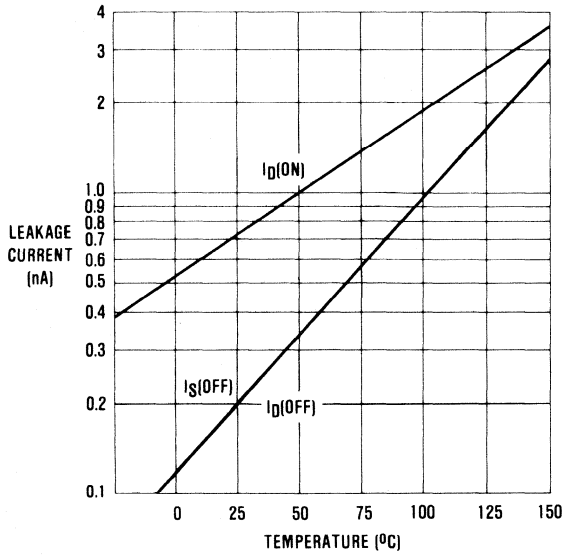
TEST CIRCUIT NO. 3*



TEST CIRCUIT NO. 4*



LEAKAGE CURRENT vs. TEMPERATURE

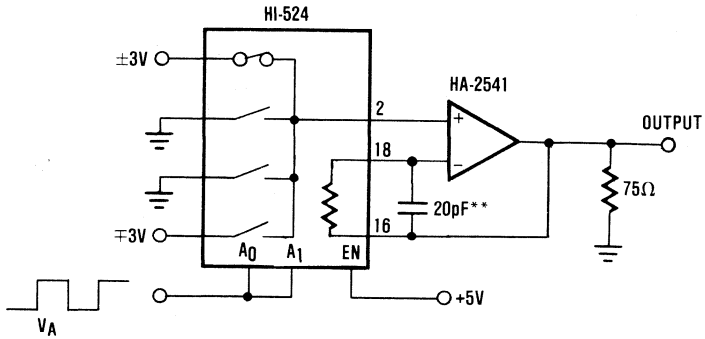


* Two measurements per channel:
+10V/-10V and -10V/+10V
(Two measurements and per device for I_D(OFF):
+10V/-10V and -10V/+10V.)

Performance Characteristics and Test Circuits (Continued)

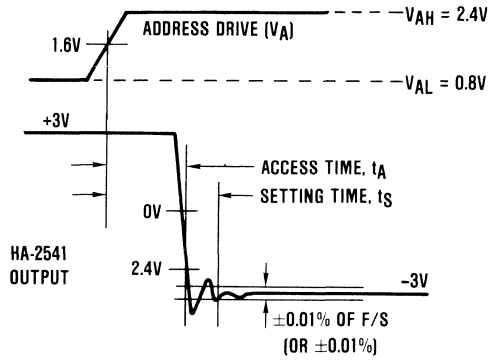
TEST CIRCUIT NO. 5

SETTLING TIME
ACCESS TIME
BREAK-BEFORE-MAKE DELAY*

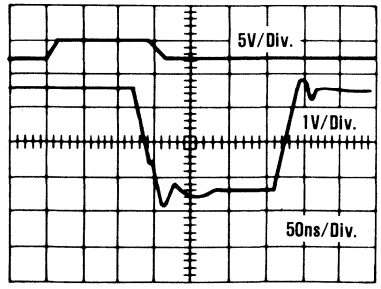


* This test requires channel inputs 1 and 4 at the same level.
** Capacitor value may be selected to optimize AC performance.

(Use Differential comparator plug-in on scope for settling time measurement)

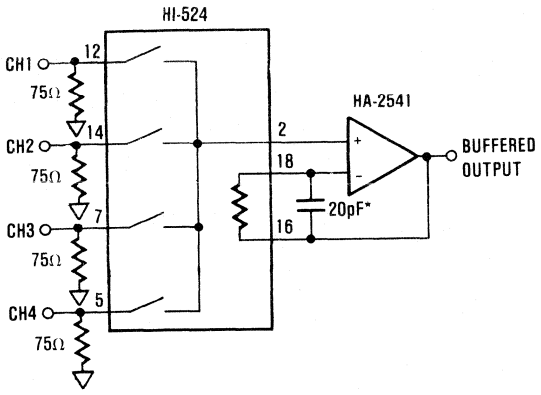


ACCESS TIME



Applications

Often it is desirable to buffer the HI-524 output, to avoid loading errors due to the channel "ON" resistance:



* Capacitor value may be selected to optimize AC performance.

The buffer amplifier should offer sufficient bandwidth and slew rate to avoid degradation of the anticipated signals. For video switching, the HA-5033 and HA-2542 offer good performance plus ±100mA output current for driving coaxial cables. For general wideband applications, the HA-2541 offers the convenience of unity gain stability plus 90ns settling (to ±0.1%) and ±10V output swing. Also, the HI-524 includes a feedback resistance for use with the HA-2541. This resistance matches and tracks the channel "ON" resistance, to minimize offset voltage due to the buffer's bias currents.

Note that the on-chip feedback element between pins 16 and 18 includes two switches in series, to simulate a channel resistance. These switches open for V_{EN} = Low. This allows two or more HI-524's to operate into one HA-2541, with their feedback elements connected in parallel. Thus, only the selected multiplexer provides feedback, and the amplifier remains stable.

All HI-524 DIP package pins labeled 'SIG GND' (pins 3, 4, 6, 13, 15) should be externally connected to signal ground for best crosstalk performance.

Bypass capacitors (0.1 to 1.0μF) are recommended from each HI-524 supply pin to power ground (pins 1 and 17 to pin 8 DIP package). Locate the buffer amplifier near the HI-524 so the two capacitors may bypass both devices.

If an analog input 1V or greater is present when supplies are off, a low resistance is seen from that input to a supply line. (For example, the resistance is approximately 160Ω for an input of -3V.) Current frow may be blocked by a diode in each supply line, or limited by a resistor in series with each channel. the best solution, of course, is to arrange that no digital or analog inputs are present when the power supplies are off.

Die Characteristics

Transistor Count 599
Die Dimensions ..... 146 x 88.6 mils
Substrate Potential* ..... $-V_{SUPPLY}$
Process: ..... CMOS-DI

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
Ceramic DIP	81	22
Plastic DIP	78	30
Ceramic LCC	76	19

*The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential.

HARRIS

HI-539

Monolithic, 4 Channel, Low Level, Differential Multiplexer

Features

- **Differential Performance, Typical:**
  - Low ΔR_{ON}, +125°C.....5.5Ω
  - Low $\Delta I_{D(ON)}$, +125°C 0.6nA
  - Low Δ(Charge Injection).....0.1pC
  - Low Crosstalk..... -124dB
- **Settling Time, ±0.01%.....900ns**
- **Wide Supply Range..... ±5V to ±18V**
- **Break-Before-Make Switching**
- **No Latch-Up**

Applications

- **Low Level Data Acquisition**
- **Precision Instrumentation**
- **Test Systems**

Description

The Harris HI-539 is a monolithic, four channel, differential multiplexer. Two digital inputs are provided for channel selection, plus an Enable input to disconnect all channels.

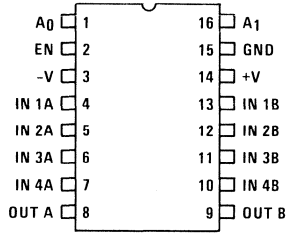
Performance is guaranteed for each channel over the voltage range ±10V, but is optimized for low level differential signals. Leakage current, for example, which varies slightly with input voltage, has its distribution centered at zero input volts.

In most monolithic multiplexers, the net differential offset due to thermal effects becomes significant for low level signals. This problem is minimized in the HI-539 by symmetrical placement of critical circuitry with respect to the few heat producing devices.

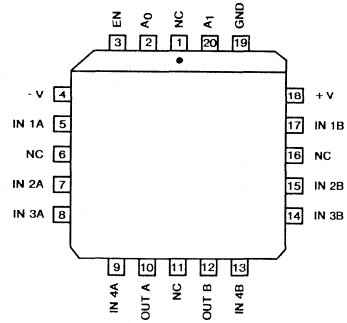
Supply voltages are ±15V and power consumption is only 2.5mW. The HI-539 is packaged in a 16 pin Ceramic or Plastic DIP, and a 20 pin Plastic Leaded Chip Carrier.

Pinouts

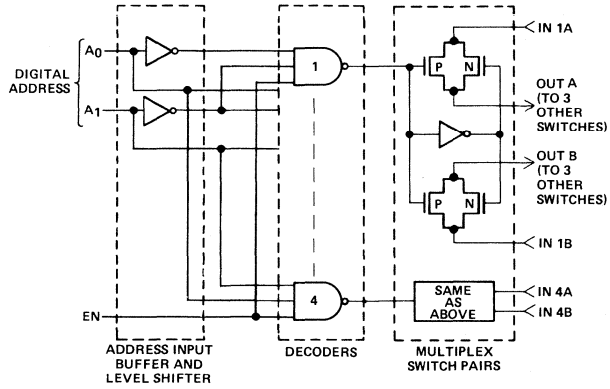
HI1-539 CERAMIC DIP
HI3-539 PLASTIC DIP
TOP VIEW



HI4P539 PLCC
TOP VIEW



Functional Diagram



CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Absolute Maximum Ratings

Voltage Between Supply Pins (-V, +V) 40V
Voltage From Either Supply to Gnd 20V
Analog Input Voltage, V_{IN} ..... $-V \leq V_{IN} \leq +V$
Digital Input Voltage, V_A ..... $-V \leq V_A \leq +V$
Junction Temperature (Max) ..... 175°C

Operating Temperature Range
HI-539-2, -8 ..... -55°C to +125°C
HI-539-4 ..... -25°C to +85°C
HI-539-5 ..... 0°C to +75°C
Storage Temperature Range ..... -65°C to +150°C

Electrical Specifications

(Unless otherwise specified) Supplies = ±15V, V_{EN} = +4.0V, V_{AH} (Logic Level High) = +4.0V, V_{AL} (Logic Level Low) = +0.8V. See the "Performance Characteristics and Test Circuits". Selected parameters are defined in "Definitions".

PARAMETER	TEMP	HI-539-2, -8 TYP	HI-539-2, -8 MAX (MIN)	HI-539-4, -5 TYP	HI-539-4, -5 MAX (MIN)	UNITS
ANALOG CHANNEL CHARACTERISTICS						
V_{IN}, Analog Signal Range	Full		(-10)/+10		(-10)/+10	V
R_{ON}, On Resistance V_{IN} = 0V	+25°C	650	850	650	850	Ω
V_{IN} = ± 10V	+25°C	700	900	700	900	Ω
V_{IN} = 0V	Full	950	1.3k	800	1k	Ω
V_{IN} = ± 10V	Full	1.1k	1.4k	900	1.1k	Ω
ΔR_{ON} [Side A - Side B]						
V_{IN} = 0V	+25°C	4.0	24	4.0	24	Ω
V_{IN} = ± 10V	+25°C	4.5	27	4.5	27	Ω
V_{IN} = 0V	Full	4.75	28	4.0	24	Ω
V_{IN} = ± 10V	Full	5.5	33	4.5	27	Ω
$I_{S(OFF)}$, Off Input Leakage Current (Note 1)						
Condition 0V	+25°C	30		30		pA
Condition ± 10V	+25°C	100		100		pA
Condition 0V	Full	2	10	0.2	1	nA
Condition ± 10V	Full	5	25	0.5	2.5	nA
$\Delta I_{S(OFF)}$, [Side A - Side B]						
Condition 0V	+25°C	3		3		pA
Condition ± 10V	+25°C	10		10		pA
Condition 0V	Full	0.2	2	0.02	0.2	nA
Condition ± 10V	Full	0.5	5	0.05	0.5	nA
$I_{D(OFF)}$, Off Output Leakage Current (Note 1)						
Condition 0V	+25°C	30		30		pA
Condition ± 10V	+25°C	100		100		pA
Condition 0V	Full	2	10	0.2	1	nA
Condition ± 10V	Full	5	25	0.5	2.5	nA
$\Delta I_{D(OFF)}$, [Side A - Side B]						
Condition 0V	+25°C	3		3		pA
Condition ± 10V	+25°C	10		10		pA
Condition 0V	Full	0.2	2	0.02	0.2	nA
Condition ± 10V	Full	0.5	5	0.05	0.5	nA
$I_{D(ON)}$, On Channel Leakage Current (Note 1)						
Condition 0V	+25°C	50		50		pA
Condition ± 10V	+25°C	150		150		pA
Condition 0V	Full	5	25	0.5	2.5	nA
Condition ± 10V	Full	6	40	0.8	4.0	nA
$\Delta I_{D(ON)}$ [Side A - Side B]						
Condition 0V	+25°C	10		10		pA
Condition ± 10V	+25°C	30		30		pA
Condition 0V	Full	0.5	5	0.05	0.5	nA
Condition ± 10V	Full	0.6	6	0.08	0.8	nA
ΔV_{OS}, Differential Offset Voltage (Note 2)	+25°C	0.02		0.02		µV
	Full	0.70		0.08		µV

PARAMETER	TEMP	HI-539-2, -8 TYP	HI-539-2, -8 MAX (MIN)	HI-539-4, -5 TYP	HI-539-4, -5 MAX (MIN)	UNITS
DIGITAL INPUT CHARACTERISTICS						
V_{AL}, Input Low Threshold	Full		0.8		0.8	V
V_{AH}, Input High Threshold	Full		(4.0)		(4.0)	V
I_{AH}, Input Leakage Current (High)	Full		1		1	μA
I_{AL}, Input Leakage Current (Low)	Full		1		1	μA
SWITCHING CHARACTERISTICS						
T_A, Access Time	+25°C	250	750	250	750	ns
	Full		1,000		1,000	ns
T_{open}, Break-Before-Make Delay	+25°C	85	(30)	85	(30)	ns
	Full		(30)		(30)	ns
$T_{ON(EN)}$, Enable Delay On	+25°C	250	750	250	750	ns
	Full		1,000		1,000	ns
$T_{OFF(EN)}$, Enable Delay Off	+25°C	160	650	160	650	ns
	Full		900		900	ns
Settling Time, to ±0.01%	+25°C	0.9		0.9		μs
Charge Injection (Output)	Full	3		3		pC
Δ Charge Injection (Output)	Full	0.1		0.1		pC
Charge Injection (Input)	Full	10		10		pC
Differential Crosstalk (Note 3)	+25°C	124		124		dB
Single Ended Crosstalk (Note 3)	+25°C	100		100		dB
$C_{S(OFF)}$, Channel Input Capacitance	Full	5		5		pF
$C_{D(OFF)}$, Channel Output Capacitance	Full	7		7		pF
$C_{D(ON)}$, Channel On Output Capacitance	Full	17		17		pF
C_{DS}, Input to Output Capacitance (Note 4)	Full	0.08		0.08		pF
C_A, Digital Input Capacitance	Full	3		3		pF
POWER REQUIREMENTS						
P_D, Power Dissipation	+25°C	2.3		2.3		mW
	Full		45		45	mW
I+ Current	+25°C	0.150		0.150		mA
	Full		2.0		2.0	mA
I- Current	+25°C	0.001		0.001		mA
	Full		1.0		1.0	mA
±V, Supply Voltage Range	Full	±15	(±5)/ ±18	±15	(±5)/ ±18	V

NOTES:

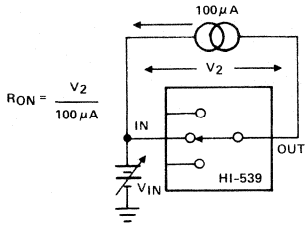
1. See Test Circuits #2, 3, 4. The condition ±10V means:
   $I_{S(OFF)}$ and $I_{D(OFF)}$: (V_S = +10V, V_D = -10V), then (V_S = -10V, V_D = +10V)
   $I_{D(ON)}$: (+10V, then -10V)
2. ΔV_{OS} (Exclusive of thermocouple effects) = R_{ON} $\Delta I_{D(ON)}$ + $I_{D(ON)}$ ΔR_{ON}.
   See Applications section for discussion of additional V_{OS} error.
3. V_{IN} = 1kHz, 15V_{p-p} on all but the selected channel. See Test Circuit #9.
4. Calculated from typical Single-Ended Crosstalk performance.

Performance Characteristics and Test Circuits

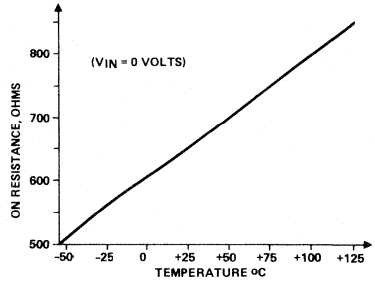
(Unless otherwise specified T_A = 25°C, +V = +15V, -V = -15V, V_{AH} = +4V and V_{AL} = +0.8V)

ON RESISTANCE MEASUREMENT

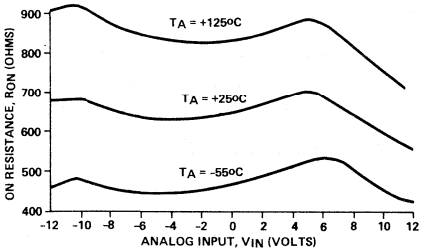
TEST CIRCUIT NO. 1



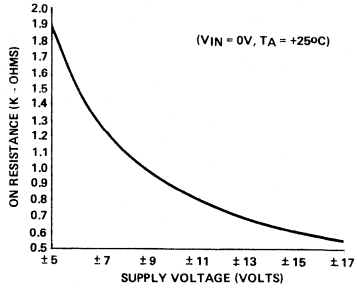
ON RESISTANCE vs. TEMPERATURE



ON RESISTANCE vs. ANALOG INPUT VOLTAGE

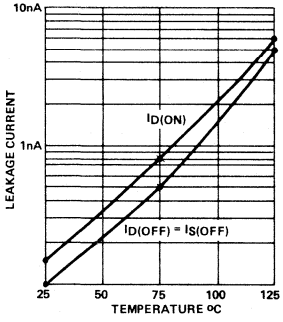


NORMALIZED ON RESISTANCE vs. SUPPLY VOLTAGE

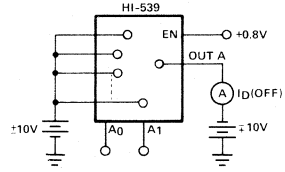


LEAKAGE CURRENT

LEAKAGE CURRENT vs. TEMPERATURE

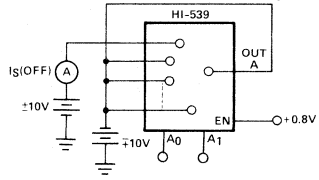


TEST CIRCUIT NO. 2*



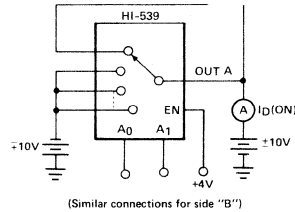
(Similar connections for side "B")

TEST CIRCUIT NO. 3*



(Similar connections for side "B")

TEST CIRCUIT NO. 4*



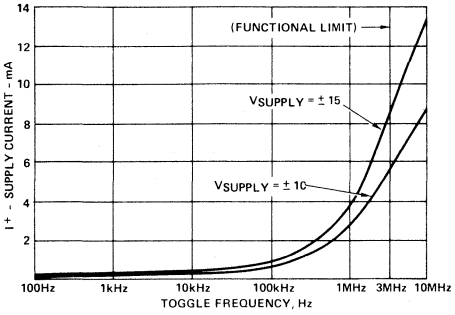
(Similar connections for side "B")

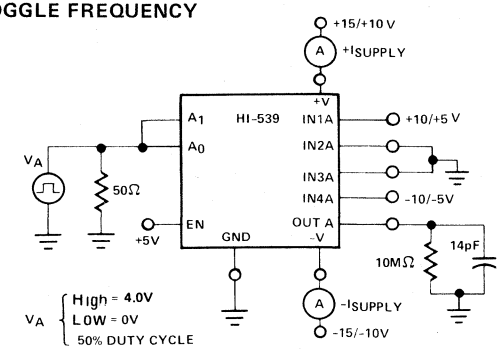
*Three measurements = +10V/-10V, -10V/+10V, and 0V

Test Circuits (Continued)

TEST CIRCUIT NO. 5

SUPPLY CURRENT vs. TOGGLE FREQUENCY

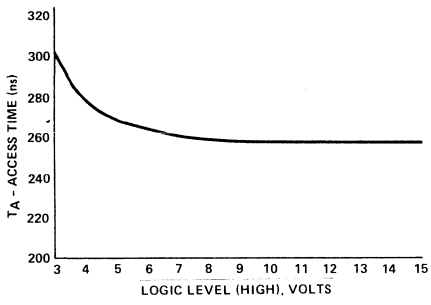


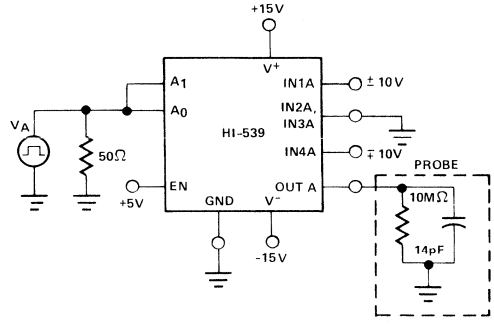


(SIMILAR CONNECTIONS FOR "B" SIDE

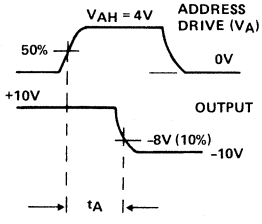
TEST CIRCUIT NO. 6

ACCESS TIME vs. LOGIC LEVEL (HIGH)

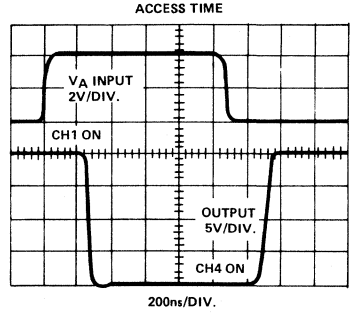




(SIMILAR CONNECTIONS FOR "B" SIDE)



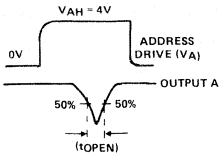
Example: t_A for 4V logic level



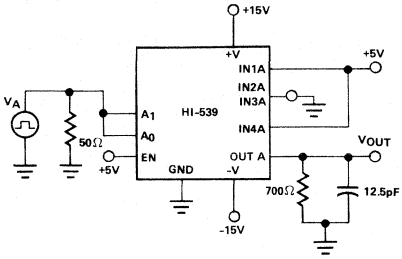
Test Circuits (Continued)

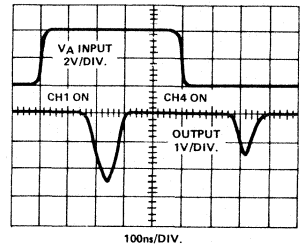
TEST CIRCUIT NO. 7

ADDRESS DRIVE



BREAK-BEFORE-MAKE DELAY (t_{OPEN})

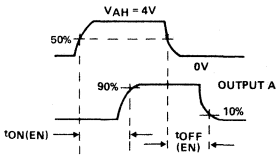




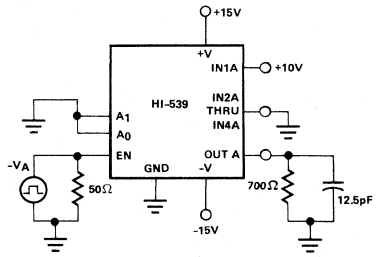
(SIMILAR CONNECTION FOR "B" SIDE)

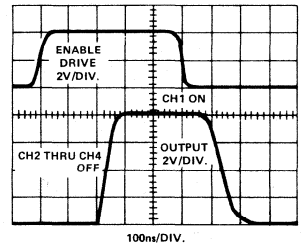
TEST CIRCUIT NO. 8

ENABLE DRIVE



ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)

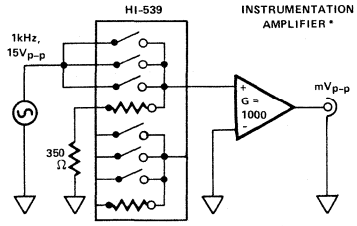




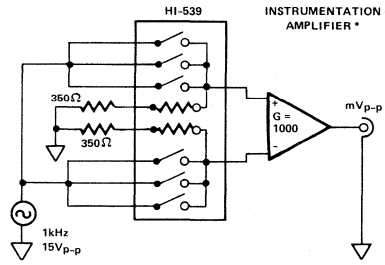
(SIMILAR CONNECTION FOR "B" SIDE)

TEST CIRCUIT NO. 9

SINGLE-ENDED CROSSTALK



DIFFERENTIAL CROSSTALK



*AD606 or BB3630, FOR EXAMPLE

Definitions

CHARGE INJECTION – Charge (in pC) transferred, during a transition between channels, through the internal gate-to-channel capacitance. The resulting voltage error varies inversely with the output (or input) capacitance.

CROSSTALK – Signal at the multiplexer output, coupling though the C_{DS} capacitance of an OFF channel. Amplitude is proportional to source resistance for the ON channel. See Test Circuit # 9 for single-ended and differential versions of crosstalk.

DIFFERENTIAL LEAKAGE CURRENT ($\Delta I_{S(OFF)}$, $\Delta I_{D(OFF)}$, $\Delta I_{D(ON)}$) – The absolute difference in leakage for the two sides of a channel.

DIFFERENTIAL OFFSET VOLTAGE (ΔV_{OS}) – Voltage between the multiplexer output terminals with both channel input terminals shorted to ground.

DIFFERENTIAL ON RESISTANCE (ΔR_{ON}) – The absolute difference in On Resistance for the two sides of a channel.

INPUT TO OUTPUT CAPACITANCE (C_{DS}) – Capacitance from one input terminal of a channel to the corresponding output of the multiplexer. This parameter is responsible for Crosstalk.

Applications

GENERAL

The HI-539 accepts inputs in the range -15V to +15V, with performance guaranteed over the ±10V range. At these higher levels of analog input voltage it is comparable to the HI-509, and is plug-in compatible with that device (as well as the HI-509A). However, as mentioned earlier, the HI-539 was designed to introduce minimum error when switching low level inputs.

Special care is required in working with these low level signals. The main concern with signals below 100mV is that noise, offset voltage, and other aberrations can represent a large percentage error. A shielded, differential signal path is essential, especially to maintain a noise level below 50 μVrms.

LOW LEVEL SIGNAL TRANSMISSION

The transmission cable carrying the transducer signal is critical in a low level system. It should be as short as practical and rigidly supported. Signal conductors should be tightly twisted for minimum enclosed area, to guard against pickup of electromagnetic interference, and the twisted pair should be shielded against capacitively coupled (electrostatic) interference. A braided wire shield may be satisfactory, but a lapped foil shield is better since it allows only one tenth as much leakage capacitance to ground per foot. A key requirement for the transmission cable is that it presents a balanced line to sources of noise interference. This means an equal series impedance in each conductor plus an equally distributed impedance from each conductor to ground. The result should be signals equal in magnitude but opposite in phase at any transverse plane. Noise will be coupled in phase to both conductors, and may be rejected as common mode voltage by a differential amplifier connected to the multiplexer output.

Coaxial cable is not suitable for low-level signals because the two conductors (center and shield) are unbalanced. Also, ground loops are produced if the shield is grounded at both ends by standard BNC connectors. If coax must be used, carry the signal on the center conductors of two equal-length cables whose shields are terminated only at the transducer end. As a general rule, terminate (ground) the shield at one end only, preferably at the end with greatest noise interference. This is usually the transducer end for both high and low level signals.

TABLE 1.

WIRE GAGE	EQUIVALENT WIDTH OF P.C. CONDUCTOR (2 oz. Cu.)	D.C. RESISTANCE PER FOOT	INDUCTANCE PER FOOT	IMPEDANCE PER FOOT	
				AT 60Hz	AT 10kHz
18	0.47"	0.0064Ω	0.36μH	0.0064Ω	0.0235Ω
20	0.30"	0.0102Ω	0.37μH	0.0102Ω	0.0254Ω
22	0.19"	0.0161Ω	0.37μH	0.0161Ω	0.0288Ω
24	0.12"	0.0257Ω	0.40μH	0.0257Ω	0.0345Ω
26	0.075"	0.041Ω	0.42μH	0.041Ω	0.0488Ω
28	0.047"	0.066Ω	0.45μH	0.066Ω	0.0718Ω
30	0.029"	0.105Ω	0.49μH	0.105Ω	0.110Ω
32	0.018"	0.168Ω	0.53μH	0.168Ω	0.171Ω

Applications (Continued)

WATCH SMALL ΔV ERRORS

Printed circuit traces and short lengths of wire can add substantial error to a signal even after it has traveled hundreds of feet and arrived on a circuit board. Here, the small voltage drops due to current flow through connections of a few milliohms must be considered, especially to meet an accuracy requirement of 12 bits or more.

Table 1 is a useful collection of data for calculating the effect of these short connections. (Proximity to a ground plane will lower the values of inductance.)

As an example, suppose the HI-539 is feeding a 12 bit converter system with an allowable error of ±1/2 LSB (±1.22mV). If the interface logic draws 100mA from the 5V supply, this current will produce 1.28mV across 6 inches of #24 wire; more than the error budget. Obviously, this digital current must not be routed through any portion of the analog ground return network.

PROVIDE PATH FOR I_{BIAS}

The input bias current for any DC-coupled amplifier must have an external path back to the amplifier's power supply. No such path exists in Figure 1A, and consequently the amplifer output will remain in saturation.

A single large resistor (1MΩ to 10MΩ) from either signal line to power supply common will provide the required path, but a resistor on each line is necessary to preserve accuracy. A single pair of these bias current resistors on the HI-539 output may be used if their loading effect can be tolerated (each forms a voltage divider with R_{ON}). Otherwise, a resistor pair on each input channel of the multiplexer is required.

The use of bias current resistors is acceptable only if one is confident that the sum of signal plus common-mode voltage will remain within the input range of the multiplexer/amplifier combination.

Another solution is to simply run a third wire from the low side of the signal source, as in Figure 1B. This wire assures a low common-mode voltage as well as providing the path for bias currents. Making the connection near the multiplexer will save wire, but it will also unbalance the line and reduce the amplifier's common-mode rejection.

DIFFERENTIAL OFFSET, ΔV_{OS}

There are two major sources of ΔV_{OS}. That part, due to the expression ($R_{ON}\,\Delta I_D(ON) + I_D(ON)\,\Delta R_{ON}$) becomes significant with increasing temperature, as shown in the Electrical Characteristics section. The other source of offset is the thermocouple effects due to dissimilar materials in the signal path. These include silicon, aluminum, tin, nickel-iron and (often) gold, just to exit the package.

For the thermocouple effects in the package alone, the constraint on ΔV_{OS} may be stated in terms of a limit on the difference in temperature for package pins leading to any channel of the HI-539. For example, a difference of 0.13°C produces a 5μV offset. Obviously, this ΔT effect can dominate the ΔV_{OS} parameter at any temperature unless care is taken in mounting the HI-539 package.

Temperature gradients across the HI-539 package should be held to a minimum in critical applications. Locate the HI-539 far from heat producing components, with any air currents flowing lengthwise across the package.

Applications (Continued)

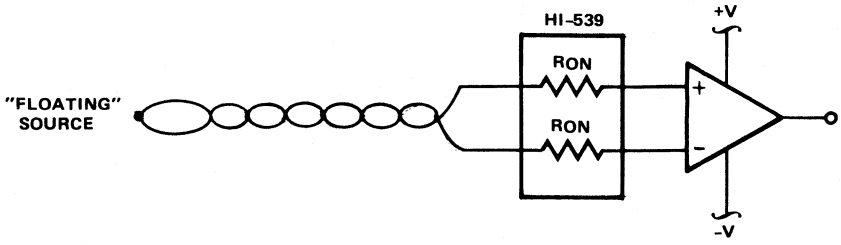


FIGURE 1A

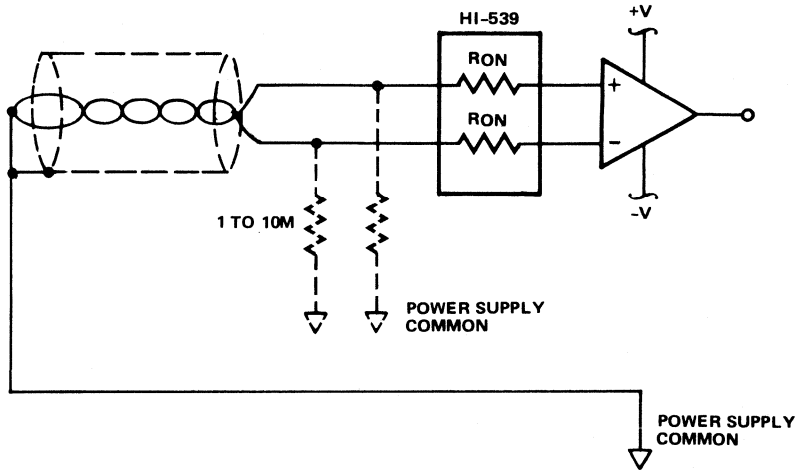


FIGURE 1B

The amplifier in Figure 1A is unusable because its bias currents cannot return to the power supply. Figure 1B shows two alternative paths for these bias currents: either a pair of resistors, or (better) a third wire from the low side of the signal source.

Die Characteristics

Transistor Count	236
Die Dimensions	92 x 100 mils
Substrate Potential*	$-V_{SUPPLY}$
Process:	CMOS-DI

Thermal Constants ($^oC/W$)	θ_{ja}	θ_{jc}
Ceramic DIP	103	34
Plastic DIP	75	22

*The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential.

HI-546/547

Single 16/Differential 8 Channel CMOS Analog Multiplexers with Active Overvoltage Protection

Features

- Analog Overvoltage Protection ..... $70V_{p-p}$
- No Channel Interaction During Overvoltage
- ESD Resistant ..... >4,000V
- Guaranteed R_{ON} Matching
- 44V Maximum Power Supply
- Break-Before-Make Switching
- Analog Signal Range ..... ±15V
- Access Time (Typical) 500ns
- Standby Power (Typical) 7.5mW

Applications

- Data Acquisition
- Industrial Controls
- Telemetry

Description

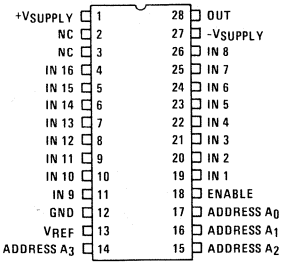
The HI-546 and HI-547 are analog multiplexers with Active Overvoltage Protection and guaranteed R_{ON} matching. Analog input levels may greatly exceed either power supply without damaging the device or disturbing the signal path of other channels. Active protection circuitry assures that signal fidelity is maintained even under fault conditions that would destroy other multiplexers. Analog inputs can withstand constant 70 volt peak-to-peak levels and typically survive static discharges beyond 4,000 volts. Digital inputs will also sustain continuous faults up to 4 volts greater than either supply. In addition, signal sources are protected from short circuiting should multiplexer supply loss occur; each input presents 1kΩ of resistance under this condition. These features make the HI-546 and HI-547 ideal for use in systems where the analog inputs originate from external equipment or separately powered circuitry. Both devices are fabricated with 44 volt dielectrically isolated CMOS technology. The HI-546 is a 16 channel device and the HI-547 is a 8 channel differential version. If input overvoltage protection is not needed, the HI-506 and HI-507 multiplexers are recommended. For further information see Application Notes 520 and 521.

The HI-546/547 are offered in both commercial and military grades. Additional Hi-Rel screening to MIL-STD-883 is available when specified by the "/883" suffix. For details, request the HI-546/883 or HI-547/883 data sheets.

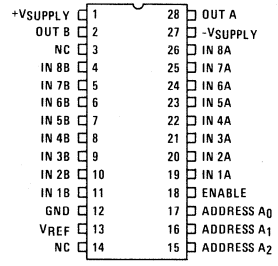
Each device is available in a 28 pin Plastic or Ceramic DIP, and a 28 pin Plastic Leaded Chip Carrier (PLCC).

Pinouts

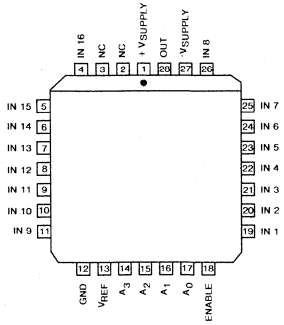
HI1-546 (CERAMIC DIP)
HI3-546 (PLASTIC DIP)
TOP VIEW



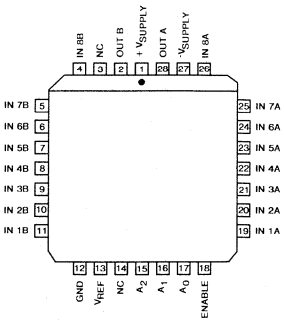
HI1-547 (CERAMIC DIP)
HI3-547 (PLASTIC DIP)
TOP VIEW



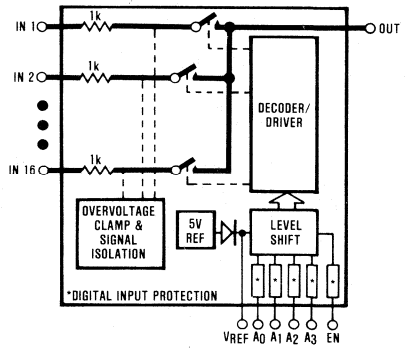
HI4P546 (PLCC)
TOP VIEW



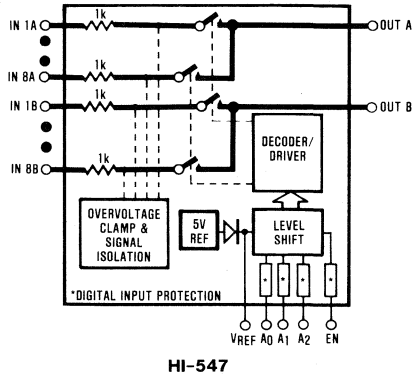
HI4P547 (PLCC)
TOP VIEW



Functional Diagrams



HI-546



HI-547

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

$V_{SUPPLY(+)}$ to $V_{SUPPLY(-)}$ 44V
$V_{SUPPLY(+)}$ to GND 22V
$V_{SUPPLY(-)}$ to GND 25V
Digital Input Overvoltage
$+V_{EN}$, $+V_A$ ..... $+V_{SUPPLY}$ +4V
$-V_{EN}$, $-V_A$ ..... $-V_{SUPPLY}$ -4V
or 20mA, whichever occurs first.
Analog Signal Overvoltage (Note 7)
$+V_S$ ..... $+V_{SUPPLY}$ +20V
$-V_S$ ..... $-V_{SUPPLY}$ -20V
Continuous Current, S or D: 20mA
Peak Current, S or D
(Pulsed at 1ms, 10% duty cycle max): 40mA
Junction Temperature ..... +175°C
Operating Temperature Ranges:
HI-546/547-2 ..... -55°C to +125°C
HI-546/547-4 ..... -25°C to +85°C
HI-546/547-5 ..... 0°C to +75°C
Storage Temperature Range ..... -65°C to +150°C

Electrical Specifications Unless Otherwise Specified:

Supplies = +15V, -15V; V_{REF} Pin = Open; V_{AH} (Logic Level High) = +4.0V;
V_{AL} (Logic Level Low) = +0.8V. For Test Conditions, consult Performance Characteristics Section.

PARAMETER	TEMP.	HI-546/HI-547 -2 MIN.	HI-546/HI-547 -2 TYP.	HI-546/HI-547 -2 MAX.	HI-546/547 -4, -5 MIN.	HI-546/547 -4, -5 TYP.	HI-546/547 -4, -5 MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS								
V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
R_{ON}, On Resistance (Note 2)	+25°C		1.2	1.5		1.5	1.8	kΩ
	Full		1.5	1.8		1.8	2.0	kΩ
$\triangle R_{ON}$, Any Two Channels	+25°C			7.0			7.0	%
I_S (OFF), Off Input Leakage Current (Note 3)	+25°C		0.03			0.03		nA
	Full			50			50	nA
I_D (OFF), Off Output Leakage Current (Note 3)	+25°C		0.1			0.1		nA
HI-546	Full			300			300	nA
HI-547	Full			200			200	nA
I_D (OFF), with Input Overvoltage Applied (Note 4)	+25°C		4.0			4.0		nA
	Full			2.0				μA
I_D (ON), On Channel Leakage Current (Note 3)	+25°C		0.1			0.1		nA
HI-546	Full			300			300	nA
HI-547	Full			200			200	nA
I_{DIFF}, Differential Off Output Leakage Current (HI-547 Only)	Full			50			50	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold TTL Drive	Full			0.8			0.8	V
V_{AH}, Input High Threshold (Note 8)	Full	4.0			4.0			V
V_{AL} MOS Drive (Note 9)	+25°C			0.8			0.8	V
V_{AH} MOS Drive (Note 9)	+25°C	6.0			6.0			V
I_A, Input Leakage Current (High or Low) (Note 5)	Full			1.0			1.0	μA
SWITCHING CHARACTERISTICS								
t_A, Access Time	+25°C		0.5			0.5		μs
	Full			1.0			1.0	μs
t_{OPEN}, Break-Before-Make Delay	+25°C	25	80		25	80		ns
t_{ON} (EN), Enable Delay (ON)	+25°C		300	500		300		ns
	Full			1000			1000	ns
t_{OFF} (EN), Enable Delay (OFF)	+25°C		300	500		300		ns
	Full			1000			1000	ns
Settling Time (0.1%)	+25°C		1.2			1.2		μs
(0.01%)	+25°C		3.5			3.5		μs
"Off Isolation" (Note 6)	+25°C	50	68		50	68		dB
C_S (OFF), Channel Input Capacitance	+25°C		5			5		pF
C_D (OFF), Channel Output Capacitance HI-546	+25°C		50			50		pF
HI-547	+25°C		25			25		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
C_{DS} (OFF), Input to Output Capacitance	+25°C		0.1			0.1		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full		7.5			7.5		mW
I+, Current Pin 1 (Note 7)	Full		0.5	2.0		0.5	2.0	mA
I−, Current Pin 27 (Note 7)	Full		0.02	1.0		0.02	1.0	mA

TRUTH TABLES

HI-546

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	NONE
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

HI-547

A_2	A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

NOTES:
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. V_{OUT} = ±10V, I_{OUT} = -100μA.
3. Ten nanoamps is the practical lower limit for high speed measurement in the production test environment.
4. Analog Overvoltage = ±33V.
5. Digital input leakage is primarily due to the clamp diodes (see Schematic). Typical leakage is less than 1nA at 25°C.
6. V_{EN} = 0.8V, R_L = 1K, C_L = 15pF, V_S = $7V_{RMS}$, f = 100kHz.
7. V_{EN}, V_A = 0V or 4.0V.
8. To drive from DTL/TTL Circuits, 1kΩ pull-up resistors to $+5.0V_{SUPPLY}$ are recommended.
9. V_{REF} = +10V.

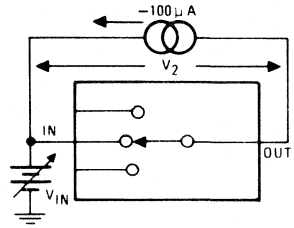
Performance Characteristics and Test Circuits

Unless Otherwise Specified: T_A = 25°C, V_{Supply} = ±15 V, V_{AH} = +4 V, V_{AL} = 0.8 V And V_{Ref} = Open.

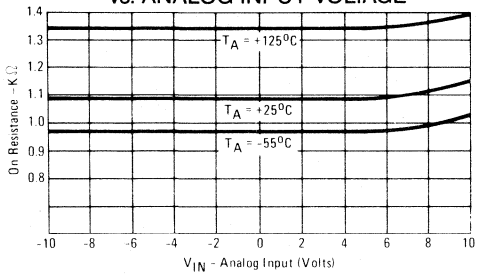
ON RESISTANCE vs.
INPUT SIGNAL LEVEL, SUPPLY VOLTAGE

$R_{ON} = \frac{V_2}{100\mu A}$

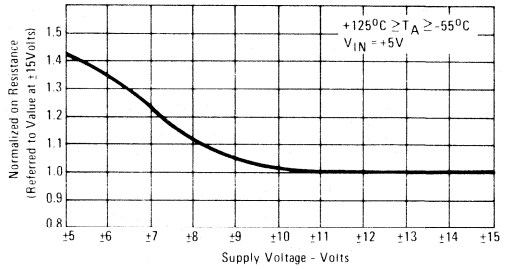
TEST CIRCUIT NO. 1



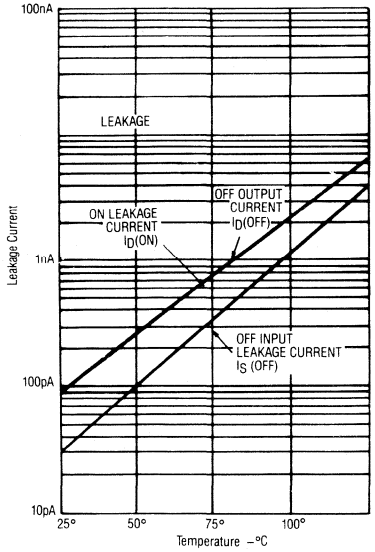
ON RESISTANCE
vs. ANALOG INPUT VOLTAGE



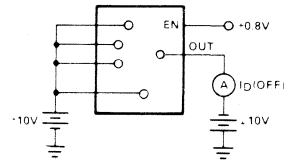
NORMALIZED ON RESISTANCE
vs. SUPPLY VOLTAGE



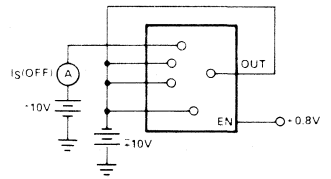
LEAKAGE CURRENT VS. TEMPERATURE



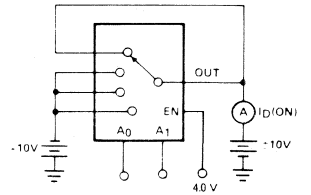
TEST CIRCUIT NO. 2*



TEST CIRCUIT NO. 3*

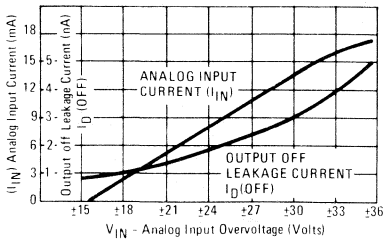


TEST CIRCUIT NO. 4*



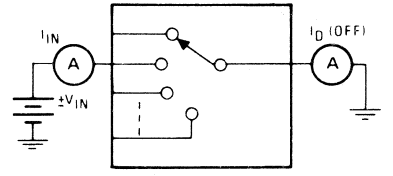
***Two measurements per channel: +10 V/−10 V and −10 V/+10 V. (Two measurements per device for $I_{D(OFF)}$: +10 V/−10 V and −10 V/+10 V.)**

ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



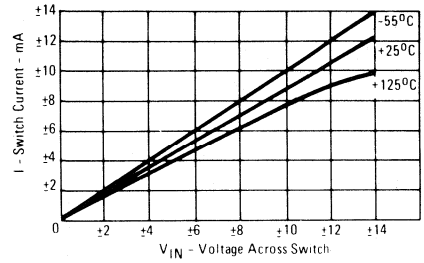
TEST CIRCUIT NO. 5

ANALOG INPUT
OVERVOLTAGE CHARACTERISTICS



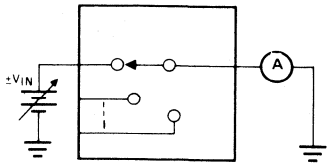
Performance Characteristics and Test Circuits (continued)

ON CHANNEL CURRENT vs. VOLTAGE

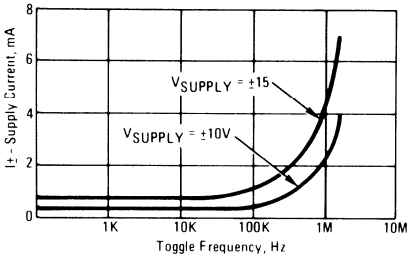


TEST CIRCUIT NO. 6

ON CHANNEL CURRENT vs. VOLTAGE

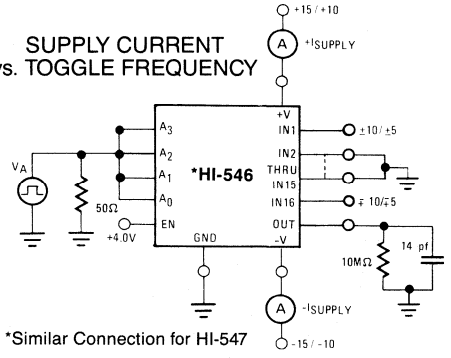


SUPPLY CURRENT vs. TOGGLE FREQUENCY



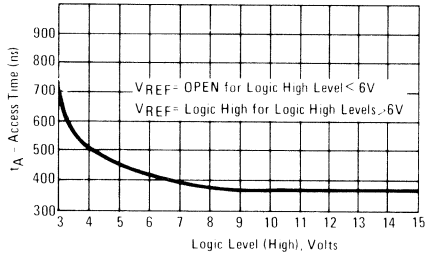
TEST CIRCUIT NO. 7

SUPPLY CURRENT vs. TOGGLE FREQUENCY



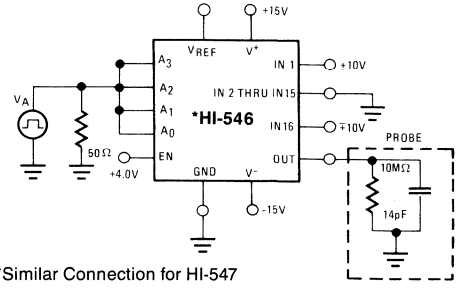
*Similar Connection for HI-547

ACCESS TIME VS. LOGIC LEVEL (HIGH)



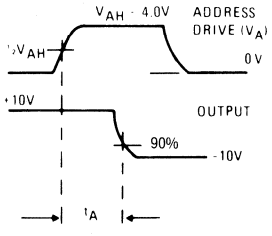
TEST CIRCUIT NO. 8

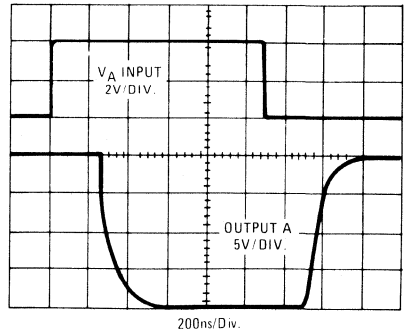
ACCESS TIME vs. LOGIC LEVEL (HIGH)



*Similar Connection for HI-547

Switching Waveforms

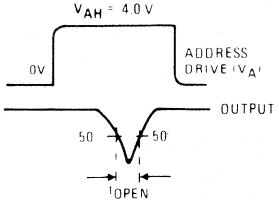


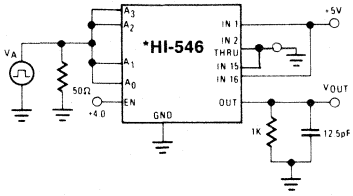


Switching Waveforms (continued)

TEST CIRCUIT NO. 9

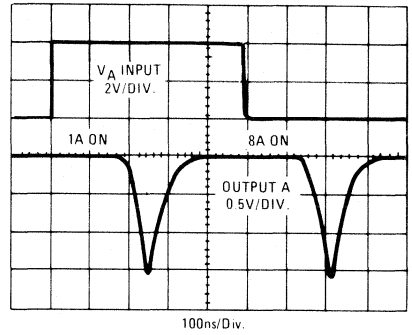
BREAK-BEFORE-MAKE DELAY (tOPEN)





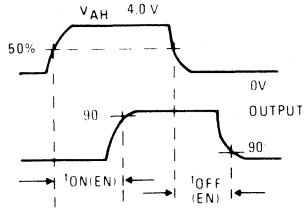
*Similar Connection for HI-547

BREAK-BEFORE-MAKE DELAY(tOPEN)

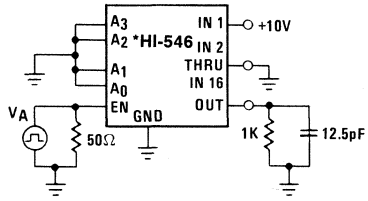


TEST CIRCUIT NO. 10

ENABLE DRIVE

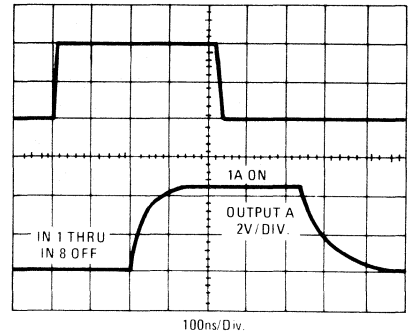


ENABLE DELAY (tON(EN),tOFF(EN))

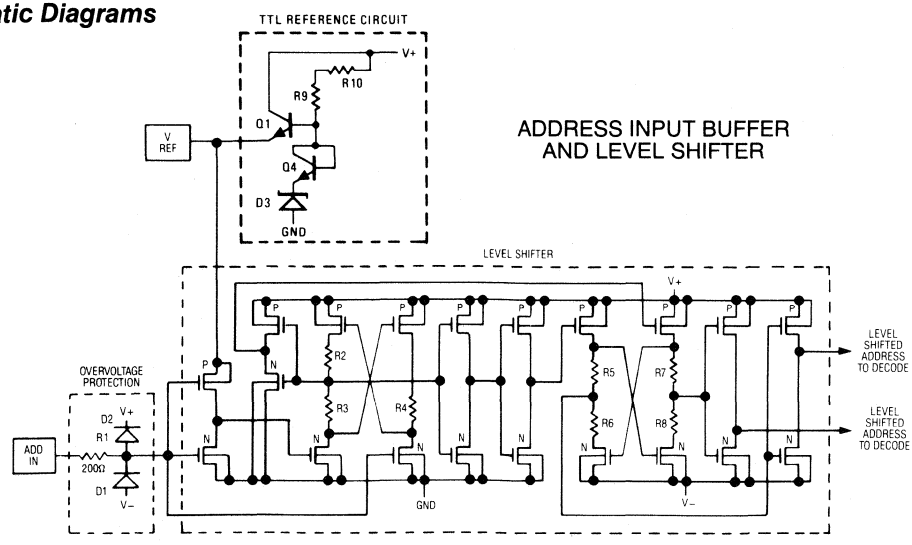


*Similar Connection for HI-547

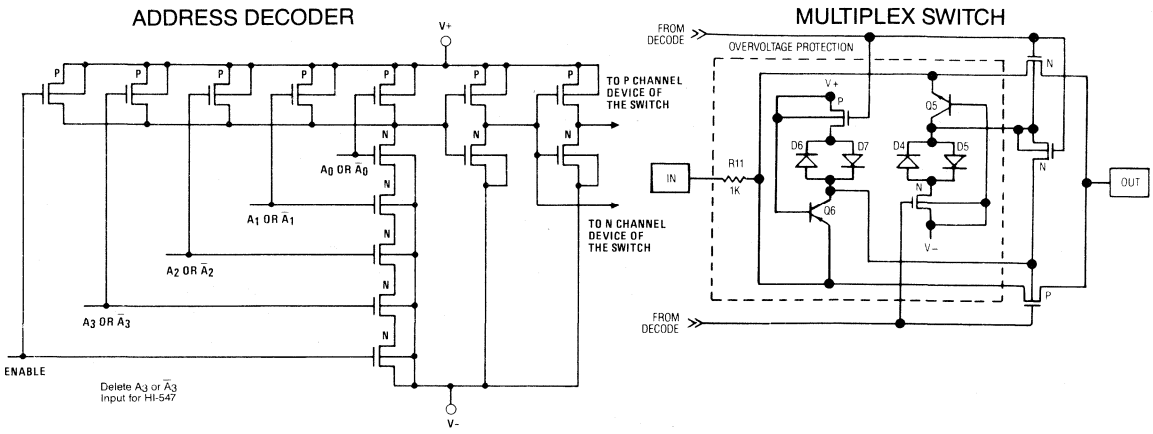
ENABLE DELAY (tON(EN),tOFF(EN))



Schematic Diagrams



Schematic Diagrams (continued)



Die Characteristics

Transistor Count		485
Die Dimensions		159 x 84 mils
Substrate Potential*		$-V_{SUPPLY}$
Process		CMOS-DI
Thermal Constants ($^oC/W$)	θ_{ja}	θ_{jc}
Ceramic DIP	50	18

*The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential.

HI-548/549

Single 8/Differential 4 Channel CMOS Analog Multiplexers with Active Overvoltage Protection

Features

- Analog Overvoltage Protection ..... $70V_{p-p}$
- No Channel Interaction During Overvoltage
- ESD Resistant ..... >4,000V
- Guaranteed RON Matching
- 44V Maximum Power Supply
- Break-Before-Make Switching
- Analog Signal Range ..... ±15V
- Access Time (Typical) 500ns
- Standby Power (Typical) 7.5mW

Applications

- Data Acquisition
- Industrial Controls
- Telemetry

Description

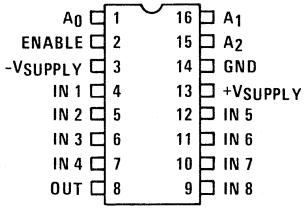
The HI-548 and 549 are analog multiplexers with Active Overvoltage Protection and guaranteed R_{ON} matching. Analog input levels may greatly exceed either power supply without damaging the device or disturbing the signal path of other channels. Active protection circuitry assures that signal fidelity is maintained even under fault conditions that would destroy other multiplexers. Analog inputs can withstand constant 70 volt peak-to-peak levels and typically survive static discharges beyond 4,000 volts. Digital inputs will also sustain continous faults up to 4 volts greater than either supply. In addition, signal sources are protected from short circuiting should multiplexer supply loss occur; each input presents 1kΩ of resistance under this condition. These features make the HI-548 and HI-549 ideal for use in systems where the analog inputs originate from external equipment or separately powered circuitry. Both devices are fabricated with 44 volt dielectrically isolated CMOS technology. The HI-548 is an 8 channel device and the HI-549 is a 4 channel differential version. If input overvoltage protection is not needed, the HI-508 and HI-509 multiplexers are recommended. For further information see Application Notes 520 and 521.

The HI-548/549 are offered in both commercial and military grades. Additional Hi-Rel screening to MIL-STD-883 is available, when specified by the "/883" suffix. For details, request the HI-548/883 or HI-549/883 data sheets.

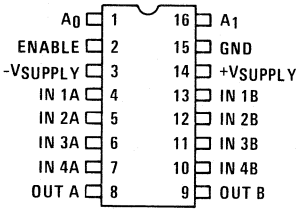
Each device is available in a 16 pin Plastic or Ceramic DIP, and a 20 pin Plastic Leaded Chip Carrier (PLCC).

Pinouts

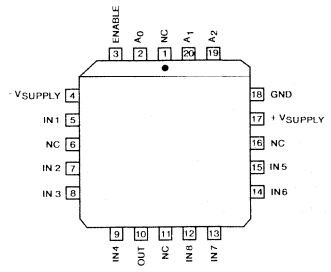
HI1-548 (CERAMIC DIP)
HI3-548 (PLASTIC DIP)
TOP VIEW



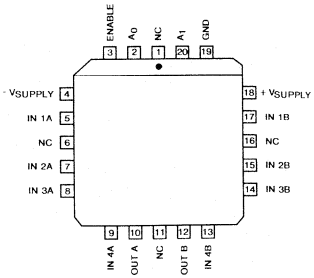
HI1-549 (CERAMIC DIP)
HI3-549 (PLASTIC DIP)
TOP VIEW



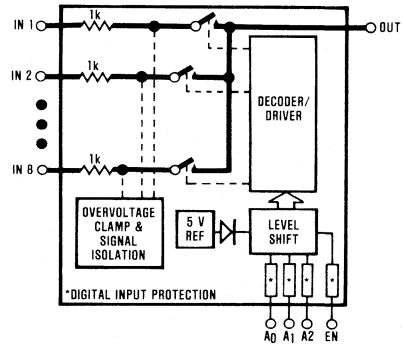
HI4P548 (PLCC)
TOP VIEW



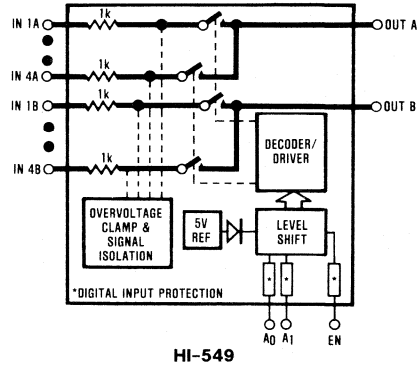
HI4P549 (PLCC)
TOP VIEW



Functional Diagrams



HI-548



HI-549

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

$V_{SUPPLY(+)}$ to $V_{SUPPLY(-)}$ 44V
$V_{SUPPLY(+)}$ to GND 22V
$V_{SUPPLY(-)}$ to GND 25V
Digital Input Overvoltage
$+V_{EN}$, $+V_A$ ..... $+V_{SUPPLY}$ +4V
$-V_{EN}$, $-V_A$ ..... $-V_{SUPPLY}$ -4V
or 20mA, whichever occurs first.
Analog Signal Overvoltage (Note 7)
$+V_S$ ..... $+V_{SUPPLY}$ +20V
$-V_S$ ..... $-V_{SUPPLY}$ -20V
Continuous Current, S or D: 20mA
Peak Current, S or D
(Pulsed at 1ms, 10% duty cycle max): 40mA
Junction Temperature ..... +175°C
Operating Temperature Ranges:
HI-548/549-2 ..... -55°C to +125°C
HI-548/549-4 ..... -25°C to +85°C
HI-548/549-5 ..... 0°C to +75°C
Storage Temperature Range ..... -65°C to +150°C

Electrical Specifications Unless Otherwise Specified:

Supplies = +15V, -15V; V_{AH} (Logic Level High) = +4.0V;
V_{AL} (Logic Level Low) = +0.8V. For Test Conditions, consult Performance Characteristics Section.

PARAMETER	TEMP.	HI-548/HI-549 -2 MIN.	HI-548/HI-549 -2 TYP.	HI-548/HI-549 -2 MAX.	HI-548/549 -4, -5 MIN.	HI-548/549 -4, -5 TYP.	HI-548/549 -4, -5 MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS								
V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
*R_{ON}, On Resistance (Note 2)	+25°C		1.2	1.5		1.5	1.8	kΩ
	Full		1.5	1.8		1.8	2.0	kΩ
$\triangle R_{ON}$, Any Two Channels	+25°C			7.0			7.0	%
I_S (OFF), Off Input Leakage Current (Note 3)	+25°C		0.03			0.03		nA
	Full			50			50	nA
I_D (OFF), Off Output Leakage Current (Note 3)	+25°C		0.1			0.1		nA
HI-548	Full			200			200	nA
HI-549	Full			100			100	nA
$I_{D(OFF)}$ with Input Overvoltage Applied (Note 4)	+25°C		4.0			4.0		nA
	Full			2.0				μA
I_D (ON), On Channel Leakage Current (Note 3)	+25°C		0.1			0.1		nA
HI-548	Full			200			200	nA
HI-549	Full			100			100	nA
I_{DIFF}, Differential Off Output Leakage Current (HI-549 Only)	Full			50			50	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold (Note 8)	Full			0.8			0.8	V
V_{AH}, Input High Threshold	Full	4.0			4.0			V
I_A, Input Leakage Current (High or Low) (Note 5)	Full			1.0			1.0	μA
SWITCHING CHARACTERISTICS								
t_A, Access Time	+25°C		0.5			0.5		μs
	Full			1.0			1.0	μs
t_{OPEN}, Break-Before-Make Delay	+25°C	25	80		25	80		ns
$t_{ON (EN)}$, Enable Delay (ON)	+25°C		300	500		300		ns
	Full			1000			1000	ns
$t_{OFF (EN)}$, Enable Delay (OFF)	+25°C		300	500		300		ns
	Full			1000			1000	ns
Settling Time (0.1%)	+25°C		1.2			1.2		μs
(0.01%)	+25°C		3.5			3.5		μs
"OFF Isolation" (Note 6)	+25°C	50	68		50	68		dB
C_S (OFF), Channel Input Capacitance	+25°C		5			5		pF
C_D (OFF), Channel Output Capacitance HI-548	+25°C		25			25		pF
HI-549	+25°C		12			12		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
C_{DS} (OFF), Input to Output Capacitance	+25°C		0.1			0.1		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full		7.5			7.5		mW
I+, Current (Note 7)	Full		0.5	2.0		0.5	2.0	mA
I−, Current (Note 7)	Full		0.02	1.0		0.02	1.0	mA

TRUTH TABLES

HI-548

A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-549

A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	L	NONE
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

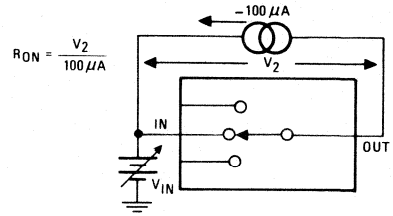
NOTES:
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. V_{OUT} = ±10V, I_{OUT} = -100μA.
3. Ten nanoamps is the practical lower limit for high speed measurement in the production test environment.
4. Analog Overvoltage = ±33V.
5. Digital input leakage is primarily due to the clamp diodes (see Schematic). Typical leakage is less than 1nA at 25°C.
6. V_{EN} = 0.8V, R_L = 1K, C_L = 15pF, V_S = 7V_{RMS}, f = 100kHz. Worst case isolation occurs on channel 4 due to proximity of the output pins.
7. V_{EN}, V_A = 0V or 4.0V.
8. To drive from DTL/TTL Circuits, 1kΩ pull-up resistors to +5.0V_{SUPPLY} are recommended.

Performance Characteristics and Test Circuits

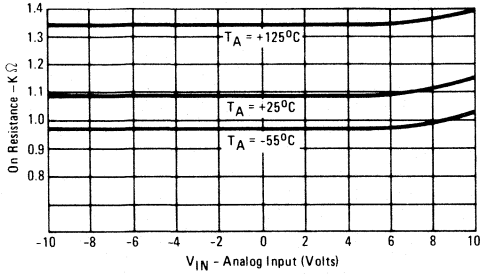
Unless Otherwise Specified T_A = 25°C, V_{Supply} = ±15 V, V_{AH} = +4 V, V_{AL} = 0.8 V

ON RESISTANCE vs. INPUT SIGNAL LEVEL, SUPPLY VOLTAGE

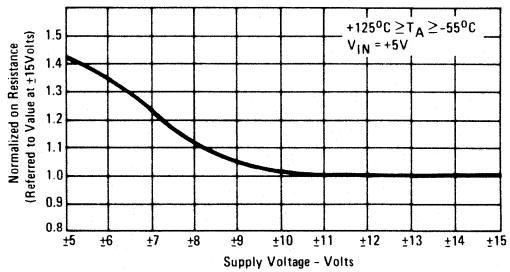
TEST CIRCUIT NO. 1



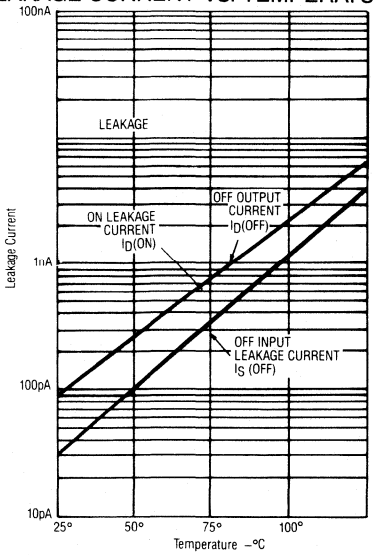
ON RESISTANCE vs. ANALOG INPUT VOLTAGE



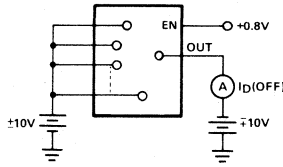
NORMALIZED ON RESISTANCE vs. SUPPLY VOLTAGE



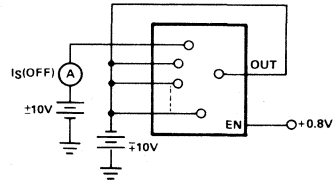
LEAKAGE CURRENT VS. TEMPERATURE



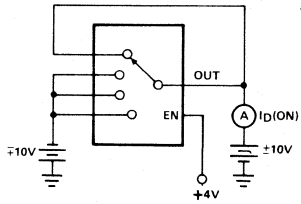
TEST CIRCUIT NO. 2*



TEST CIRCUIT NO. 3*

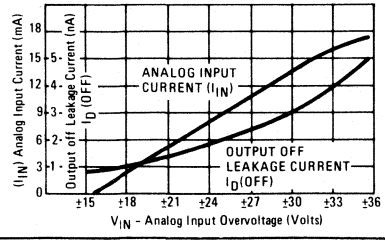


TEST CIRCUIT NO. 4*



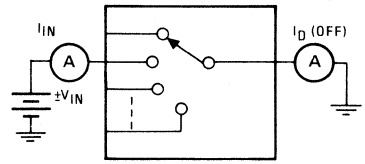
***Two measurements per channel: +10 V/−10 V and −10 V/+10 V. (Two measurements per device for $I_{D(OFF)}$: +10 V/−10 V and −10 V/+10 V.)**

ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



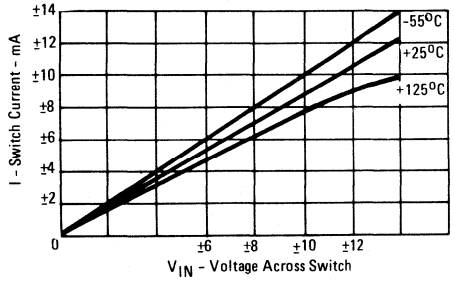
TEST CIRCUIT NO. 5

ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



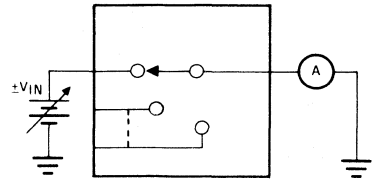
Performance Characteristics and Test Circuits (continued)

ON CHANNEL CURRENT vs. VOLTAGE

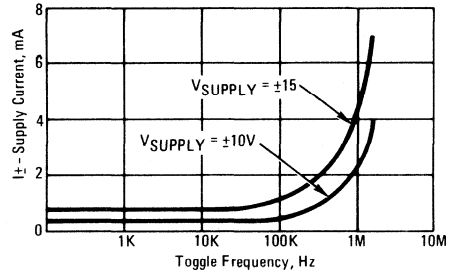


TEST CIRCUIT NO. 6

ON CHANNEL CURRENT vs. VOLTAGE

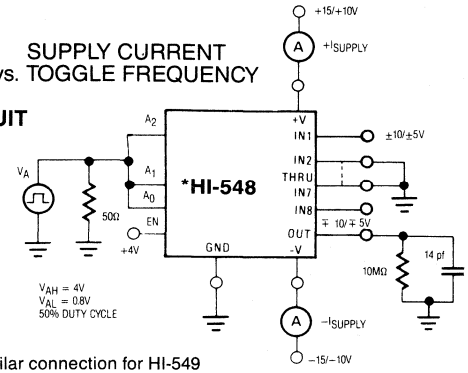


SUPPLY CURRENT vs. TOGGLE FREQUENCY



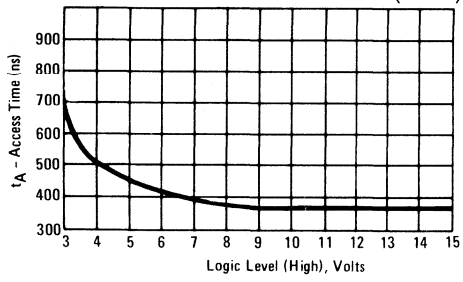
TEST CIRCUIT NO. 7

SUPPLY CURRENT vs. TOGGLE FREQUENCY



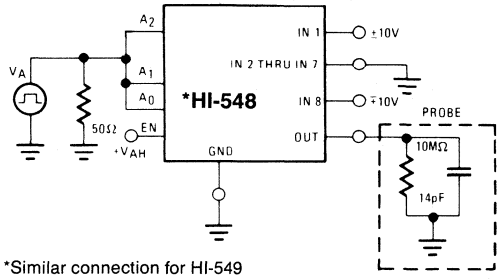
*Similar connection for HI-549

ACCESS TIME VS. LOGIC LEVEL (HIGH)



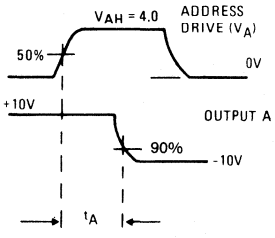
TEST CIRCUIT NO. 8

ACCESS TIME vs. LOGIC LEVEL (HIGH)

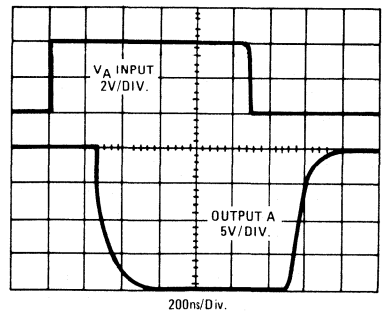


*Similar connection for HI-549

Switching Waveforms



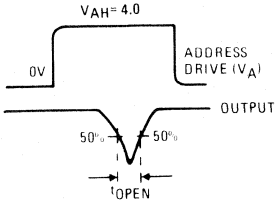
ACCESS TIME

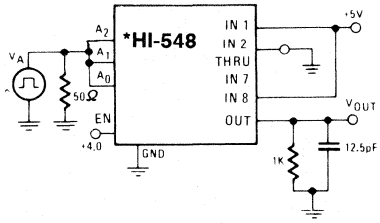


Switching Waveforms (continued)

TEST CIRCUIT NO. 9

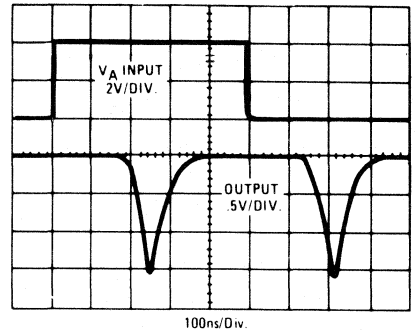
BREAK-BEFORE-MAKE DELAY(tOPEN)





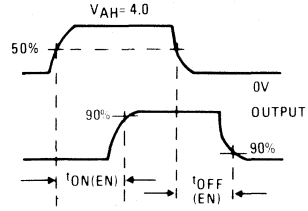
*Similar connection for HI-549

BREAK-BEFORE-MAKE DELAY (tOPEN)

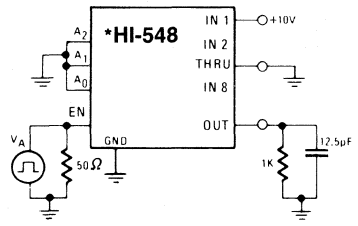


TEST CIRCUIT NO. 10

ENABLE DRIVE

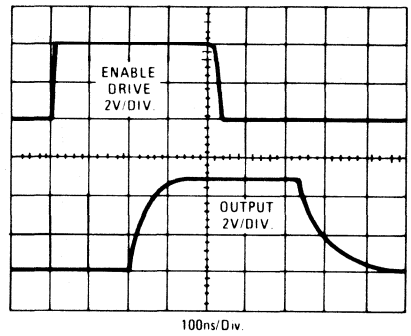


ENABLE DELAY (tON(EN),tOFF(EN))

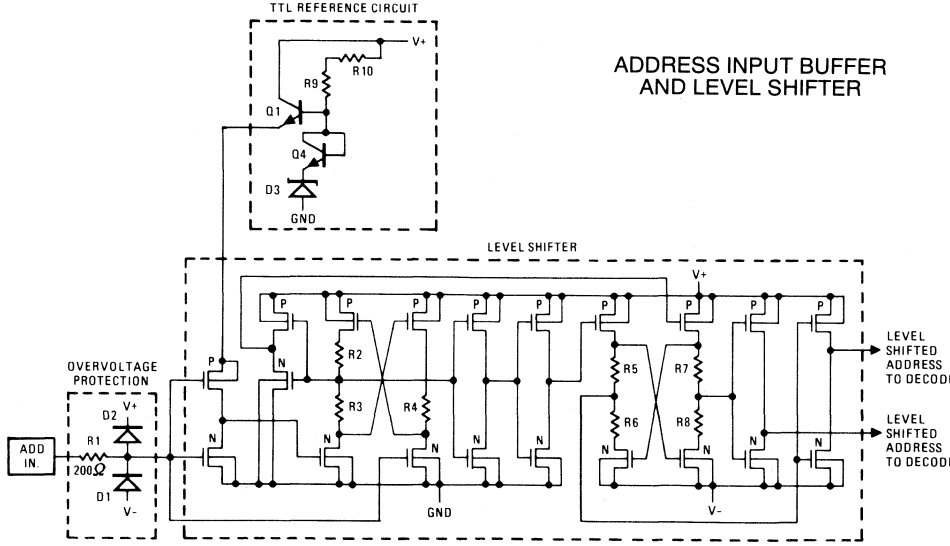


*Similar connection for HI-549

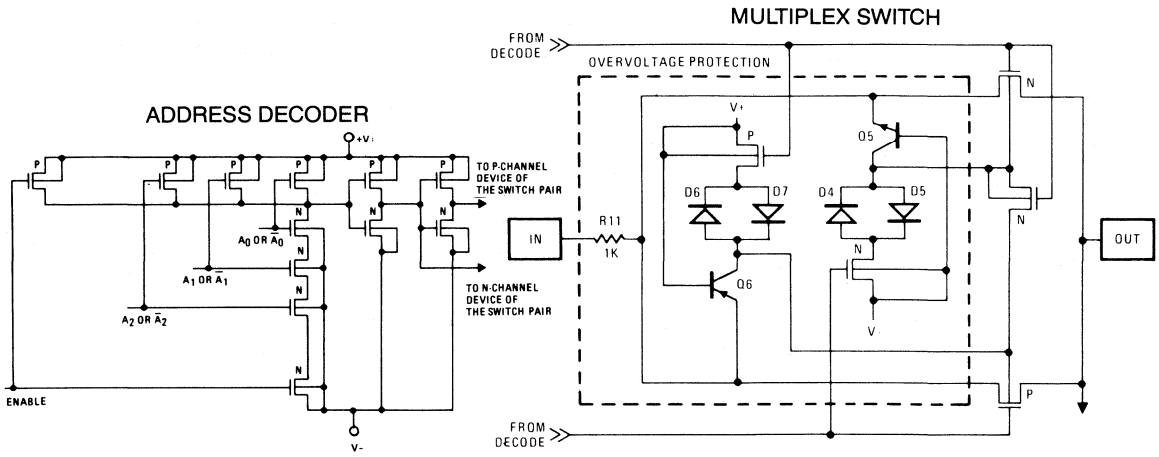
ENABLE DELAY (tON(EN),tOFF(EN))



Schematic Diagrams



Schematic Diagrams (continued)



Die Characteristics

Transistor Count		253
Die Dimensions		108 x 83 mils
Substrate Potential*		$-V_{SUPPLY}$
Process		CMOS-DI
Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
Ceramic DIP	104	35
Plastic DIP	75	23

*The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential.

HI-1818A/1828A

Low Resistance Single 8/Differential 4 Channel CMOS Analog Multiplexers

Features

- Signal Range ..... ±15V
- "ON" Resistance (Typ.) 250Ω
- Input Leakage (Max) 50nA
- Access Time (Typ.) 350ns
- Power Consumption (Typ.) 5mW
- DTL/TTL Compatible Address
- -55°C to +125°C Operation

Applications

- Data Acquisition Systems
- Precision Instrumentation
- Demultiplexing
- Selector Switch

Description

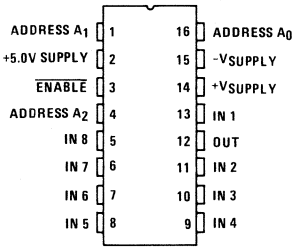
The HI-1818A/1828A are monolithic high performance CMOS analog multiplexers offering built-in channel selection decoding plus an inhibit (enable) input for disabling all channels. Dielectric Isolation (DI) processing is used for enhanced reliability and performance (see Application Note 521). Substrate leakage and parasitic capacitance are much lower, resulting in extremely low static errors and high throughput rates. Low output leakage (typically 0.1nA) and low channel ON resistance (250Ω) assure optimum performance in low level or current mode applications.

The HI-1818A is a single-ended 8 channel multiplexer, while the HI-1828A is a differential 4 channel version. Either device is ideally suited for medical instrumentation, telemetry systems, and microprocessor based data acquisition systems.

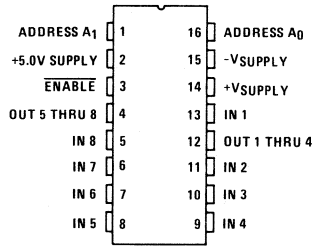
The HI-1818A/1828A is offered in a 16 pin Ceramic or Plastic DIP and a 20 pin Plastic Leaded Chip Carrier (PLCC). For MIL-STD-883 compliant parts, request the HI-1818A/883; HI-1828A/883 data sheet.

Pinouts

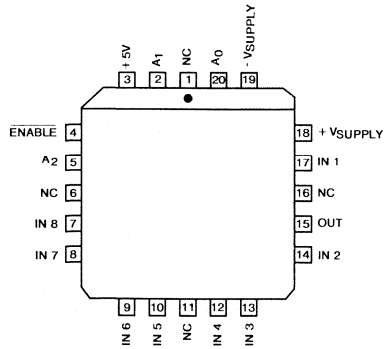
HI-1818A CERAMIC/PLASTIC DIP
TOP VIEW



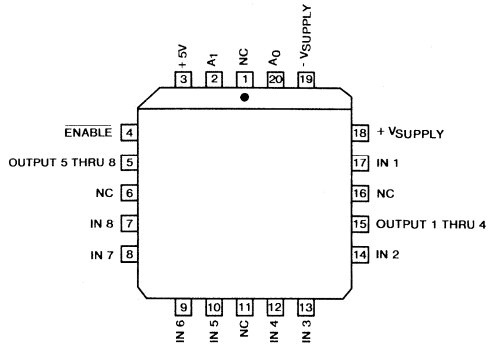
HI-1828A CERAMIC/PLASTIC DIP
TOP VIEW



HI-1818A PLASTIC LEADED CHIP CARRIER
TOP VIEW



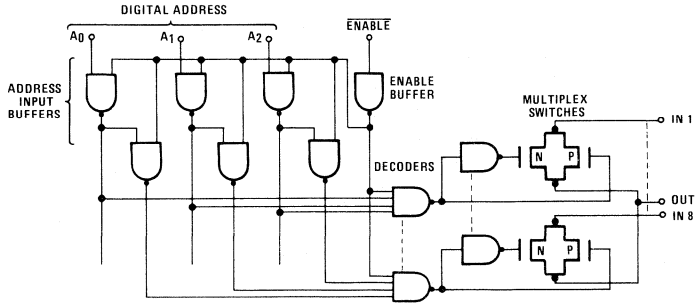
HI-1828A PLASTIC LEADED CHIP CARRIER
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Functional Diagrams

HI-1818A

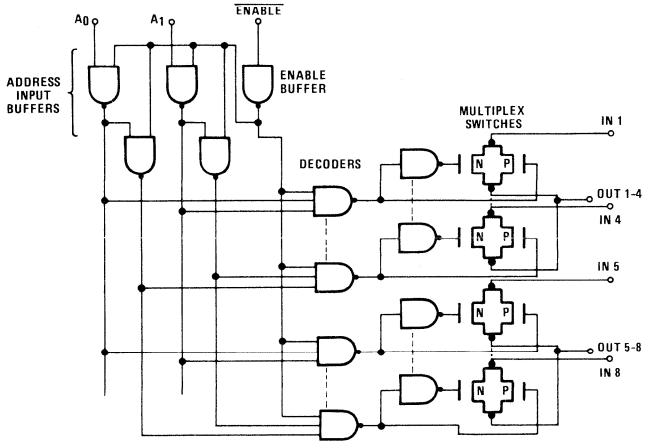


TRUTH TABLES

HI-1818A

ADDRESS A_2	A_1	A_0	$\overline{EN}$	"ON" CHANNEL
L	L	L	L	1
L	L	H	L	2
L	H	L	L	3
L	H	H	L	4
H	L	L	L	5
H	L	H	L	6
H	H	L	L	7
H	H	H	L	8
X	X	X	H	NONE

HI-1828A



HI-1828A

ADDRESS A_1	A_0	$\overline{EN}$	"ON" CHANNELS
L	L	L	1 and 5
L	H	L	2 and 6
H	L	L	3 and 7
H	H	L	4 and 8
X	X	H	NONE

Die Characteristics

Transistor Count 210

Die Dimensions ..... 67.7 x 103.5 mils

Substrate Potential* ..... $-V_{SUPPLY}$

Process: ..... CMOS-DI

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
Ceramic DIP	111	41
Plastic DIP	81	33

*The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential.

Absolute Maximum Ratings (Note 1)

Voltage Between Supply Pins 40.0V
Logic Supply Voltage 30.0V
Analog Input Voltage:
$+V_{IN}$ ..... $+V_{SUPPLY}$ +2V
$-V_{IN}$ ..... $-V_{SUPPLY}$ -2V
Junction Temperature (Max) ..... 175°C

Storage Temperature Range ..... -65°C to +150°C
Digital Input Voltage ..... $-V_{SUPPLY}$ to $+V_{SUPPLY}$
Operating Temperature Ranges:
HI-1818A/1828A-2, -8 ..... -55°C to +125°C
HI-1818A/1828A-5 ..... 0°C to 75°C

Electrical Specifications

Unless Otherwise Specified: Supplies = +15V, -15V, +5V; V_{AL} = 0.4V, V_{AH} = 4.0V, V_{IN} = 0.8V

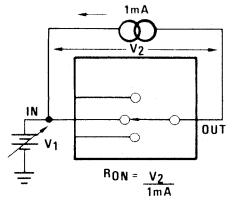
PARAMETER	TEMP	HI-1818A/1828A -2, -8 MIN	HI-1818A/1828A -2, -8 TYP	HI-1818A/1828A -2, -8 MAX	HI-1818A/1828A -5 MIN	HI-1818A/1828A -5 TYP	HI-1818A/1828A -5 MAX	UNITS
ANALOG CHANNEL CHARACTERISTICS								
*V_{IN}, Analog Signal Range	Full	-15		+15	-15		+15	V
*R_{ON}, ON Resistance (Note 2)	+25°C		250	400		250	400	Ω
	Full			500			500	Ω
*I_S(OFF), Input Leakage Current	Full			50			50	nA
*I_D(ON), On Channel Leakage Current								
(HI-1818A)	Full			250			250	nA
(HI-1828A)	Full			125			125	nA
I_D(OFF) Output Leakage Current								
(HI-1818A)	Full			250			250	nA
(HI-1828A)	Full			125			125	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full			0.4			0.4	V
V_{AH}, Input High Threshold (Note 3)	Full	4.0			4.0			V
I_A, Input Leakage Current	Full			1			1	μA
SWITCHING CHARACTERISTICS								
T_S, Access Time (Note 4)	+25°C		350	500		350		ns
	Full			1000			1000	ns
Break-Before-Make Delay	+25°C		25			100		ns
Settling Time (0.1%)	+25°C		1.08			1.08		μs
(0.025%)	+25°C		2.8			2.8		μs
C_{IN}, Channel Input Capacitance	+25°C		4			4		pF
C_{OUT}, Channel Output Capacitance								
(HI-1818A)	+25°C		20			20		pF
(HI-1828A)	+25°C		10			10		pF
C_{DS}(OFF), Drain-To-Source Capacitance	+25°C		0.6			0.6		pF
C_D, Digital Input Capacitance	+25°C		5			5		pF
t_{ON}(EN), Enable Delay (ON)	+25°C		300	500		300		ns
	Full			1000			1000	ns
t_{OFF}(EN), Enable Delay (OFF)	+25°C		300	500		300		ns
	Full			1000			1000	ns
POWER REQUIREMENTS								
P_D, Power Dissipation	Full			27.5			27.5	mW
*I+, Current	Full			0.5			0.5	mA
*I-, Current	Full			1			1	mA
*I_L, Current	Full			1			1	mA

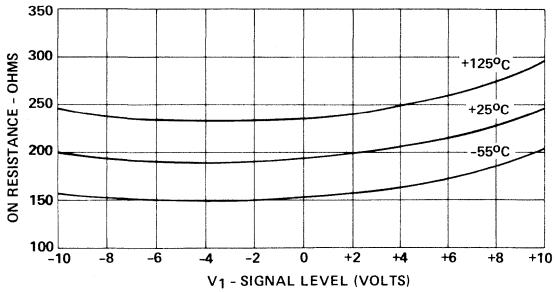
*100% Tested for Dash 8. Leakage currents not tested at -55°C.

NOTES:
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. V_{OUT} = ±10V, I_{OUT} = -1mA.
3. To drive from DTL/TTL circuits, 1kΩ pull-up resistors to +5.0V supply are recommended.
4. Time measured to 90% of final output level; V_{OUT} = -5.0V to +5.0V, Digital Inputs = 0V to +4.0V.

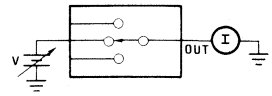
Performance Characteristics

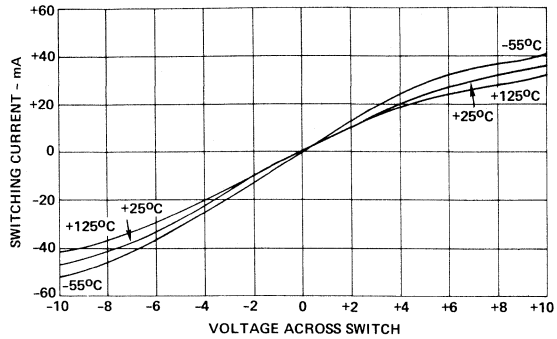
ON RESISTANCE vs. ANALOG SIGNAL LEVEL





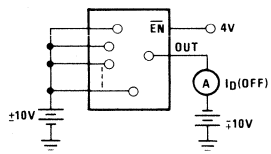
ON CHANNEL CURRENT vs. VOLTAGE

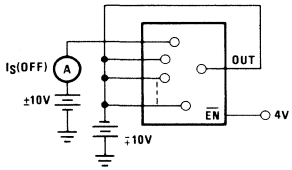




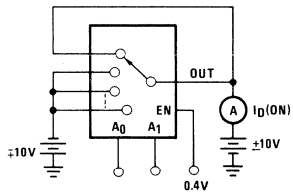
LEAKAGE CURRENTS vs. TEMPERATURE *

OFF LEAKAGE

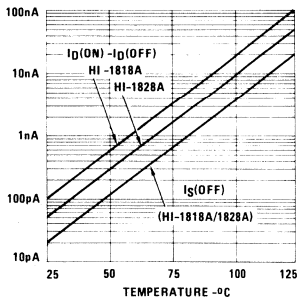




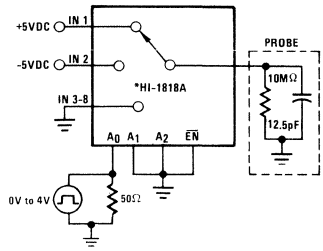
ON LEAKAGE



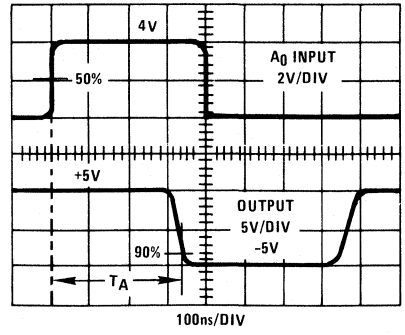
*Two measurements per channel: +10V/-10V and -10V/+10V. (Two measurements per device for $I_{D(OFF)}$: +10V/-10V and -10V/+10V).



ACCESS TIME

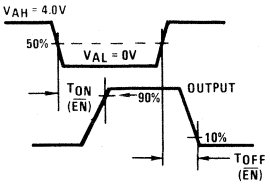


*Similar connection for HI-1828A.

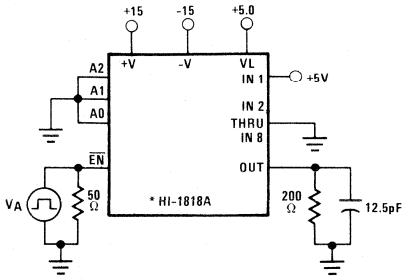


Switching Waveforms

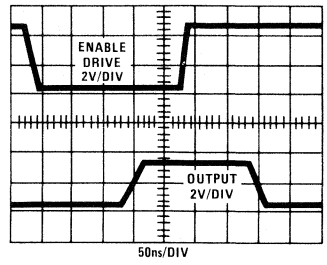
ENABLE DRIVE



ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)

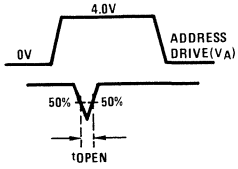


ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)

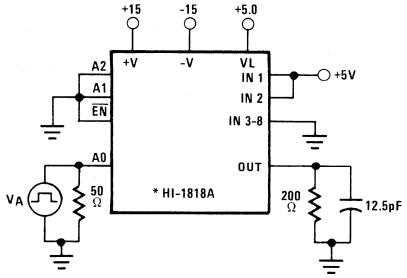


*Similar Connection For HI-1828A

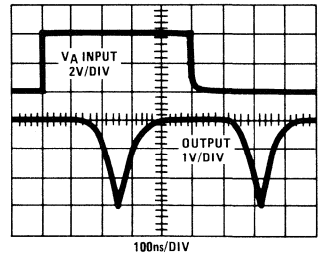
ADDRESS DRIVE



BREAK-BEFORE-MAKE DELAY (t_{OPEN})



BREAK-BEFORE-MAKE DELAY (t_{OPEN})

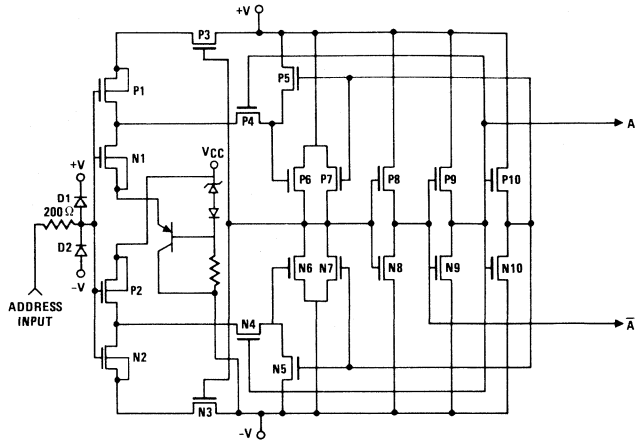


*Similar Connection For HI-1828A

Schematic Diagrams

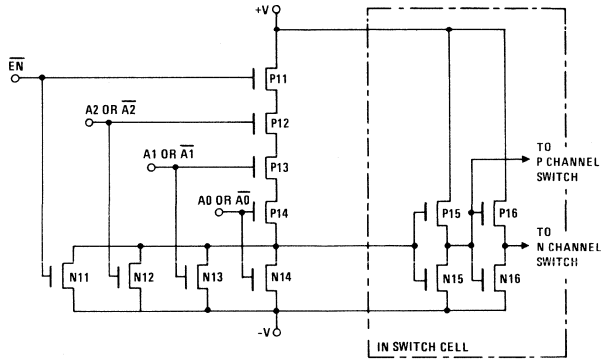
ADDRESS INPUT BUFFER

All N-Channel Bodies to V-
All P-Channel Bodies to V+
Unless Otherwise Indicated



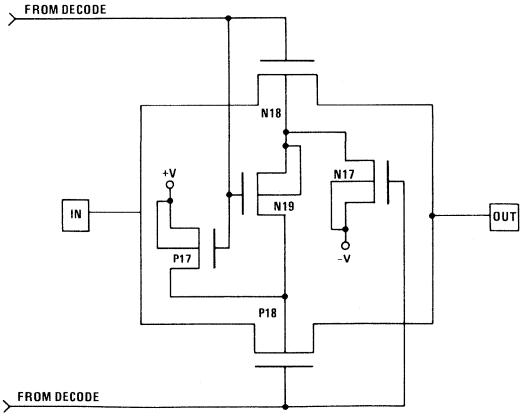
ADDRESS DECODER

All N-Channel Bodies to V-
All P-Channel Bodies to V+
A_2 or $\overline{A_2}$ not used for HI-1828A



MULTIPLEXER SWITCH

All N-Channel Bodies to V-
All P-Channel Bodies to V+
Unless Otherwise Indicated



ANALOG

Analog-to-Digital Converters

5

ABSOLUTE MAXIMUM RATINGS

As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Specifications" are the only conditions recommended for satisfactory operation.

Ordering Information

HARRIS PRODUCT CODE EXAMPLE

H I 1 — 574A — 5

PREFIX:
H (HARRIS)

FAMILY:
A : Analog
C : Communications
D : Digital
F : Filters
I : Interface
M : Memory
V : Analog High Voltage
Y : Analog Hybrids

PACKAGE:
1 : Dual-In-Line Ceramic
2 : Metal Can
3 : Dual-In-Line Plastic
4 : Leadless Chip Carriers (LCC)
5 : LCC Hybrid
7 : Mini-DIP, Ceramic
0 : Chip Form

PART NUMBER

TEMPERATURE:
1 : 0°C to +200°C *
2 : -55°C to +125°C
4 : -25°C to +85°C
5 : 0°C to +75°C
6 : 100% +25°C Probe (Dice Only)
7 : Dash-7 High Reliability Commercial Product 0°C to +75°C
8 : Dash-8 Program HA2-2520-8 (Example Only)
9 : -40°C to +85°C

* Special High Temperature Testing Available on Certain Product Types. Consult Factory for Availability.

Standard Products Packaging Availability†

PACKAGE	CERAMIC DIP			SURFACE MOUNT LCC
TEMPERATURE	**-5**	**-2**	**-8**	**-8**
DEVICE NUMBER				
ANALOG TO DIGITAL				
HI-574A	K	K	K	*
HI-674A	K	K	K	*
HI-774	K	K		

* Available as MIL-STD-883 Only.
† Letter codes in this chart indicate available packages as shown in Packaging Section 11.

Selection Guide

A/D CONVERTERS

PART NUMBER	RESOLUTION BITS	TEMPERATURE RANGE -55°C TO +125°C	TEMPERATURE RANGE 0°C TO +75°C	TEMPERATURE RANGE -40°C TO +85°C	PACKAGE	NON-LINEARITY MAX. 25°C (LSB)	DIFFERENTIAL NON-LINEARITY * MAX. 25°C	GAIN DRIFT ppm/°C MAX. FULL TEMP	CONVERSION SPEED (µs) (INTERNAL CLOCK) 12-BITS	CONVERSION SPEED (µs) (INTERNAL CLOCK) 8-BITS	PAGE
HI-574AJD			X			±1	11-Bits	±45			
HI-574AKD			X			±1/2	12-Bits	±25			
HI-574ALD	12		X		28 Pin	±1/2	12-Bits	±10	20	13	5-4
HI-574ASD		X			Cerdip	±1	11-Bits	±50			
HI-574ATD		X				±1/2	12-Bits	±25			
HI-674AJD			X			±1	11-Bits	±45			
HI-674AKD			X			±1/2	12-Bits	±25			
HI-674ALD	12		X		28 Pin	±1/2	12-Bits	±10	12	8	5-15
HI-674ASD		X			Cerdip	±1	11-Bits	±50			
HI-674ATD		X				±1/2	12-Bits	±25			
HI-774J	12		X			±1	11-Bits	±45	8.0	6.4	5-26
HI-774K			X		28 Pin	±1/2	12-Bits	±25			
HI-774S	12	X			Cerdip	±1	11-Bits	±50	9.0	6.8	
HI-774T		X				±1/2	12-Bits	±25			

* Maximum resolution with no missing codes guaranteed.

HARRIS

HI-574A

Fast, Complete 12-Bit A/D Converter with Microprocessor Interface

Features

- Complete 12-Bit A/D Converter with Reference and Clock
- Full 8-, 12- or 16-Bit Microprocessor Bus Interface
- 150ns Bus Access Time
- No Missing Codes Over Temperature
- Minimal Set-up Time for Control Signals
- 25μs Maximum Conversion Time
- Low Noise, via Current-Mode Signal Transmission Between Chips
- Byte Enable/Short Cycle (A_0 Input)
  - Guaranteed Break-Before-Make Action, Eliminating Bus Contention During Read Operation. Latched by the Start Convert Input (To Set the Conversion Length)
- Improved Second Source for AD574A and HS574
- $\pm$12V to $\pm$15V Operation

Applications

- Military and Industrial Data Acquisition Systems
- Electronic Test and Scientific Instrumentation
- Process Control Systems

Description

The HI-574A is a complete 12-bit Analog-to-Digital Converter, including a +10V reference, clock, three-state outputs and a digital interface for microprocessor control. Successive approximation conversion is performed by two monolithic dice housed in a 28 pin package. The bipolar analog die features the Harris Dielectric Isolation process, which provides enhanced AC performance and freedom from latch-up.

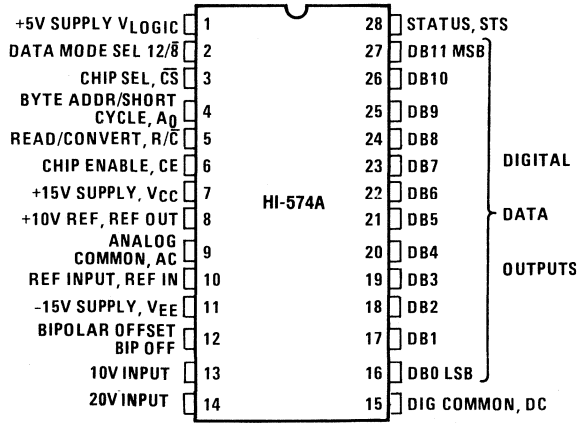
Custom design of each IC (bipolar analog and CMOS digital) has yielded improved performance over existing versions of this converter. The voltage comparator features high PSRR plus a high speed current-mode latch, and provides precise decisions down to 0.1 LSB of input overdrive. More than 2X reduction in noise has been achieved by using current instead of voltage for transmission of all signals between the analog and digital IC's. Also, the clock oscillator is current-controlled for excellent stability over temperature. The oscillator is trimmed for a nominal conversion time of 20 $\pm$ 1μs.

The HI-574A offers standard unipolar and bipolar input ranges, laser trimmed for specified linearity, gain and offset accuracy. The buried zener reference circuit is trimmed for minimum temperature coefficient.

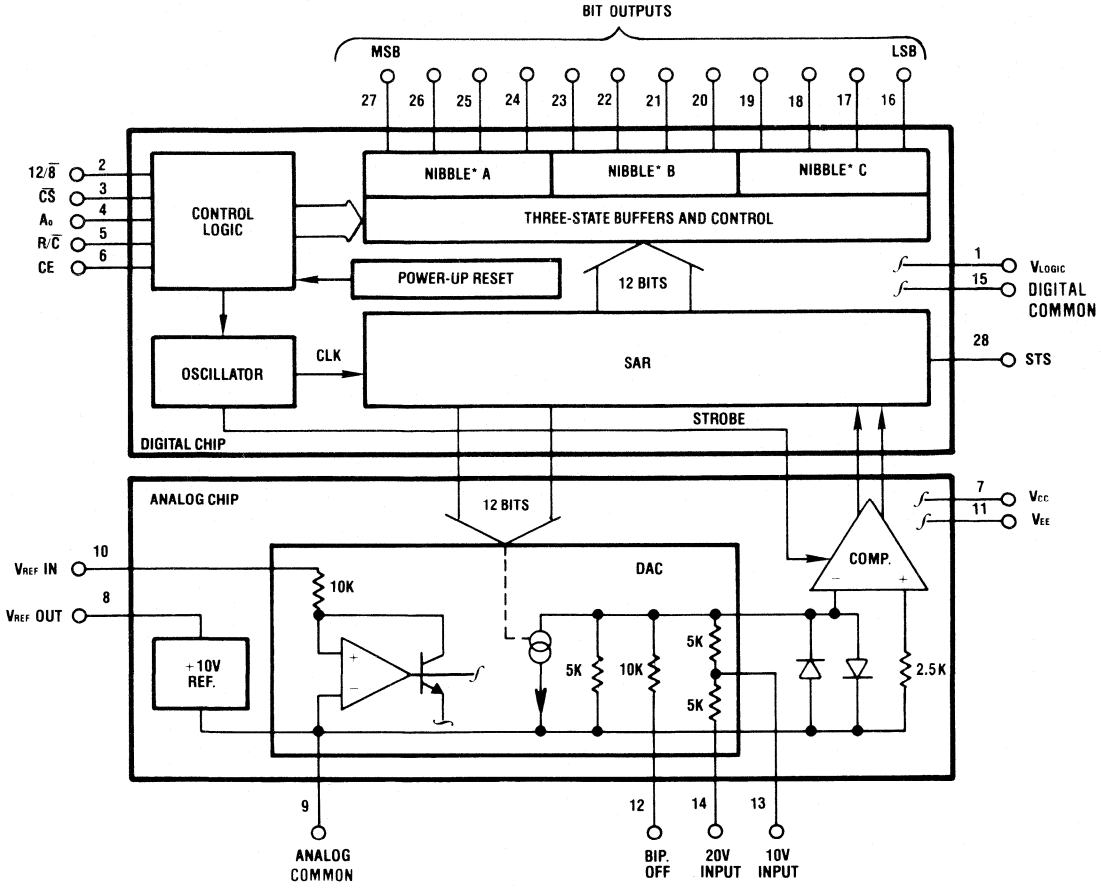
Power requirements are +5V and $\pm$12V to $\pm$15V, with typical dissipation of 385mW at $\pm$12V. All models are available in a 28 pin Sidebrazed DIP. For additional Hi-Rel screening including 160 hour burn-in, specify the "-8" suffix. For MIL-STD-883 compliant parts, request the HI-574A/883 data sheet.

Pinouts

SIDEBRAZE DIP
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.



*("NIBBLE" IS A 4 BIT DIGITAL WORD.)

(Typical @ +25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = −15V or −12V unless otherwise specified)

DC and Transfer Accuracy Specifications

MODEL	HI-574AJ	HI-574AK	HI-574AL	UNITS
Temperature Range		-5		
Resolution (max)	12	12	12	Bits
Linearity Error				
25°C (max)	±1	±1/2	±1/2	LSB
0°C to +75°C (max)	±1	±1/2	±1/2	LSB
Differential Linearity Error (Maximum resolution for which no missing codes is guaranteed)				
25°C	11	12	12	Bits
T_{min} to T_{max}	11	12	12	Bits
Unipolar Offset (max) (Adjustable to zero)	±2	±2	±2	LSB
Bipolar Offset (max) (Adjustable to zero)	±10	±4	±4	LSB
Full Scale Calibration Error				
25°C (max), with fixed 50 Ω resistor from REF OUT to REF IN (Adjustable to zero)	0.3	0.3	0.3	% of F.S.
T_{min} to T_{max}				
(No adjustment at +25°C)	0.5	0.4	0.35	% of F.S.
(With adjustment to zero at +25°C)	0.22	0.12	0.05	% of F.S.
Temperature Coefficients				
Guaranteed max change, T_{min} to T_{max} (Using internal reference)				
Unipolar Offset	±2	±1	±1	LSB
	(10)	(5)	(5)	(ppm/°C)
Bipolar Offset	±2	±1	±1	LSB
	(10)	(5)	(5)	(ppm/°C)
Full Scale Calibration	±9	±5	±2	LSB
	(45)	(25)	(10)	(ppm/°C)
Power Supply Rejection				
Max change in Full Scale Calibration				
+13.5V<V_{CC}<+16.5V or +11.4V<V_{CC}<+12.6V	±2	±1	±1	LSB
+4.5V<V_{LOGIC}<+5.5V	±1/2	±1/2	±1/2	LSB
−16.5V<V_{EE}<−13.5V or −12.6V<V_{EE}<−11.4V	±2	±1	±1	LSB
Analog Inputs				
Input Ranges				
Bipolar	−5 to +5			Volts
	−10 to +10			Volts
Unipolar	0 to +10			Volts
	0 to +20			Volts
Input Impedance				
10 Volt Span	5K, ± 25%			Ohms
20 Volt Span	10K, ± 25%			Ohms
Power Supplies				
Operating Voltage Range				
V_{LOGIC}	+4.5 to +5.5			Volts
V_{CC}	+11.4 to +16.5			Volts
V_{EE}	−11.4 to −16.5			Volts
Operating Current				
I_{LOGIC}	7 TYP, 15 MAX			mA
I_{CC} +15V Supply	11 TYP, 15 MAX			mA
I_{EE} -15V Supply	21 TYP, 28 MAX			mA
Power Dissipation				
±15V, +5V	515 TYP, 720 MAX			mW
±12V, +5V	385 TYP			mW
Internal Reference Voltage, T_{min} to T_{max}	+10.00 ± 0.5 MAX			Volts
Output current,[1] available for external loads (External load should not change during conversion).	2.0 MAX			mA

1. *When supplying an external load (not including the ADC) and operating on* ±12V supplies, a buffer amplifier must be provided for the Reference Output.

(Typical @ +25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = −15V or −12V unless otherwise specified)

DC and Transfer Accuracy Specifications

MODEL	HI-574AS	HI-574AT	UNITS
Temperature Range	-2, -8		
Resolution (max)	12	12	Bits
Linearity Error			
25°C (max)	±1	±1/2	LSB
−55°C to +125°C (max)	±1	±1	LSB
Differential Linearity Error (Maximum resolution for which no missing codes is guaranteed)			
25°C	11	12	Bits
T_{min} to T_{max}	11	12	Bits
Unipolar Offset (max) (Adjustable to zero)	±2	±2	LSB
Bipolar Offset (max) (Adjustable to zero)	±10	±4	LSB
Full Scale Calibration Error			
25°C (max), with fixed 50 Ω resistor from REF OUT to REF IN (Adjustable to zero)	0.3	0.3	% of F.S.
T_{min} to T_{max}			
(No adjustment at +25°C)	0.8	0.6	% of F.S.
(With adjustment to zero at +25°C)	0.5	0.25	% of F.S.
Temperature Coefficients			
Guaranteed max change, T_{min} to T_{max} (Using internal reference)			
Unipolar Offset	±2	±1	LSB
	(5)	(2.5)	(ppm/°C)
Bipolar Offset	±4	±2	LSB
	(10)	(5)	(ppm/°C)
Full Scale Calibration	±20	±10	LSB
	(50)	(25)	(ppm/°C)
Power Supply Rejection			
Max change in Full Scale Calibration			
+13.5V<V_{CC}<+16.5V or +11.4V<V_{CC}<+12.6V	±2	±1	LSB
+4.5V<V_{LOGIC}<+5.5V	±1/2	±1/2	LSB
−16.5V<V_{EE}<−13.5V or −12.6V<V_{EE}<−11.4V	±2	±1	LSB
Analog Inputs			
Input Ranges			
Bipolar	−5 to +5		Volts
	−10 to +10		Volts
Unipolar	0 to +10		Volts
	0 to +20		Volts
Input Impedance			
10 Volt Span	5K Ω, ± 25%		Ohms
20 Volt Span	10K Ω, ± 25%		Ohms
Power Supplies			
Operating Voltage Range			
V_{LOGIC}	+4.5 to +5.5		Volts
V_{CC}	+11.4 to +16.5		Volts
V_{EE}	−11.4 to −16.5		Volts
Operating Current			
I_{LOGIC}	7 TYP, 15 MAX		mA
I_{CC} +15V Supply	11 TYP, 15 MAX		mA
I_{EE} -15V Supply	21 TYP, 28 MAX		mA
Power Dissipation			
±15V, +5V	515 TYP, 720 MAX		mW
±12V, +5V	385 TYP		mW
Internal Reference Voltage, T_{min} to T_{max}	+10.00 ±.05 MAX		Volts
Output current,[1] available for external loads (External load should not change during conversion).	2.0 MAX		mA

1. *When supplying an external load (not including the ADC) and operating on* ±12V supplies, a buffer amplifier must be provided for the Reference Output.

DIGITAL CHARACTERISTICS[1]
(ALL MODELS, OVER FULL TEMP. RANGE)

	MIN	TYP	MAX
Logic Inputs (CE, $\overline{CS}$, R/$\overline{C}$, AO, 12/$\overline{8}$)[2]			
Logic "1"	+2.4V		+5.5V
Logic "0"	−0.5V		+0.8V
Current	−5μA	±0.1μA	+5μA
Capacitance		5pF	
Logic Outputs (DB11-DB0, STS)			
Logic "0" (I_{SINK} — 1.6mA)			+0.4V
Logic "1" (I_{SOURCE} — 500μA)	+2.4V		
Leakage (High - Z State, DB11-DB0 ONLY)	−5μA	±0.1μA	+5μA
Capacitance		5pF	

[1] *See "HI-574A Timing Specifications" for a detailed listing of digital timing parameters.*

[2] *Although this guaranteed threshold is higher than standard TTL (+2.0V), bus loading is much less, i.e., typical input current is only 0.25% of a TTL load.*

Absolute Maximum Ratings

(Specifications apply to all grades, except where noted)

V_{CC} to Digital Common ..... 0 to +16.5V
V_{EE} to Digital Common ..... 0 to −16.5V
V_{LOGIC} to Digital Common ..... 0 to +7V
Analog Common to Digital Common ..... ±1V
Control Inputs (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$) to
Digital Common ..... −0.5V to V_{LOGIC} +0.5V
Analog Inputs (REF IN, BIP OFF, $10V_{IN}$) to
Analog Common ..... ±16.5V
$20V_{IN}$ to Analog Common ..... ±24V
REF OUT ..... Indefinite short to common
Momentary short to V_{CC}
Junction Temperature ..... 175°C
Lead Temperature, Soldering ..... 300°C, 10 sec.
Storage Temperature ..... −65°C to +150°C

*Derate 20.8mW/°C above 75°C

HI-574A Ordering Guide

MODEL	TEMP. RANGE	LINEARITY ERROR MAX (T_{MIN} to T_{MAX})	RESOLUTION (NO MISSING CODES, T_{MIN} to T_{MAX})	FULL SCALE TC (PPM/°C MAX)
HI1-574AJD-5	0 to 75°C	±1 LSB	11 Bits	45.0
HI1-574AKD-5	0 to 75°C	±1/2 LSB	12 Bits	25.0
HI1-574ALD-5	0 to 75°C	±1/2 LSB	12 Bits	10.0
HI1-574ASD-2	−55 to +125°C	±1 LSB	11 Bits	50.0
HI1-574ASD-8*	−55 to +125°C	±1 LSB	11 Bits	50.0
HI1-574ATD-2	−55 to +125°C	±1 LSB	12 Bits	25.0
HI1-574ATD-8*	−55 to +125°C	±1 LSB	12 Bits	25.0

** The MIL-STD-883 data sheet is available on request*

Definitions of Specifications

LINEARITY ERROR

Linearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale". The point used as "zero" occurs ½LSB (1.22mV for 10 volt span) before the first code transition (all zeros to only the LSB "on"). "Full scale" is defined as a level 1½LSB beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The HI-574AK, AL, AT, and AU grades are guaranteed for maximum nonlinearity of ±½LSB. For these grades, this means that an analog value which falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The HI-574AJ and AS grades are guaranteed to ±1LSB max error. For these grades, an analog value which falls within a given code width will result in either the correct code for that region or either adjacent one.

Note that the linearity error is not user-adjustable.

DIFFERENTIAL LINEARITY ERROR (NO MISSING CODES)

A specification which guarantees no missing codes requires that every code combination appear in a monotonic increasing sequence as the analog input level is increased. Thus every code must have a finite width. For the HI-574AK, AL, AT, and AU grades, which

Definitions of Specifications (Continued)

guarantee no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temperature ranges. The HI-574AJ and AS grades guarantee no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11 bits must be present; in practice very few of the 12-bit codes are missing.

UNIPOLAR OFFSET

The first transition should occur at a level ½LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following pages. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with or without external adjustment.

BIPOLAR OFFSET

Similarly, in the bipolar mode, the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value ½LSB below analog common. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error over temperature.

FULL SCALE CALIBRATION ERROR

The last transition (from 1111 1111 1110 to 1111 1111 1111) should occur for an analog value 1½LSB below the nominal full scale (9.9963 volts for 10.000 volts full scale). The full scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which is typically 0.05 to 0.1% of full scale, can be trimmed out as shown in Figures 2 and 3. The full scale calibration error over temperature is given with and without the initial error trimmed out. The temperature coefficients for each grade indicate the maximum change in the full scale gain from the initial value using the internal 10 volt reference.

TEMPERATURE COEFFICIENTS

The temperature coefficients for full-scale calibration, unipolar offset, and bipolar offset specify the maximum change from the initial (25°C) value to the value at T_{min} or T_{max}.

POWER SUPPLY REJECTION

The standard specifications for the HI-574A assume use of +5.00 and ±15.00 or ±12.00 volt supplies. The only effect of power supply error on the performance of the device will be a small change in the full scale calibration. This will result in a linear change in all lower order codes. The specifications show the maximum change in calibration from the initial value with the supplies at the various limits.

CODE WIDTH

A fundamental quantity for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 least significant bit (LSB) of the full scale range or 2.44mV out of 10 volts for a 12-bit ADC.

QUANTIZATION UNCERTAINTY

Analog-to-digital converters exhibit an inherent quantization uncertainty of ±½LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of given resolution.

LEFT-JUSTIFIED DATA

The data format used in the HI-574A is left-justified. This means that the data represents the analog input as a fraction of full-scale, ranging from 0 to $\frac{4095}{4096}$. This implies a binary point to the left of the MSB.

Applying the HI-574A

For each application of this converter, the ground connections, power supply bypassing, analog signal source, digital timing and signal routing on the circuit board must be optimized to assure maximum performance. These areas are reviewed in the following sections, along with basic operating modes and calibration requirements.

PHYSICAL MOUNTING AND LAYOUT CONSIDERATIONS

Layout –

Unwanted, parasitic circuit components, (L, R, and C) can make 12 bit accuracy impossible, even with a perfect A/D converter. The best policy is to eliminate or minimize these parasitics through proper circuit layout, rather than try to quantify their effects.

The recommended construction is a double-sided printed circuit board with a ground plane on the component side. Other techniques, such as wire-wrapping or point-to-point wiring on vectorboard, will have an unpredictable effect on accuracy.

In general, sensitive analog signals should be routed between ground traces and kept well away from digital lines. If analog and digital lines must cross, they should do so at right angles.

Power Supplies

Supply voltages to the HI-574A (+15V, −15V and +5V) must be "quiet" and well regulated. Voltage spikes on these lines can affect the converter's accuracy, causing several LSB's to flicker when a constant input is applied. Digital noise and spikes from a switching power supply are especially troublesome. If switching supplies must be used, outputs should be carefully filtered to assure "quiet" DC voltage at the converter terminals.

Further, a bypass capacitor pair on each supply voltage terminal is necessary to counter the effect of variations in supply current. Connect one pair from pin 1 to 15 (V_{LOGIC} supply), one from pin 7 to 9 (V_{CC} to Analog Common) and one from pin 11 to 9 (V_{EE} to Analog Common). For each capacitor pair, a 10μF tantalum type in parallel with a 0.1μF ceramic type is recommended.

Ground Connections

The typical HI-574A ground currents are 5.5mADC into pin 9 (Analog Common) and 7mADC out of pin 15 (Digital Common). These pins should be tied together at the package to guarantee specified performance for the converter. In addition, a wide PC trace should run directly from pin 9 to (usually) 15V common, and from pin 15 to (usually) the +5V Logic Common. If the converter is located some distance from the system's "single point" ground, make only these connections to pins 9 and 15: Tie them together at the package, and back to the system ground with a single path. This path should have low resistance since it will carry about 1.5mA of DC current. (Code dependent currents flow in the V_{CC}, V_{EE} and V_{LOGIC} terminals, but not through the HI-574A's Analog Common or Digital Common).

ANALOG SIGNAL SOURCE

The device chosen to drive the HI-574A analog input will see a nominal load of 5KΩ (10V range) or 10KΩ (20V range). However, the other end of these input resistors may change ±400mV with each bit decision, creating abrupt changes in current at the analog input. Thus, the signal source must maintain its output voltage while furnishing these step changes in load current, which occur at 1.6μS intervals. This requires low output impedance and fast settling by the signal source.

The output impedance of an op amp, for example, has an open loop value which, in a closed loop, is divided by the loop gain available at a frequency of interest. The amplifier should have acceptable loop gain at 600KHz for use with the HI-574A. To check whether the output properties of a signal source are suitable, monitor the 574A's input (pin 13 or 14) with an oscilloscope while a conversion is in progress. Each of the twelve disturbances should subside in one microsecond or less. (The comparator decision is made about 1.5μS after each code change from the SAR).

If the application calls for a Sample/Hold to precede the converter, it should be noted that not all Sample/Holds are compatible with the HI-574A in the manner described above. These will require an additional wideband buffer amplifier to lower their output impedance. A simpler solution is to use the Harris HA-5320 Sample/Hold, which was designed for use with the HI-574A.

RANGE CONNECTIONS AND CALIBRATION PROCEDURES

The HI-574A is a "complete" A/D converter, meaning it is fully operational with addition of the power supply voltages, a Start Convert signal, and a few external components as shown in Figures 2 and 3. Nothing more is required for most applications.

Whether controlled by a processor or operating in the stand-alone mode, the HI-574A offers four standard input ranges: 0V to +10V, 0V to +20V, ±5V and ±10V. The maximum errors for gain and offset are listed under Specifications. If required, however, these errors may be adjusted to zero as explained below. Power supply and ground connections have been discussed in an earlier section.

Unipolar Connections and Calibration –

Refer to Fig. 2. The resistors shown* are for calibration of offset and gain. If this is not required, replace R2 with a 50Ω, 1% metal film resistor and remove the network on pin 12. Connect pin 12 to pin 9. Then, connect the analog signal to pin 13 for the 0V to 10V range, or to pin 14 for the 0V to 20V range. Inputs to +20V (5V over the power supply) are no problem – the converter operates normally.

Calibration consists of adjusting the converter's most negative output to its ideal value (offset adjustment), then, adjusting the most positive output to its ideal value (gain adjustment). To understand the procedure, note that in principle, one is setting the output with respect to the midpoint of an increment of analog input, as denoted by two adjacent code changes. Nominal value of an increment is one

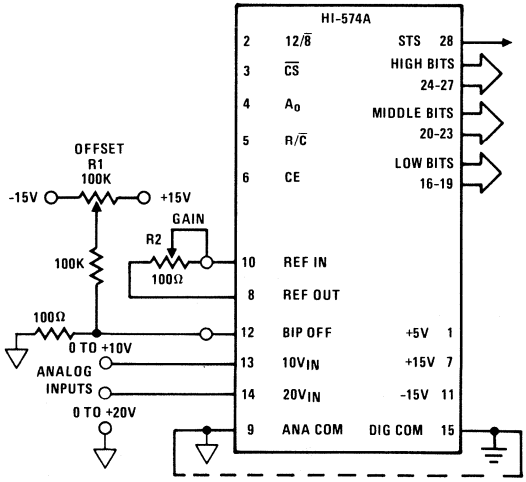


FIGURE 2. UNIPOLAR CONNECTIONS

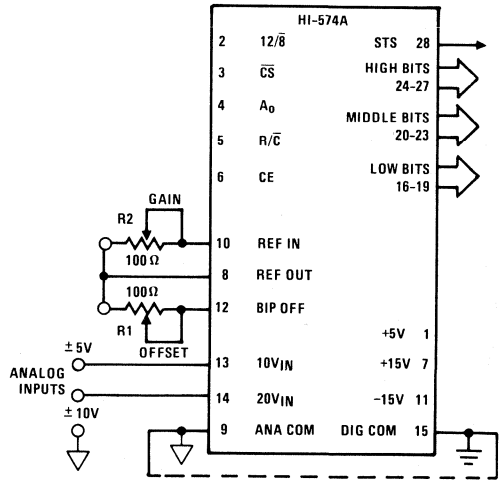


FIGURE 3 BIPOLAR INPUT CONNECTIONS

LSB. However, this approach is impractical because nothing "happens" at a midpoint to indicate that an adjustment is complete. Therefore, calibration is performed in terms of the observable code changes instead of the midpoint between code changes.

For example, midpoint of the first LSB increment should be positioned at the origin, with an output code of all 0's. To do this, apply an input of +1/2 LSB (+1.22mV for the 10V range; +2.44mV for the 20V range). Adjust the Offset potentiometer R1 until the first code transition flickers between 0000 0000 0000 and 0000 0000 0001.

Next, perform a Gain Adjust at positive full scale. Again, the ideal input corresponding to the last code change is applied. This is 1-1/2 LSB's below the nominal full scale (+9.9963V for 10V range; +19.9927V for 20V range). Adjust the Gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

Bipolar Connections and Calibration –

Refer to Figure 3. The gain and offset errors listed under Specifications may be adjusted to zero using potentiometers R1 and R2*. If this isn't required, either or both pots may be replaced by a 50Ω, 1% metal film resistor.

Connect the Analog signal to pin 13 for a ±5V range, or to pin 14 for a ±10V range. Calibration of offset and gain is similar to that for the unipolar ranges as discussed above. First apply a DC input voltage 1/2 LSB above negative full scale (i.e., −4.9988V for the ±5V range, or −9.9976V for the ±10V range). Adjust the offset potentiometer R1 for flicker between output codes 0000 0000 0000 and 0000 0000 0001. Next, apply a DC input voltage 1-1/2 LSB's below positive full scale (+4.9963V for ±5V range; +9.9927V for ±10V range). Adjust the Gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

* The 100Ω potentiometer R2 provides Gain Adjust for the 10V and 20V ranges. In some applications, a full scale of 10.24V (LSB equals 2.5mV) or 20.48V (LSB equals 5.0mV) is more convenient. For these, replace R2 by a 50Ω, 1% metal film resistor. Then, to provide Gain Adjust for the 10.24V range, add a 200Ω potentiometer in series with pin 13. For the 20.48V range, add a 500Ω potentiometer in series with pin 14.

CONTROLLING THE HI-574A

The HI-574A includes logic for direct interface to most microprocessor systems. The processor may take full control of each conversion, or the converter may operate in the "stand-alone" mode, controlled only by the R/C̄ input. Full control consists of selecting an 8 or 12 bit conversion cycle, initiating the conversion, and reading the output data when ready – choosing either 12 bits at once or 8 followed by 4, in a left-justified format. The five control inputs are all TTL/CMOS-compatible: (12/8̄, CS̄, A_0, R/C̄ and CE). Table 1 illustrates the use of these inputs in controlling the converter's operations. Also, a simplified schematic of the internal control logic is shown in Figure 4.

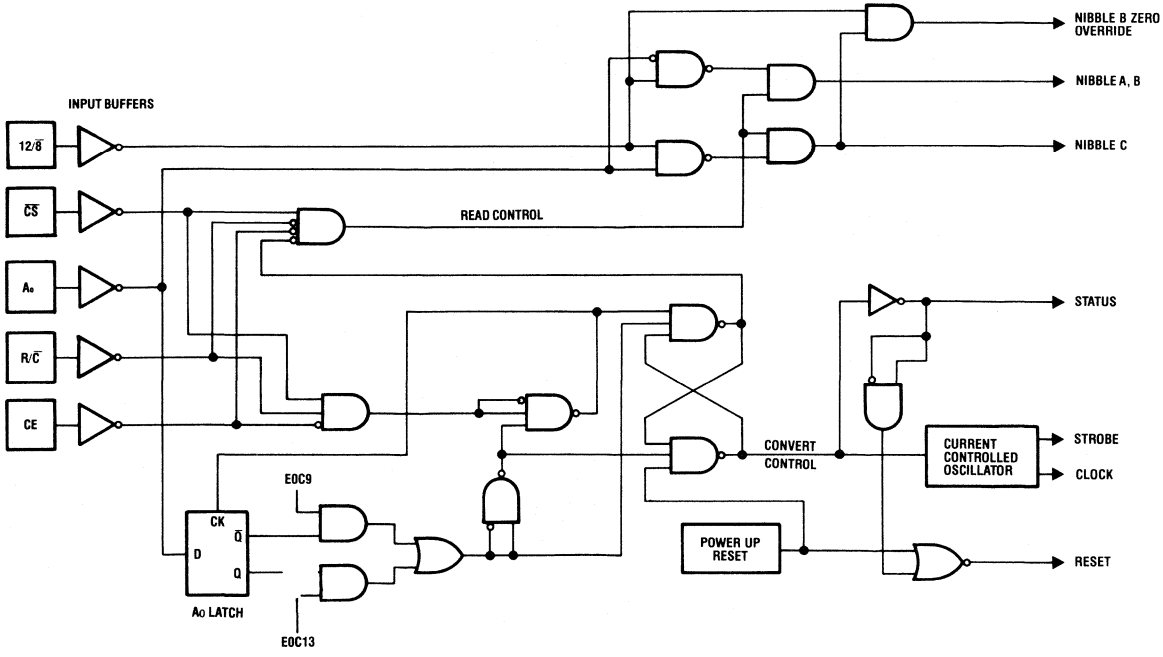


FIGURE 4. HI-574A CONTROL LOGIC

"Stand-Alone Operation"

The simplest control interface calls for a single control line connected to R/$\overline{C}$. Also, CE and 12/$\overline{8}$ are wired high, $\overline{CS}$ and A_0 are wired low, and the output data appears in words of 12 bits each.

The R/$\overline{C}$ signal may have any duty cycle within (and including) the extremes shown in Figures 5 and 6. In general, data may be read when R/$\overline{C}$ is high unless STS is also high, indicating a conversion is in progress. Timing parameters particular to this mode of operation are listed below under "Stand-Alone Mode Timing."

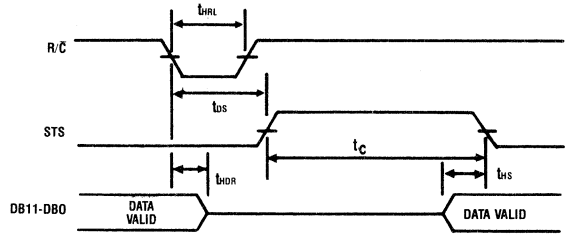


FIGURE 5. LOW PULSE FOR R/$\overline{C}$ – OUTPUTS ENABLED AFTER CONVERSION

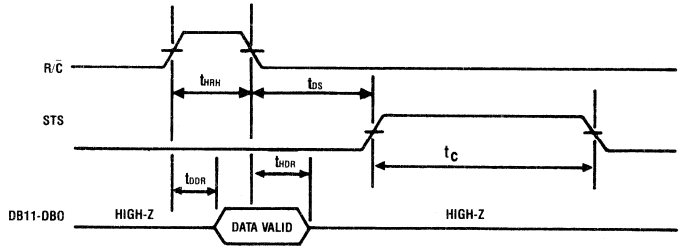


FIGURE 6. HIGH PULSE FOR R/$\overline{C}$ – OUTPUTS ENABLED WHILE R/C HIGH, OTHERWISE HIGH-Z

STAND-ALONE MODE TIMING

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
tHRL	Low R/C Pulse Width	50	–	–	ns
tDS	STS Delay From R/C	–	–	200	ns
tHDR	Data Valid After R/C Low	25	–	–	ns
tHS	STS Delay After Data Valid	300	–	1200	ns
tHRH	High R/C Pulse Width	150	–	–	ns
tDDR	Data Access Time	–	–	150	ns

Time is measured from 50% level of digital transitions. Tested with a 50pF and 3kΩ load.

Conversion Length

A Convert Start transition (see Table 1) latches the state of A_0, which determines whether the conversion continues for 12 bits (A_0 low) or stops with 8 bits (A_0 high). If all 12 bits are read following an 8 bit conversion, the three LSB's will read zero and DB3 will read ONE. A_0 is latched because it is also involved in enabling the output buffers (see "Reading the Output Data"). No other control inputs are latched.

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12 bit conversion
↑	0	0	X	1	Initiate 8 bit conversion
1	↓	0	X	0	Initiate 12 bit conversion
1	↓	0	X	1	Initiate 8 bit conversion
1	0	↓	X	0	Initiate 12 bit conversion
1	0	↓	X	1	Initiate 8 bit conversion
1	0	1	1	X	Enable 12 bit Output
1	0	1	0	0	Enable 8 MSB's Only
1	0	1	0	1	Enable 4 LSB's Plus 4 Trailing Zeroes

TABLE 1
Truth Table for HI-574A Control Inputs.

Conversion Start

A conversion may be initiated as shown in Table 1 by a logic transition on any of three inputs: CE, $\overline{CS}$ or R/$\overline{C}$. The last of the three to reach the correct state starts the conversion, so one, two or all three may be dynamically controlled. The nominal delay from each is the same, and if necessary, all three may change state simultaneously. To assure that a particular input controls the start of conversion, the other two should be set up at least 50nS earlier, however. See the HI-574A Timing Specifications, Convert mode.

This variety of HI-574A control modes allows a simple interface in most system applications. The Convert Start timing relationships are illustrated in Figure 7.

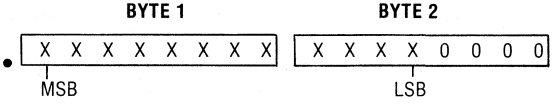
The output signal STS indicates status of the converter by going high only while a conversion is in progress. While STS is high, the output buffers remain in a high impedance state and data cannot be read. Also, an additional Start Convert will not reset the converter or reinitiate a conversion while STS is high. (However, if A_0 changes state after a conversion begins, an additional Start Convert signal will latch the new state of A_0, possibly causing a wrong cycle length (8 vs 12 bits) for that conversion).

Reading the Output Data

The output data buffers remain in a high impedance state until four conditions are met: R/$\overline{C}$ high, STS low, CE high and $\overline{CS}$ low. At that time, data lines become active according to the state of inputs 12/$\overline{8}$ and A_0. Timing constraints are illustrated in Figure 8.

The 12/$\overline{8}$ input will be tied high or low in most applications, though it is fully TTL/CMOS-compatible. With 12/$\overline{8}$ high, all 12 output lines become active simultaneously, for interface to a 12 or 16 bit data bus. The A_0 input is ignored.

With 12/$\overline{8}$ low, the output is organized in two 8 bit bytes, selected one at a time by A_0. This allows an 8 bit data bus to be connected as shown in Figure 9. A_0 is usually tied to the least significant bit of the address bus, for storing the HI-574A output in two consecutive memory locations. (With A_0 low, the 8 MSB's only are enabled. With A_0 high, 4 MSB's are disabled, bits 4 through 7 are forced to zero, and the 4 LSB's are enabled). This two byte format is considered "left justified data", for which a decimal (or binary!) point is assumed to the left of byte 1:



Further, A_0 may be toggled at any time without damage to the converter. Break-before-make action is guaranteed between the two data bytes, which assures that the outputs strapped together in Figure 9 will never be enabled at the same time.

A read operation usually begins after the conversion is complete and STS is low. For earliest access to the data however, the read should begin no later than ($t_{DD} + t_{HS}$) before STS goes low. See Figure 8.

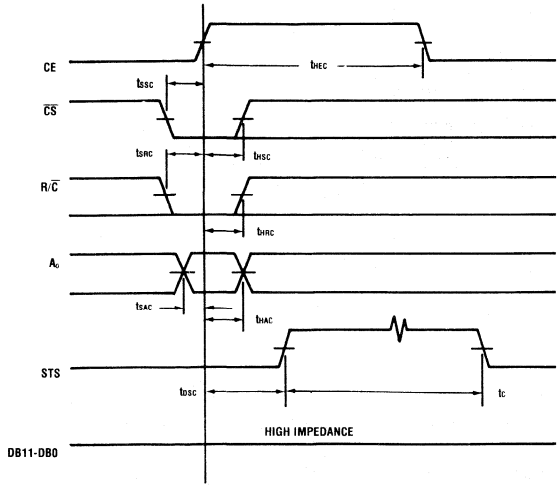


FIGURE 7. CONVERT START TIMING

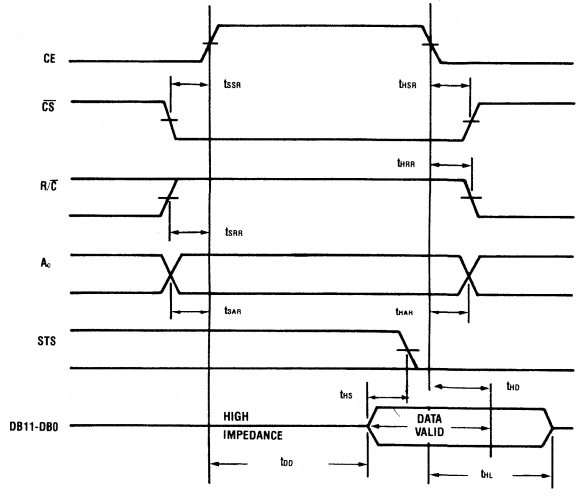


FIGURE 8. READ CYCLE TIMING

Timing Specifications +25°C Unless Otherwise Specified

Symbol	Parameter	Min	Typ	Max	Units
Convert Mode					
t_{DSC}	STS Delay from CE			200	nS
t_{HEC}	$\overline{CE}$ Pulse width	50			nS
t_{SSC}	$\overline{CS}$ to CE Setup	50			nS
t_{HSC}	$\overline{CS}$ Low during CE High	50			nS
t_{SRC}	R/$\overline{C}$ to CE Setup	50			nS
t_{HRC}	R/$\overline{C}$ Low during CE high	50			nS
t_{SAC}	A_0 to CE Setup	0			nS
t_{HAC}	A_0 Valid during CE high	50			nS
t_C	Conversion time, 12 bit cycle T min to T max	15	20	25	μS
	8 bit cycle T min to T max	10	13	17	μS
Read Mode					
t_{DD}	Access time from CE		75	150	nS
t_{HD}	Data Valid after CE low	25			nS
t_{HL}	Output float delay		100	150	nS
t_{SSR}	$\overline{CS}$ to CE setup	50			nS
t_{SRR}	R/$\overline{C}$ to CE setup	0			nS
t_{SAR}	A_0 to CE setup	50			nS
t_{HSR}	$\overline{CS}$ valid after CE low	0			nS
t_{HRR}	R/$\overline{C}$ high after CE low	0			nS
t_{HAR}	A_0 valid after CE low	50			nS
t_{HS}	STS delay after data valid	300		1200	nS

NOTE: Time is measured from 50% level of digital transitions. Tested with a 50pF and 3kΩ load.

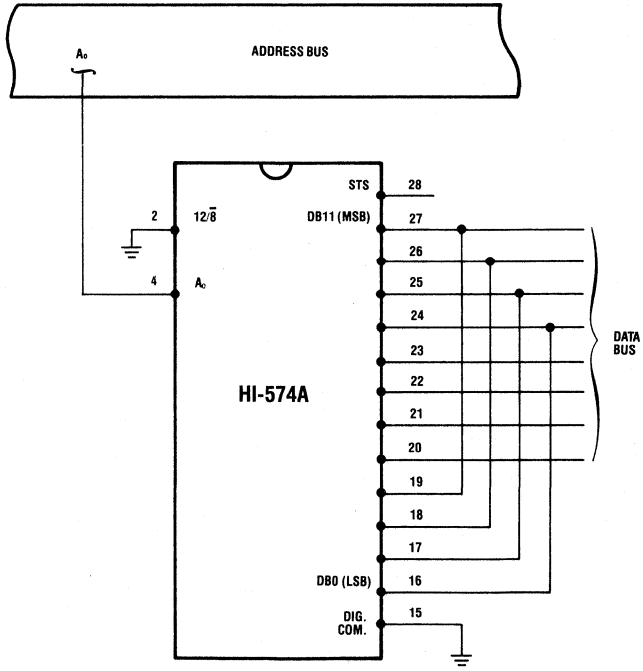


FIGURE 9 INTERFACE TO AN 8 BIT DATA BUS

DIE CHARACTERISTICS

Transistor Count		1117	Thermal Constants;	θja	48°C/W
Die Size:	Analog	204 x 104 mils		θjc	15°C/W
	Digital	158 x 84 mils	Process:		Bipolar – DI and CMOS – JI

HI-674A

12μs, Complete 12-Bit A/D Converter with Microprocessor Interface

Features

- Complete 12-Bit A/D Converter with Reference and Clock
- Full 8-, 12- or 16-Bit Microprocessor Bus Interface
- 150ns Bus Access Time
- No Missing Codes Over Temperature
- Minimal Set-up Time for Control Signals
- 15μs Maximum Conversion Time
- Low Noise, via Current-Mode Signal Transmission Between Chips
- Byte Enable/Short Cycle (A_0 Input)
  - ▸ Guaranteed Break-Before-Make Action, Eliminating Bus Contention During Read Operation. Latched by the Start Convert Input (To Set the Conversion Length)
- Faster Version of the HI-574A
- Same Pinout as the HI-574A
- ±12V to ±15V Operation

Applications

- Military and Industrial Data Acquisition Systems
- Electronic Test and Scientific Instrumentation
- Process Control Systems

Description

The HI-674A is a complete 12-bit Analog-to-Digital Converter, including a +10V reference, clock, three-state outputs and a digital interface for microprocessor control. Successive approximation conversion is performed by two monolithic dice housed in a 28 pin package. The bipolar analog die features the Harris Dielectric Isolation process, which provides enhanced AC performance and freedom from latch-up.

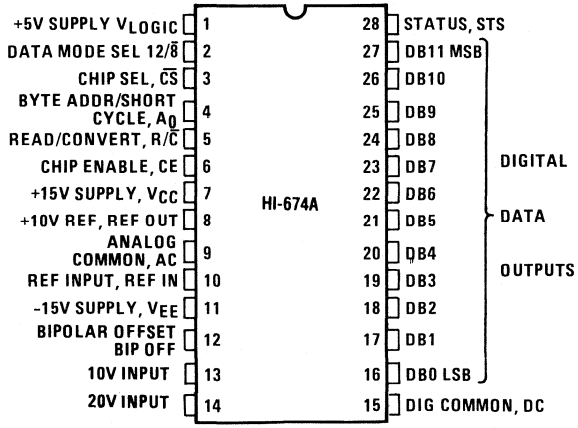
Custom design of each IC (bipolar analog and CMOS digital) has yielded improved performance over existing versions of this converter. The voltage comparator features high PSRR plus a high speed current-mode latch, and provides precise decisions down to 0.1 LSB of input overdrive. More than 2X reduction in noise has been achieved by using current instead of voltage for transmission of all signals between the analog and digital IC's. Also, the clock oscillator is current-controlled for excellent stability over temperature. The oscillator is trimmed for a nominal conversion time of 12 ± 1μs.

The HI-674A offers standard unipolar and bipolar input ranges, laser trimmed for specified linearity, gain and offset accuracy. The buried zener reference circuit is trimmed for minimum temperature coefficient.

Power requirements are +5V and ±12V to ±15V, with typical dissipation of 385mW at ±12V. All models are available in a 28 pin Sidebrazed DIP. For additional Hi-Rel screening including 160 hour burn-in specify the "-8" suffix. For MIL-STD-883 compliant parts, request the HI-674A/883 data sheet.

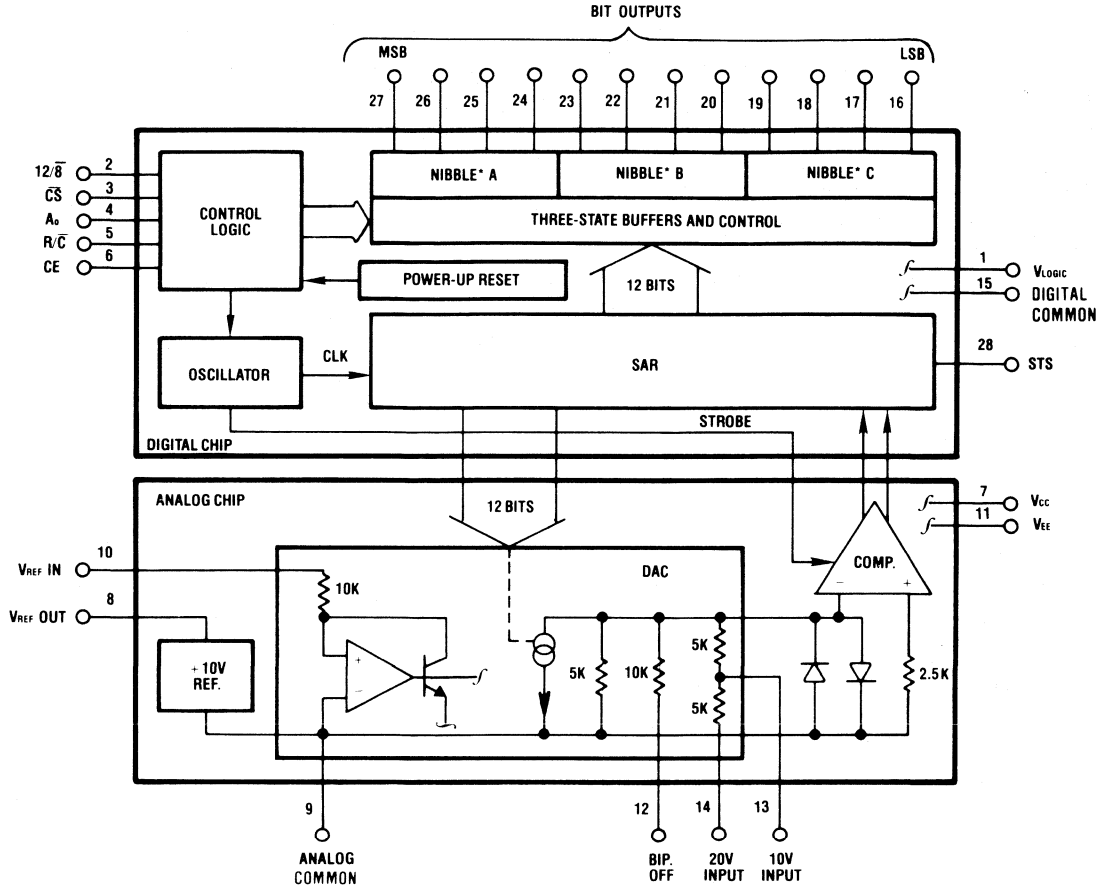
Pinout

CERAMIC DIP
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Block Diagram



*("NIBBLE" IS A 4 BIT DIGITAL WORD.)

(Typical @ +25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = −15V or −12V unless otherwise specified)

DC and Transfer Accuracy Specifications

MODEL	HI-674AJ	HI-674AK	HI-674AL	UNITS
Temperature Range		-5		
Resolution (max)	12	12	12	Bits
Linearity Error				
25°C (max)	±1	±1/2	±1/2	LSB
0°C to +75°C (max)	±1	±1/2	±1/2	LSB
Differential Linearity Error				
(Maximum resolution for which no missing codes is guaranteed)				
25°C	11	12	12	Bits
T_{min} to T_{max}	11	12	12	Bits
Unipolar Offset (max)				
(Adjustable to zero)	±2	±2	±2	LSB
Bipolar Offset (max)				
(Adjustable to zero)	±10	±4	±4	LSB
Full Scale Calibration Error				
25°C (max), with fixed 50 Ω resistor from				
REF OUT to REF IN (Adjustable to zero)	0.3	0.3	0.3	% of F.S.
T_{min} to T_{max}				
(No adjustment at +25°C)	0.5	0.4	0.35	% of F.S.
(With adjustment to zero at +25°C)	0.22	0.12	0.05	% of F.S.
Temperature Coefficients				
Guaranteed max change, T_{min} to T_{max} (Using internal reference)				
Unipolar Offset	±2	±1	±1	LSB
	(10)	(5)	(5)	(ppm/°C)
Bipolar Offset	±2	±1	±1	LSB
	(10)	(5)	(5)	(ppm/°C)
Full Scale Calibration	±9	±5	±2	LSB
	(45)	(25)	(10)	(ppm/°C)
Power Supply Rejection				
Max change in Full Scale Calibration				
+13.5V<V_{CC}<+16.5V or +11.4V<V_{CC}<+12.6V	±2	±1	±1	LSB
+4.5V<V_{LOGIC}<+5.5V	±1/2	±1/2	±1/2	LSB
−16.5V<V_{EE}<−13.5V or −12.6V<V_{EE}<−11.4V	±2	±1	±1	LSB
Analog Inputs				
Input Ranges				
Bipolar	−5 to +5			Volts
	−10 to +10			Volts
Unipolar	0 to +10			Volts
	0 to +20			Volts
Input Impedance				
10 Volt Span	5K, ± 25%			Ohms
20 Volt Span	10K, ± 25%			Ohms
Power Supplies				
Operating Voltage Range				
V_{LOGIC}	+4.5 to +5.5			Volts
V_{CC}	+11.4 to +16.5			Volts
V_{EE}	−11.4 to −16.5			Volts
Operating Current				
I_{LOGIC}	7 TYP, 15 MAX			mA
I_{CC} +15V Supply	11 TYP, 15 MAX			mA
I_{EE} -15V Supply	21 TYP, 28 MAX			mA
Power Dissipation				
±15V, +5V	515 TYP, 720 MAX			mW
±12V, +5V	385 TYP			mW
Internal Reference Voltage, T_{min} to T_{max}	+10.00 ±.05 MAX			Volts
Output current,[1]	2.0 MAX			mA
available for external loads (External load				
should not change during conversion).				

1. *When supplying an external load (not including the ADC) and operating on ±12V supplies, a buffer amplifier must be provided for the Reference Output.*

(Typical @ +25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = −15V or −12V unless otherwise specified)

DC and Transfer Accuracy Specifications

MODEL	HI-674AS	HI-674AT	UNITS
Temperature Range	-2, -8		
Resolution (max)	12	12	Bits
Linearity Error			
25°C (max)	±1	±1/2	LSB
−55°C to +125°C (max)	±1	±1	LSB
Differential Linearity Error			
(Maximum resolution for which no missing codes is guaranteed)			
25°C	11	12	Bits
T_{min} to T_{max}	11	12	Bits
Unipolar Offset (max)			
(Adjustable to zero)	±2	±2	LSB
Bipolar Offset (max)			
(Adjustable to zero)	±10	±4	LSB
Full Scale Calibration Error			
25°C (max), with fixed 50 Ω resistor from			
REF OUT to REF IN (Adjustable to zero)	0.3	0.3	% of F.S.
T_{min} to T_{max}			
(No adjustment at +25°C)	0.8	0.6	% of F.S.
(With adjustment to zero at +25°C)	0.5	0.25	% of F.S.
Temperature Coefficients			
Guaranteed max change, T_{min} to T_{max} (Using internal reference)			
Unipolar Offset	±2	±1	LSB
	(5)	(2.5)	(ppm/°C)
Bipolar Offset	±4	±2	LSB
	(10)	(5)	(ppm/°C)
Full Scale Calibration	±20	±10	LSB
	(50)	(25)	(ppm/°C)
Power Supply Rejection			
Max change in Full Scale Calibration			
+13.5V<V_{CC}<+16.5V or +11.4V<V_{CC}<+12.6V	±2	±1	LSB
+4.5V<V_{LOGIC}<+5.5V	±1/2	±1/2	LSB
−16.5V<V_{EE}<−13.5V or −12.6V<V_{EE}<−11.4V	±2	±1	LSB
Analog Inputs			
Input Ranges			
Bipolar	−5 to +5		Volts
	−10 to +10		Volts
Unipolar	0 to +10		Volts
	0 to +20		Volts
Input Impedance			
10 Volt Span	5K Ω, ± 25%		Ohms
20 Volt Span	10K Ω, ± 25%		Ohms
Power Supplies			
Operating Voltage Range			
V_{LOGIC}	+4.5 to +5.5		Volts
V_{CC}	+11.4 to +16.5		Volts
V_{EE}	−11.4 to −16.5		Volts
Operating Current			
I_{LOGIC}	7 TYP, 15 MAX		mA
I_{CC} +15V Supply	11 TYP, 15 MAX		mA
I_{EE} -15V Supply	21 TYP, 28 MAX		mA
Power Dissipation			
±15V, +5V	515 TYP, 720 MAX		mW
±12V, +5V	385 TYP		mW
Internal Reference Voltage, T_{min} to T_{max}	+10.00 ±.05 MAX		Volts
Output current,[1]	2.0 MAX		mA
available for external loads (External load			
should not change during conversion).			

1. *When supplying an external load (not including the ADC) and operating on* ±12V supplies, a buffer amplifier must be provided for the Reference Output.

Digital Specifications[1] (All Models, Over Full Temperature Range)

	MIN	TYP	MAX
Logic Inputs (CE, $\overline{CS}$, R/$\overline{C}$, A0, 12/$\overline{8}$)[2]			
Logic "1"	+2.4V		+5.5V
Logic "0"	−0.5V		+0.8V
Current	−5μA	±0.1μA	+5μA
Capacitance		5pF	
Logic Outputs (DB11-DB0, STS)			
Logic "0" (I_{SINK} — 1.6mA)			+0.4V
Logic "1" (I_{SOURCE} — 500μA)	+2.4V		
Leakage (High - Z State, DB11-DB0 ONLY)	−5μA	±0.1μA	+5μA
Capacitance		5pF	

1 *See "HI-674A Timing Specifications" for a detailed listing of digital timing parameters.*

2 *Although this guaranteed threshold is higher than standard TTL (+2.0V), bus loading is much less, i.e., typical input current is only 0.25% of a TTL load.*

Absolute Maximum Ratings

(Specifications apply to all grades, except where noted)

V_{CC} to Digital Common ..... 0 to +16.5V
V_{EE} to Digital Common ..... 0 to −16.5V
V_{LOGIC} to Digital Common ..... 0 to +7V
Analog Common to Digital Common ..... ±1V
Control Inputs (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$) to
Digital Common ..... −0.5V to V_{LOGIC} +0.5V
Analog Inputs (REF IN, BIP OFF, 10V_{IN}) to
Analog Common ..... ±16.5V
20V_{IN} to Analog Common ..... ±24V
REF OUT ..... Indefinite short to common
Momentary short to V_{CC}
Junction Temperature ..... 175°C
Lead Temperature, Soldering ..... 300°C, 10 sec.
Storage Temperature ..... −65°C to +150°C

HI-674A Ordering Guide

MODEL	TEMP. RANGE	LINEARITY ERROR MAX (T_{MIN} to T_{MAX})	RESOLUTION (NO MISSING CODES, T_{MIN} to T_{MAX})	FULL SCALE TC (PPM/°C MAX)
HI1-674AJD-5	0 to 75°C	±1 LSB	11 Bits	45.0
HI1-674AKD-5	0 to 75°C	±1/2 LSB	12 Bits	25.0
HI1-674ALD-5	0 to 75°C	±1/2 LSB	12 Bits	10.0
HI1-674ASD-2	−55 to +125°C	±1 LSB	11 Bits	50.0
HI1-674ASD-8*	−55 to +125°C	±1 LSB	11 Bits	50.0
HI1-674ATD-2	−55 to +125°C	±1 LSB	12 Bits	25.0
HI1-674ATD-8*	−55 to +125°C	±1 LSB	12 Bits	25.0

** The MIL-STD-883 data sheet is available on request*

Definitions of Specifications

LINEARITY ERROR

Linearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale". The point used as "zero" occurs ½LSB (1.22mV for 10 volt span) before the first code transition (all zeros to only the LSB "on"). "Full scale" is defined as a level 1½LSB beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The HI-674AK, AL, AT, and AU grades are guaranteed for maximum nonlinearity of ±½LSB. For these grades, this means that an analog value which falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The HI-674AJ and AS grades are guaranteed to ±1LSB max error. For these grades, an analog value which falls within a given code width will result in either the correct code for that region or either adjacent one.

Note that the linearity error is not user-adjustable.

DIFFERENTIAL LINEARITY ERROR (NO MISSING CODES)

A specification which guarantees no missing codes requires that every code combination appear in a monotonic increasing sequence as the analog input level is increased. Thus every code must have a finite width. For the HI-674AK, AL, AT, and AU grades, which

Definitions of Specifications (Continued)

guarantee no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temperature ranges. The HI-674AJ and AS grades guarantee no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11 bits must be present; in practice very few of the 12-bit codes are missing.

UNIPOLAR OFFSET

The first transition should occur at a level ½LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following pages. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with or without external adjustment.

BIPOLAR OFFSET

Similarly, in the bipolar mode, the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value ½LSB below analog common. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error over temperature.

FULL SCALE CALIBRATION ERROR

The last transition (from 1111 1111 1110 to 1111 1111 1111) should occur for an analog value 1½LSB below the nominal full scale (9.9963 volts for 10.000 volts full scale). The full scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which is typically 0.05 to 0.1% of full scale, can be trimmed out as shown in Figures 2 and 3. The full scale calibration error over temperature is given with and without the initial error trimmed out. The temperature coefficients for each grade indicate the maximum change in the full scale gain from the initial value using the internal 10 volt reference.

TEMPERATURE COEFFICIENTS

The temperature coefficients for full-scale calibration, unipolar offset, and bipolar offset specify the maximum change from the initial (25°C) value to the value at T_{min} or T_{max}.

POWER SUPPLY REJECTION

The standard specifications for the HI-674A assume use of +5.00 and ±15.00 or ±12.00 volt supplies. The only effect of power supply error on the performance of the device will be a small change in the full scale calibration. This will result in a linear change in all lower order codes. The specifications show the maximum change in calibration from the initial value with the supplies at the various limits.

CODE WIDTH

A fundamental quantity for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 least significant bit (LSB) of the full scale range or 2.44mV out of 10 volts for a 12-bit ADC.

QUANTIZATION UNCERTAINTY

Analog-to-digital converters exhibit an inherent quantization uncertainty of ±½LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of given resolution.

LEFT-JUSTIFIED DATA

The data format used in the HI-674A is left-justified. This means that the data represents the analog input as a fraction of full-scale, ranging from 0 to $\frac{4095}{4096}$. This implies a binary point to the left of the MSB.

Applying the HI-674A

For each application of this converter, the ground connections, power supply bypassing, analog signal source, digital timing and signal routing on the circuit board must be optimized to assure maximum performance. These areas are reviewed in the following sections, along with basic operating modes and calibration requirements.

PHYSICAL MOUNTING AND LAYOUT CONSIDERATIONS

Layout –

Unwanted, parasitic circuit components, (L, R, and C) can make 12 bit accuracy impossible, even with a perfect A/D converter. The best policy is to eliminate or minimize these parasitics through proper circuit layout, rather than try to quantify their effects.

The recommended construction is a double-sided printed circuit board with a ground plane on the component side. Other techniques, such as wire-wrapping or point-to-point wiring on vectorboard, will have an unpredictable effect on accuracy.

In general, sensitive analog signals should be routed between ground traces and kept well away from digital lines. If analog and digital lines must cross, they should do so at right angles.

Power Supplies

Supply voltages to the HI-674A (+15V, −15V and +5V) must be "quiet" and well regulated. Voltage spikes on these lines can affect the converter's accuracy, causing several LSB's to flicker when a constant input is applied. Digital noise and spikes from a switching power supply are especially troublesome. If switching supplies must be used, outputs should be carefully filtered to assure "quiet" DC voltage at the converter terminals.

Further, a bypass capacitor pair on each supply voltage terminal is necessary to counter the effect of variations in supply current. Connect one pair from pin 1 to 15 (V_{LOGIC} supply), one from pin 7 to 9 (V_{CC} to Analog Common) and one from pin 11 to 9 (V_{EE} to Analog Common). For each capacitor pair, a 10μF tantalum type in parallel with a 0.1μF ceramic type is recommended.

Ground Connections

The typical HI-674A ground currents are 6mADC into pin 9 (Analog Ground) and 3mADC out of pin 15 (Digital Common). These pins should be tied together at the package to guarantee specified performance for the converter. In addition, a wide PC trace should run directly from pin 9 to (usually) 15V common, and from pin 15 to (usually) the +5V Logic Common. If the converter is located some distance from the system's "single point" ground, make only these connections to pins 9 and 15: Tie them together at the package, and back to the system ground with a single path. This path should have low resistance since it will carry about 3mA of DC current. (Code dependent currents flow in the V_{CC}, V_{EE} and V_{LOGIC} terminals, but not through the HI-674A's Analog Common or Digital Common).

ANALOG SIGNAL SOURCE

The device chosen to drive the HI-674A analog input will see a nominal load of 5KΩ (10V range) or 10KΩ (20V range). However, the other end of these input resistors may change ±400mV with each bit decision, creating abrupt changes in current at the analog input. Thus, the signal source must maintain its output voltage while furnishing these step changes in load current, which occur at 950 nS intervals. This requires low output impedance and fast settling by the signal source.

The output impedance of an op amp, for example, has an open loop value which, in a closed loop, is divided by the loop gain available at a frequency of interest. The amplifier should have acceptable loop gain at 1MHz for use with the HI-674A. To check whether the output properties of a signal source are suitable, monitor the 674A's input (pin 13 or 14) with an oscilloscope while a conversion is in progress. Each of the twelve disturbances should subside in one half microsecond or less. (The comparator decision is made about 850 nS after each code change from the SAR).

If the application calls for a Sample/Hold to precede the converter, it should be noted that not all Sample/Holds are compatible with the HI-674A in the manner described above. These will require an additional wideband buffer amplifier to lower their output impedance. A simpler solution is to use the Harris HA-5320 Sample/Hold, which was designed for use with the HI-674A.

RANGE CONNECTIONS AND CALIBRATION PROCEDURES

The HI-674A is a "complete" A/D converter, meaning it is fully operational with addition of the power supply voltages, a Start Convert signal, and a few external components as shown in Figures 2 and 3. Nothing more is required for most applications.

Whether controlled by a processor or operating in the stand-alone mode, the HI-674A offers four standard input ranges: 0V to +10V, 0V to +20V, ±5V and ±10V. The maximum errors for gain and offset are listed under Specifications. If required, however, these errors may be adjusted to zero as explained below. Power supply and ground connections have been discussed in an earlier section.

Unipolar Connections and Calibration –

Refer to Fig. 2. The resistors shown* are for calibration of offset and gain. If this is not required, replace R2 with a 50Ω, 1% metal film resistor and remove the network on pin 12. Connect pin 12 to pin 9. Then, connect the analog signal to pin 13 for the 0V to 10V range, or to pin 14 for the 0V to 20V range. Inputs to +20V (5V over the power supply) are no problem – the converter operates normally.

Calibration consists of adjusting the converter's most negative output to its ideal value (offset adjustment), then, adjusting the most positive output to its ideal value (gain adjustment). To understand the procedure, note that in principle, one is setting the output with respect to the midpoint of an increment of analog input, as denoted by two adjacent code changes. Nominal value of an increment is one

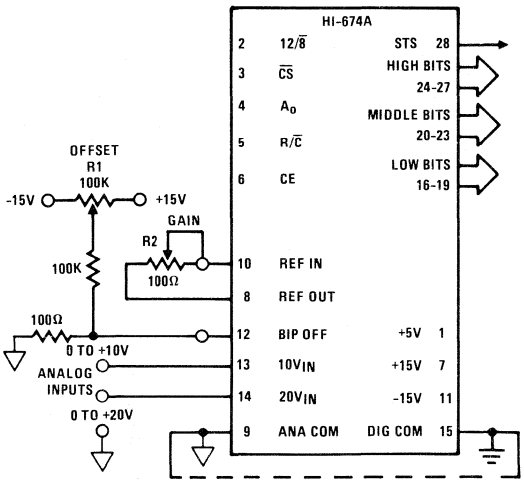


FIGURE 2. UNIPOLAR CONNECTIONS

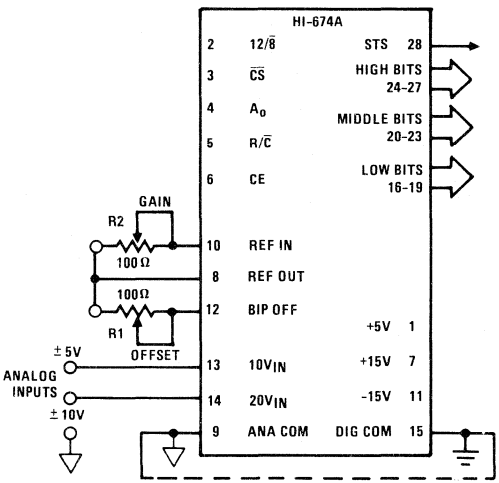


FIGURE 3 BIPOLAR INPUT CONNECTIONS

LSB. However, this approach is impractical because nothing "happens" at a midpoint to indicate that an adjustment is complete. Therefore, calibration is performed in terms of the observable code changes instead of the midpoint between code changes.

For example, midpoint of the first LSB increment should be positioned at the origin, with an output code of all 0's. To do this, apply an input of +1/2 LSB (+1.22mV for the 10V range; +2.44mV for the 20V range). Adjust the Offset potentiometer R1 until the first code transition flickers between 0000 0000 0000 and 0000 0000 0001.

Next, perform a Gain Adjust at positive full scale. Again, the ideal input corresponding to the last code change is applied. This is 1-1/2 LSB's below the nominal full scale (+9.9963V for 10V range; +19.9927V for 20V range). Adjust the Gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

Bipolar Connections and Calibration –

Refer to Figure 3. The gain and offset errors listed under Specifications may be adjusted to zero using potentiometers R1 and R2*. If this isn't required, either or both pots may be replaced by a 50Ω, 1% metal film resistor.

Connect the Analog signal to pin 13 for a ±5V range, or to pin 14 for a ±10V range. Calibration of offset and gain is similar to that for the unipolar ranges as discussed above. First apply a DC input voltage 1/2 LSB above negative full scale (i.e., −4.9988V for the ±5V range, or −9.9976V for the ±10V range). Adjust the offset potentiometer R1 for flicker between output codes 0000 0000 0000 and 0000 0000 0001. Next, apply a DC input voltage 1-1/2 LSB's below positive full scale (+4.9963V for ±5V range; +9.9927V for ±10V range). Adjust the Gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

* The 100Ω potentiometer R2 provides Gain Adjust for the 10V and 20V ranges. In some applications, a full scale of 10.24V (LSB equals 2.5mV) or 20.48V (LSB equals 5.0mV) is more convenient. For these, replace R2 by a 50Ω, 1% metal film resistor. Then, to provide Gain Adjust for the 10.24V range, add a 200Ω potentiometer in series with pin 13. For the 20.48V range, add a 500Ω potentiometer in series with pin 14.

CONTROLLING THE HI-674A

The HI-674A includes logic for direct interface to most microprocessor systems. The processor may take full control of each conversion, or the converter may operate in the "stand-alone" mode, controlled only by the R/C̄ input. Full control consists of selecting an 8 or 12 bit conversion cycle, initiating the conversion, and reading the output data when ready – choosing either 12 bits at once or 8 followed by 4, in a left-justified format. The five control inputs are all TTL/CMOS-compatible: (12/8̄, CS̄, A_0, R/C̄ and CE). Table 1 illustrates the use of these inputs in controlling the converter's operations. Also, a simplified schematic of the internal control logic is shown in Figure 4.

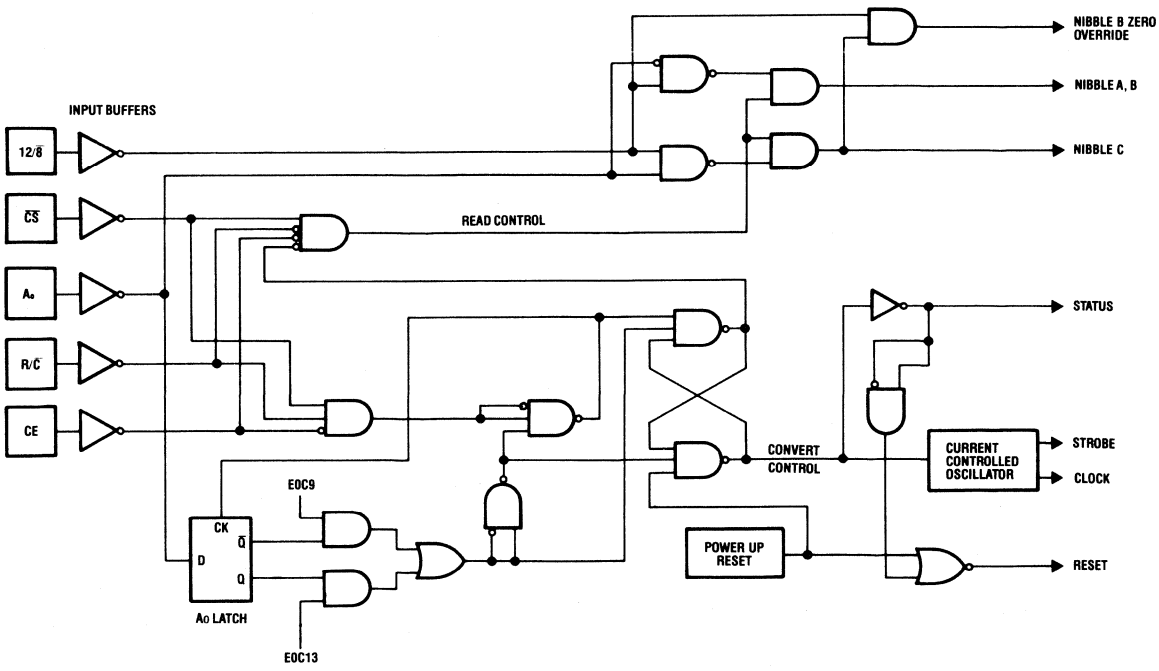


FIGURE 4. HI-674A CONTROL LOGIC

"Stand-Alone Operation"

The simplest control interface calls for a single control line connected to R/$\overline{C}$. Also, CE and 12/$\overline{8}$ are wired high, $\overline{CS}$ and A_0 are wired low, and the output data appears in words of 12 bits each.

The R/$\overline{C}$ signal may have any duty cycle within (and including) the extremes shown in Figures 5 and 6. In general, data may be read when R/$\overline{C}$ is high unless STS is also high, indicating a conversion is in progress. Timing parameters particular to this mode of operation are listed below under "Stand-Alone Mode Timing."

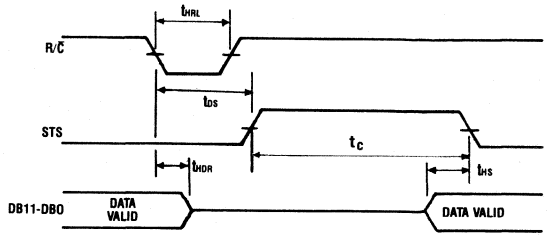


FIGURE 5. LOW PULSE FOR R/$\overline{C}$ – OUTPUTS ENABLED AFTER CONVERSION

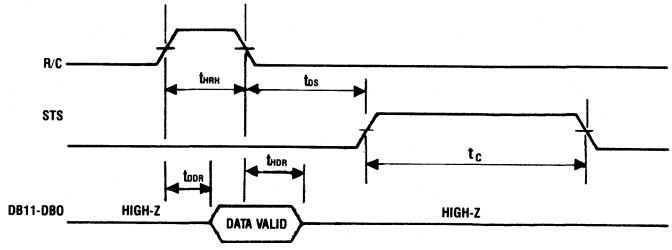


FIGURE 6. HIGH PULSE FOR R/$\overline{C}$ – OUTPUTS ENABLED WHILE R/C HIGH, OTHERWISE HIGH-Z

STAND-ALONE MODE TIMING

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
tHRL	Low R/C Pulse Width	50	–	–	ns
tDS	STS Delay From R/C	–	–	200	ns
tHDR	Data Valid After R/C Low	25	–	–	ns
tHS	STS Delay After Data Valid	25	–	850	ns
tHRH	High R/C Pulse Width	150	–	–	ns
tDDR	Data Access Time	–	–	150	ns

Time is measured from 50% level of digital transitions. Tested with a 50pF and 3kΩ load.

Conversion Length

A Convert Start transition (see Table 1) latches the state of A_0, which determines whether the conversion continues for 12 bits (A_0 low) or stops with 8 bits (A_0 high). If all 12 bits are read following an 8 bit conversion, the three LSB's will read zero and DB3 will read ONE. A_0 is latched because it is also involved in enabling the output buffers (see "Reading the Output Data"). No other control inputs are latched.

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12 bit conversion
↑	0	0	X	1	Initiate 8 bit conversion
1	↓	0	X	0	Initiate 12 bit conversion
1	↓	0	X	1	Initiate 8 bit conversion
1	0	↓	X	0	Initiate 12 bit conversion
1	0	↓	X	1	Initiate 8 bit conversion
1	0	1	1	X	Enable 12 bit Output
1	0	1	0	0	Enable 8 MSB's Only
1	0	1	0	1	Enable 4 LSB's Plus 4 Trailing Zeroes

TABLE 1

Truth Table for HI-674A Control Inputs.

Conversion Start

A conversion may be initiated as shown in Table 1 by a logic transition on any of three inputs: CE, $\overline{CS}$ or R/$\overline{C}$. The last of the three to reach the correct state starts the conversion, so one, two or all three may be dynamically controlled. The nominal delay from each is the same, and if necessary, all three may change state simultaneously. To assure that a particular input controls the start of conversion, the other two should be set up at least 50nS earlier, however. See the HI-674A Timing Specifications, Convert mode.

This variety of HI-674A control modes allows a simple interface in most system applications. The Convert Start timing relationships are illustrated in Figure 7.

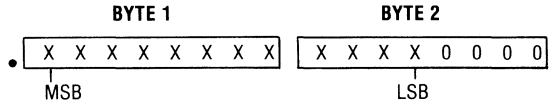
The output signal STS indicates status of the converter by going high only while a conversion is in progress. While STS is high, the output buffers remain in a high impedance state and data cannot be read. Also, an additional Start Convert will not reset the converter or reinitiate a conversion while STS is high. (However, if A_0 changes state after a conversion begins, an additional Start Convert signal will latch the new state of A_0, possibly causing a wrong cycle length (8 vs 12 bits) for that conversion).

Reading the Output Data

The output data buffers remain in a high impedance state until four conditions are met: R/$\overline{C}$ high, STS low, CE high and $\overline{CS}$ low. At that time, data lines become active according to the state of inputs 12/$\overline{8}$ and A_0. Timing constraints are illustrated in Figure 8.

The 12/$\overline{8}$ input will be tied high or low in most applications, though it is fully TTL/CMOS-compatible. With 12/$\overline{8}$ high, all 12 output lines become active simultaneously, for interface to a 12 or 16 bit data bus. The A_0 input is ignored.

With 12/$\overline{8}$ low, the output is organized in two 8 bit bytes, selected one at a time by A_0. This allows an 8 bit data bus to be connected as shown in Figure 9. A_0 is usually tied to the least significant bit of the address bus, for storing the HI-674A output in two consecutive memory locations. (With A_0 low, the 8 MSB's only are enabled. With A_0 high, 4 MSB's are disabled, bits 4 through 7 are forced to zero, and the 4 LSB's are enabled). This two byte format is considered "left justified data", for which a decimal (or binary!) point is assumed to the left of byte 1:



Further, A_0 may be toggled at any time without damage to the converter. Break-before-make action is guaranteed between the two data bytes, which assures that the outputs strapped together in Figure 9 will never be enabled at the same time.

A read operation usually begins after the conversion is complete and STS is low. For earliest access to the data however, the read should begin no later than (t_{DD} + t_{HS}) before STS goes low. See Figure 8.

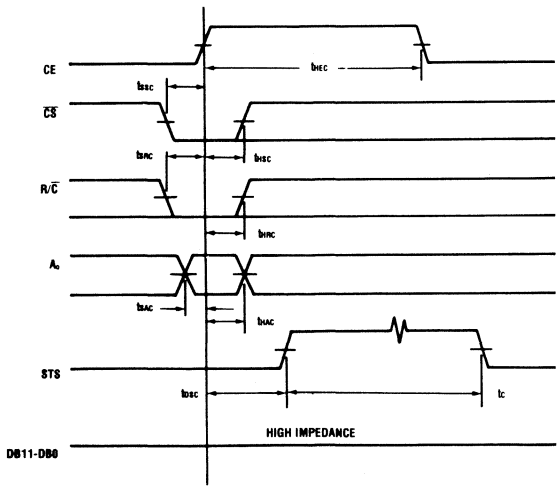


FIGURE 7. CONVERT START TIMING

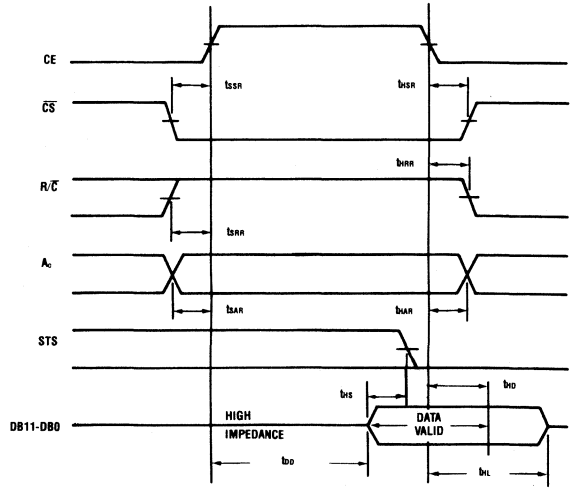


FIGURE 8. READ CYCLE TIMING

Timing Specifications +25°C Unless Otherwise Specified

Symbol	Parameter	Min	Typ	Max	Units
Convert Mode					
t_{DSC}	STS Delay from CE			200	nS
t_{HEC}	CE Pulse width	50			nS
t_{SSC}	$\overline{CS}$ to CE Setup	50			nS
t_{HSC}	$\overline{CS}$ Low during CE High	50			nS
t_{SRC}	R/$\overline{C}$ to CE Setup	50			nS
t_{HRC}	R/$\overline{C}$ Low during CE high	50			nS
t_{SAC}	A_0 to CE Setup	0			nS
t_{HAC}	A_0 Valid during CE high	50			nS
t_C	Conversion time, 12 bit cycle T min to T max	9	12	15	μS
	8 bit cycle T min to T max	6	8	10	μS
Read Mode					
t_{DD}	Access time from CE		75	150	nS
t_{HD}	Data Valid after CE low	25			nS
t_{HL}	Output float delay		100	150	nS
t_{SSR}	$\overline{CS}$ to CE setup	50			nS
t_{SRR}	R/$\overline{C}$ to CE setup	0			nS
t_{SAR}	A_0 to CE setup	50			nS
t_{HSR}	$\overline{CS}$ valid after CE low	0			nS
t_{HRR}	R/$\overline{C}$ high after CE low	0			nS
t_{HAR}	A_0 valid after CE low	50			nS
t_{HS}	STS delay after data valid	25		850	nS

NOTE: Time is measured from 50% level of digital transitions. Tested with a 50pF and 3kΩ load.

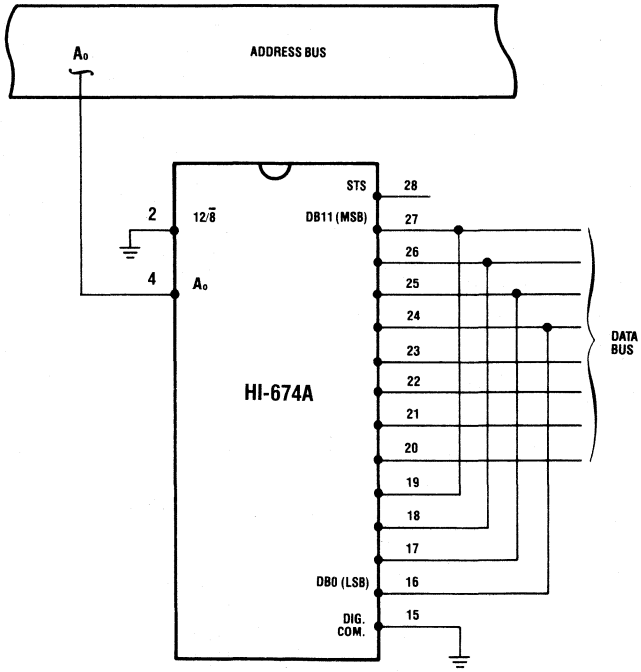


FIGURE 9. INTERFACE TO AN 8 BIT DATA BUS

Die Characteristics

Transistor Count	1117	Thermal Constants; θ_{ja}	48°C/W
Die Size; Analog	204 × 104 mils	θ_{jc}	15°C/W
Digital	158 × 84 mils	Process	Bipolar-DI
			CMOS-JI

HARRIS

HI-774

8μs, Complete 12-Bit A/D Converter With Microprocessor Interface

Features

- Complete 12 Bit A/D Converter With Reference and Clock
- Digital Error Correction
- Full 8-, 12-, or 16-Bit Microprocessor Bus Interface
- 150ns Bus Access Time
- No Missing Codes Over Temperature
- Minimal Setup Time For Control Signals
- 9μs Maximum Conversion Time Over Temperature
- Low Noise, Via Current-Mode Signal Transmission between Chips
- Byte Enable/Short Cycle (A_0 Input)
  - ▸ Guarantees break-before-make action, eliminating bus contention during read operation. Latched by the Start Convert Input (To Set the Conversion Length)
- Faster Version of the HI-574A and HI-674A
- Same Pinout as HI-574A and HI-674A
- ±12V to ±15V Operation

Applications

- Industrial Data Acquisition Systems
- Electronics Test and Scientific Instrumentation
- Process Control Systems

Description

The HI-774 is a complete 12 bit Analog-to-Digital Converter, including a +10V reference clock, three-state outputs and a digital interface for microprocessor control. Successive approximation conversion is performed by two monolithic dice housed in a 28-pin package. The bipolar analog die features the Harris Dielectric Isolation process, whch provides enhanced AC performance and freedom from latch-up. The digital die features the Smart SAR (SSAR™), which includes a digital error correction circuit.

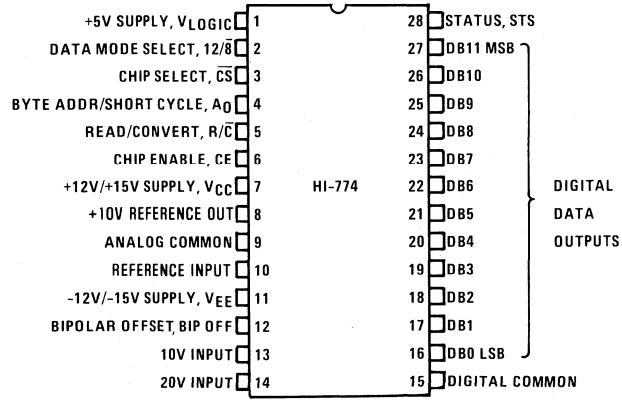
Custom design of each IC (bipolar and CMOS digital) has yielded improved performance over existing versions of this converter. The voltage comparator features high PSRR plus a high speed current-mode latch, and provides precise decisions down to 0.1 LSB of input overdrive. More than 2X reduction in noise has been achieved by using current instead of voltage for transmission of all signals between the analog and digital IC's. Also, the clock oscillator is current controlled for excellent stability over temperature.

The HI-774 offers standard unipolar and bipolar input ranges, laser trimmed for specified linearity, gain and offset accuracy. The low noise buried zener reference circuit is trimmed for minimum temperature coefficient.

Power requirements are +5V and ±12V to ±15V, with typical dissipation of 390mW at ±12V. All models are packaged in a 28 pin Ceramic Sidebrazed DIP.

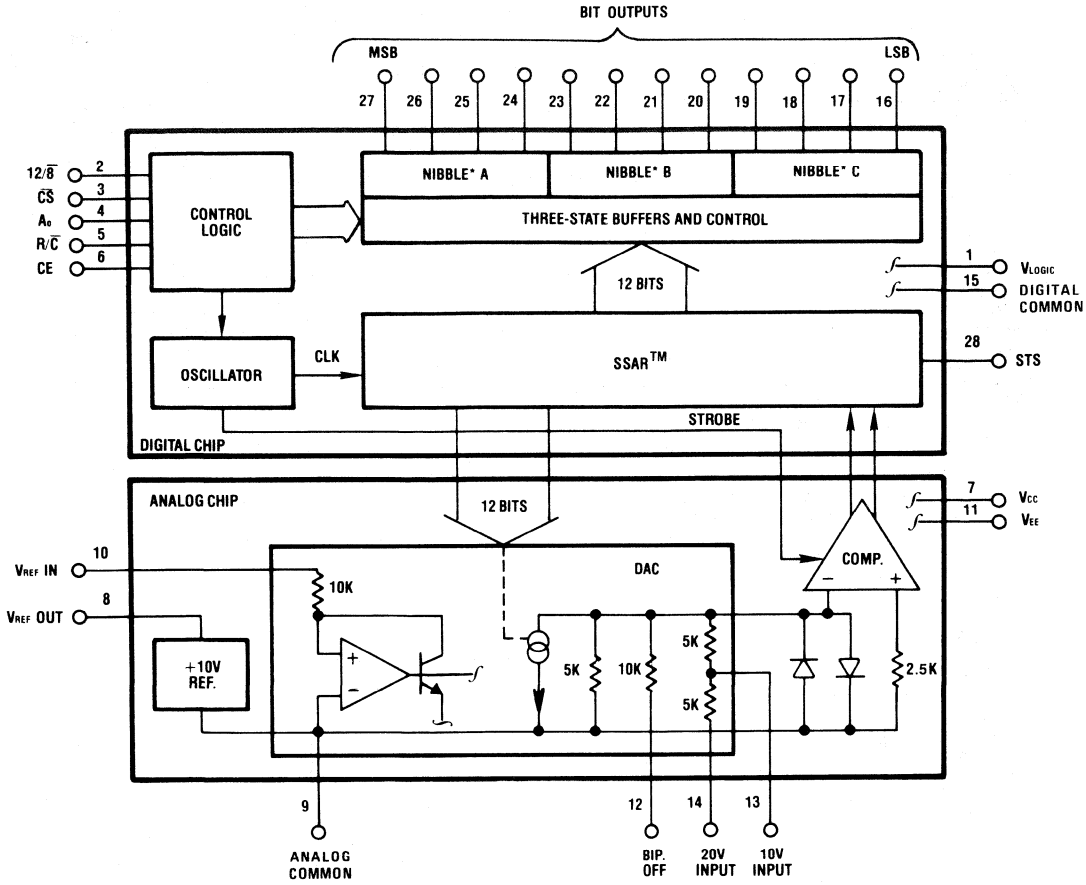
Pinout

SIDEBRAZE DIP
TOP VIEW



CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

Block Diagram



*("NIBBLE" IS A 4 BIT DIGITAL WORD.)

Die Characteristics

Transistor Count 2117

Die Dimensions

Analog ..... 204 x 104 mils

Digital ..... 200 x 82 mils

Process ..... Bipolar-DI and CMOS-JI

Thermal Constants (°C/W)

	θ_{ja}	θ_{jc}
	47	14

DC and Transfer Accuracy Specifications

(T_A = +25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = -15V or -12V unless otherwise specified)

MODEL	HI-774J	HI-774K	UNITS
Temperature Range	-5		
Resolution (max)	12	12	Bits
Linearity Error			
25°C (max)	±1	±1/2	LSB
0°C to +75°C (max)	±1	±1/2	LSB
Differential Linearity Error			
(Maximum resolution for which no missing codes is guaranteed)			
25°C	11	12	Bits
Tmin to Tmax	11	12	Bits
Unipolar Offset (max)			
(Adjustable to zero)	±2	±2	LSB
Bipolar Offset (max)			
(Adjustable to zero)	±10	±4	LSB
Full Scale Calibration Error			
25°C (max), with fixed 50Ω resistor from			
REF OUT to REF IN (Adjustable to zero)	0.3	0.3	% of F.S.
Tmin to Tmax			
(No adjustmeat at +25°C)	0.5	0.4	% of F.S.
(With adjustment to zero at +25°C)	0.22	0.12	% of F.S.
Temperature Coefficients (see definitions)			
Guaranteed max change, Tmin to Tmax (Using internal reference)			
Unipolar Offset	±2	±1	LSB
Bipolar Offset	±2	±1	LSB
Full Scale Calibration	±9	±5	LSB
Power Supply Rejection			
Max change in Full Scale Calibration			
+13.5V<V_{CC}<+16.5V or +11.4V<V_{CC}<+12.6V	±2	±1	LSB
+4.5V<V_{LOGIC}<+5.5V	±1/2	±1/2	LSB
-16.5V<V_{EE}<-13.5 or -12.6<V_{EE}<-11.4V	±2	±1	LSB
Analog Inputs			
Input Ranges			
Bipolar	-5 to +5		Volts
	-10 to +10		Volts
Unipolar	0 to +10		Volts
	0 to +10		Volts
Input Impedance			
10 Volt Span	5K, ± 25%		Ohms
20 Volt Span	10K, ± 25%		Ohms
Power Supplies			
Operating Voltage Range			
V_{LOGIC}	+4.5 to +5.5		Volts
V_{CC}	+11.4 to +16.5		Volts
V_{EE}	-11.4 to -16.5		Volts
Operating Current			
I_{LOGIC}	8 TYP, 17 MAX		mA
I_{CC} +15V Supply	11 TYP, 15 MAX		mA
I_{EE} -15V Supply	21 TYP, 28 MAX		mA
Power Dissipation ±15V, +5V Supplies	520 TYP, 730 MAX		mW
±12V, +5V Supplies	390 TYP		mW
Internal Reference Voltage, Tmin to Tmax	+10.00 ±0.05 MAX		Volts
Output current, ①	2.0 MAX		mA
available for external loads (External load should not change during conversion).			

① When supplying an external load and operating on ±12V supplies, a buffer amplifier must be provided for the Reference Output.

DC and Transfer Accuracy Specifications

(T_A = +25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = -15V or -12V unless otherwise specified)

MODEL	HI-774S	HI-774T	UNITS
Temperature Range	-2		
Resolution (max)	12	12	Bits
Linearity Error			
25°C (max)	±1	±1/2	LSB
-55°C to +125°C (Max)	±1	+1	LSB
Differential Linearity Error			
(Maximum resolution for which no missing codes is guaranteed)			
25°C	11	12	Bits
Tmin to Tmax	11	12	Bits
Unipolar Offset (max)			
(Adjustable to zero)	±2	±2	LSB
Bipolar Offset (max)			
(Adjustable to zero)	±10	±4	LSB
Full Scale Calibration Error			
25°C (max), with fixed 50Ω resistor from			
REF OUT to REF IN (Adjustable to zero)	0.3	0.3	% of F.S.
Tmin to Tmax			
(No adjustmeat at +25°C)	0.8	0.6	% of F.S.
(With adjustment to zero at +25°C)	0.5	0.25	% of F.S.
Temperature Coefficients (see definitions)			
Guaranteed max change, Tmin to Tmax (Using internal reference)			
Unipolar Offset	±2	±1	LSB
Bipolar Offset	±4	±2	LSB
Full Scale Calibration	±20	±10	LSB
Power Supply Rejection			
Max change in Full Scale Calibration			
+13.5V<V_{CC}<+16.5V or +11.4V<V_{CC}<+12.6V	±2	±1	LSB
+4.5V<V_{LOGIC}<+5.5V	±1/2	±1/2	LSB
-16.5V<V_{EE}<-13.5 or -12.6<V_{EE}<-11.4V	±2	±1	LSB
Analog Inputs			
Input Ranges			
Bipolar	-5 to +5		Volts
	-10 to +10		Volts
Unipolar	0 to +10		Volts
	0 to +10		Volts
Input Impedance			
10 Volt Span	5K, ± 25%		Ohms
20 Volt Span	10K, ± 25%		Ohms
Power Supplies			
Operating Voltage Range			
V_{LOGIC}	+4.5 to +5.5		Volts
V_{CC}	+11.4 to +16.5		Volts
V_{EE}	-11.4 to -16.5		Volts
Operating Current			
I_{LOGIC}	8 TYP, 17 MAX		mA
I_{CC} +15V Supply	11 TYP, 15 MAX		mA
I_{EE} -15V Supply	21 TYP, 28 MAX		mA
Power Dissipation ±15V, +5V Supplies	520 TYP, 730 MAX		mW
±12V, +5V Supplies	390 TYP		mW
Internal Reference Voltage, T_{min} to T_{max}	+10.00 ± .05 MAX		Volts
Output current, ①	2.0 MAX		mA
available for external loads (External load should not change during conversion).			

① When supplying an external load and operating on ±12V supplies, a buffer amplifier must be provided for the Reference Output.

Digital Specifications (All Models, Over Full Temperature Range)

	MIN	TYP	MAX
Logic Inputs (CE, $\overline{CS}$, R/$\overline{C}$, A_0, 12/$\overline{8}$)			
Logic "1"	+2.0V		+5.5V
Logic "0"	-0.5V		+0.8V
Current		0.1μA	+5μA
Capacitance		5pF	
Logic Outputs (DB11-DB0, STS)			
Logic "0" (I_{SINK} — 1.6mA)			+0.4V
Logic "1" (I_{SOURCE} — 500μA)	+2.4V		
Logic "1" (I_{SOURCE} — 10μA)	+4.5V		
Leakage (High Z State, DB11-DB0 only)		±0.1μA	±5μA
Capacitance		5pF	

HI-774 Timing Specifications (+25°C Unless Otherwise Specified) Into a load with R_L = 3kΩ and C_L = 50pF

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
CONVERT MODE					
tDSC	STS Delay From CE	-	100	200	ns
tHEC	CE Pulse Width	50	30	-	ns
tSSC	CS to CE Setup	50	20	-	ns
tHSC	CS Low During CE High	50	20	-	ns
tSRC	R/C to CE Setup	50	0	-	ns
tHRC	R/C Low During CE High	50	20	-	ns
tSAC	A_0 to CE Setup	0	0	-	ns
tHAC	A_0 Valid During CE High	50	30	-	ns
t_C	Conversion time, 12 bit Cycle Tmin to Tmax (-5)	-	8.0	9	µs
	8 bit Cycle Tmin to Tmax (-5)	-	6.4	6.8	µs
	12 bit Cycle Tmin to Tmax (-2)	-	9	11	µs
	8 bit Cycle Tmin to Tmax (-2)	-	6.8	8.3	µs
READ MODE					
tDD	Access Time From CE	-	75	150	ns
tHD	Data Valid After CE Low	25	35	-	ns
tHL	Output Float Delay	-	70	150	ns
tSSR	CS to CE Setup	50	0	-	ns
tSRR	R/C to CE Setup	0	0	-	ns
tSAR	A_0 to CE Setup	50	25	-	ns
tHSR	CS Valid After CE Low	0	0	-	ns
tHRR	R/C High After CE Low	0	0	-	ns
tHAR	A_0 Valid After CE Low	50	25	-	ns
tHS	STS Delay After Data Valid	-	90	300	ns

NOTE: Time is measured from 50% level of digital transitions, except High Z output conditions which are measured at the 10% or 90% point.

Absolute Maximum Ratings (Specifications apply to all grades, except where noted)

V_{CC} to Digital Common ..... 0 to +16.5V
V_{EE} to Digital Common ..... 0 to -16.5V
V_{LOGIC} to Digital Common ..... 0 to +7V
Analog Common to Digital Common ..... ±1V
Control Inputs (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$) to Digital Common ..... -0.5V to V_{LOGIC} +0.5V
Analog Inputs (REF IN, BIP OFF, 10V_{IN}) to Analog Common ..... ±16.5V
20V_{IN} to Analog Common ..... ±24V
REF OUT ..... Indefinite short to common
Momentary short to V_{CC}
Junction Temperature ..... +175°C
Lead Temperature, Soldering ..... 300°C, 10 sec.
Storage Temperature ..... -65°C to +150°C

Definitions of Specifications

Linearity Error

Linearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale". The point used as "zero occurs ½LSB (1.22mV for 10 volt span) before the first code transition (all zeros to only the LSB "on"). "Full scale" is defined as a level 1½LSB beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The HI-774K and L, grades are guaranteed for maximum nonlinearity of ±½LSB. For these grades, this means that an analog value which falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The HI-774J grade is guaranteed to ±1LSB max error. For this grade, an analog value which falls within a given code width will result in either the correct code for that region or either adjacent one.

Note that the linearity error is not user-adjustable.

Differential Linearity Error (No Missing Codes)

A specification which guarantees no missing codes requires that every combination appear in a monotonic increasing sequence as the analog input level is increased. Thus every code must have a finite width. For the HI-774 K and L grades which guarantee no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temerature ranges. The HI-774J grade guarantees no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11 bits must be present; in practice very few of the 12-bit codes are missing.

Unipolar Offset

The first transition should occur at a level ½LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following pages. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with or without external adjustment.

Bipolar Offset

Similarly, in the bipolar mode, the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value ½LSB below analog common. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error over temperature.

Full Scale Calibration Error

The last transition (from 1111 1111 1110 to 1111 1111 1111) should occur for an analog value 1½LSB below the nominal full scale (9.9963 volts for 10.000 volts full scale). The full scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which is typically 0.05 to 0.1% of full scale, can be trimmed out as shown in Figures 2 and 3. The full scale calibration error over temperature is given with and without the initial error trimmed out. The temperature coefficients for each grade indicate the maximum change in the full scale gain from the initial value using the internal 10 volt reference.

Temperature Coefficients

The temperature coefficients for full-scale calibration, unipolar offset, and bipolar offset specify the maximum change from the initial (25°C) value to the value at Tmin or Tmax.

Power Supply Rejection

The standard specifications for the HI-774 assume use of +5.00 and ±15.00 or ±12.00 volt supplies. The only effect of power supply error on the performance of the device will be a small change in the full scale calibration. This will result in a linear change in all lower order codes. The specifications show the maximum change in calibration from the initial value with the supplies at the various limits.

Code Width

A fundamental quantity for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 least significant bit (LSB) of the full scale range or 2.44mV out of 10 volts for a 12-bit ADC.

Quantization Uncertainty

Analog-to-digital converters exhibit an inherent quantization uncertainty of ±½LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of given resolution.

Left-Justified Data

The data format used in the HI-774 is left-justified. This means that the data represents the analog input as a fraction of full-scale, ranging from 0 to $\frac{4095}{4096}$. This implies a binary point to the left of the MSB.

Applying the HI-774

For each application of this converter, the ground connections, power supply bypassing, analog signal source, digital timing and signal routing on the circuit board must be optimized to assure maximum performance. These areas are reviewed in the following sections, along with basic operating modes and calibration requirements.

PHYSICAL MOUNTING AND LAYOUT CONSIDERATIONS

Layout—

Unwanted, parasitic circuit components, (L, R, and C) can make 12 bit accuracy impossible, even with a perfect A/D converter. The best policy is to eliminate or minimize these parasitics through proper circuit layout, rather than try to quantify their effects.

The recommended construction is a double-sided printed circuit board with a ground plane on the component side. Other techniques, such as wire-wrapping or point-to-point wiring on vectorboard, will have an unpredictable effect on accuracy.

In general, sensitive analog signals should be routed between ground traces and kept well away from digital lines. If analog and digital lines must cross, they should do so at right angles.

Power Supplies

Supply voltages to the HI-774 (+15V, -15V and +5V) must be "quiet" and well regulated. Voltage spikes on these lines can affect the converter's accuracy, causing several LSB's to flicker when a constant input is applied. Digital noise and spikes from a switching power supply are especially troublesome. If switching supplies must be used, outputs should be carefully filtered to assure "quiet" DC voltage at the converter terminals.

Further, a bypass capacitor pair on each supply voltage terminal is necessary to counter the effect of variations in supply current. Connect one pair from pin 1 to 15 (V_{LOGIC} supply), one from pin 7 to 9 (V_{CC} to Analog Common) and one from pin 11 to 9 (V_{EE} to Analog Common). For each capacitor pair, a 10μF tantalum type in parallel with a 0.1μF ceramic type is recommended.

Ground Connections

The typical HI-774 ground currents are 6mADC into pin 9 (Analog Common) and 3mADC out of pin 15 (Digital Common). These pins should be tied together at the package to guarantee specified performance for the converter. In addition, a wide PC trace should run directly from pin 9 to (usually) 15V common, and from pin 15 to (usually) the +5V Logic Common. If the converter is located some distance from the system's "single point" ground, make only these connections to pins 9 and 15: Tie them together at the package, and back to the system ground with a single path. This path should have low resistance since it will carry about 3mA of DC current. (Code dependent currents flow in the VCC, VEE and VLOGIC terminals, but not through the HI-774's Analog Common or Digital Common).

ANALOG SIGNAL SOURCE

The device driving the HI-774 analog input will see a nominal load of 5KΩ (10V range) or 10KΩ (20V range). However, the other end of these input resistors may change as much as $\pm$400mV with each bit decision. These input disturbances are caused by the internal DAC changing codes which causes a glitch on the summing junction. This creates abrupt changes in current at the analog input causing a "kick back" glitch from the input. Because the algorithm starts with the MSB, the first glitches will be the largest and get smaller as the conversion proceeds. These glitches can occur at 350ns intervals so an op-amp with a low output impedance and fast settling is desirable. Ultimately, the input must settle to within the window of figure 1 at the bit decision points in order to achieve 12 bit accuracy.

The HI-774 differs from the most high-speed successive approximation type ADC's in that it does not require a high performance buffer or sample and hold. With error correction the input can settle while the conversion is underway, but only during the first 4.8μs. The input must be within $\pm$0.76% of the final value when the MSB decision is made. This occurs approximately 650ns after the conversion has been initiated. Digital error correction also loosens the bandwidth requirements of the buffer or sample and hold. As long as the input "kick back" disturbances settle within the window of figure 1 the device will remain accurate. The combined effect of settling and the "kick back' disturbances must remain in the figure 1 window.

If the design is being optimized for speed, the input device should have a closed loop bandwidth to 3MHz, and a low output impedance (calculated by dividing the open loop output resistance by the open loop gain). If the application requires a high speed sample and hold the Harris HA-5330 or HA-5320 are recommended.

In any design the input (pin 13 or 14) should be checked during a conversion to make sure that the input stays within the correctable window of figure 1.

DIGITAL ERROR CORRECTION

The HI-774 features the smart sucessive approximation register (SSAR™) which includes digital error correction. This has the advantage of allowing the initial input to vary within a +31 to -32LSB window about the final value. The input can move during the first 4.8μs, after which it must remain stable within ±½LSB. With this feature a conversion can start before the input has settled completely; however, it must be within the window as described in Figure 1.

The conversion cycle starts by making the first 8-bit decisions very quickly, allowing the internal DAC to settle only to 8-bit accuracy. Then the converter goes through two error correction cycles. At this point the input must be stable within ±½LSB. These cycles correct the 8-bit word to 12-bit accuracy for any errors made (up to +16 or -32 bits). This is up one count or down two counts at 8-bit resolution. The converter then continues to make the 4LSB decisions, settling out to 12-bit accuracy. The last four bits can adjust the code in the positive direction by up to 15 bits. This results in a total correction range of +31 to -32 bits. When an 8-bit conversion is performed, the input must settle to within ±½LSB at 8 bit resolution (which equals ±8 bits at 12-bit resolution).

With the HI-774 a conversion can be initiated before the input has completely settled, as long as it meets the constraints of the Figure 1 window. This allows the user to start conversion up to 4.8μs earlier than with a typical analog to digital converter. A typical successive approximation type ADC must have a constant input during a conversion because once a bit decision is made it is locked in and cannot change.

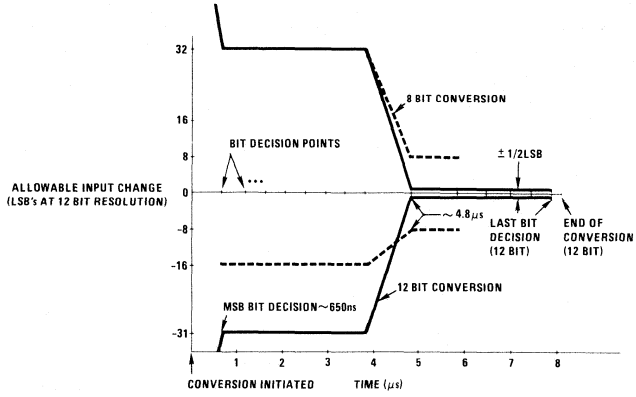


FIGURE 1. HI-774 ERROR CORRECTION WINDOW VS. TIME

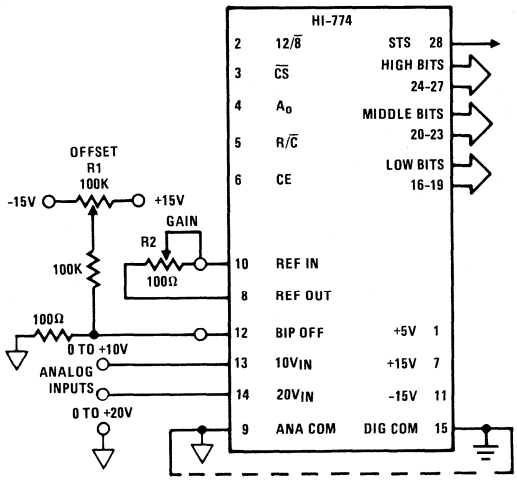


FIGURE 2. UNIPOLAR CONNECTIONS

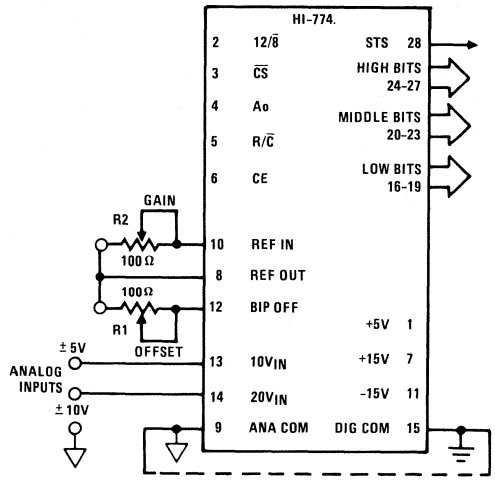


FIGURE 3. BIPOLAR INPUT CONNECTIONS

RANGE CONNECTIONS AND CALIBRATION PROCEDURES

The HI-774 is a "complete" A/D converter, meaning it is fully operational with addition of the power supply voltages, a Start Convert signal, and a few external components as shown in figures 2 and 3. Nothing more is required for most applications.

Whether controlled by a processor or operating in the stand-alone mode, the HI-774 offers four standard input ranges: 0V to +10V, 0V to +20V, ±5V and ±10V. The maximum errors for gain and offset are listed under Specifications. If required, however, these errors may be adjusted to zero as explained below. Power supply and ground connections have been discussed in an earlier section.

Unipolar Connections and Calibration—

Refer to figure 2. The resistors shown* are for calibration of offset and gain. If this is not required, replace R2 with a 50Ω, 1% metal film resistor and remove the network on pin 12. Connect pin 12 to pin 9. Then, connect the analog signal to pin 13 for the 0V to 10V range, or to pin 14 for the 0V to 20V range. Inputs to +20V (5V over the power supply) are no problem—the converter operates normally.

Calibration consists in adjusting the converters's most negative output to its ideal value (offset adjustment), then, adjusting the most positive output to its ideal value (gain adjustment). To understand the procedure, note that in principle, one is settling the output with respect to the midpoint of an increment of analog input, as denoted by two adjacent code changes. Nominal value of an increment is one LSB. However, this approach is impractical because nothing "happens" at a midpoint to indicate that an adjustment is complete. Therefore, calibration is performed in terms of the observable code changes instead of the midpoint between code changes.

For example, midpoint of the first LSB increment should be positioned at the origin, with an output code of all 0's. To do this, apply an input of +½LSB (+1.22mV for the 10V range; +2.44mV for the 20V range). Adjust the Offset potentiometer R1 until the first code transition flickers between 0000 0000 0000 and 0000 0000 0001.

Next, perform a Gain Adjust at positive full scale. Again, the ideal input corresponding to the last code change is applied. This is 1½LSB's below the nominal full scale (+9.9963V for 10V range; +19.9927V for 20V range). Adjust the Gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

Bipolar Connections and Calibration—

Refer to Figure 3. The gain and offset errors listed under Specifications may be adjusted to zero using potentiometers R1 and R2*. If this isn't required, either or both pots may be replaced by a 50Ω, 1% metal film resistor.

Connect the Analog signal to pin 13 for a ±5V range, or to pin 14 for a ±10V range. Calibration of offset and gain is similar to that for the unipolar ranges as discussed above. First apply a DC input voltage ½LSB above negative full scale (i.e., -4.9988V for the ±5V range, or -9.9976V for the ±10V range). Adjust the offset potentiometer R1 for flicker between output codes 0000 0000 0000 and 0000 0000 0001. Next, apply a DC input voltage 1½LSB's below positive full scale (+4.9963V for ±5V range; +9.9927V for ±10V range). Adjust the Gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

*The 100Ω potentiometer R2 provides Gain Adjust for the 10V and 20V ranges. In some applications, a full scale of 10.24V (LSB equals 2.5mV) or 20.48V (LSB equals 5.0mV) is more convenient. For these, replace R2 by a 50Ω, 1% metal film resistor. Then, to provide Gain Adjust for the 10.24V range, add a 200Ω potentiometer in series with pin 13. For the 20.48 range, add a 500Ω potentiometer in series with the pin 14.

Controlling the HI-774

The HI-774 includes logic for direct interface to most microprocessor systems. The processor may take full control of each conversion, or the converter may operate in the "stand-alone" mode, controlled only by the R/$\overline{C}$ input. Full control consists of selecting an 8 or 12 bit conversion cycle, initiating the conversion, and reading the output data when ready—choosing either 12 bits at once or 8 followed by 4, in a left-justified format. The five control inputs are all TTL/CMOS- compatible: (12/$\overline{8}$, $\overline{CS}$, A_0, R/$\overline{C}$ and CE). Table 1 illustrates the use of these inputs in controlling the converter's operations. Also, a simplified schematic of the internal control logic is shown in Figure 4.

"Stand-Alone Operation"

The simplest control interface calls for a single control line connected to R/$\overline{C}$. Also, CE and 12/8 are wired high, $\overline{CS}$ and A_0 are wired low, and the output data appears in words of 12 bits each.

The R/$\overline{C}$ signal may have any duty cycle within (and including) the extremes shown in Figures 5 and 6. In general, data may be read when R/$\overline{C}$ is high unless STS is also high, indicating a conversion is in progress. Timing parameters particular to this mode of operation are listed in the "Stand-Alone Mode Timing" chart.

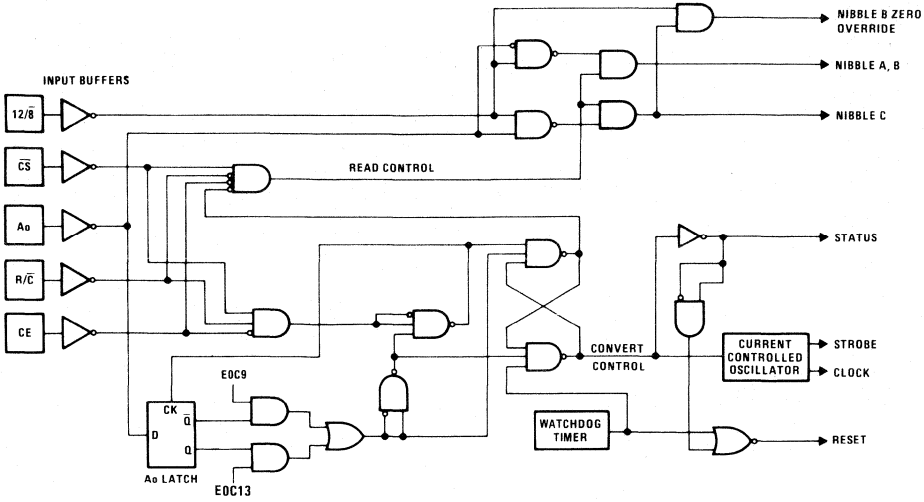


FIGURE 4. HI-774 CONTROL LOGIC

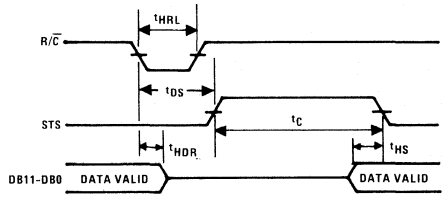


FIGURE 5. LOW PULSE FOR R/$\overline{C}$—OUTPUTS ENABLED AFTER CONVERSION

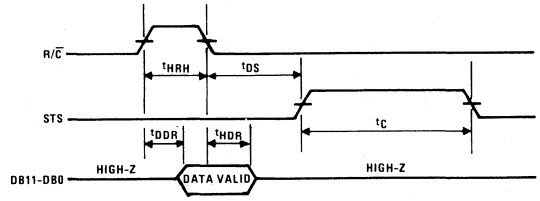


FIGURE 6. HIGH PULSE FOR R/$\overline{C}$—OUTPUTS ENABLE WHILE R/$\overline{C}$ HIGH, OTHERWISE HIGH-Z

Stand-Alone Mode Timing

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{HRL}	Low R/$\overline{C}$ Pulse Width	50			ns
t_{DS}	STS Delay from R/$\overline{C}$			200	ns
t_{HDR}	Data Valid After R/$\overline{C}$ Low	20			ns
t_{HS}	STS Delay After Data Valid		90	300	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	150			ns
t_{DDR}	Data Access Time			150	ns

Conversion Length

A Convert Start transition (see Table 1) latches the state of A_0, which determines whether the conversion continues for 12 bits (A_0 low) or stops with 8 bits (A_0 high). If all 12 bits are read following an 8 bit conversion, the last three LSB's will read zero and DB3 will read ONE. A_0 is latched because it is also involved in enabling the output buffers (see "Reading the Output Data"). No other control inputs are latched.

TABLE 1
TRUTH TABLE FOR HI-774 CONTROL INPUTS

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12 bit conversion
↑	0	0	X	1	Initiate 8 bit conversion
1	↓	0	X	0	Initiate 12 bit conversion
1	↓	0	X	1	Initiate 8 bit conversion
1	0	↓	X	0	Initiate 12 bit conversion
1	0	↓	X	1	Initiate 8 bit conversion
1	0	1	1	X	Enable 12 bit Output
1	0	1	0	0	Enable 8 MSB's Only
1	0	1	0	1	Enable 4 LSB's Plus 4 Trailing Zeroes

Conversion Start

A conversion may be initiated as shown in Table 1 by a logic transition on any of three inputs: CE, $\overline{CS}$ or R/$\overline{C}$. The last of the three to reach the correct state starts the conversion, so one, two or all three may be dynamically controlled. The nominal delay from each is the same, and if necessary, all three may change state simultaneously. To assure that a particular input controls the start of conversion, the other two should be set up at least 50nS earlier, however. See the HI-774 Timing Specifications, Convert mode.

This variety of HI-774 control modes allows a simple interface in most system applications. The Convert Start timing relationships are illustrated in Figure 7.

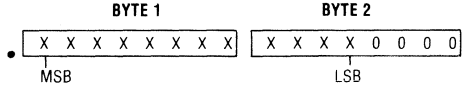
The output signal STS indicates status of the converter by going high only while a conversion is in progress. While STS is high, the output buffers remain in a high impedance state and data cannot be read. Also, an additional Start Convert will not reset the converter or reinitiate a conversion while STS is high.

Reading the Output Data

The output data buffers remain in a high impedance state until four conditions are met: R/$\overline{C}$ high, STS low, CE high and $\overline{CS}$ low. At that time, data lines become active according to the state of inputs 12/$\overline{8}$ and A_0. Timing constraints are illustrated in Figure 8.

The 12/$\overline{8}$ input will be tied high or low in most applications, though it is fully TTL/CMOS-compatible. With 12/$\overline{8}$ high, all 12 output lines become active simultaneously, for interface to a 12 or 16 bit data bus. The A_0 input is ignored.

With 12/8 low, the output is organized in two 8 bit bytes, selected one at a time by A_0. This allows an 8 bit data bus to be connected as shown in figure 9. A_0 is usually tied to the least significant bit of the address bus, for storing the HI-774 output in two consecutive memory locations. (With A_0 low, the 8 MSB's only are enabled. With A_0 high, 4 MSB's are disabled, bits 4 through 7 are forced low, and the 4 LSB's are enabled). This two byte format is considered "left justified data", for which a decimal (or binary!) point is assumed to the left of byte 1:



Further, A_0 may be toggled at any time without damage to the converter. Break-before-make action is guaranteed between the two data bytes, which assures that the outputs strapped together in Figure 9 will never be enabled at the same time.

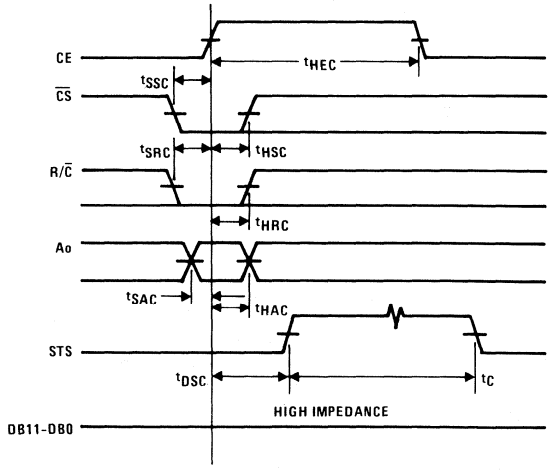


FIGURE 7. CONVERT START TIMING

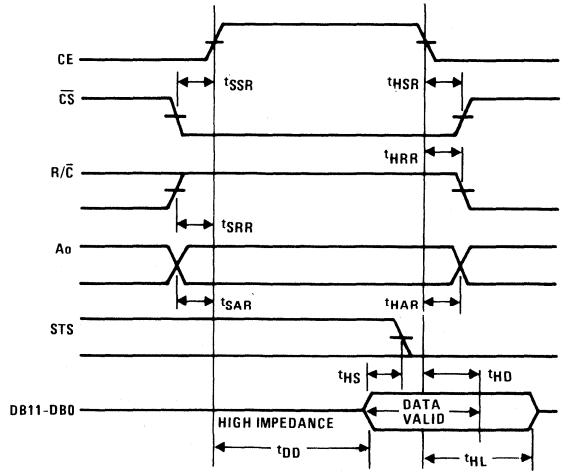


FIGURE 8. READ CYCLE TIMING

See HI-774 Timing Specifications for more information

A read operation usually begins after the conversion is complete and STS is low. For earliest access to the data however, the read should begin no later than ($t_{DD} + t_{HS}$) before STS goes low. See Figure 8.

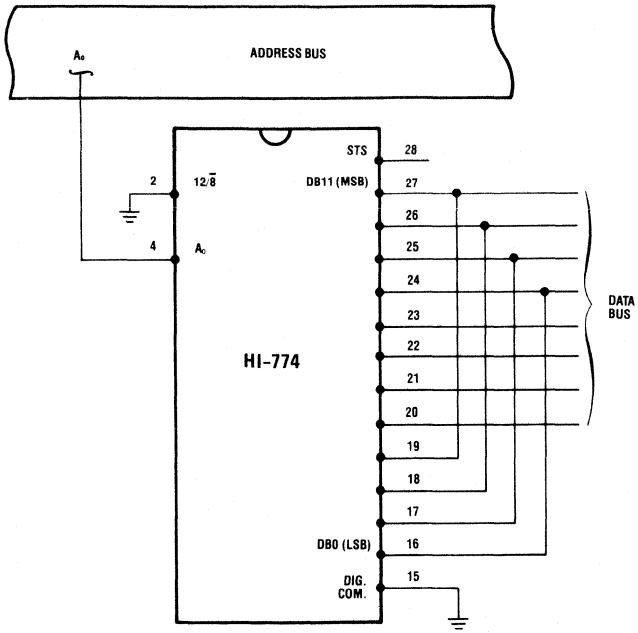


FIGURE 9. INTERFACE TO AN 8 BIT DATA BUS

HI-774 Ordering Guide

MODEL	TEMPERATURE RANGE	LINEARITY ERROR MAX (T_{MIN} TO T_{MAX})	RESOLUTION (NO MISSING CODES, T_{MIN} TO T_{MAX})	FULL SCALE TC (PPM/°C MAX)
HI1-774J-5	0°C To +75°C	±1 LSB	11 Bits	45.0
HI1-774K-5	0°C To +75°C	±1/2 LSB	12 Bits	25.0
HI1-774S-2	-55°C To +125°C	±1 LSB	11 Bits	50.0
HI1-774T-2	-55°C To +125°C	±1 LSB	12 Bits	25.0

ANALOG

Digital-to-Analog Converters

6

ABSOLUTE MAXIMUM RATINGS

As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Specifications" are the only conditions recommended for satisfactory operation.

Ordering Information

HARRIS PRODUCT CODE EXAMPLE

H I 1 — 0562A — 5

PREFIX:
H (HARRIS)

FAMILY:
A : Analog
C : Communications
D : Digital
F : Filters
I : Interface
M : Memory
V : Analog High Voltage
Y : Analog Hybrids

PACKAGE:
1 : Dual-In-Line Ceramic
2 : Metal Can
3 : Dual-In-Line Plastic
4 : Leadless Chip Carriers (LCC)
5 : LCC Hybrid
7 : Mini-DIP, Ceramic
0 : Chip Form

PART NUMBER

TEMPERATURE:
1 : 0°C to +200°C *
2 : -55°C to +125°C
4 : -25°C to +85°C
5 : 0°C to +75°C
6 : 100% +25°C Probe (Dice Only)
7 : Dash-7 High Reliability Commercial Product 0°C to +75°C
8 : Dash-8 Program HA2-2520-8 (Example Only)
9 : -40°C to +85°C

* Special High Temperature Testing Available on Certain Product Types. Consult Factory for Availability.

Standard Products Packaging Availability†

PACKAGE	PLASTIC DIP	CERAMIC DIP					SURFACE MOUNT LCC
TEMPERATURE	-5	-2	-4	-5	-7	-8	-8
DEVICE NUMBER							
DIGITAL TO ANALOG							
HI-562A		J		J		**	**
HI-565A		J		J		J	
HI-5618A		D		D		D	
HI-5618B		D		D		D	
HI-5660		J		J		J	
HI-5660A		J		J		J	
HI-5680I				J			
HI-5680V				J	J		
HI-5685AI			J				
HI-5685AV			J				
HI-5685I			J				
HI-5685V			J				
HI-5687I		J				J	
HI-5687V		J				J	**
HI-5690V				J			
HI-5695V			J				
HI-5697V		J				**	**
HI-DAC16B/16C				L			

** Available as MIL-STD-883 Only.
† Letter codes in this chart indicate available packages as shown in Packaging Section 11.

Selection Guide

)/A CONVERTERS

PART NUMBER	FEATURES	RESOLUTION (BITS)	MAXIMUM OUTPUT RANGE	SETTLING TIME TO ±1/2 LSB (TYP)	GAIN ERROR (% FSR)	DIFFERENTIAL NON-LINEARITY (MAX @ 25°C) (LSB) -5/-2	INTEGRAL NON-LINEARITY (MAX @ 25°C) (LSB) -5/-2	REFERENCE REQUIREMENTS VIN/RIN (V/Ω)	SUPPLY VOLTAGE POWER DISSIPATION † (V/mW, TYP)	DIP PACKAGE PIN COUNT	PAGE
HI-562A	Industry Standard	12	-2mA	300ns	±0.024	±1/2 to ±1/4	±1/2 to ±1/4	+10/20K	+5, -15/280	24*	6-4
HI-565A	+10V Reference On-Chip	12	-2mA	350ns	±0.1	±1/2 to ±3/4	±1/4 to ±1/2	+10/20K (Internal)	±15/320	24	6-10
HI-5618A	High Speed	8	-5mA	65ns	±0.78	±1/4	±1/4	+10/8K	+5, -15/330	18	6-17
HI-5618B	High Speed	8	-5mA	65ns	±0.78	±1/2	±1/2	+10/8K	+5, -15/330	18	6-17
HI-5660	Low Glitch	12	-2mA	500ns	±0.1	±3/4	±1/2	+10/20K	±15/230	24	6-24
HI-5660A	Low Glitch	12	-2mA	500ns	±0.1	±1/2	±1/4	+10/20K	±15/230	24	6-24
HI-5680V/I	Voltage Current DAC 80, 0°C to +75°C	12	±10V -2mA	1.5µs/ 300ns	±0.1	±3/4	±1/2	+6.3/12.6K (Internal)	+5, ±12/320	24	6-33
HI-5685V/I	Voltage/Current DAC 80, -25°C to +85°C	12	±10V -2mA	1.5µs/ 300ns	±0.1	±3/4	±1/2	+6.3/12.6K (Internal)	+5, ±12/320	24	6-39
HI-5685AV/I	Voltage/Current Low Drift -25°C to +85°C	12	±10V -2mA	1.5µs/ 300ns	±0.1	±3/4	±1/2	+6.3/12.6K (Internal)	+5, ±12/320	24	6-39
HI-5687V/I	Voltage/Current DAC 80, -55°C to +125°C	12	±10V -2mA	1.5µs/ 300ns	±0.1	±3/4	±1/2	+6.3/12.6K (Internal)	+5, ±12/320	24*	6-45
HI-5690V	Fast Settling V_O; DAC 80 0°C to +75°C	12	±10V	750ns	±0.1	±3/4	±1/2	+6.3/12.6K (Internal)	±12/555	24	6-51
HI-5695V	Fast Settling V_O; DAC 80, -25°C to +85°C	12	±10V	750ns	±0.1	±3/4	±1/2	+6.3/12.6K (Internal)	±12/555	24	6-51
HI-5697V	Fast Settling V_O; DAC 80, -55°C to +125°C	12	±10V	750ns	±0.1	±3/4	±1/2	+6.3/12.6K (Internal)	±12/555	24*	6-51
HI-DAC16B	16 Bit Monolithic	16	-2mA	1.0µs (14 Bits)	±0.1	±1 Typ	±1.5 Typ	+10/10K	±15/465	40	6-57
HI-DAC16C	16 Bit Monolithic	16	-2mA	1.0µs (14 Bits)	±0.1	±2 Typ	±3 Typ	+10/10K	±15/465	40	6-57

* Surface mount package available.

† Most supplies can be varied from ±12 volts to ±15 volts, please see data sheets for specific information.

HARRIS

HI-562A

12-Bit High Speed Monolithic Digital-to-Analog Converter

Features

- Output Current ..... 2mA, F.S.
- Monolithic Construction
- Extremely Fast Settling ..... 300ns To 0.01% (Typ)
- Low Gain Drift ..... ±10ppm/°C (Max)
- Linearity Guaranteed Over Temperature... ±1/2 LSB (Max)
- Designed for Minimum Glitches
- Monotonic Over Temperature

Applications

- CRT Display Generation
- High Speed A/D Converters
- Video Signal Reconstruction
- Waveform Synthesizers
- High Speed Data Acquisition
- High-Rel Applications
- Precision Instruments

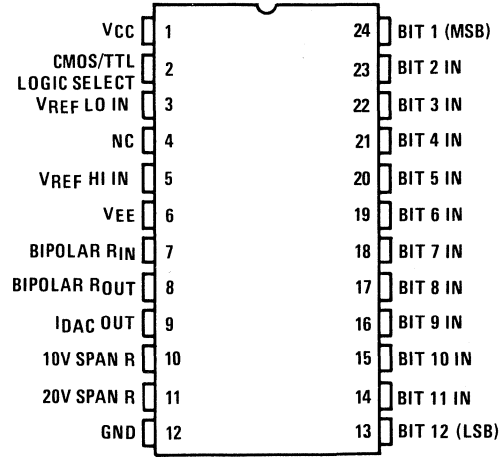
Description

The Harris HI-562A is the first monolithic digital-to-analog converter to combine both high speed performance and 12-bit accuracy on the same chip. The HI-562A's fast output current settling of 300ns to 0.01% is achieved using Dielectric Isolation processing to reduce internal parasitics for fast rise and fall times during switching. Output glitches are minimized in the HI-562A by incorporating equally weighted current sources switched into an R-2R ladder network for symmetrical turn-ON and turn-OFF switching times. This creates within the chip a very uniform and constant thermal distribution for excellent linearity and also completely eliminates thermal transients during switching. High stability thin film resistor processing together with laser trimming provide the HI-562A with guaranteed 12-bit linearity to within ±1/2LSB maximum at +25°C for -4 and -5 parts and to within ±1/4LSB maximum at +25°C for -2 and -8 parts. The HI-562A is recommended as a replacement for higher cost hybrid and modular units for increased reliability and accuracy in applications such as CRT displays, precision instruments and data acquisition systems requiring throughput rates as high as 3.3MHz for full range transitions. Its small size makes it an ideal choice as the heart of high speed A/D converter designs or as a building block in high speed or high resolution industrial process control systems. The HI-562A is also ideally suited for aircraft and space instrumentation where operation over a wide temperature range is required.

The HI-562A is offered in commercial, industrial and military grades. The HI-562A is available in a 24 pin Ceramic Sidebraze DIP. For MIL-STD-883 compliant parts, request the HI-562A/883 data sheet.

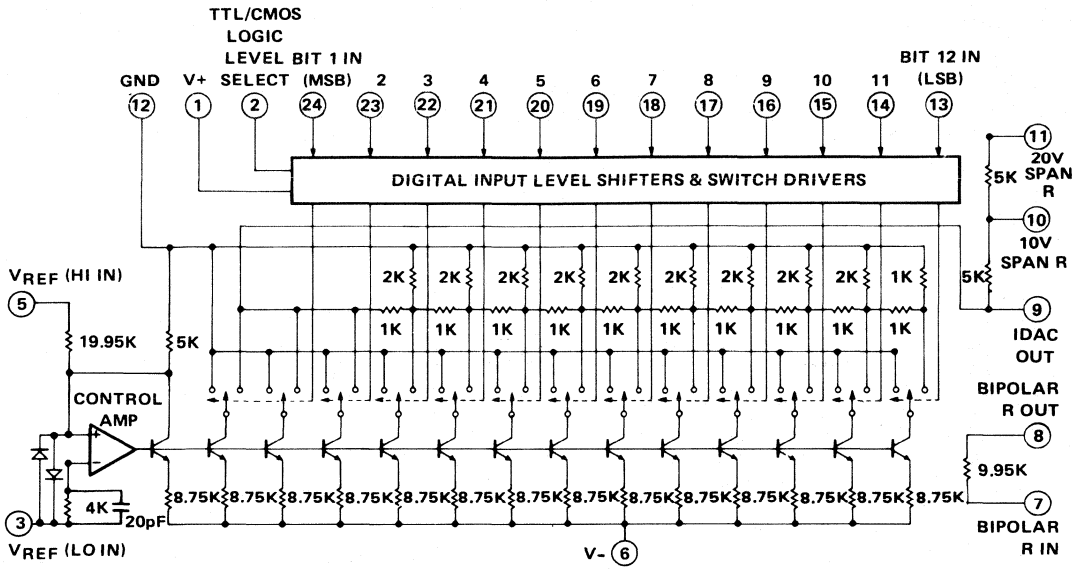
Pinouts

HI1-562A (CERAMIC SIDEBRAZE DIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC handling procedures.

Functional Diagram



NOTE: Pin Numbers Refer to DIP Package Only.

Absolute Maximum Ratings (Referred to GND, Note 1)

Power Supply Inputs
- V_{PS+} ..... +20V
- V_{PS-} ..... -20V

Reference Inputs
- V_{REF} (High) ..... ±16.5V

Digital Inputs
- Bits 1-12 (TTL) ..... -1V, +7.5V
- Bits 1-12 (CMOS) ..... -1V, V_{PS+}
- CMOS/TTL Logic Select ..... -1V, +16.5V

Outputs
- Pins 7, 8, 10, 11 ..... $\pm V_{PS}$
- Pin 9 ..... $+V_{PS}$, -5V

Junction Temperature ..... +175°C

Operating Temperature Range

HI-562A-2 ..... -55°C to +125°C
HI-562A-4 ..... -25°C to +85°C
HI-562A-5 ..... 0°C to +75°C
Storage Temperature Range ..... -65°C to +150°C

Electrical Specifications

(@ +25°C, V_{PS+} = +5V, V_{PS-} = -15V, V_{REF} = +10V, CMOS/TTL Logic Select = GND, Unless Otherwise Specified.)

PARAMETER	CONDITION	HI-562A-2 MIN	HI-562A-2 TYP	HI-562A-2 MAX	HI-562A-4/HI-562A-5 MIN	HI-562A-4/HI-562A-5 TYP	HI-562A-4/HI-562A-5 MAX	UNITS
INPUT CHARACTERISTICS								
Digital Inputs (Note 3)	Bit ON "Logic 1"							
TTL/CMOS Input Voltage (Note 2)	Bit OFF "Logic 0"							
Logic "1"		2.0			2.0			V
Logic "0"	(V_{PS+} <9.5V)			0.8			0.8	V
Input Current (Note 2)	Pin 2 Tied to Pin 12							
Logic "1"	Over Full Temperature Range		20	±500		20	±500	nA
Logic "0"			-50	-100		-50	-100	µA
CMOS Input Voltage								
Logic "1"		0.7V_{PS+}			0.7V_{PS+}			V
Logic "0"	Pin 2 Tied to Pin 1			0.3V_{PS+}			0.3V_{PS+}	V
Input Current	($V_{PS+} \geq$ +9.5V)							
Logic "1"	Over Full Temperature Range		20	±500		20	±500	nA
Logic "0"			-50	-100		50	-100	µA
Reference Input								
Input Resistance	(±20%)		19.95K			19.95K		Ω
Input Voltage			+10			+10		V
TRANSFER CHARACTERISTICS								
Resolution	Over Full Temperature Range			12			12	Bits
Nonlinearity (Note 3)	@ +25°C			±1/4		±1/4	±1/2	LSB
	Over Full Temperature Range		±1/2	±1			±1	LSB
Differential Nonlinearity (Note 3)	@ +25°C			±1/4		±1/4	±1/2	LSB
	Over Full Temperature Range		MONOTONICITY GUARANTEED					
Relative Accuracy (Note 6)	With 50Ω (1%) Resistors							
Gain Error	All Bits ON		±0.024	±0.25		±0.024	±0.25	%FSR
Bipolar Offset Error	All Bits OFF		±0.024	±0.25		±0.024	±0.25	%FSR
Unipolar Offset Error	All Bits OFF		±0.012	±0.05		±0.012	±0.05	%FSR (Note 4)
Adjustment Range	See Operating Instructions							
Gain	With 100Ω Trim		±0.3			±0.3		%FSR
Bipolar Offset	Potentiometers		±0.6			±0.6		%FSR
Temperature Stability	Drift Specified With Internal Span Resistors For Volt. Output							
Gain Drift (Note 3)	Over Full Temperature Range		±6	±10			±10	ppm of FSR/°C
Offset Drift (Note 3)	Over Full Temperature Range							
Unipolar Offset	All Bits OFF			±2			±2	ppm of FSR/°C
Bipolar Offset	All Bits OFF			±4			±4	
Differential Nonlin.	Over Full Temperature Range		±1	±2		±1	±2	ppm of FSR/°C
Settling Time (Note 3) to ±1/2LSB	All Bits ON-to-OFF or OFF-to-ON		300	400		300	400	ns

Electrical Specifications (Continued)

PARAMETER	CONDITIONS	HI-562A-2 MIN	HI-562A-2 TYP	HI-562A-2 MAX	HI-562A-4/HI-562A-5 MIN	HI-562A-4/HI-562A-5 TYP	HI-562A-4/HI-562A-5 MAX	UNITS
Major Carry Transient								
Peak Amplitude Settling	From 011...1 to 100...0		0.7			0.7		mA
Time to 90% Complete	or 100...0 to 011...1		35			35		ns
Power Supply Sensitivity (Note 3)								
Unipolar Offset								
V_{ps+} @ +5V or +15V	All Bits OFF		±0.5			±0.5		ppm of FSR/ %V_{ps}
V_{ps-} @ -15V	"		±0.5			±0.5		
Bipolar Offset								
V_{ps+} @ +5V or +15V	All Bits OFF, Bipolar Mode		±1.5			±1.5		ppm of FSR/ %V_{ps}
V_{ps-} @ -15V	"		±1.5			±1.5		
Gain								
V_{ps+} @ +5V or +15V	All Bits ON			±3.5			±3.5	ppm of FSR/ %V_{ps}
V_{ps-} @ -15V				±7.5			±7.5	
OUTPUT CHARACTERISTICS								
Output Current								
Unipolar		-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar		±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance			2K			2K		Ω
Capacitance			20			20		pF
Output Voltage Ranges								
Unipolar	Using External Op Amp		0 to +5			0 to +5		V
	and Internal Scaling Resistors.		0 to +10			0 to +10		V
Bipolar	See Figure 1 and Table 1		±2.5			±2.5		V
	For Connections		±5			±5		V
			±10			±10		V
Compliance Limit (Note 3)		-3		+10	-3		+10	V
Compliance Voltage (Note 3)	Over Full Temperature Range		±1.0			±1.0		V
Output Noise	0.1 to 10Hz (All Bits ON)		30			30		μV_{p-p}
	0.1 to 5MHz (All Bits ON)		100			100		μV_{p-p}
POWER REQUIREMENTS								
V_{ps+} (Note 7)	Over Full Temperature Range	4.5	5	16.5	4.75	5	16.5	V
V_{ps-}	Over Full Temperature Range	-13.5	-15	-16.5	-13.5	-15	-16.5	V
I_{ps+} (Note 5)	All Bits ON or OFF in Either		8	15		8	15	mA
I_{ps-} (Note 5)	TTL or CMOS Mode (25°C)		16	23		16	23	mA
I_{ps+} (Note 5)	Same as Above Except		11	20		11	20	mA
I_{ps-} (Note 5)	Over Full Temperature Range		20	30		20	30	mA
Power Dissipation (25°C)	V_{ps+} = +5V, V_{ps-} = -15V		280	420		280	420	mW

NOTES:
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. V_{ps+} tolerance is ±10% for HI-562A-2, and ±5% for HI-562A-4, -5.
3. See Definitions.
4. FSR is "Full Scale Range" and is 20V for ±10V ranges, 10V for ±5V ranges, etc., or 2mA (±20%) for current output.
5. After 30 seconds warm-up.
6. Using an external op amp with internal span resistors and specified external trim resistors in place of potentiomenters R1 and R2. Errors are adjustable to zero using R1 and R2 potentiometers. (See Operating Instructions Figure 2.)
7. The HI-562A is designed for V_{ps+} = 5V, but +4.5V ≤ V_{ps+} ≤ 16.5V maybe connected if convenient (For V_{ps+} above +5V, there is an increase in power dissipation but little change in performance.)

Die Characteristics

Transistor Count 150
Die Dimensions ..... 103 x 209 mils
Thermal Impedance (°C/W) θ_{ja} θ_{jc}
Sidebraze DIP 50 15
Ceramic LCC 81 40
Tie Substrate to ..... V_{REF} Low (Analog Ground)
Process ..... Bipolar-DI

Definitions of Specifications

Digital Inputs

The HI-562A accepts digital input codes in binary format and may be user connected for any one of three binary codes: Straight Binary, Two's Complement, or Offset Binary (see Operating Instructions).

DIGITAL INPUT	ANALOG OUTPUT		
	Straight Binary	Offset Binary	Two's Complement*
MSB LSB			
000...000	Zero	-FS (Full Scale)	Zero
100...000	1/2 FS	Zero	-FS
111...111	+FS - 1 LSB	+FS - 1 LSB	1/2 FS - 1 LSB
011...111	1/2 FS - 1 LSB	Zero - 1 LSB	+FS - 1 LSB

*Invert MSB with external inverter to obtain Two's Complement Coding

Accuracy

INTEGRAL NONLINEARITY — The maximum deviation of the actual transfer characteristic from an ideal straight line. The ideal line is positioned according to "end-point linearity" for D/A converter products from Harris Semiconductor, i.e. the line is drawn between the end-points of the actual transfer characteristic (codes 00...0 and 11...1).

DIFFERENTIAL NONLINEARITY — The difference between one LSB and the output voltage change corresponding to any two consecutive codes. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity.

MONOTONICITY — The property of a D/A converter's transfer function which guarantees that the output derivative will not change sign in response to a sequence of increasing (or decreasing) input codes. That is, the only output response to a code change is to remain constant, increase for increasing code, or decrease for decreasing code.

Settling Time

That interval between application of a digital step input, and final entry of the analog output within a specified window about the settled value. Harris Semiconductor usually specifies a unipolar 10V full scale step, to be measured from 50% of the input digital transition, and a window of ±1/2 LSB about the final value. The device output is then rated according to the worst (longest settling) case: low to high, or high to low.

Drift

GAIN DRIFT — The change in full scale analog output over the specified temperature range expressed in parts per million of full scale range per ^{o}C (ppm of FSR/^{o}C). Gain error is measured with respect to +25^{o}C at high (T_H) and low (T_L) temperatures. Gain drift is calculated for both high (T_H -25^{o}C) and low (+25^{o}C - T_L) ranges by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst case drift.

OFFSET DRIFT — The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per ^{o}C (ppm of FSR/^{o}C). Offset error is measured with respect to +25^{o}C at high (T_H) and low (T_L) temperatures. Offset Drift is calculated for both high (T_H -25^{o}C) and low (+25^{o}C - T_L) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst-case drift.

Power Supply Sensitivity

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in -15V, +5V or +15V supplies. It is specified under DC conditions and expressed as parts per million of full scale range per percent of change in power supply (ppm of FSR/%Vps).

Compliance

Compliance Voltage is the maximum output range for which specified accuracy limits are guaranteed. Compliance Limit implies functional operation only and makes no claims to accuracy.

Glitch

A glitch on the output of a D/A converter is a large transient spike resulting from unequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale or the major carry code transition from 011...1 to 100...0 or vice versa. For example, if turn ON is greater than turn OFF for 011...1 to 100...0, an intermediate state of 000...0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably.

Operating Instructions

Decoupling and Grounding

For best accuracy and high frequency performance, the grounding and decoupling scheme shown in Figure 1 should be used. Decoupling capacitors should be connected close to the HI-562A (preferably to the device pins) and should be tantalum or electrolytic bypassed with ceramic types for best high frequency noise rejection.

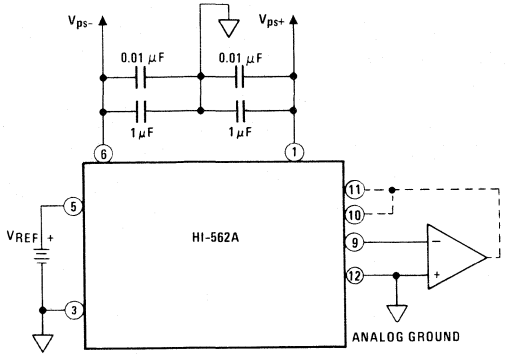
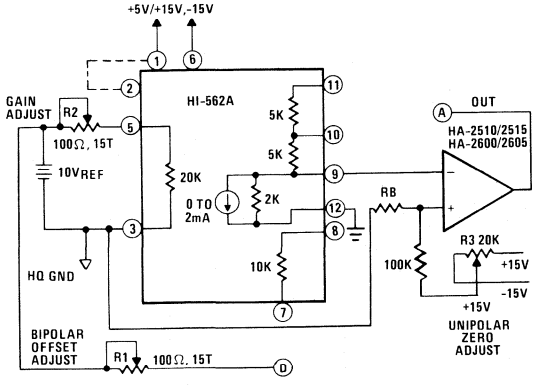


FIGURE 1.

Unipolar and Bipolar Voltage Output Connections

CONNECTIONS — Using an external resistive load, the output compliance should not exceed ±1V to maintain specified accuracy. For higher output voltages, accuracy can be maintained by using an external op amp and the internal span resistors as shown in Figure 2 and defined in Table 1 for unipolar and bipolar modes.



*For TTL and DTL compatibility, connect +5V to pin 1 and tie pin 2 to pin 12. For CMOS compatibility, connect digital power supply (9.5V ≤ VDD ≤ +12V) to pin 1 and short pin 2 to pin 1.

**Bias resistor, RB, should be chosen to equalize op amp offset voltage due to bias current. Its value is calculated from the parallel combination of the current source output resistance (2K) and the op amp feedback resistor. See Table 1 for values of RB.

FIGURE 2.

TABLE 1.

	CONNECTIONS					
	OUTPUT RANGE	PIN 7 TO	PIN 8 TO	PIN 10 TO	PIN 11 TO	BIAS (RB) RESISTOR
Unipolar	0 to +10V	NC	NC	A	NC	1.43K
Mode	0 to +5V	NC	NC	A	9	1.11K
Bipolar	±10V	D	9	NC	A	760Ω
Mode	±5V	D	9	A	NC	840Ω
	±2.5V	D	9	A	9	766Ω

External Gain and Zero Calibration (See Figure 2)

The input reference resistor (20K nominal) and bipolar offset resistors shown in Figure 2 are both intentionally set low by 50Ω to allow the user to externally trim-out initial errors to a very high degree of precision. The adjustments are made in the voltage output mode using an external op amp as current-to-voltage converter and the HI-562A internal scaling resistors as feedback elements for optimum accuracy and temperature coefficient. For best accuracy over temperature, select an op amp that has good front-end temperature coefficients such as the HA-2600/2605 with offset voltage and offset current tempco's of 5µV/°C in 1nA/°C, respectively. For high speed voltage mode applications where fast settling is required, the HA-2510/2515 is recommended for better than 1.5µs settling to 0.01%. Using either one, potentiometer R3 conveniently nulls unipolar offset plus op amp offset in one operation (for HA-2510/2515 and HA-2600/2605 use R3 = 20K and 100K, respectively). For bipolar mode operation, R3 should be used to null op amp offset to optimize its tempco (i.e., short 9 to A and adjust R3 for zero before calibrating in bipolar mode). The gain and bipolar offset adjustment range using 100Ω potentiometers is ±12 LSB and ±25 LSB, respectively. If desired, the potentiometers can be replaced with fixed 50Ω (1%) resistors resulting in an initial gain and bipolar offset accuracy of typically ±1/2 LSB.

UNIPOLAR CALIBRATION

Step 1: Unipolar Offset
- Turn all bits OFF
- Adjust R3 for zero volts output

Step 2: Gain
- Turn all bits ON
- Adjust R2 for an output of FS - 1 LSB
  That is, adjust for:
  9.9976V for 0V to +10V range
  4.9988V for 0V to +5V range

BIPOLAR CALIBRATION

Step 1: Bipolar Offset
- Turn all bits OFF
- Adjust R1 for an output of:
  -10V for ±10V range
  -5V for ±5V range
  -2.5V for ±2.5V range

Step 2: Gain
- Turn bit 1 (MSB) ON; all other bits OFF
- Adjust R2 for zero volts output

HARRIS

HI-565A

High Speed Monolithic Digital-to-Analog Converter with Reference

Features

- DAC AND REFERENCE ON A SINGLE CHIP
- PIN COMPATIBLE WITH AD565A
- VERY HIGH SPEED: SETTLES TO 1/2 LSB IN 250ns, MAX. FULL SCALE SWITCHING TIME 30ns, TYP.
- GUARANTEED FOR OPERATION WITH ±12V SUPPLIES
- MONOTONICITY GUARANTEED OVER TEMPERATURE
- 1/2 LSB MAX NONLINEARITY GUARANTEED OVER TEMPERATURE
- LOW GAIN DRIFT (MAX, DAC PLUS REFERENCE) 25ppm/°C
- LOW POWER DISSIPATION 250mW

Applications

- CRT DISPLAYS
- HIGH SPEED A/D CONVERTERS
- SIGNAL RECONSTRUCTION
- WAVEFORM SYNTHESIS

Description

The HI-565A is a fast, 12 bit current output, digital to analog converter. The monolithic chip includes a precision voltage reference, thin-film R-2R ladder, reference control amplifier and twelve high-speed bipolar current switches.

The Harris Semiconductor dielectric isolation process provides latch-free operation while minimizing stray capacitance and leakage currents, to produce an excellent combination of speed and accuracy. Also, ground currents are minimized to produce a low and constant current through the ground terminal, which reduces error due to code-dependent ground currents.

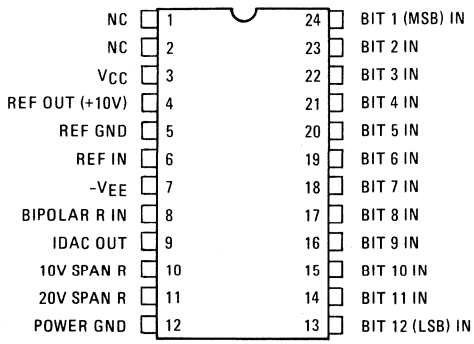
HI-565A dice are laser trimmed for a maximum integral non-linearity error of ±1/4 LSB at +25°C. In addition, the low noise buried zener reference is trimmed both for absolute value and minimum temperature coefficient.

The HI-565A is offered in both commercial and military grades. For additional Hi-Rel screening including 160 hour burn-in, specify the "-8" suffix. See Ordering Information.

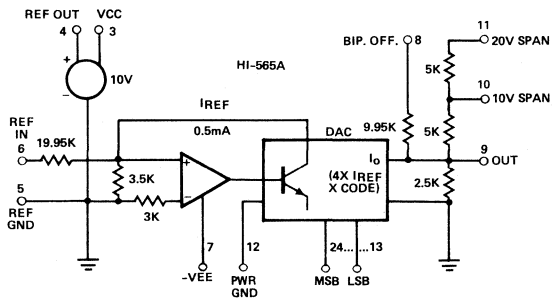
Package is a 24 pin side-brazed ceramic DIP. Power dissipation is typically 250mW, with ±15V supplies.

Pinout

TOP VIEW



Functional Diagram



Absolute Maximum Ratings*

V_{CC} to Power Ground . . . . . 0V to +18V
V_{EE} to Power Ground . . . . . 0V to -18V
Voltage on DAC Output (Pin 9) . . . . . -3V to +12V
Digital Inputs (Pins 13-24) to Power Ground . . . . . -1V to +7.0V
Ref In to Reference Ground . . . . . ±12V
Bipolar Offset to Reference Ground . . . . . ±12V
Junction Temperature . . . . . 175°C

10V Span R to Reference Ground . . . . . ±12V
20V Span R to Reference Ground . . . . . ±24V
Ref Out . . . . . Indefinite Short to Power Ground
Momentary Short to V_{CC}
Operating Temperature Ranges:
HI-565AS, T-2 . . . . . -55°C to +125°C
HI-565AJ, K-5 . . . . . 0°C to +75°C
HI-565AS, T-8 . . . . . -55°C to +125°C

*Absolute maximum ratings are limiting values beyond which the serviceability of the circuit may be impaired.

Electrical Specifications (T_A = +25°C, V_{CC} = +15V, V_{EE} = -15V, unless otherwise specified)

MODEL	HI-565AJ, HI-565AS			HI-565AK, HI-565AT			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
DATA INPUTS (Note 1) (Pins 13 to 24)							
TTL or 5V CMOS (T_{MIN} to T_{MAX})							
Input Voltage							
Bit ON Logic "1"	+2.0		+5.5	+2.0		+5.5	V
Bit OFF Logic "0"			+0.8			+0.8	V
Logic Current (Each Bit)							
Bit ON Logic "1"		.01	+1.0		.01	+1.0	μA
Bit OFF Logic "0"		-2.0	-20		-2.0	-20	μA
RESOLUTION			12			12	Bits
OUTPUT							
Current Unipolar (All Bits On)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar (All Bits on or Off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (Exclusive of Span Resistors)	1.8k	2.5k	3.2k	1.8k	2.5k	3.2k	Ω
Offset Unipolar		0.01	0.05		0.01	0.05	% of F.S.
Bipolar (Figure 2, R_3 = 50Ω Fixed)		0.05	0.15		0.05	0.1	% of F.S.
Capacitance		20			20		pF
Compliance Voltage, T_{MIN} to T_{MAX}	-1.5		+10	-1.5		+10	V
ACCURACY (Error Relative to Full Scale)							
+25°C		±1/4 (0.006)	±1/2 (0.012)		±1/8 (0.003)	±1/4 (0.006)	LSB % of F.S.
T_{MIN} to T_{MAX}		±1/2 (0.012)	±3/4 (0.018)		±1/4 (0.006)	±1/2 (0.012)	LSB % OF F.S.
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_{MIN} to T_{MAX}	MONOTONICITY GUARANTEED						
TEMPERATURE COEFFICIENTS							
With Internal Reference							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		15	40		10	25	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
SETTLING TIME TO 1/2 LSB							
With High Z External Load (Note 2)		350	500		350	500	ns
With 75Ω External Load		150	250		150	250	ns

MODEL	HI-565AJ, HI-565AS MIN	HI-565AJ, HI-565AS TYP	HI-565AJ, HI-565AS MAX	HI-565AK, HI-565AT MIN	HI-565AK, HI-565AT TYP	HI-565AK, HI-565AT MAX	UNITS
FULL SCALE TRANSITION (From 50% of Logic Input to 90% of Analog Output)							
Rise Time		15	30		15	30	ns
Fall Time		30	50		30	50	ns
TEMPERATURE RANGE							
Operating (HI-565AJ/K)	0		+75	0		+75	°C
(HI-565AS/T)	-55		+125	-55		+125	°C
Storage							
D Package (All)	-65		+150	-65		+150	°C
N Package (J, K)	-25		+150	-25		+150	°C
POWER REQUIREMENTS							
I_{CC}, +11.4 to +16.5V DC		9.0	11.8		9.0	11.8	mA
I_{EE}, -11.4 to -16.5V DC		-9.5	-14.5		-9.5	-14.5	mA
POWER SUPPLY GAIN SENSITIVITY (Note 3)							
V_{CC} = +11.4 to +16.5 VDC		3	10		3	10	ppm of F.S./%
V_{EE} = -11.4 to -16.5 VDC		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT RANGES (See Table 1)	0 to +5 -2.5 to +2.5 0 to +10 -5 to +5 -10 to +10			0 to +5 -2.5 to +2.5 0 to +10 -5 to +5 -10 to +10			V V V V V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor for R2 (Figure 1)		±0.1	±0.25		±0.1	±0.25	% of F.S.
Bipolar Zero Error with Fixed 50Ω Resistor for R3 (Figure 2)		±0.05	±0.15		±0.05	±0.1	% of F.S.
Gain Adjustment Range (Figure 1)	±0.25			±0.25			% of F.S.
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S.
REFERENCE INPUT							
Input Impedance	15K	20K	25K	15K	20K	25K	
REFERENCE OUTPUT							
Voltage	9.90	10.00	10.10	9.90	10.00	10.10	V
Current (Available for External Loads)	1.5	2.5		1.5	2.5		mA
POWER DISSIPATION		250	375		250	375	mW

NOTES:
1. Guaranteed but not tested over the operating temperature range.
2. See settling time discussion and Figure 3.
3. The Power Supply Gain Sensitivity is tested in reference to a V_{CC}, V_{EE} of ±15V.

Definitions of Specifications

DIGITAL INPUTS

The HI-565A accepts digital input codes in binary format and may be user connected for any one of three binary codes. Straight Binary, Two's Complement*, or Offset Binary, (See Operating Instructions).

DIGITAL INPUT	ANALOG OUTPUT		
	Straight Binary	Offset Binary	Two's Complement*
MSB...LSB			
000...000	Zero	-FS (Full Scale)	Zero
100...000	½FS	Zero	-FS
111...111	+FS – 1 LSB	+FS – 1 LSB	Zero – 1 LSB
011...111	½FS – 1 LSB	Zero – 1 LSB	+FS – 1 LSB

*Invert MSB with external inverter to obtain Two's Complement Coding

ACCURACY

NONLINEARITY – Nonlinearity of a D/A converter is an important measure of its accuracy. It describes the deviation from an ideal straight line transfer curve drawn between zero (all bits OFF) and full scale (all bits ON).

DIFFERENTIAL NONLINEARITY – For a D/A converter, it is the difference between the actual output voltage change and the ideal (1 LSB) voltage change for a one bit change in code. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity; i.e., the output always increases and never decreases for an increasing input.

SETTLING TIME

Settling time is the time required for the output to settle to within the specified error band for any input code transition. It is usually specified for a full scale or major carry transition, settling to within 1/2 LSB of final value.

DRIFT

GAIN DRIFT – The change in full scale analog output over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Gain error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Gain drift is calculated for both high (T_H -25°C) and low ranges (+25°C -T_L) by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst case drift.

OFFSET DRIFT – The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Offset error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Offset Drift is calculated for both high (T_H -25°C) and low (+25°C -T_L) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst-case drift.

POWER SUPPLY SENSITIVITY

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in –15V or +15V supplies. It is specified under DC conditions and expressed as parts per million of full scale range per percent of change in power supply (ppm of FSR/%).

COMPLIANCE

Compliance Voltage is the maximum output voltage range that can be tolerated and still maintain its specified accuracy. Compliance Limit implies functional operation only and makes no claims to accuracy.

GLITCH

A glitch on the output of a D/A converter is a transient spike resulting from unequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale or the major carry code transition from 011...1 to 100...0 or vice versa. For example, if turn ON is greater than turn OFF for 011...1 to 100...0, an intermediate state of 000...0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably.

Applying the HI-565A

OP AMP SELECTION

The HI-565A's current output may be converted to voltage using the standard connections shown in Figures 1 and 2. The choice of operational amplifier should be reviewed for each application, since a significant trade-off may be made between speed and accuracy.

For highest precision, use an HA-5130. This amplifier contributes negligible error, but requires about 11μs to settle within ±0.1% following a 10V step.

The Harris Semiconductor HA-2600 is the best all-around choice for this application, and it settles in 1.5μs (also to ±0.1% following a 10V step). Remember, settling time for the DAC-amplifier combination is $\sqrt{t_D^2 + t_A^2}$, where t_D, t_A are settling times for the DAC and amplifier.

NO-TRIM OPERATION

The HI-565A will perform as specified without calibration adjustments. To operate without calibration, substitute 50 Ω resistors for the 100Ω trimming potentiometers: In Figure 1 replace R2 with 50Ω ; also remove the network on pin 8 and connect 50Ω to ground. For bipolar operation in Figure 2, replace R3 and R4 with 50Ω resistors.

Applying the HI-565A, (Continued)

Table 1 – Operating Modes and Calibration

MODE	CIRCUIT CONNECTIONS: OUTPUT RANGE	PIN10 TO	PIN 11 TO	RESISTOR (R)	CALIBRATION: APPLY INPUT CODE	ADJUST	TO SET V_O
Unipolar (See Fig. 1)	0 to +10V	V_O	Pin 10	1.43K	All 0's All 1's	R1 R2	0V +9.99756V
	0 to +5V	V_O	Pin 9	1.1K	All 0's All 1's	R1 R2	0V +4.99878V
Bipolar (See Fig. 2)	±10V	NC	V_O	1.69K	All 0's All 1's	R3 R4	-10V +9.99512V
	±5V	V_O	Pin 10	1.43K	All 0's All 1's	R3 R4	-5V +4.99756V
	±2.5V	V_O	Pin 9	1.1K	All 0's All 1's	R3 R4	-2.5V +2.49878V

With these changes, performance is guaranteed as shown under Specifications, "External Adjustments". Typical unipolar zero will be ±1/2 LSB plus the op amp offset.

The feedback capacitor C must be selected to minimize settling time.

CALIBRATION

Calibration provides the maximum accuracy from a converter by adjusting its gain and offset errors to zero. For the HI-565A, these adjustments are similar whether the current output is used, or whether an external op amp is added to convert this current to a voltage. Refer to Table 1 for the voltage output case, along with Figure 1 or 2.

Calibration is a two step process for each of the five output ranges shown in Table 1. First adjust the negative full scale (zero for unipolar ranges). This is an offset adjust which translates the output characteristic, i.e. affects each code by the same amount.

Next adjust positive FS. This is a gain error adjustment, which rotates the output characteristic about the negative FS value.

For the bipolar ranges, this approach leaves an error at the zero code, whose maximum value is the same as for integral nonlinearity error. In general, only two values of output may be calibrated exactly; all others must tolerate some error. Choosing the extreme end points (plus and minus full scale) minimizes this distributed error for all other codes.

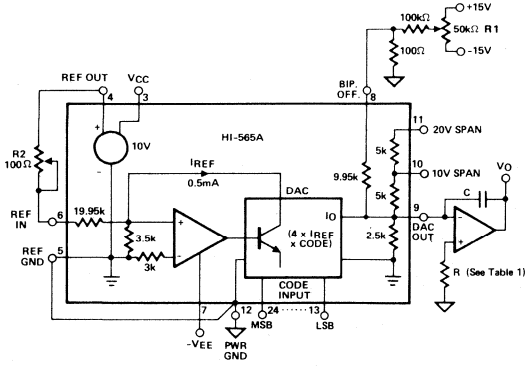


FIGURE 1. UNIPOLAR VOLTAGE OUTPUT

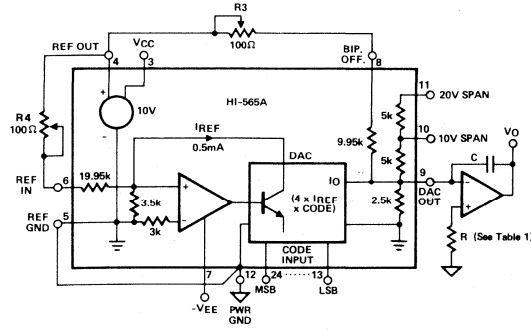


FIGURE 2. BIPOLAR VOLTAGE OUTPUT

Settling Time

This is a challenging measurement, in which the result depends on the method chosen, the precision and quality of test equipment and the operating configuration of the DAC (test conditions). As a result, the different techniques in use by converter manufacturers can lead to consistently different results. An engineer should understand the advantage and limitations of a given test method before using the specified settling time as a basis for design.

The approach used for several years at Harris Analog Products Division calls for a strobed comparator to sense final perturbations of the DAC output waveform. This gives the LSB a reasonable magnitude (814μV for the HI-565A), which provides the comparator with enough overdrive to establish an accurate ±1/2 LSB window about the final settled value. Also, the required test conditions simulate the DAC's environment for a common application – use in a successive approximation A/D converter. Considerable experience has shown this to be a reliable and repeatable way to measure settling time.

The usual specification is based on a 10V step, produced by simultaneously switching all bits from off-to-on (t_{ON}) or on-to-off (t_{OFF}). The slower of the two cases is specified, as measured from 50% of the digital input transition to the final entry within a window of ±1/2 LSB about the settled value. Four measurements characterize a given type of DAC:

(a) t_{ON}, to final value +1/2 LSB
(b) t_{ON}, to final value -1/2 LSB
(c) t_{OFF}, to final value +1/2 LSB
(d) t_{OFF}, to final value -1/2 LSB

(Cases (b) and (c) may be eliminated unless the overshoot exceeds 1/2 LSB). For example, refer to Figure 3 for the measurement of case (d).

PROCEDURE

As shown in Figure 3B, settling time equals t_X plus the comparator delay (t_D = 15ns). To measure t_X,

- Adjust the delay on generator # 2 for a t_X of several microseconds. This assures that the DAC output has settled to its final value.
- Switch on the LSB (+5V).
- Adjust the V_{LSB} supply for 50 percent triggering at COMPARATOR OUT. This is indicated by traces of equal brightness on the oscilloscope display as shown in Figure 3B. Note DVM reading.
- Switch the LSB to Pulse (P).
- Readjust the V_{LSB} supply for 50% triggering as before, and note DVM reading. One LSB equals one tenth the difference in the DVM readings noted above.
- Adjust the V_{LSB} supply to reduce the DVM reading by 5 LSB's (DVM reads 10X, so this sets the comparator to sense the final settled value minus 1/2 LSB). Comparator output disappears.
- Reduce generator # 2 delay until comparator output reappears, and adjust for "equal brightness".
- Measure t_X from scope as shown in Figure 3B. Settling time equals $t_X + t_D$, i.e. t_X +15ns.

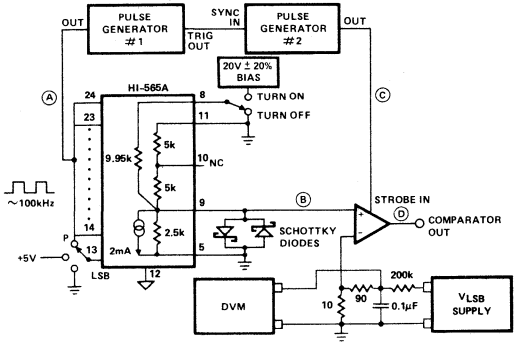


FIGURE 3A.

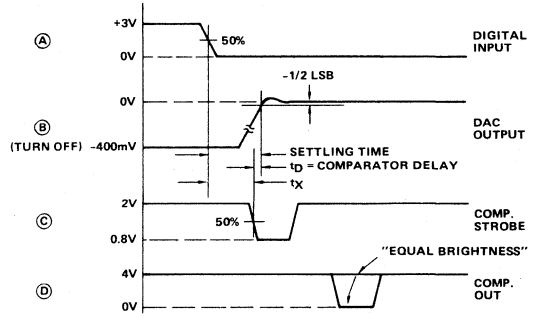


FIGURE 3B.

Other Considerations

GROUNDS

The HI-565A has two ground terminals, pin 5 (REF GND) and pin 12 (PWR GND). These should not be tied together near the package unless that point is also the system signal ground to which all returns are connected. (If such a point exists, then separate paths are required to pins 5 and 12).

The current through pin 5 is near-zero DC*; but pin 12 carries up to 1.75mA of code – dependent current from bits 1, 2, and 3. The general rule is to connect pin 5 directly to the system "quiet" point, usually called signal or analog ground. Connect pin 12 to the local digital or power ground. Then, of course, a single path must connect the analog/signal and digital/power grounds.

LAYOUT

Connections to pin 9 (I_{OUT}) on the HI-565A are most critical for high speed performance. Output capacitance of the DAC is only 20pF, so a small change or additional capacitance may alter the op amp's stability and affect settling time. Connections to pin 9 should be short and few. Component leads should be short on the side connecting to pin 9 (as for feedback capacitor C). See the Settling Time section.

BYPASS CAPACITORS

Power supply bypass capacitors on the op amp will serve the HI-565A also. If no op amp is used, a 0.01μF ceramic capacitor from each supply terminal to pin 12 is sufficient, since supply current variations are small.

*Current cancellation is a two-step process within the HI-565A in which code-dependent variations are eliminated, then the resulting DC current is supplied internally. First an auxiliary 9 bit R-2R ladder is driven by the complement of the DAC's input code. Together, the main and auxiliary ladders draw a continuous 2.25mA from the internal ground node, regardless of input code. Part of this DC current is supplied by the zener voltage reference, and the remainder is sourced from the positive supply via a current mirror which is laser trimmed for zero current through the external terminal (pin 5).

Die Characteristics

Transistor Count	200
Die Size	179 x 107 mils
Thermal Constants; θ_{ja}	51°C/W
θ_{jc}	16°C/W
Tie Substrate to:	Ref. Ground
Process:	Bipolar - DI

HARRIS HI-5618A/5618B

8-Bit High Speed Digital-to-Analog Converters

Features

- **Very Fast Settling Current .... 75ns (Max) Output**
- **Minimal Nonlinearity Error @ 25°C:**
  HI-5618A .....±1/4 LSB Max
  HI-5618B .....±1/2 LSB Max
- **Low Power Operation ..... 330mW Typ**
- **On-Chip Resistors for Gain and Bipolar Offset**
- **Guaranteed Monotonic Over Temperature**
- **CMOS, TTL, or DTL Compatible**

Applications

- **High Speed Process Control**
- **CRT Display Generation**
- **High Speed A/D Conversion**
- **Waveform Synthesis**
- **High Reliability Applications**
- **Video Signal Reconstruction**

Description

The HI-5618A/B are very high speed 8-bit current output D/A converters. These monolithic devices are fabricated with dielectrically isolated bipolar processing, which reduces internal parasitic capacitance to allow fast rise and fall times. This achieves a typical full scale settling time of 75ns (max) to ±1/2 LSB. Output glitches are minimized by incorporation of equally weighted current sources, switched to either an R-2R ladder network or ground for symmetrical turn ON and turn OFF times. High stability thin film resistors provide excellent accuracy. For example, the HI-5618A has ±1/4 LSB maximum nonlinearity error at +25°C, with ±3/8 LSB guaranteed over the full operating temperature range.

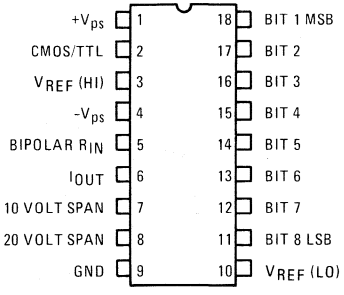
The HI-5618A/B are recommended for any application requiring high speed and accurate conversions. They can be used in CRT displays and systems requiring throughput rates as high as 20MHz for full scale transitions. Other applications include high speed process control, defense systems, avionics, and space instrumentation.

The HI-5618A-5 and HI-5618B-5 are specified for operation from 0°C to +75°C. The "-2" versions are specified from -55°C to +125°C. The HI-5618A/B is offered in both commercial and military grades. For additional Hi-Rel screening, including 160 hour burn-in, specify the "-8" suffix.

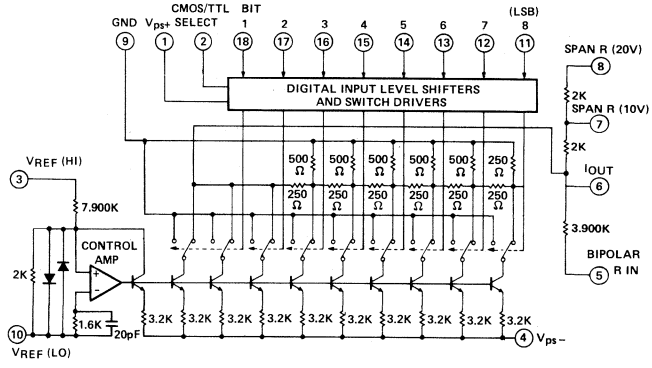
Power requirements are +5V and -15V. The HI-5618A/B is packaged in an 18 pin Ceramic DIP.

Pinout

TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Absolute Maximum Ratings (Referred to Ground) (1)

Power Supply Inputs	Vps+ . . . . . +20V	Junction Temperature	175°C
	Vps- . . . . . −20V		
Reference Inputs	VREF (Hi) . . . . . ±16.5V	Operating Temperature Range	
	VREF (Lo) 0V	HI-5618A/B-2	-55°C to +125°C
		HI-5618A/B-5	0°C to +75°C
Digital Inputs	Bits 1-12 (TTL) . . . -1V, +7.5V	HI-5618A/B-8	-55°C to +125°C
	Bits 1-12 (CMOS) . . . -1V, Vps+		
	CMOS/TTL Logic Sel -1V, +16.5V	Storage Temperature Range	-65°C to +150°C
Outputs	Pins 5, 7, 8 . . . . . ±Vps		
	Pin 6 . . . . . +Vps, -2.5V		

Electrical Specifications (V_{ps^+} = +5V; V_{ps^-} = -15V; V_{REF} = +10V; Pin 2 to GND, unless otherwise specified.)

PARAMETER		TEMP	HI-5618A/B-2 HI-5618A/B-8 MIN	TYP	MAX	HI-5618A/B-5 MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS									
Digital Inputs (2)									
TTL Logic Input Voltage (3)	Logic "1"	Full	2.0			2.0			V
	Logic "0"	Full			0.8			0.8	V
TTL Logic Input Current	Logic "1"	Full			500			500	nA
	Logic "0"	Full			-100			-100	μA
CMOS Logic Input Voltage (4)	Logic "1"	Full	$0.7V_{ps^+}$			$0.7V_{ps^+}$			V
	Logic "0"	Full			$0.3V_{ps^+}$			$0.3V_{ps^+}$	V
CMOS Logic Input Current	Logic "1"	Full			500			500	nA
	Logic "0"	Full			-100			-100	μA
Reference Input									
Input Resistance		+25°C		8K			8K		Ω
Input Voltage (I_{OUT} = 5mA ± 20%)		+25°C		+10			+10		V
TRANSFER CHARACTERISTICS									
Resolution		Full		8			8		Bits
Nonlinearity, Integral and Differential	HI-5618A	25°C			±1/4			±1/4	LSB
		Full			±3/8			±3/8	LSB
	HI-5618B	25°C			±1/2			±1/2	LSB
		Full			±5/8			±5/8	LSB
Initial Accuracy (6) (Relative to External +10V Reference)									
Gain		25°C			±2			±2	LSB
Unipolar Zero		25°C			±1/8			±1/8	LSB
Bipolar Offset (Neg. Full Scale)		25°C			±2			±2	LSB
Temperature Stability									
Gain Drift		Full			±1/4			±1/4	LSB
Unipolar Zero Drift		Full			±1/16			±1/16	LSB
Bipolar Zero Drift		Full			±1/4			±1/4	LSB
Settling Time (5) to 1/2 LSB									
High Impedance (11)	(from all 0's to all 1's)	+25°C		65	75		65	75	ns
or	(from all 1's to all 0's)								

PARAMETER		TEMP	HI-5618A/B-2 HI-5618A/B-8 MIN	TYP	MAX	HI-5618A/B-5 MIN	TYP	MAX	UNITS
TRANSFER CHARACTERISTICS (Continued)									
Glitch (5) - Major Carry Transition									
Duration		+25°C		20			20		ns
Amplitude (See Fig. 4)		+25°C		350			350		mV
Area		+25°C		3500			3500		mV-ns
Power Supply Sensitivity (5)									
V_{ps+} = +5V, V_{ps-} = -13.5V to -16.5V									
Gain	(Input Code 11 . . . 1)	+25°C			±5			±5	
Unipolar Zero	(Input Code 00 . . . 0)	+25°C		±0.5			±0.5		ppm of
Bipolar Offset	(Input Code 00 . . . 0)	+25°C		±1.5			±1.5		FSR/% Vps
									(9)
V_{ps-} = -15V, V_{ps+} = 4.5V to 5.5V									
Gain	(Input Code 11 . . . 1)	+25°C			±5			±5	
Unipolar Zero	(Input Code 00 . . . 0)	+25°C		±0.5			±0.5		
Bipolar Offset	(Input Code 00 . . . 0)	+25°C		±1.5			±1.5		
OUTPUT CHARACTERISTICS									
Output Current	Unipolar	+25°C	-4	-5	-6	-4	-5	-6	mA
	Bipolar	+25°C	±2.0	±2.5	±3.0	±2.0	±2.5	±3.0	mA
Output Resistance		+25°C		500			500		Ω
Output Capacitance		+25°C		20			20		pF
Output Voltage Range (7)	Unipolar	+25°C		+10			+10		V
		+25°C		+5			+5		V
	Bipolar	+25°C		±10			±10		V
		+25°C		±5			±5		V
		+25°C		±2.5			±2.5		V
Output Compliance Voltage (5)		+25°C		±1.5			±1.5		V
Output Noise Voltage (8)	0.1Hz to 100Hz	+25°C		30			30		μV_{p-p}
	0.1Hz to 1MHz	+25°C		100			100		μV_{p-p}
POWER REQUIREMENTS (4)									
V_{ps+}		Full	4.5	5	16.5	4.5	5	16.5	V
V_{ps-}		Full	-13.5	-15	-16.5	-13.5	-15	-16.5	V
I_{ps+} (10) (All 1's or all 0's in either		+25°C		9			9		mA
TTL or CMOS mode) (3, 4)		Full			12			12	mA
I_{ps-} (10) (All 1's or all 0's in either		+25°C		19			19		mA
TTL or CMOS mode) (3, 4)		Full			26			26	mA

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. The HI-5618 accepts digital input codes in binary format and may be user connected for any one of three binary codes. Straight binary, offset binary, or two's complement binary. (See operating instructions)
3. For TTL and DTL compatibility connect +5V to pin 1 and ground pin 2. The V_{ps+} tolerance is ± 10% for HI-5618A/B -2, -8; and ± 5% for HI-5618A/B-5.
4. For CMOS compatibility based on $V_{ps+} \geqslant 9.5V$, (switching thresholds equal $V_{ps+}/2$), connect pins 1 and 2. For CMOS levels below 9.5V, connect pin 2 to ground only (this provides a threshold of approximately +1.4V).
5. See definitions.
6. These errors may be adjusted to zero using external potentiometers R_1, R_2, R_3. R_1 and R_2 each provide more than ± 3 LSB's adjustment. (See Operating Instructions). The specifications listed under initial accuracy are based on use of an external op amp, internal span and offset resistors, and 100Ω ± 1% resistors, in place of R_1 and R_2.
7. Using an external op amp with the internal span and offset resistors. See Operating Instructions.
8. Specified for all "1's" or all "0's" digital input.
9. FSR is "Full Scale Range", i.e., 20V for ± 10V range; 10V for ± 5V range, etc. Nominal full scale output current is 5mA.
10. After 30 seconds warm-up.
11. See Test Circuit, Figure 3.
12. See Test Circuit , Figure 4.

Definitions of Specifications

ACCURACY

INTEGRAL NONLINEARITY – The maximum deviation of the actual transfer characteristic from an ideal straight line. The ideal line is positioned according to "end-point linearity" for D/A converter products from Harris Semiconductor, i.e. the line is drawn between the end-points of the actual transfer characteristic (codes 00. . .0 and 11. . .1).

DIFFERENTIAL NONLINEARITY – The difference between one LSB and the output voltage change corresponding to any two consecutive codes. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity.

MONOTONICITY – The property of a D/A converter's transfer function which guarantees that the output derivative will not change sign in response to a sequence of increasing (or decreasing) input codes. That is, the only output response to a code change is to remain constant, increase for increasing code, or decrease for decreasing code.

GAIN DRIFT – The change in full scale analog output over the specified temperature range expressed in fractional LSB's, or parts per million of full scale range per °C (ppm of FSR/°C). Gain error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Gain drift is calculated for both high (T_H -25°C) and low ranges (+25°C -T_L) by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst case drift.

ZERO DRIFT – The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Zero error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Zero Drift is calculated for high (T_H -25°C) and low (+25°C -T_L) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two representing worst case drift.

SETTLING TIME

Settling time is the time required for the output to settle to within the specified error band for any input code transition. It is usually specified for a full scale transition. D/A settling time may vary depending upon the impedance level being driven. A comparator presents a high impedance, while an op amp connected for current to voltage conversion presents a low impedance. Figure 3a shows the test circuit used for testing the HI-5618A/B for T_S (OFF) into a high impedance.

GLITCH

A glitch on the output of a D/A converter is a transient spike resulting from unequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale or the major carry code transition from 011. . .1 to 100. . .0 or vice versa. For example, if turn ON is greater than turn OFF for 100. . .1 to 100. . .0, an intermediate state of 000. . .0 exists, such that, the output momentarily glitches toward zero output. In general, when a D/A is driven by a set of external logic gates, the unmatched turn on – turn off times at the gates will add to the glitch problem. See Figure 4.

POWER SUPPLY SENSITIVITY

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in the +5V or -15V supplies. It is specified under DC conditions and expressed as parts per million of full scale range per percent of change in power supply (ppm of FSR/%).

COMPLIANCE

Compliance Voltage is the maximum output voltage range that can be tolerated and still maintain its specified accuracy. Compliance Limit implies functional operation only and makes no claim to accuracy.

Operating Instructions

DECOUPLING AND GROUNDING

For best accuracy and high speed performance, the grounding and decoupling scheme shown in Figure 1 should be used. Decoupling capacitors should be connected close to the HI-5618A/B; preferably to the device pin. A solid tantalum or electrolytic capacitor in parallel with a smaller ceramic type is recommended.

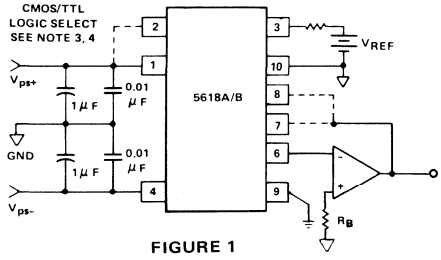


FIGURE 1

UNIPOLAR AND BIPOLAR VOLTAGE OUTPUT CONNECTIONS

Make connections as shown in the table and Figure 2, for five standard output ranges:

	OUTPUT RANGE	CONNECTIONS PIN 5 TO	CONNECTIONS PIN 7 TO	CONNECTIONS PIN 8 TO	BIAS RESISTOR R_B
Unipolar Mode	0 to +10V	NC	A	NC	400Ω
	0 to +5V	NC	A	6	330Ω
Bipolar Mode	± 10V	D	NC	A	400Ω
	± 5V	D	A	NC	360Ω
	± 2.5V	D	A	6	310Ω

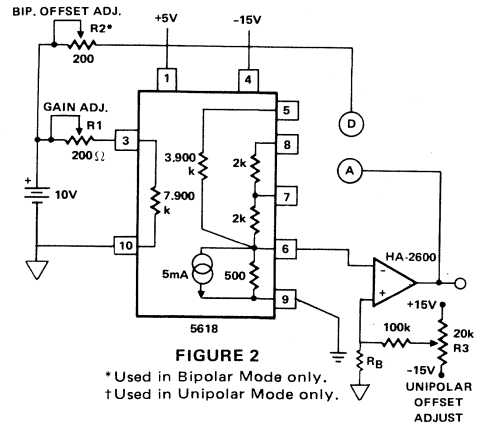


FIGURE 2

*Used in Bipolar Mode only.
†Used in Unipolar Mode only.

Operating Instructions

The HI-5618A/B accepts an 8 bit digital word in Straight Binary code. In the bipolar mode this code becomes Offset Binary. Also in bipolar mode, the MSB may be complemented using an external inverter to obtain 2's complement code. Here are the correct outputs for some key input codes:

UNIPOLAR - STRAIGHT BINARY
0V TO +10V OUTPUT RANGE

DIGITAL INPUT	ANALOG OUTPUT	
11 1	FS - 1 LSB	= 9.96094V
10 0	½FS	= 5.00000V
01 1	½FS - 1 LSB	= 4.96094V
00 0	Zero	= 0.00000V

UNIPOLAR - STRAIGHT BINARY
0V TO +5V OUTPUT RANGE

DIGITAL INPUT	ANALOG OUTPUT	
11 1	FS - 1 LSB	= 4.98047V
10 0	½FS	= 2.50000V
01 1	½FS - 1 LSB	= 2.48047V
00 0	Zero	= 0.00000V

BIPOLAR - OFFSET BINARY
± 10V OUTPUT VOLTAGE RANGE

DIGITAL INPUT	ANALOG OUTPUT	
11 1	+FS -1 LSB	= +9.92188V
10 0	Zero	= +0.00000V
01 1	Zero -1 LSB	= -0.07813V
00 0	-FS	= -10.0000V

BIPOLAR - TWO'S COMPLEMENT **
± 10V OUTPUT VOLTAGE RANGE

DIGITAL INPUT	ANALOG OUTPUT	
01 1	+FS - 1 LSB	= +9.92188V
00 0	Zero	= +0.00000V
11 1	Zero - 1 LSB	= -0.07813V
10 0	-FS	= -10.0000V

** Invert MSB with external inverter to obtain two's complement coding.

Output Accuracy of the HI-5618A/B is affected directly by the reference voltage, since $I_0(F/S) \simeq 4\ (V_{REF}/8k\Omega)$. For precision performance, a stable +10V reference with low temperature coefficient is recommended.

The output current may be converted to voltage using an external op amp with the internal span and offset resistors, as shown above in the table. The op amp should have good front end temperature coefficients. For example, the HA-2600/2605 is well suited to this application, with offset voltage and offset current tempco's of 5 μV/°C and 1nA/°C, respectively. The input reference resistor (7.9kΩ) and bipolar offset resistor (3.9kΩ) are both intentionally set low by 100Ω to allow the user to externally trim out initial errors to a high degree of precision.

For high speed voltage output applications where fast settling is required, the HA-2510/25 is recommended for settling times better than 250ns to 1/2 LSB. The HA-5190/95 is recommended for applications requiring settling times less than 150ns. (See Applications).

CALIBRATION (See Figure 2)

UNIPOLAR MODE -

1. Apply zero (all 0's) input, and adjust R_3 for 0V output.
2. Apply full scale (all 1's) input, and adjust R_1 for:
   +9.96094 Volts, +10 Volt range
   +4.98047 Volts, +5 Volt range

BIPOLAR MODE -

1. Apply negative full scale (also called bipolar offset): All 0's for offset binary; 1000 . . . . for 2's complement. Adjust R_2 for output voltages as follows:
   -10 Volts, ±10 Volt Range
   -5 Volts, ± 5 Volt Range
   -2.5 Volts, ±2.5 Volt Range
2. Apply positive full scale (all 1's for offset Binary; 0111. . . . for 2's complement) Adjust R_1 for output voltages as follows:
   +9.92188 Volts, ± 10 Volt Range
   +4.96094 Volts, ±5 Volt Range
   +2.48047 Volts, ±2.5 Volt Range
3. Apply zero input (1000. . . . for offset Binary; 0000. . . . for 2's complement). Output should be zero volts. Any error is due to nonlinearity in the DAC, and cannot be nulled without disrupting the calibration in steps 2 and 3.

Test Circuits

SETTLING TIME

Turn-off settling time ($T_{S(OFF)}$) is somewhat longer than $T_{S(ON)}$ for the HI-5618. Typical $T_{S(OFF)}$ performance is shown in Figure 3C, using the circuit of Figure 3A.

Refer to Figure 3B; Settling time following turn-off equals T_X plus T_D. The comparator delay T_D may be measured at 1mV/cm, using a Tektronix 7A13 differential comparator or equivalent. Then, T_X is easily measured in a short procedure:

- Adjust delay on generator # 2 for T_X approximately 1μs
- Switch the LSB to +5V (ON).
- Adjust the V_{LSB} supply for 50 percent triggering at COMP. OUT (equal brightness).
- DVM reads -1 LSB. Adjust V_{LSB} supply so DVM reads -1/2 LSB.
- Switch the LSB to P (pulse); COMP. OUT pulse disappears.
- Reduce generator # 2 delay until COMP. OUT pulse reappears; adjust delay for "equal brightness".
- Measure T_X from scope. (Any overshoot will be less than 1/2 LSB, so it is not necessary to examine the other side of the envelope, i.e. final value plus 1/2 LSB.)

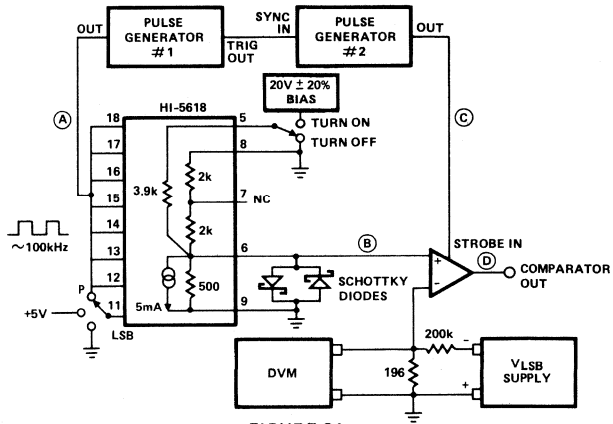


FIGURE 3A

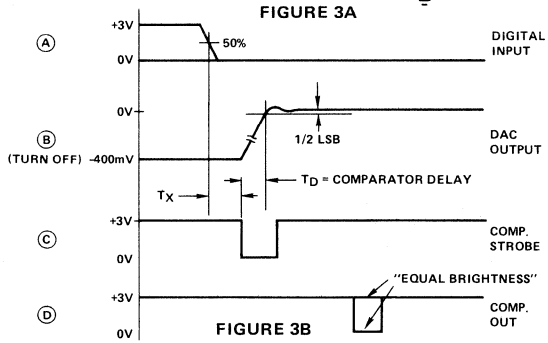


FIGURE 3B

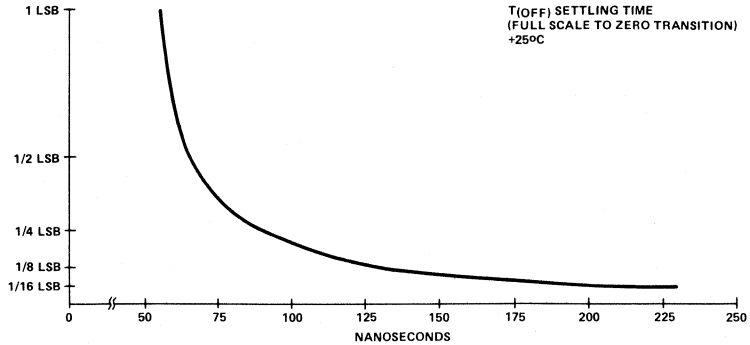
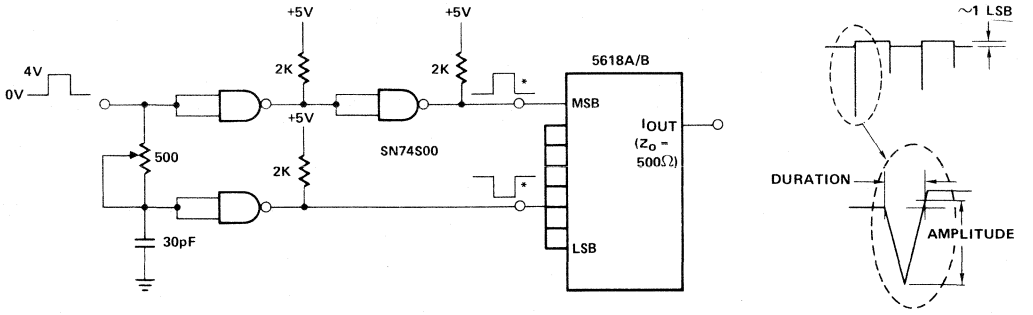


FIGURE 3C

Test Circuits

OUTPUT GLITCH MEASUREMENT

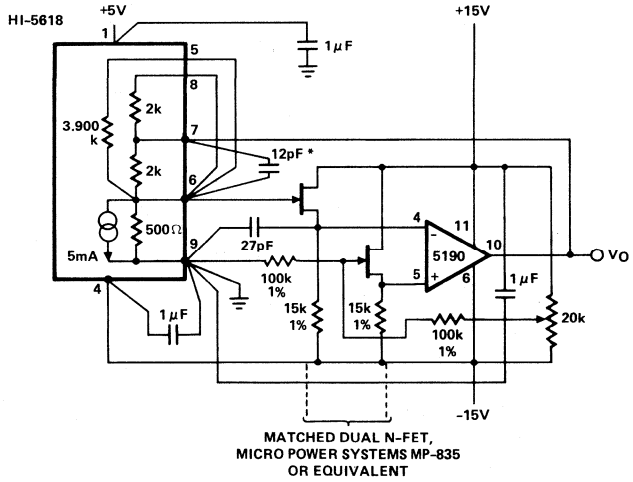


* ADJUST 500Ω TRIMMER SO THAT INPUT SIGNALS CROSS THEIR RESPECTIVE SWITCHING THRESHOLDS AT THE SAME TIME.

FIGURE 4

Applications

HIGH SPEED VOLTAGE OUTPUT



* NOMINAL VALUE, SELECTED FOR OPTIMUM STEP RESPONSE.

Die Characteristics

Transistor Count		122
Die Size:		103 x 209 mils
Thermal Constants;	θ_{ja}	75°C/W
	θ_{jc}	17°C/W
Tie Substrate to:		Ground (V_{REF} Lo)
Process:		Bipolar - DI

HARRIS

HI-5660/5660A

High Speed Monolithic Digital-to-Analog Converter

Features

- MONOLITHIC CONSTRUCTION
- FAST SETTLING (TO ±1/2 LSB) 500ns
- ±1/2 LSB MAX. NONLINEARITY GUARANTEED OVER TEMPERATURE
- INTERNAL CANCELLATION OF GROUND CURRENT
- EXCELLENT POWER SUPPLY REJECTION 1ppm/%PS
- LOW COST

Applications

- HIGH SPEED A/D CONVERTERS
- CRT DISPLAYS
- WAVEFORM SYNTHESIS

Description

The HI-5660 is a current output, 12 bit monolithic digital-to-analog converter. It offers high speed plus enhanced accuracy, through internal cancellation of ground currents.

Fabrication of the HI-5660 features the Harris bipolar dielectric isolation process, which eliminates latchup and minimizes parasitic capacitance and leakage currents. The chip includes nichrome thin-film resistors, laser trimmed at the wafer level to a maximum linearity error of ±1/4 LSB at +25°C.

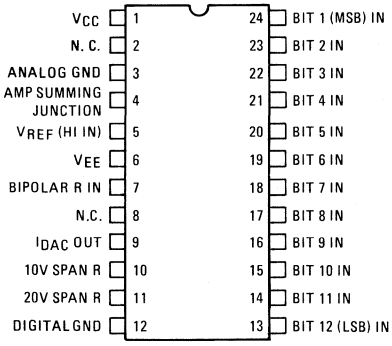
Near zero current in the Analog Ground terminal simplifies use of the HI-5660 by minimizing noise and offsets between the package and the system analog ground. This is accomplished by adding a complement current to the internal ground from an auxiliary R-2R ladder, and then supplying the resultant DC current from the positive power supply.

Electrical performance is similar to that of the AD566A. Pinouts are identical except for pin 1, which requires a +5V supply (versus no connection on the AD566A).

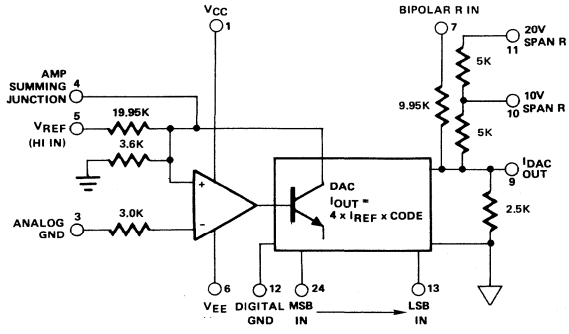
The HI-5660 is offered in two accuracy grades each for the commercial and military temperature ranges. Package is a 24 pin ceramic DIP, and power requirements are ± 12V to +15V.

Pinout

TOP VIEW
24 LEAD DIP



Functional Diagram



Absolute Maximum Ratings †

V_{CC} to Power Ground	0V to +18V	10V Span R to Reference Ground	±12V
V_{EE} to Power Ground	0V to -18V	20V Span R to Reference Ground	±24V
Voltage on DAC Output (Pin 9)	-3V to +12V	Junction Temperature	175°C
Digital Inputs (Pins 13-24) to Power Ground	-1V to +7.0V	Operating Temperature Ranges	
Ref In to Reference Ground	±12V	HI-5660/A-2,-8	-55°C to +125°C
Bipolar Offset to Reference Ground	±12V	HI-5660/A-5	0°C to +75°C
		Storage Temperature Range	-65°C to +150°C

†Absolute maximum ratings are limiting values beyond which the serviceability of the circuit may be impaired.

Electrical Specifications (T_A = +25°C, V_{CC} = +15V, V_{EE} = -15V, V_{REF} = 10V, unless otherwise specified)

MODEL	HI-5660-5 MIN	HI-5660-5 TYP	HI-5660-5 MAX	HI-5660A-5 MIN	HI-5660A-5 TYP	HI-5660A-5 MAX	UNITS
DATA INPUTS (Note 1) (Pins 13 to 24)							
TTL or 5V CMOS (T_{MIN} to T_{MAX})							
Input Voltage							
Bit ON Logic "1"	2.0		5.5	2.0		5.5	V
Bit OFF Logic "0"	0.0		0.8	0.0		0.8	V
Logic Current (Each Bit)							
Bit ON Logic "1"		2	10		2	10	µA
Bit OFF Logic "0"		-10	-50		-10	-50	µA
RESOLUTION			12			12	Bits
OUTPUT							
Current Unipolar (All Bits On)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar (All Bits on or Off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (Exclusive of Span Resistors)	2.0K	2.5K	3.0K	2.0K	2.5K	3.0K	Ω
Offset Unipolar		.01	.05		.01	.05	% of FS
Bipolar (Figure 2, R_3 = 50Ω Fixed)		.05	.15		.05	0.10	% of FS
Capacitance		25			25		pF
Compliance Voltage, T_{MIN} to T_{MAX}	-3		+12	-3		+12	V
ACCURACY (Error Relative to Full Scale)							
+25°C		±1/4 (0.006)	±1/2 (0.012)		±1/8 (0.003)	±1/4 (0.006)	LSB % of FS
T_{MIN} to T_{MAX}		±1/2 (0.012)	±3/4 (0.018)		±1/4 (0.006)	±1/2 (0.012)	LSB % of FS
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_{MIN} to T_{MAX}	MONOTONICITY GUARANTEED (±1 LSB MAX)						
TEMPERATURE COEFFICIENTS							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		7	10		7	10	ppm/°C
Differential Nonlinearity		2	6		2	2	ppm/°C
SETTLING TIME TO 1/2 LSB							
With 50Ω External Load		500			500		ns

MODEL	HI-5660-5 MIN	HI-5660-5 TYP	HI-5660-5 MAX	HI-5660A-5 MIN	HI-5660A-5 TYP	HI-5660A-5 MAX	UNITS
TEMPERATURE RANGE							
Operating	0		+75	0		+75	°C
Storage	-25		+150	-25		+150	°C
POWER REQUIREMENTS							
V_{CC}, +4.5V to +16.5V_{DC}		7	12		7	12	mA
V_{EE}, -11.4 to -16.5V_{DC}		-13	-17		-13	-17	mA
POWER SUPPLY GAIN SENSITIVITY (Note 3)							
V_{CC} = +4.5 to +16.5V_{DC} ; V_{EE} = -15V		1	10		1	10	ppm of FS/%
V_{EE} = -11.4 to -16.5V_{DC} ; V_{CC} = +15V		1	10		1	10	ppm of FS/%
PROGRAMMABLE OUTPUT RANGES (See Table 1)		0 to +5 -2.5 to +2.5 0 to +10 -5 to +5 -10 to +10			0 to +5 -2.5 to +2.5 0 to +10 -5 to +5 -10 to +10		V V V V V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor for R_2 (Figure 1)		±0.1	±0.25		±0.1	±0.25	% of FS
Bipolar Zero Error with Fixed 50Ω Resistor for R_3 (Figure 2)		±0.05	±0.15		±0.05	±0.1	% of FS
Gain Adjustment Range (Figure 1)	±0.25			±0.25			% of FS
Bipolar Zero Adjustment Range (Fig. 2)	±0.15			±0.15			% of FS
REFERENCE INPUT							
Input Impedance	16K	20K	24K	16K	20K	24K	Ω
POWER DISSIPATION		230	330		230	330	mW

MULTIPLYING MODE PERFORMANCE (All Models)

Quadrants	Two (2): Bipolar Operation at Digital Input Only.
Reference Voltage	Unipolar: +10V Max, +2V Min.
Accuracy	10 Bits (±0.05% of Reduced F.S.) for 2V_{DC} Reference Voltage.
Reference Feedthrough (Unipolar Mode, All Bits OFF, and +2V to +10V (p-p), Sinewave Frequency for 1/2 LSB (p-p) Feedthrough)	22kHz Typical
Output Slew Rate 10%-90%	1.3mA/μs
90%-10%	1.3mA/μs
Output Settling Time (All Bits ON and a +2V to +10V Step Change in Reference Voltage)	1.5μs to 0.01% F.S.

CONTROL AMPLIFIER							
Full Power Bandwidth (+10V to +3V)		200			200		kHz
Small Signal Closed-Loop Bandwidth		2.4			2.4		MHz

NOTES:

1. The Digital Input Levels are Guaranteed but not Over the Temperature Range.
2. See Settling Time Section.

Electrical Specifications (T_A = +25°C, V_{CC} = +15V, V_{EE} = -15V, unless otherwise specified.)

MODEL	HI-5660-2, HI-5660-8			HI-5660A-2, HI-5660A-8			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
DATA INPUTS (Note 1) (Pins 13 to 24)							
TTL or 5V CMOS (T_{MIN} to T_{MAX})							
Input Voltage							
Bit ON Logic "1"	2.0		5.5	2.0		5.5	V
Bit OFF Logic "0"	0.0		0.8	0.0		0.8	V
Logic Current (Each Bit)							
Bit ON Logic "1"		2	10		2	10	μA
Bit OFF Logic "0"		-10	-50		-10	-50	μA
RESOLUTION			12			12	Bits
OUTPUT							
Current Unipolar (All Bits On)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar (All Bits on or Off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (Exclusive of Span Resistors)	2.0K	2.5K	3.0K	2.0K	2.5K	3.0K	Ω
Offset Unipolar		.01	.05		.01	.05	% of FS
Bipolar (Figure 2, R_3 = 50Ω Fixed)		.05	.15		.05	.10	% of FS
Capacitance		25			25		pF
Compliance Voltage, T_{MIN} to T_{MAX}	-3		+12	-3		+12	V
ACCURACY (Error Relative to Full Scale)							
+25°C		±1/4 (0.006)	±1/2 (0.012)		±1/8 (0.003)	±1/4 (0.006)	LSB % of FS
T_{MIN} to T_{MAX}		±1/2 (0.012)	±3/4 (0.018)		±1/4 (0.006)	±1/2 (0.012)	LSB % of FS
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_{MIN} to T_{MAX}	MONOTONICITY GUARANTEED (±1 LSB MAX)						
TEMPERATURE COEFFICIENTS							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		7	10		7	10	ppm/°C
Differential Nonlinearity		2	6		2	2	ppm/°C
SETTLING TIME TO 1/2 LSB							
With 50Ω External Load		500			500		ns

MODEL	HI-5660-2, HI-5660-8 MIN	HI-5660-2, HI-5660-8 TYP	HI-5660-2, HI-5660-8 MAX	HI-5660A-2, HI-5660A-8 MIN	HI-5660A-2, HI-5660A-8 TYP	HI-5660A-2, HI-5660A-8 MAX	UNITS
TEMPERATURE RANGE							
Operating	-55		+125	-55		+125	°C
Storage	-65		+150	-65		+150	°C
POWER REQUIREMENTS							
V_{CC}, +4.5V to +16.5V_{DC}		7	12		7	12	mA
V_{EE}, -11.4 to -16.5V_{DC}		-13	-17		-13	-17	mA
POWER SUPPLY GAIN SENSITIVITY							
V_{CC} = +4.5 to +16.5V_{DC}; V_{EE} = -15V		1	10		1	10	ppm of FS/%
V_{EE} = -11.4 to -16.5V_{DC}; V_{CC} = +15V		1	10		1	10	ppm of FS/%
PROGRAMMABLE OUTPUT RANGES (See Table 1)	0 to +5 -2.5 to +2.5 0 to +10 -5 to +5 -10 to +10			0 to +5 -2.5 to +2.5 0 to +10 -5 to +5 -10 to +10			V V V V V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor for R_2 (Figure 1)		±0.1	±0.25		±0.1	±0.25	% of FS
Bipolar Offset Error with Fixed 50Ω Resistor for R_3 (Figure 2)		±0.05	±0.15		±0.05	±0.1	% of FS
Gain Adjustment Range (Figure 1)	±0.25			±0.25			% of FS
Bipolar Offset Adjustment Range (Fig. 2)	±0.15			±0.15			% of FS
REFERENCE INPUT							
Input Impedance	16K	20K	24K	16K	20K	24K	Ω
POWER DISSIPATION		230	330		230	330	mW
CONTROL AMPLIFIER							
Full Power Bandwidth (+10V to +3V)		200			200		kHz
Small Signal Closed-Loop Bandwidth		2.4			2.4		MHz

MULTIPLYING MODE PERFORMANCE (All Models)

Quadrants	Two (2): Bipolar Operation at Digital Input Only.
Reference Voltage	Unipolar: +10V Max, +2V Min.
Accuracy	10 Bits (±0.05% of Reduced F.S.) for 2V_{DC} Reference Voltage.
Reference Feedthrough (Unipolar Mode, All Bits OFF, and +2V to +10V (p-p), Sinewave Frequency for 1/2 LSB (p-p) Feedthrough)	22kHz Typical
Output Slew Rate 10%-90%	1.3mA/μs
90%-10%	1.3mA/μs
Output Settling Time (All Bits ON and a +2V to +10V Step Change in Reference Voltage)	1.5μs to 0.01% F.S.

NOTES:
1. The Digital Input Levels are Guaranteed but not Tested Over the Temperature Range.
2. See Settling Time Section.

DIGITAL INPUTS

The HI-5660 accepts digital input codes in binary format and may be user connected for any one of three binary codes: Straight Binary, Two's Complement*, or Offset Binary (See Operating Instructions).

	ANALOG OUTPUT		
DIGITAL INPUT	Straight Binary	Offset Binary	Two's Complement*
MSB...LSB			
000...000	Zero	-FS (Full Scale)	Zero
100...000	½FS	Zero	-FS
111...111	+FS – 1 LSB	+FS – 1 LSB	Zero – 1 LSB
011...111	½FS – 1 LSB	Zero – 1 LSB	+FS – 1 LSB

*Invert MSB with external inverter to obtain Two's Complement Coding

ACCURACY

INTEGRAL NONLINEARITY – The maximum deviation of the actual transfer characteristic from an ideal straight line. The ideal line is positioned according to "end-point linearity" for D/A converter products from Harris Semiconductor, i. e. the line is drawn between the end-points of the actual transfer characteristic (codes 00. . .0 and 11. . .1).

DIFFERENTIAL NONLINEARITY – The difference between one LSB and the output voltage change corresponding to any two consecutive codes. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity.

MONOTONICITY – The property of a D/A converter's transfer function which guarantees that the output derivative will not change sign in response to a sequence of increasing (or decreasing) input codes. That is, the only output response to a code change is to remain constant, increase for increasing code, or decrease for decreasing code.

SETTLING TIME

That interval between application of a digital step input, and final entry of the analog output within a specified window about the settled value. Harris Semiconductor usually specifies a unipolar 10V full scale step, to be measured from 50% of the input digital transition, and a window of ±1/2 LSB about the final value. The device output is then rated according to the worst (longest settling) case: low to high, or high to low.

DRIFT

GAIN DRIFT – The change in full scale analog output over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Gain error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Gain drift is calculated for both high (T_H -25°C) and low ranges (+25°C -T_L) by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst case drift.

OFFSET DRIFT – The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Offset error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Offset Drift is calculated for both high (T_H -25°C) and low (+25°C -T_L) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst-case drift.

POWER SUPPLY SENSITIVITY

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in –15V or +15V supplies. It is specified under DC conditions and expressed as parts per million of full scale range per percent of change in power supply (ppm of FSR/%).

COMPLIANCE

Compliance Voltage is the maximum output voltage range that can be tolerated and still maintain its specified accuracy. Compliance Limit implies functional operation only and makes no claims to accuracy.

GLITCH

A glitch on the output of a D/A converter is a transient spike resulting from unequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale or the major carry code transition from 011...1 to 100...0 or vice versa. For example, if turn ON is greater than turn OFF for 011...1 to 100...0, an intermediate state of 000...0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably.

Applying the HI-5660

OP AMP SELECTION

The HI-5660's current output may be converted to voltage using the standard connections shown in Figures 1 and 2. The choice of operational amplifier should be reviewed for each application, since a significant trade-off may be made between speed and accuracy.

For highest precision, use an HA-5130. This amplifier contributes negligible error, but requires about 11μs to settle within ±0.1% following a 10V step.

The Harris Semiconductor HA-2600 is the best all-around choice for this application, and it settles in 1.5μs (also to ±0.1% following a 10V step). Remember, settling time for the DAC-amplifier combination is $\sqrt{t_D^2 + t_A^2}$, where t_D, t_A are settling times for the DAC and amplifier.

Applying the HI-5660 (Continued)

TABLE 1. OPERATING MODES AND CALIBRATION

MODE	CIRCUIT CONNECTIONS: OUTPUT RANGE	PIN10 TO	PIN 11 TO	RESISTOR (R)*	CALIBRATION: APPLY INPUT CODE	ADJUST	TO SET V_O
Unipolar (See Fig. 1)	0 to +10V	V_O	Pin 10	1.43K	All 0's All 1's	R1 R2	0V +9.99756V
	0 to +5V	V_O	Pin 9	1.1K	All 0's All 1's	R1 R2	0V +4.99878V
Bipolar (See Fig. 2)	±10V	NC	V_O	1.69K	All 0's All 1's	R3 R4	-10V +9.99512V
	±5V	V_O	Pin 10	1.43K	All 0's All 1's	R3 R4	-5V +4.99756V
	±2.5V	V_O	Pin 9	1.1K	All 0's All 1's	R3 R4	-2.5V +2.49878V

*Many op amps do not require this resistor, since a bias current of 60nA produces a worst case output error of only 100μV. For a low bias current amplifier, connect its non-inverting input directly to ground.

NO-TRIM OPERATION

The HI-5660 will perform as specified without calibration adjustments. To operate without calibration, substitute 50 Ω resistors for the 100 Ω trimming potentiometers: In Figure 1 replace R2 with 50 Ω ; also remove the network on pin 7 and connect 50 Ω to ground. For bipolar operation in Figure 2, replace R3 and R4 with 50 Ω resistors.

With these changes, performance is guaranteed as shown under Specifications, "External Adjustments". Typical unipolar zero will be ±1/2 LSB plus the op amp offset.

When using wide bandwidth op amps, the feedback capacitor C may be selected to minimize settling time.

CALIBRATION

Calibration provides the maximum accuracy from a converter by adjusting its gain and offset errors to zero. For the HI-5660, these adjustments are similar whether the current output is used, or whether an external op amp is added to convert this current to a voltage. Refer to Table 1 for the voltage output case, along with Figure 1 or 2.

Calibration is a two step process for each of the five output ranges shown in Table 1. First adjust the negative full scale (zero for unipolar ranges). This is an offset adjust which translates the output characteristic, i.e. affects each code by the same amount.

Next adjust positive FS. This is a gain error adjustment, which rotates the output characteristic about the negative FS value.

For the bipolar ranges, this approach leaves an error at the zero code, whose maximum value is the same as for integral nonlinearity error. In general, only two values of output may be calibrated exactly; all others must tolerate some error. Choosing the extreme end points (plus and minus full scale) minimizes this distributed error for all other codes.

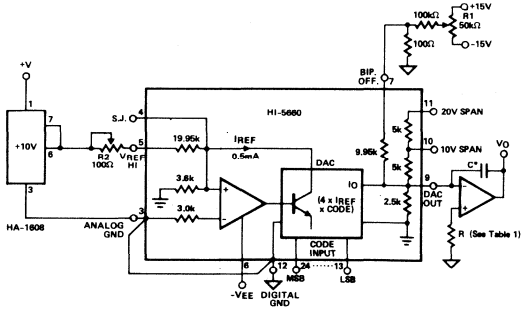


FIGURE 1. UNIPOLAR VOLTAGE OUTPUT

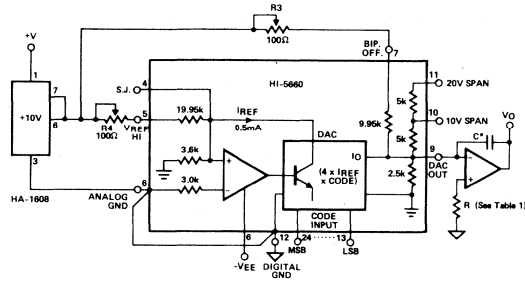


FIGURE 2. BIPOLAR VOLTAGE OUTPUT

Settling Time

This is a challenging measurement, in which the result depends on the method chosen, the precision and quality of test equipment and the operating configuration of the DAC (test conditions). As a result, the different techniques in use by converter manufacturers can lead to consistently different results. An engineer should understand the advantage and limitations of a given test method before using the specified settling time as a basis for design.

The approach used for several years at Harris Analog Products Division calls for a strobed comparator to sense final perturbations of the DAC output waveform. This gives the LSB a reasonable magnitude (814μV for the HI-5660), which provides the comparator with enough overdrive to establish an accurate ±1/2 LSB window about the final settled value. Also, the required test conditions simulate the DAC's environment for a common application – use in a successive approximation A/D converter. Considerable experience has shown this to be a reliable and repeatable way to measure settling time.

The usual specification is based on a 10V step, produced by simultaneously switching all bits from off-to-on (t_{ON}) or on-to-off (t_{OFF}). The slower of the two cases is specified, as measured from 50% of the digital input transition to the final entry within a window of ±1/2 LSB about the settled value. Four measurements characterize a given type of DAC:

(a) t_{ON}, to final value +1/2 LSB
(b) t_{ON}, to final value -1/2 LSB
(c) t_{OFF}, to final value +1/2 LSB
(d) t_{OFF}, to final value -1/2 LSB

(Cases (b) and (c) may be eliminated unless the overshoot exceeds 1/2 LSB). For example, refer to Figure 3 for the measurement of case (d).

PROCEDURE

As shown in Figure 3B, settling time equals t_X plus the comparator delay (t_D = 15ns). To measure t_X,

- Adjust the delay on generator # 2 for a t_X of several microseconds. This assures that the DAC output has settled to its final value.
- Switch on the LSB (+5V).
- Adjust the V_{LSB} supply for 50 percent triggering at COMPARATOR OUT. This is indicated by traces of equal brightness on the oscilloscope display as shown in Figure 3B. Note DVM reading.
- Switch the LSB to Pulse (P).
- Readjust the V_{LSB} supply for 50% triggering as before, and note DVM reading. One LSB equals one tenth the difference in the DVM readings noted above.
- Adjust the V_{LSB} supply to reduce the DVM reading by 5 LSB's (DVM reads 10X, so this sets the comparator to sense the final settled value minus 1/2 LSB). Comparator output disappears.
- Reduce generator # 2 delay until comparator output reappears, and adjust for "equal brightness".
- Measure t_X from scope as shown in Figure 3B. Settling time equals $t_X + t_D$, i.e. t_X +15ns.

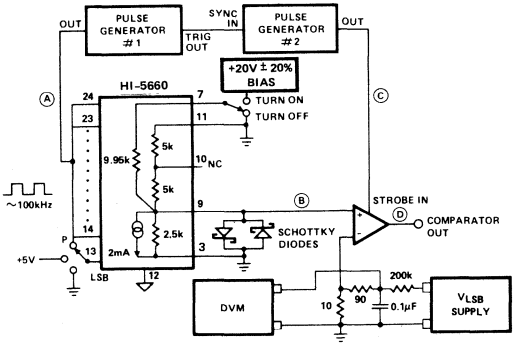


FIGURE 3A.

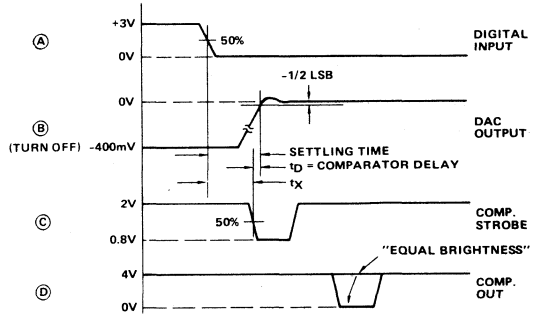


FIGURE 3B.

Other Considerations

GROUNDS

The HI-5660 has two ground terminals, pin 3 (ANALOG GND) and pin 12 (DIGITAL GND). The current through pin 3 is near-zero DC, but pin 12 carries up to 1.75mA of code-dependent current from bits 1, 2 and 3. The general rule is to connect pin 3 to the system analog ground and pin 12 to the power or digital ground. If the system has a single ground point, provide separate paths to pins 3 and 12.

Current cancellation in pin 3 is accomplished as follows: An auxiliary 9 bit R-2R ladder is driven by the complement of the HI-5660 input code. Together, the main and auxiliary ladders draw a constant 2.25mA from the internal analog ground, regardless of input code. This current is then sourced from the positive supply via a current mirror, yielding near-zero current through pin 3.

LAYOUT

Connections to pin 9 (I_{OUT}) on the HI-5660 are very critical for high speed performance. Output capacitance of the DAC is only 25pF, so a small change or additional capacitance may alter the output op amp's stability and affect settling time. Connections to pin 9 should be short and few. Component leads should be short on the side connecting to pin 9 (as for feedback capacitor C).

BYPASS CAPACITORS

Power supply bypass capacitors on the op amp will serve the HI-5660 also. If no op amp is used, a 0.01μF ceramic capacitor from each supply terminal to pin 12 is sufficient.

Die Characteristics

Transistor Count		158
Die Size:		104 x 172 mils
Thermal Constants;	θ_{ja}	52°C/W
	θ_{jc}	17°C/W
Tie Substrate to:		Analog Ground
Process:		Bipolar - DI

HI-5680

12-Bit Low Cost Monolithic Digital-to-Analog Converter

Features

- DAC 80 ALTERNATE SOURCE
- MONOLITHIC CONSTRUCTION (SINGLE CHIP)
- FAST SETTLING
- GUARANTEED MONOTONIC 0°C to 75°C
- WAFER LASER TRIMMED
- APPLICATIONS RESISTORS ON-CHIP
- ON-BOARD REFERENCE
- DIELECTRIC ISOLATION (DI) PROCESSING
- ±12V POWER SUPPLY OPERATION

Applications

- HIGH SPEED A/D CONVERTERS
- PRECISION INSTRUMENTATION
- CRT DISPLAY GENERATION

Description

The HI-5680 is a monolithic, direct replacement for the popular DAC80-CBI, DAC80Z-CBI, and DAC85C-CBI, incorporating the best features of each. Single chip construction, along with several design innovations, make the HI-5680 the optimum choice for low cost, high reliability applications.

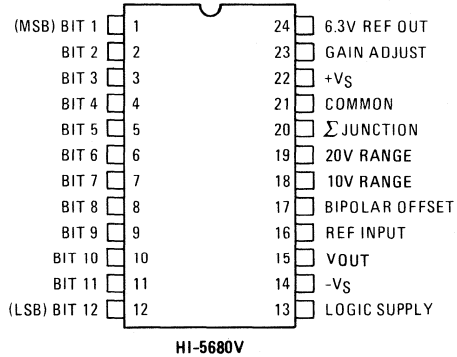
Harris' unique Dielectric Isolation(DI) processing reduces internal parasitics, resulting in fast switching times and minimum glitch. On-board span resistors are provided for good tracking over temperature, and are laser trimmed to high accuracy. These may be used with the on-board op-amp (voltage output models; HI-5680V), or with a user supplied external amplifier (HI-5680I).

Internally, the HI-5680 eliminates code dependent ground currents by routing current from the positive supply to the internal ground node, as determined by an auxiliary R-2R ladder. This results in a cancellation of code dependent ground currents allowing virtually zero variation in current through the package common, pin 21.

The HI-5680 is available in both current and voltage output models which are guaranteed over the 0°C to +75°C temperature range. All models include a buried zener reference featuring low temperature coefficient. In addition, the voltage output models include an on-board output amplifier. Both versions operate with a +5V logic supply and a $\pm V_S$ in the range of ±(11.4V to 16.5V).

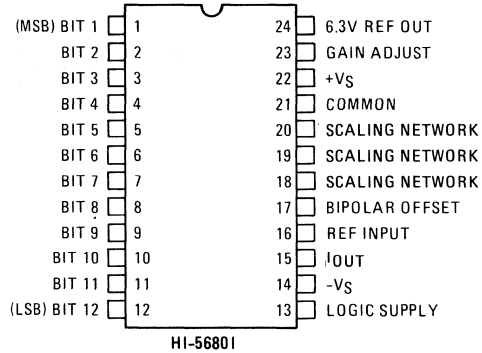
Pinouts

TOP VIEW



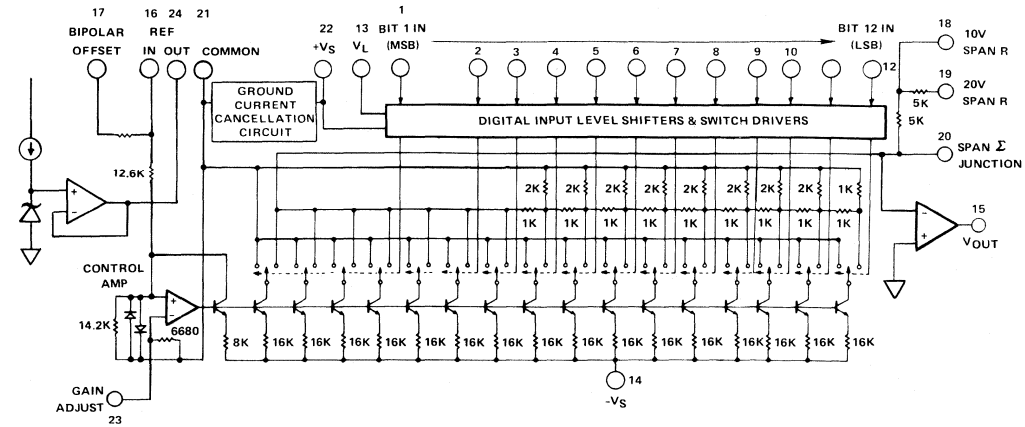
HI-5680V
VOLTAGE OUTPUT

TOP VIEW



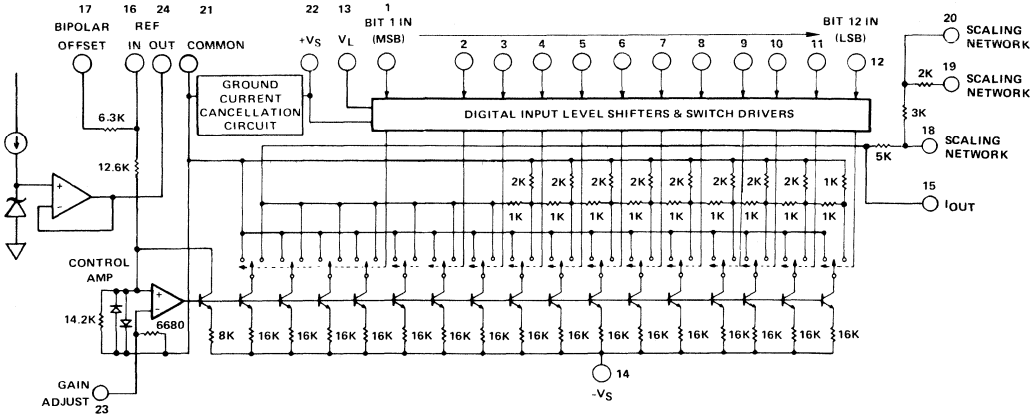
HI-5680I
CURRENT OUTPUT

Functional Diagram Voltage Output



HI-5680 V

Functional Diagram Current Output



HI-5680 I

Absolute Maximum Ratings (Note 1)

Power Supply Inputs	$+V_S$	+20V	Junction Temperature	175°C
	$-V_S$	−20V	Operating Temperature Range	
	$+V_{LOGIC}$	+20V	HI-5680I/V-5	0°C to +75°C
Reference	Input (pin 16)	$+V_S$	Storage Temperature Range	−65°C to +150°C
	Output drain	2.5mA		
Digital Inputs	Bits 1 to 12	−1V to +12V		

Electrical Specifications

(T_A = +25°C, V_S = ± 15V, V_{LOGIC} = +5V, Pin 16 connected to Pin 24 unless otherwise specified.)

PARAMETER	CONDITIONS	HI-5680 MIN	HI-5680 TYP	HI-5680 MAX	UNITS
DIGITAL INPUT (3)					
Resolution				12	Bits
Logic Levels	TTL Compatible				
Logic "1"	at +1 μA	+2		+5.5	Volts
Logic "0"	at -100 μA	0		+0.8	Volts
ACCURACY (3)					
Linearity Error	0°C to +75°C		±¼	±½	LSB
Differential Lin. Error	0°C to +75°C		±½	±¾	LSB
Gain Error (2)			±0.1	±0.3	%FSR (4)
Offset Error (2)			±.05	±0.15	%FSR
Monotonicity	0°C to +75°C		Guaranteed		
DRIFT (3)	0°C to +75°C				
Total Bipolar Drift (Includes gain, offset and linearity drifts.)				±20	ppm/°C
Total Error	0°C to +75°C				
Unipolar (Note 6)			± 0.08	±0.15	%FSR
Bipolar (Note 6)			± 0.06	±.1	%FSR
Gain	Including internal reference		±15	±30	ppm/°C
	Exclusive of internal reference		±5	±7	ppm/°C
Unipolar Offset			±1	±3	ppm/°C
Bipolar Offset			±5	±10	ppm/°C
CONVERSION SPEED (3)					
Voltage Models					
Settling time (3)	to ±0.01% of FSR for FSR Change				
With 10kΩ Feedback			3		μs
With 5kΩ Feedback			1.5		μs
For 1 LSB change			1.5		μs
Slew Rate		10	15		V/μs
Current Models					
Settling time (3)	to ±0.01% of FSR for FSR Change				
10 to 100Ω load			300		ns
1kΩ load			1000		ns
ANALOG OUTPUT					
Voltage Models					
Output current		±5			mA
Output Resistance			.05		Ω
Short Circuit Duration	to common		continuous		

PARAMETER	CONDITIONS	HI-5680X MIN	HI-5680X TYP	HI-5680X MAX	UNITS
ANALOG OUTPUT					
Current Models					
Output Current					
Unipolar		-1.6	−2	-2.4	mA
Bipolar		± 0.8	±1	± 1.2	mA
Output Resistance					
Unipolar			2.0		kΩ
Bipolar			2.0		kΩ
Compliance Limit (3)		-2.5		+10	V
INTERNAL REFERENCE					
Output Voltage		+6.174	+6.3	+6.426	V
Output Impedance			1.5		Ω
External Current				+2.5	mA
Tempco of Drift			20		ppm/°C
POWER SUPPLY SENSITIVITY (3)					
+15V supply				.002	$\frac{\%FSR}{\Delta V_s}$
−15V supply				.002	
+5V supply				.002	
POWER SUPPLY REQUIREMENTS (5)					
Range					
+15V		+11.4	+15	+16.5	V
−15V		-11.4	-15	-16.5	V
+5V		+ 4.5	+ 5	+16.5	V
Current					
+15V			8	11	mA
-15V			-12	-20	mA
+5V			4.5	8	mA

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Adjustable to zero using external potentiometers.
3. See definitions.
4. FSR is "Full Scale Range" and is 20V for ± 10V range, 10V for ± 5V range, etc., or 2mA (± 20%) for current output.
5. The HI-5680 will operate with supply voltages as low as ± 11.4V. It is recommended that output voltage range -10V to +10V not be used if the supply voltages are less than ± 12V.
6. With gain and offset errors adjusted to zero at 25°C.

Die Characteristics

Transistor Count		259
Die Size:		210 x 125 mils
Thermal Constants;	θ_{ja}	49°C/W
	θ_{jc}	12°C/W
Tie Substrate to:		Ground
Process:		Bipolar - DI

Definitions of Specifications

DIGITAL INPUTS

The HI-5680 accepts digital input codes in complementary binary, complementary offset binary, and complementary two's complement binary.

DIGITAL INPUT	ANALOG OUTPUT		
	Complementary Binary	Complementary Offset Binary	Complementary Two's Complement *
MSB LSB			
000...000	+ Full Scale	+ Full Scale	-LSB
100...000	Mid Scale -1 LSB	-1 LSB	+ Full Scale
111...111	Zero	- Full Scale	Zero
011...111	+½ Full Scale	Zero	- Full Scale
* Invert MSB with external inverter to obtain CTC Coding			

SETTLING TIME

That interval between application of a digital step input, and final entry of the analog output within a specified window about the settled value. Harris Semiconductor usually specifies a unipolar 10V or bipolar full scale step, to be measured from 50% of the input digital transition, and a window of ±½ LSB about the final value. The device output is then rated according to the worst (longest settling) case: low to high, or high to low.

DRIFT

GAIN DRIFT – The change in full scale analog output over the specified temperature range expressed in parts per million of full scale per °C (ppm of FSR/°C). Gain error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Gain drift is calculated for both high (T_H –25°C) and low ranges (+25°C–T_L) by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst case drift.

OFFSET DRIFT – The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Offset error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Offset Drift is calculated for both high (T_H –25°C) and low (+25°C –T_L) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst-case drift.

ACCURACY

INTEGRAL NONLINEARITY – The maximum deviation of the actual transfer characteristic from an ideal straight line. The ideal line is positioned according to "end-point linearity" for D/A converter products from Harris Semiconductor, i.e. the line is drawn between the end-points of the actual transfer characteristic (codes 00...0 and 11...1).

DIFFERENTIAL NONLINEARITY – The difference between one LSB and the output voltage change corresponding to any two consecutive codes. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity.

MONOTONICITY – The property of a D/A converter's transfer function which guarantees that the output derivative will not change sign in response to a sequence of increasing (or decreasing) input codes. That is, the only output response to a code change is to remain constant, increase for increasing code, or decrease for decreasing code.

POWER SUPPLY SENSITIVITY

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in -15V, or +15V supplies. It is specified under DC conditions and expressed as parts per million of full scale range per percent of change in power supply (ppm of FSR/%).

COMPLIANCE

Compliance Voltage is the maximum output voltage range that can be tolerated and still maintain its specified accuracy. Compliance Limit implies functional operation only and makes no claims to accuracy.

GLITCH

A glitch on the output of a D/A converter is a transient spike resulting from inequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale or the major carry code transition from 011...1 to 100...0 or vice versa. For example, if turn ON is greater than turn OFF for 011...1 to 100...0, an intermediate state of 000...0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably. (Measured as one half the product of duration and amplitude.)

DECOUPLING AND GROUNDING

For best accuracy and high frequency performance, the grounding and decoupling scheme shown in Figure 1 should be used. Decoupling capacitors should be connected close to the HI-5680 (preferrably to the device pins) and should be tantalum or electrolytic bypassed with ceramic types for best high frequency noise rejection.

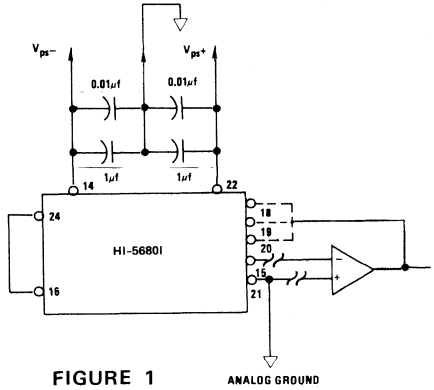


FIGURE 1

REFERENCE SUPPLY

An internal 6.3Volt reference is provided on board all HI-5680 models. This voltage (pin 24) is accurate to ±2% and must be connected to the reference input (pin 16) for specified operation. This reference may be used externally, provided current drain is limited to 2.5mA. An external buffer amplifier is recommended if this reference is to be used to drive other system components. Otherwise, variations in the load driven by the reference will result in gain variations of the HI-5680. All gain adjustments should be made under constant load conditions.

VOLTAGE OUTPUT HI-5680V

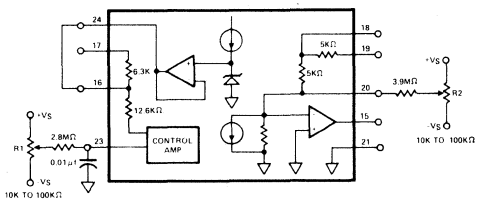


FIGURE 2

RANGE CONNECTIONS

	RANGE	CONNECT PIN 15	CONNECT PIN 17	CONNECT PIN 19
Unipolar	0 to +5V	18	N.C.	20
	0 to + 10V	18	N.C.	N.C.
Bipolar	±2.5V	18	20	20
	±5V	18	20	N.C.
	±10V	19	20	15

CURRENT OUTPUT HI-5680I

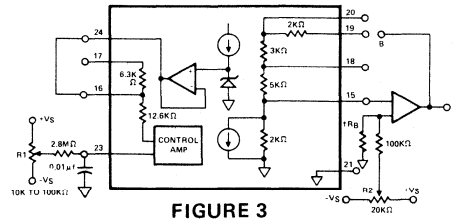


FIGURE 3

†R_B should equal the DAC's output resistance, which is 2KΩ // $R_{FEEDBACK}$.

EXTERNAL AMPLIFIER CONNECTIONS

To use the HI-5680I with an external amplifier, connect as follows:

RANGE	PIN 17 to	PIN 18 to	PIN 19 to	PIN 20 to
0 to +10V	N.C.	B	18*	19*
0 to +5V	N.C.	B	15	N.C.
±10V	15	N.C.	B	N.C.
±5V	15	B	18*	19*
±2.5V	15	B	15	N.C.

*these connections help reduce stray capacitance in the feedback loop.

GAIN AND OFFSET CALIBRATION

(Applies to Figure 2 and 3.)

UNIPOLAR CALIBRATION

Step 1: Offset
- Turn all bits OFF (11...1)
- Adjust R_2 for zero volts out

Step 2: Gain
- Turn all bits ON (00...0)
- Adjust R_1 for FS-1LSB
- That Is:
  - 4.9988 for 0 to +5V range
  - 9.9976 for 0 to +10V range

BIPOLAR CALIBRATION

Step 1: Offset
- Turn all bits OFF (11...1)
- Adjust R_2 for Negative FS
- That Is:
  - −10V for ±10V range
  - −5V for ±5V range
  - −2.5V for ±2.5 range

Step 2: Gain
- Turn all bits ON (00...0)
- Adjust R_1 for positive FS-1LSB
- That Is:
  - +9.9951V for ±10V range
  - +4.9976V for ±5V range
  - +2.4988V for ±2.5V range

This Bipolar procedure adjusts the output range end points. The maximum error at zero (half scale) will not exceed the Linearity error. See the "Accuracy" specifications.

HI-5685/5685A

High Performance Monolithic 12-Bit Digital-to-Analog Converter

Features

- DAC 85 ALTERNATE SOURCE
- MONOLITHIC CONSTRUCTION
- FAST SETTLING
- GUARANTEED MONOTONIC –25°C TO +85°C
- WAFER LASER TRIMMED
- APPLICATIONS RESISTORS ON-CHIP
- ON-BOARD REFERENCE
- DIELECTRIC ISOLATION (DI) PROCESSING
- ±12V POWER SUPPLY OPERATION

Applications

- HIGH SPEED A/D CONVERTERS
- PRECISION INSTRUMENTATION
- CRT DISPLAY GENERATION

Description

The HI-5685 is a monolithic direct replacement for the popular DAC85-CBI and the ACCA85LD-CBI. Single chip construction along with several design innovations make the HI-5685 the optimum choice for low cost, high reliability applications.

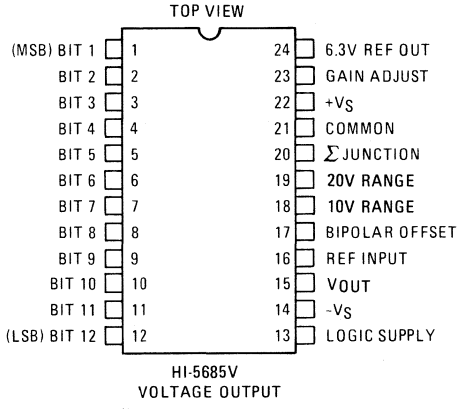
Harris unique Dielectric Isolation (DI) processing reduces internal parasitics resulting in fast switching times and minimum glitch. On board span resistors are provided for good tracking over temperature, and are laser trimmed to high accuracy. These may be used with the on-board op-amp (voltage output models; HI-5685V), or with a user supplied external amplifier (HI-5685).

Internally, the HI-5685 eliminates code dependent ground currents by routing current form the positive supply to the internal ground node, as determined by an auxiliary R-2R ladder. This results in a cancellation of code dependent ground currents allowing virtually zero variation in current through the package common, pin 21.

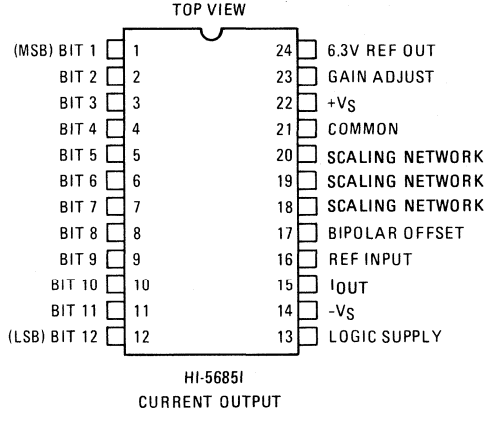
The HI-5685 and HI-5685A are available in both current and voltage output models which are guaranteed over the -25°C to +85°C temperature range. All models include a buried zener reference featuring low temperature coefficient. In addition, the voltage output models include and on-board output amplifier. Both versions operate with a +5V logic supply and a ± V_S in the range of ± (11.4V to 16.5V).

The HI-5685A offers exceptionally low drift over temperature. Gain drift is a maximum +10ppm/°C, over -25°C to +85°C.

Pinouts

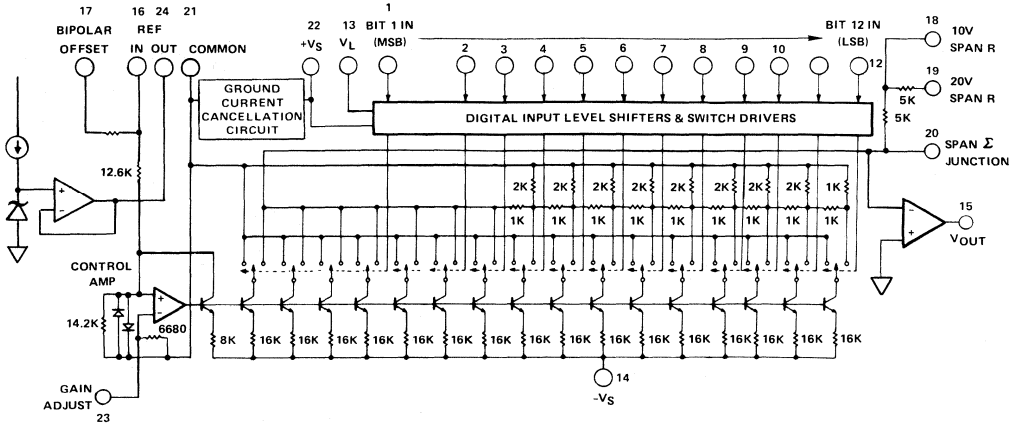


HI-5685V
VOLTAGE OUTPUT



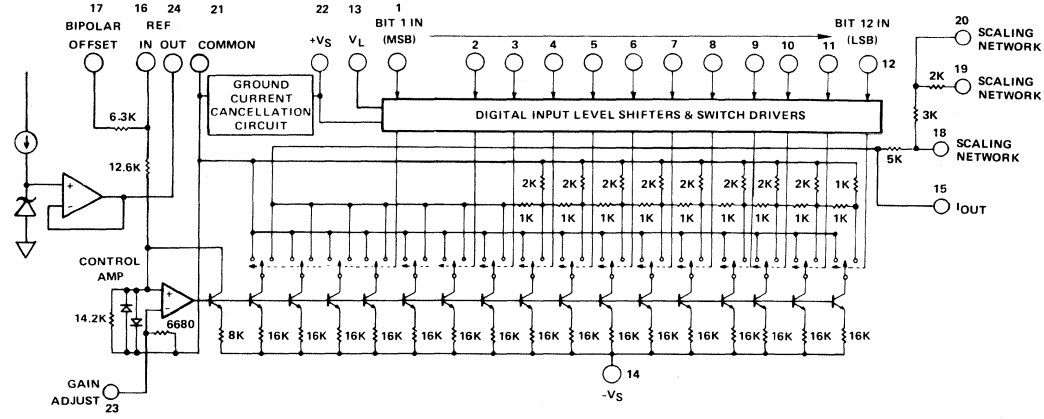
HI-5685I
CURRENT OUTPUT

Functional Diagram Voltage Output



HI-5685 V

Functional Diagram Current Output



HI-5685 I

Absolute Maximum Ratings (1)

Power Supply Inputs	$+V_S$	+20V	Junction Temperature	175°C
	$-V_S$	−20V		
	$+V_{LOGIC}$	+20V	Operating Temperature Range	
Reference	Input (pin 16)	$\pm V_S$	HI-5685I/V−4	−25°C to +85°C
	Output drain	2.5mA	HI-5685AI/V−4	−25°C to +85°C
Digital Inputs	Bits 1 to 12	−1V to +12V	Storage Temperature Range	−65° to +150°C

Electrical Specifications

(T_A = +25°C, V_S = ± 15V, V_{LOGIC} = 5V, Pin 16 connected to Pin 24 unless otherwise specified.)

PARAMETER	CONDITIONS	HI-5685 MIN	HI-5685 TYP	HI-5685 MAX	UNITS
DIGITAL INPUT (3)					
Resolution				12	Bits
Logic Levels	TTL Compatible				
Logic "1"	at +1 μA	+2		+5.5	V
Logic "0"	at −100 μA	0		+0.8	V
Accuracy (3)					
Linearity Error	at +25°C			±½	LSB
	−25°C to +85°C			±½	LSB
Differential Lin. Error				±½	LSB
Gain Error (2)			±0.1	±0.15	%FSR (4)
Offset Error (2)			±0.05	±0.1	%FSR
Monotonicity	-25°C to +85°C		GUARANTEED		
DRIFT (3) HI-5685	−25°C to +85°C				
Gain				±20	
Offset					
Unipolar			±1	±3	ppm/°C
Bipolar			±5	±10	
DRIFT (3) HI-5685A (Low Drift)	−25°C to +85°C				
Gain				±10	
Offset					ppm/°C
Unipolar			±1		
Bipolar				±5	
CONVERSION SPEED					
Voltage Models					
Settling Time (3)	to ±0.01% of FSR for FSR Change				
With 10 kΩ Feedback			3		μs
With 5kΩ Feedback			1.5		μs
For 1 LSB Change			1.5		μs
Slew Rate			15		V/μs
Current Models					
Settling Time (3)	to ±0.01% of FSR for FSR Change				
10 to 100 Ω load			300		ns
1kΩ load			1.0		μs

PARAMETER	CONDITIONS	HI-5685 MIN	HI-5685 TYP	HI-5685 MAX	UNITS
ANALOG OUTPUT					
Voltage Models					
Output Current		±5			mA
Output Impedance (DC)			0.05		Ω
Current Models					
Output Current	Full Scale				
Unipolar		-1.6	−2	-2.4	mA
Bipolar		±0.8	±1	±1.2	mA
Output Resistance					
Unipolar			2.0		kΩ
Bipolar			2.0		kΩ
Compliance Limit (3)		−2.5		+10	V
INTERNAL REFERENCE					
Output voltage		+6.174	+6.3	+6.426	V
Output Impedance			1.5		Ω
External Current				+2.5	mA
Tempco of Drift			±10	±20	ppm/°C
POWER SUPPLY SENSITIVITY (3)					
+15V				.002	$\frac{\%FSR}{\Delta V_S}$
−15V				.002	
+5V				.002	
POWER SUPPLY REQUIREMENTS(5)					
Range					
+15V		+11.4	+15	+16.5	V
−15V		−11.4	−15	−16.5	V
+5V		+4.5	+5	+16.5	V
Current					
+15V			8	11	mA
−15V			-12	-20	mA
+5V			4.5	8	mA

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Adjustable to zero using external potentiometers.
3. See Definitions.
4. FSR is "full scale range" and is 20V for ±10V range, 10V for ±5V range, etc., or 2mA (±20%) for current output.
5. The HI-5685 will operate with supply voltages as low as ±11.4V. It is recommended that output voltage range −10V to +10V not be used if the supply voltages are less than ±12.5V.

Die Characteristics

Transistor Count		259
Die Size:		210 x 125 mils
Thermal Constants;	θ ja	49°C/W
	θ jc	12°C/W
Tie Substrate to:		Ground
Process:		Bipolar - DI

Definitions of Specifications

DIGITAL INPUTS

The HI-5685 accepts digital input codes in complementary binary, complementary offset binary, and complementary two's complement binary.

DIGITAL INPUT	ANALOG OUTPUT		
	Complementary Binary	Complementary Offset Binary	Complementary Two's Complement *
MSB LSB			
000...000	+ Full Scale	+ Full Scale	-LSB
100...000	Mid Scale -1 LSB	-1 LSB	+ Full Scale
111...111	Zero	- Full Scale	Zero
011...111	+½ Full Scale	Zero	- Full Scale
* Invert MSB with external inverter to obtain CTC Coding			

SETTLING TIME

That interval between application of a digital step input, and final entry of the analog output within a specified window about the settled value. Harris Semiconductor usually specifies a unipolar 10V or bipolar full scale step, to be measured from 50% of the input digital transition, and a window of ±½ LSB about the final value. The device output is then rated according to the worst (longest settling) case: low to high, or high to low.

DRIFT

GAIN DRIFT - The change in full scale analog output over the specified temperature range expressed in parts per million of full scale per ^{o}C (ppm of FSR/^{o}C). Gain error is measured with respect to +25^{o}C at high (T_H) and low (T_L) temperatures. Gain drift is calculated for both high (T_H -25^{o}C) and low ranges (+25^{o}C – T_L) by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst case drift.

OFFSET DRIFT - The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per ^{o}C (ppm of FSR/^{o}C). Offset error is measured with respect to +25^{o}C at high (T_H) and low (T_L) temperatures. Offset Drift is calculated for both high (T_H -25^{o}C) and low (+25^{o}C – T_L) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst-case drift.

ACCURACY

INTEGRAL NONLINEARITY – The maximum deviation of the actual transfer characteristic from an ideal straight line. The ideal line is positioned according to "end-point linearity" for D/A converter products from Harris Semiconductor, i.e. the line is drawn between the end-points of the actual transfer characteristic (codes 00...0 and 11...1).

DIFFERENTIAL NONLINEARITY – The difference between one LSB and the output voltage change corresponding to any two consecutive codes. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity.

MONOTONICITY – The property of a D/A converter's transfer function which guarantees that the output derivative will not change sign in response to a sequence of increasing (or decreasing) input codes. That is, the only output response to a code change is to remain constant, increase for increasing code, or decrease for decreasing code.

POWER SUPPLY SENSITIVITY

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in -15V, or +15V supplies. It is specified under DC conditions and expressed as parts per million of full scale range per percent of change in power supply (ppm of FSR/%).

COMPLIANCE

Compliance Voltage is the maximum output voltage range that can be tolerated and still maintain its specified accuracy. Compliance Limit implies functional operation only and makes no claims to accuracy.

GLITCH

A glitch on the output of a D/A converter is a transient spike resulting from inequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale or the major carry code transition from 011...1 to 100...0 or vice versa. For example, if turn ON is greater than turn OFF for 011...1 to 100...0, an intermediate state of 000...0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably. (Measured as one half the product of duration and amplitude.)

DECOUPLING AND GROUNDING

For best accuracy and high frequency performance, the grounding and decoupling scheme shown in Figure 1 should be used. Decoupling capacitors should be connected close to the HI-5685 (preferrably to the device pins) and should be tantalum or electrolytic bypassed with ceramic types for best high frequency noise rejection.

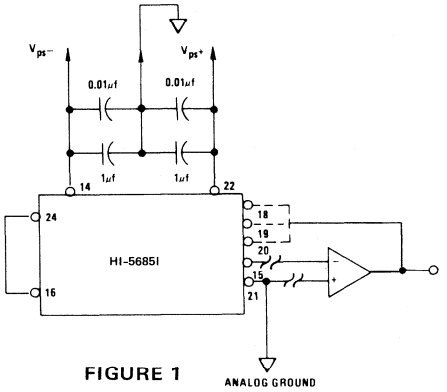


FIGURE 1

REFERENCE SUPPLY

An internal 6.3Volt reference is provided on board all HI-5685 models. This voltage (pin 24) is accurate to ±2% and must be connected to the reference input (pin 16) for specified operation. This reference may be used externally, provided current drain is limited to 2.5mA. An external buffer amplifier is recommended if this reference is to be used to drive other system components. Otherwise, variations in the load driven by the reference will result in gain variations of the HI-5685. All gain adjustments should be made under constant load conditions.

VOLTAGE OUTPUT HI-5685V

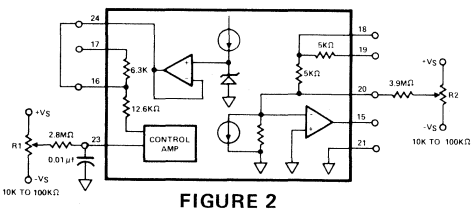


FIGURE 2

RANGE CONNECTIONS

		CONNECT		
	RANGE	PIN 15	PIN 17	PIN 19
Unipolar	0 to +5V	18	N.C.	20
	0 to + 10V	18	N.C.	N.C.
Bipolar	±2.5V	18	20	20
	±5V	18	20	N.C.
	±10V	19	20	15

CURRENT OUTPUT HI-5685I

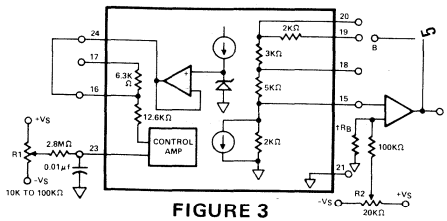


FIGURE 3

†R_B should equal the DAC's output resistance, which is 2KΩ // $R_{FEEDBACK}$.

EXTERNAL AMPLIFIER CONNECTIONS

To use the HI-5685I with an external amplifier, connect as follows:

RANGE	PIN 17 to	PIN 18 to	PIN 19 to	PIN 20 to
0 to +10V	N.C.	B	18*	19*
0 to +5V	N.C.	B	15	N.C.
±10V	15	N.C.	B	N.C.
±5V	15	B	18*	19*
±2.5V	15	B	15	N.C.

*these connections help reduce stray capacitance in the feedback loop.

GAIN AND OFFSET CALIBRATION

(Applies to Figure 2 and 3.)

UNIPOLAR CALIBRATION

Step 1: Offset
- Turn all bits OFF (11...1)
- Adjust R_2 for zero volts out

Step 2: Gain
- Turn all bits ON (00...0)
- Adjust R_1 for FS-1LSB
- That Is:
  - 4.9988 for 0 to +5V range
  - 9.9976 for 0 to +10V range

BIPOLAR CALIBRATION

Step 1: Offset
- Turn all bits OFF (11...1)
- Adjust R_2 for Negative FS
- That Is:
  - −10V for ±10V range
  - −5V for ±5V range
  - −2.5V for ±2.5 range

Step 2: Gain
- Turn all bits ON (00...0)
- Adjust R_1 for positive FS-1LSB
- That Is:
  - +9.9951V for ±10V range
  - +4.9976V for ±5V range
  - +2.4988V for ±2.5V range

This Bipolar procedure adjusts the output range end points. The maximum error at zero (half scale) will not exceed the Linearity error. See the "Accuracy" specifications.

HI-5687

Wide Temperature Range Monolithic 12-Bit Digital-to-Analog Converter

Features

- DAC 87 ALTERNATE SOURCE
- MONOLITHIC CONSTRUCTION
- FAST SETTLING
- GUARANTEED SPECIFICATIONS -55°C to 125°C
- WAFER LASER TRIMMED
- APPLICATIONS RESISTORS ON-CHIP
- ON-BOARD REFERENCE
- DIELECTRIC ISOLATION (DI) PROCESSING
- ±12V POWER SUPPLY OPERATION
- MIL-STD-883 PROCESSING AVAILABLE

Applications

- HIGH SPEED A/D CONVERTERS
- PRECISION INSTRUMENTATION
- CRT DISPLAY GENERATION

Description

The HI-5687 is a monolithic direct replacement for the popular DAC87-CBI wide temperature range d-to-a converter. Single chip construction, along with several design innovations make the HI-5687 the optimum choice for low cost, high reliablility applications.

Harris unique Dielectric Isolation (DI) processing reduces internal parasitics resulting in fast switching times and minimum glitch. ON board span resistors are provided for good tracking over temperature, and are laser trimmed to high accuracy. These may be used with the on-board op-amp (voltage output models; HI-5687V), or with a user supplied external amplifier (HI-5687I).

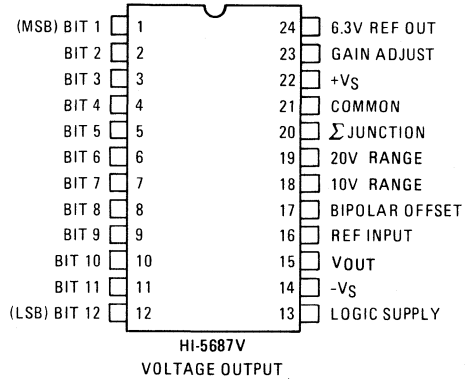
Internally, the HI-5687 eliminates code dependent ground currents by routing current from the positive supply to the internal ground mode, as determined by an auxiliary R-2R ladder. This results in a cancellation of code dependent ground currents allowing virtually zero variation in current through the package common, pin 21.

The HI-5687 is available in both current and voltage output models which are 100% tested over the -55°C to +125°C temperature range. All models include a buried zener reference featuring low temperature coefficient. In addition, the voltage output models include an on-board output amplifier. Both versions operate with a +5V logic supply and a $\pm V_S$ in the range of ± (11.4V to 16.5V).

For additional Hi-Rel screening including a 160 hour burn-in, specify the "-8" suffix. For MIL-STD-883 compliant parts, request the HI-5697V/883 data sheet.

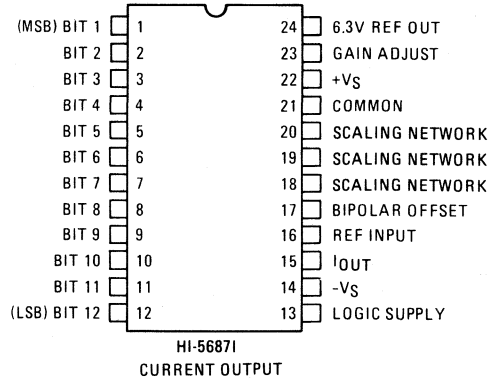
Pinouts

TOP VIEW



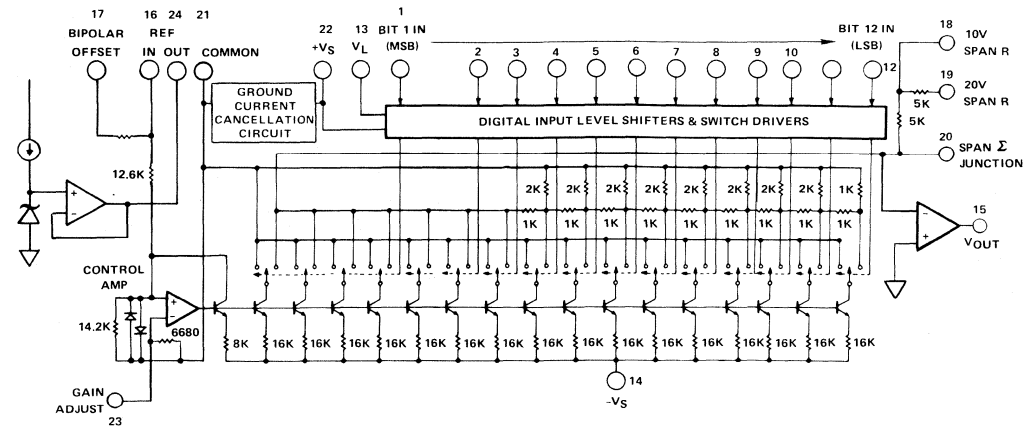
HI-5687V
VOLTAGE OUTPUT

TOP VIEW



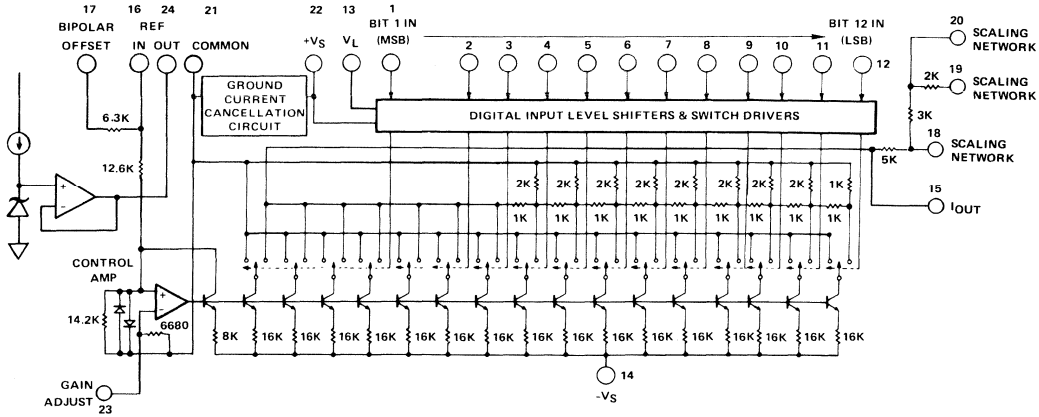
HI-5687I
CURRENT OUTPUT

Functional Diagram Voltage Output



HI-5687 V

Functional Diagram Current Output



HI-5687 I

Absolute Maximum Ratings (1)

Power Supply Inputs	$+V_S$	+20V	Junction Temperature	175°C
	$-V_S$	−20V		
	$+V_{LOGIC}$	+20V	Operating Temperature Range	
Reference	Input (pin 16)	$\pm V_S$	HI-5687I/V-2	−55°C to +125°C
	Output drain	2.5mA	HI-5687I/V-8	−55°C to +125°C
Digital Inputs	Bits 1 to 12	−1V to +12V	Storage Temperature Range	−65°C to +150°C

Electrical Specifications

(T_A = +25°C, V_S = ± 15V, V_{LOGIC} = +5V, Pin 16 connected to Pin 24 unless otherwise specified.)

PARAMETER	CONDITIONS	HI-5687 MIN	HI-5687 TYP	HI-5687 MAX	UNITS
DIGITAL INPUT (3)					
Resolution				12	Bits
Logic Levels	TTL Compatible				
Logic "1"	at +1μA	+2		+5.5	V
Logic "0"	at −100μA	0		+0.8	V
ACCURACY (3)					
Linearity Error	At +25°C		±¼	±½	LSB
	−55°C to +125°C			+¾	LSB
Differential Lin. Error	at +25°C			±¾	LSB
	−55°C to +125°C		±½	±1	LSB (4)
Gain Error (2)			±0.1	±0.2	%FSR
Offset Error (2)			±0.05	±0.1	%FSR
Monotonicity	-55°C to +125°C		GUARANTEED		
DRIFT (3)	−55°C to +125°C				
Total Bipolar Drift (includes gain, offset and linearity drifts)			±15	±30	ppm/°C
Total Error (NOTE 6)					
Unipolar			±0.13	±0.3	%FSR
Bipolar			±0.12	±0.24	%FSR
Gain					
including internal reference			±10	±25	ppm/°C
excluding internal reference			±5	±10	ppm/°C
Unipolar Offset			±1	±3	ppm/°C
Bipolar Offset			±5	±10	ppm/°C
CONVERSION SPEED					
Voltage Models					
Settling Time (3)	to ±0.01% of FSR for FSR Change				
With 10kΩ Feedback			3		μs
With 5kΩ Feedback			1.5		μs
For 1 LSB Change			1.5		μs
Slew Rate			15		V/μs
Current Models					
Settling Time (3)	to ±0.01% of FSR for FSR Change				
10 to 100Ω load			300		ns
1kΩ load			1.0		μs

PARAMETER	CONDITIONS	HI-5687 MIN	HI-5687 TYP	HI-5687 MAX	UNITS
ANALOG OUTPUT					
Voltage Models					
Output Current		+5			mA
Output Impedance (DC)			0.05		Ω
Current Models					
Output Current	Full Scale				
Unipolar		-1.6	–2	-2.4	mA
Bipolar		±0.8	±1	±1.2	mA
Output Resistance					
Unipolar			2.0		kΩ
Bipolar			2.0		kΩ
Compliance Limit (3)		-2.5		+10	V
INTERNAL REFERENCE					
Output Voltage		+6.174	+6.3	+6.426	V
Output Impedance			1.5		Ω
External Current				+2.5	mA
Tempco of Drift (-8, -2)			±5	±10, ±20	ppm/°C
POWER SUPPLY SENSITIVITY (3)					
+15V				±.002	$\frac{\%FSR}{\Delta V_S}$
–15V				±.002	
+5V				±.002	
POWER SUPPLY REQUIREMENTS (5)					
Range					
+15V		+11.4	+15	+16.5	V
–15V		–11.4	–15	–16.5	V
+5V		+4.5	+5	+16.5	V
Current					
+15V			8	11	mA
–15V			-12	-20	mA
+5V			4.5	8	mA

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Adjustable to zero using external potentiometers.
3. See Definitions.
4. FSR is a "full scale range" and is 20V for ±10V range, 10V for ±5V range, etc., or 2mA (±20%) for current output.
5. The HI-5687 will operate with supply voltages as low as ±11.4V. It is recommended that output voltage ranges -10V to +10V and not be used if the supply voltages are less than ±12.5V.
6. With gain and offset errors adjusted to zero at 25°C.

Die Characteristics

Transistor Count		259
Die Size:		210 x 125 mils
Thermal Constants;	θ ja	49°C/W
	θ jc	12°C/W
Tie Substrate to:		Ground
Process:		Bipolar - DI

Definitions of Specifications

DIGITAL INPUTS

The HI-5687 accepts digital input codes in complementary binary, complementary offset binary, and complementary two's complement binary.

DIGITAL INPUT	ANALOG OUTPUT		
	Complementary Binary	Complementary Offset Binary	Complementary Two's Complement *
MSB LSB			
000...000	+ Full Scale	+ Full Scale	-LSB
100...000	Mid Scale -1 LSB	-1 LSB	+ Full Scale
111...111	Zero	- Full Scale	Zero
011...111	+½ Full Scale	Zero	- Full Scale

* Invert MSB with external inverter to obtain CTC Coding

SETTLING TIME

That interval between application of a digital step input, and final entry of the analog output within a specified window about the settled value. Harris Semiconductor usually specifies a unipolar 10V or bipolar full scale step, to be measured from 50% of the input digital transition, and a window of ±½ LSB about the final value. The device output is then rated according to the worst (longest settling) case: low to high, or high to low.

DRIFT

GAIN DRIFT - The change in full scale analog output over the specified temperature range expressed in parts per million of full scale per ^{o}C (ppm of FSR/^{o}C). Gain error is measured with respect to +25^{o}C at high (T_H) and low (T_L) temperatures. Gain drift is calculated for both high (T_H -25^{o}C) and low ranges (+25^{o}C – T_L) by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst case drift.

OFFSET DRIFT - The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per ^{o}C (ppm of FSR/^{o}C). Offset error is measured with respect to +25^{o}C at high (T_H) and low (T_L) temperatures. Offset Drift is calculated for both high (T_H -25^{o}C) and low (+25^{o}C – T_L) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst-case drift.

ACCURACY

INTEGRAL NONLINEARITY – The maximum deviation of the actual transfer characteristic from an ideal straight line. The ideal line is positioned according to "end-point linearity" for D/A converter products from Harris Semiconductor, i.e. the line is drawn between the end-points of the actual transfer characteristic (codes 00...0 and 11...1).

DIFFERENTIAL NONLINEARITY – The difference between one LSB and the output voltage change corresponding to any two consecutive codes. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity.

MONOTONICITY – The property of a D/A converter's transfer function which guarantees that the output derivative will not change sign in response to a sequence of increasing (or decreasing) input codes. That is, the only output response to a code change is to remain constant, increase for increasing code, or decrease for decreasing code.

POWER SUPPLY SENSITIVITY

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in -15V, or +15V supplies. It is specified under DC conditions and expressed as parts per million of full scale range per percent of change in power supply (ppm of FSR/%).

COMPLIANCE

Compliance Voltage is the maximum output voltage range that can be tolerated and still maintain its specified accuracy. Compliance Limit implies functional operation only and makes no claims to accuracy.

GLITCH

A glitch on the output of a D/A converter is a transient spike resulting from inequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale or the major carry code transition from 011...1 to 100...0 or vice versa. For example, if turn ON is greater than turn OFF for 011...1 to 100...0, an intermediate state of 000...0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably. (Measured as one half the product of duration and amplitude.)

DECOUPLING AND GROUNDING

For best accuracy and high frequency performance, the grounding and decoupling scheme shown in Figure 1 should be used. Decoupling capacitors should be connected close to the HI-5687 (preferrably to the device pins) and should be tantalum or electrolytic bypassed with ceramic types for best high frequency noise rejection.

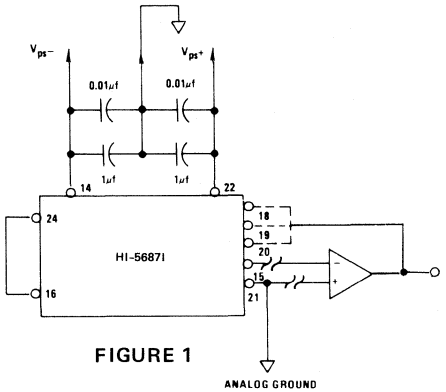


FIGURE 1

REFERENCE SUPPLY

An internal 6.3Volt reference is provided on board all HI-5687 models. This voltage (pin 24) is accurate to ±2% and must be connected to the reference input (pin 16) for specified operation. This reference may be used externally, provided current drain is limited to 2.5mA. An external buffer amplifier is recommended if this reference is to be used to drive other system components. Otherwise, variations in the load driven by the reference will result in gain variations of the HI-5687. All gain adjustments should be made under constant load conditions.

VOLTAGE OUTPUT HI-5687V

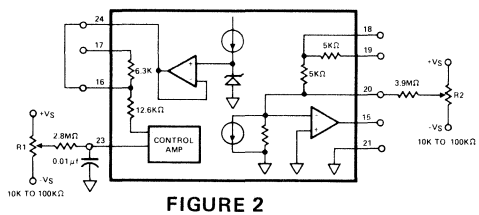


FIGURE 2

RANGE CONNECTIONS

		CONNECT		
	RANGE	PIN 15	PIN 17	PIN 19
Unipolar	0 to +5V	18	N.C.	20
	0 to + 10V	18	N.C.	N.C.
Bipolar	±2.5V	18	20	20
	±5V	18	20	N.C.
	±10V	19	20	15

CURRENT OUTPUT HI-5687I

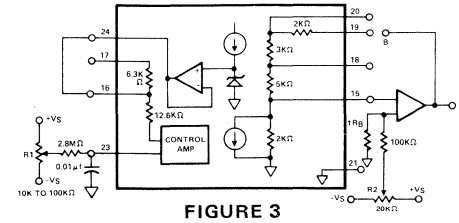


FIGURE 3

†R_B should equal the DAC's output resistance, which is 2KΩ // $R_{FEEDBACK}$.

EXTERNAL AMPLIFIER CONNECTIONS

To use the HI-5687I with an external amplifier, connect as follows:

RANGE	PIN 17 to	PIN 18 to	PIN 19 to	PIN 20 to
0 to +10V	N.C.	B	18*	19*
0 to +5V	N.C.	B	15	N.C.
±10V	15	N.C.	B	N.C.
±5V	15	B	18*	19*
±2.5V	15	B	15	N.C.

*these connections help reduce stray capacitance in the feedback loop.

GAIN AND OFFSET CALIBRATION

(Applies to Figure 2 and 3.)

UNIPOLAR CALIBRATION

Step 1: Offset
- Turn all bits OFF (11...1)
- Adjust R_2 for zero volts out

Step 2: Gain
- Turn all bits ON (00...0)
- Adjust R_1 for FS-1LSB
- That Is:
  - 4.9988 for 0 to +5V range
  - 9.9976 for 0 to +10V range

BIPOLAR CALIBRATION

Step 1: Offset
- Turn all bits OFF (11...1)
- Adjust R_2 for Negative FS
- That Is:
  - −10V for ±10V range
  - −5V for ±5V range
  - −2.5V for ±2.5 range

Step 2: Gain
- Turn all bits ON (00...0)
- Adjust R_1 for positive FS-1LSB
- That Is:
  - +9.9951V for ±10V range
  - +4.9976V for ±5V range
  - +2.4988V for ±2.5V range

This Bipolar procedure adjusts the, output range end points. The maximum error at zero (half scale) will not exceed the Linearity error. See the "Accuracy" specifications.

HARRIS HI-5690V/95V/97V

High Speed, 12-Bit Low Cost Monolithic Digital-to-Analog Converter

Features

- Voltage Output with Fast Settling 750ns
  High Slew Rate 50V/μs
- Industry Standard Pinout - AD-DAC 80 & HI-5680 Compatible
- Two-Supply Operation ..... 11.4V to 16.5V
  -11.4V to -16.5V
- Low Noise Voltage Reference
  1/f (0.1Hz to 10Hz) ..... 15μV_{p-p}
- Guaranteed Monotonic Over Full Temperature Range
- Application Resistors On-Chip
- Complementary Binary Input Code
- Voltage Output
- Complete Family of Temperature Grades

Applications

- High Speed A/D Converters
- Precision Instrumentation
- CRT Display Generation

Description

The HI-5690V series of complete 12 bit digital to analog converters includes a low noise, low temperature coefficient buried zener reference and a fast settling output amplifier. The series consists of the HI-5690V, -5695V and -5697V, for the commercial, industrial and military temperature ranges. Monolithic construction along with several design innovations make these converters an optimum choice for high speed, high reliability applications.

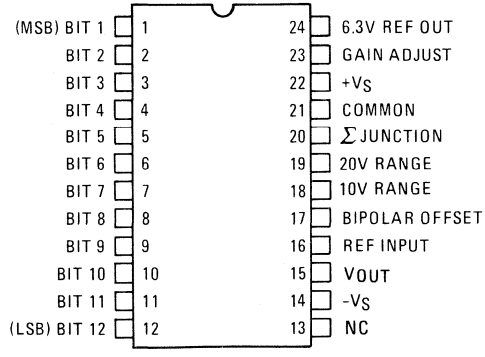
The Harris unique Dielectric Isolation (DI) processing reduces internal parasitics, resulting in fast switching times and minimum glitch. Wafer-level laser trimming of span resistors and bit current cells ensures high accuracy and exceptional tracking over temperature.

Internally, the HI-5690V series eliminates code dependent ground currents by routing current from the positive supply to the internal ground node, as determined by an auxiliary R-2R ladder. This results in a cancellation of code dependent ground currents, allowing virtually zero variation in current through the package common, thus minimizing analog ground noise seen by the converter.

The HI-5690V series operates from two supplies $\pm V_S$ in the range of $\pm$11.4 Volts to $\pm$16.5 volts. It is pin compatible with the AD-DAC 80 series and HI-5680 series, and since Pin 13 is not internally connected (Logic supply on standard 5680's) this device is compatible in applications with or without +5 Volts applied to Pin 13. The converter performance is guaranteed over the full power supply operating range, but not all output ranges are available with low supply voltages. The package is a 24 pin Ceramic Sidebrazed DIP. For Mil-Std-883 compliant parts, request the HI-5697V/883 data sheet.

Pinouts

DIP
TOP VIEW



Absolute Maximum Ratings (Note 1)

Power Supply Inputs +Vs ..... +20V
-Vs ..... -20V
Reference
Input (pin 16) +Vs
Output can be shorted to common or either supply
Analog output can be shorted to common or either supply. (Note 2)
Digital Inputs
Bits 1 to 12 ..... -1V to +12V
Junction Temperature ..... 175°C

Operating Temperature Range

HI-5690V-5 ..... 0°C to +75°C
HI-5695V-4 ..... -25°C to +85°C
HI-5697V-2 ..... -55°C to +125°C
HI-5697V/883 ..... See Separate Data Sheet
Storage Temperature Range ..... -65°C to +150°C

Electrical Specifications

(T_A = +25°C, V_S = ±15V. Pin 16 connected to Pin 24, unless otherwise noted. R_L = 2kΩ)

PARAMETER	HI-5690V, HI-5695V, and HI-5697V				
	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUT (Note 3)					
Resolution				12	Bits
Logic Levels	TTL Compatible				
Logic '1'	+1μA	+2		+5.5	Volts
Logic '0'	-100μA	0		+0.8	Volts
Input Currents					
I_{IH}	+2V			+1	μA
I_{IL}	+0.8V			-100	μA
ACCURACY (Note 3)					
Linearity Error All grades	+25°C		±3/16	±1/2	LSB
HI-5690V, HI-5695V			±1/5	±1/2	LSB
HI-5697V			±1/4	±3/4	LSB
Differential Linearity Error					
HI-5690V, HI-5695V			±1/5	±3/4	LSB
HI-5697V			±1/4	±1	LSB
Monotonicity		Guaranteed			
Gain Error (Note 4)					
HI-5690	+25°C		±0.05	±0.30	%FSR (5)
HI-5695V, HI-5697V	+25°C		±0.05	±0.20	%FSR
Offset Error (Note 4)					
HI-5690V	+25°C		±0.02	±0.15	%FSR
HI-5695V, HI-5697V	+25°C		±0.02	±0.10	%FSR
THERMAL DRIFT (Note 3)					
Total Bipolar Drift (Includes gain, offset & linearity drifts.)					
HI-5690V			±15	±25	ppm/°C
HI-5695V			±10	±20	ppm/°C
HI-5697V			±15	±30	ppm/°C
Gain					
HI-5690V			±10	±30	ppm/°C
HI-5695V, HI-5697V			±8	±20	ppm/°C

PARAMETER	HI-5690V, HI-5695V, and HI-5697V				
	CONDITIONS	MIN	TYP	MAX	UNITS
Unipolar Offset			±1.5	±4	ppm/°C
Bipolar Offset			±5	±15	ppm/°C
Total Error (Note 6)					
Unipolar					
HI-5690V			±0.08	±0.17	%FSR
HI-5695V			±0.10	±0.20	%FSR
HI-5697V			±0.13	±0.30	%FSR
Bipolar					
HI-5690V			±0.06	±0.12	%FSR
HI-5695V			±0.09	±0.12	%FSR
HI-5697V			±0.12	±0.30	%FSR
CONVERSION SPEED (Note 3)					
Settling Time (Note 3)	to ±0.01% of FSR for FSR Change				
With 10kΩ Feedback	FSR = 20V; ±15V Supplies		0.9	1.5	μs
With 5kΩ Feedback	FSR = 10V		0.75	1.2	μs
For 1 LSB change	Major Carry		0.50		μs
Slew Rate			50		V/μs
ANALOG OUTPUT					
Output Current		±5	0.05		mA
Output Resistance	DC				Ω
INTERNAL REFERENCE					
Output Voltage		+6.250	+6.3	+6.350	V
Output Resistance	DC		1.5		Ω
External Current				+2.5	mA
Reference Drift			±5	±20	ppm/°C
Output Noise at +25°C					
Wideband	10Hz to 10kHz		12.5		μVrms
Low Frequency	0.1Hz to 10Hz		15		μVp-p
POWER SUPPLY SENSITIVITY (Note 3)					
+Vs (Pin 22)			0.0008	0.002	%FSR/%Vs
-Vs (Pin 14)			0.001	0.002	%FSR/%Vs
POWER SUPPLY REQUIREMENT (Note 7)					
Range					
+Vs (Pin 22)		+11.4	+15	+16.5	V
-Vs (Pin 14)		-11.4	-15	-16.5	V
Current					
+Vs (Pin 22)	≤ +15V		18.5	22	mA
-Vs (Pin 14)	≥ -15V		-20.5	-26	mA
Pin 13 (No Connection)			0		mA

NOTES:
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. The output is designed to withstand a temporary short to common or either supply for at least one minute.
3. See definitions.
4. Adjustable to zero using external potentiometers.
5. FSR is "Full Scale Range" and is equal to the full scale output voltage minus the zero scale output voltage (i.e. 20V for ±10V range, 10V for ±5V range, etc.)
6. With gain and offset errors adjusted to zero at 25°C.
7. The HI-569XV series will operate with supply voltages as low as ±11.4V. It is recommended that output voltage range -10V to +10V not be used if the supply voltages are less than ±13V.

Digital Inputs

The HI-5690V series accepts digital input codes in complementary binary, complementary offset binary, and complementary two's complement binary.

	ANALOG OUTPUT		
DIGITAL INPUT	COMPLEMENTARY BINARY	COMPLEMENTARY OFFSET BINARY	COMPLEMENTARY TWO's COMPLEMENT*
MSB LSB			
000....000	+Full Scale	+Full Scale	-LSB
100....000	Mid Scale -1 LSB	-1 LSB	+Full Scale
111....111	Zero	-Full Scale	Zero
011....111	+1/2 Full Scale	Zero	-Full Scale

*Invert MSB with external inverter to obtain CTC Coding

Settling Time

That interval between application of a digital step input, and final entry of the analog output within a specified window about the settled value. Harris Semiconductor usually specifies a unipolar 10V full scale step, to be measured from 50% of the input digital transition, and a window of ±1/2 LSB about the final value. The device output is then rated according to the worst (longest settling) case: low to high, or high to low. In a 12 bit system ±1/2 LSB = ±0.012% of FSR.

Thermal Drift

Thermal drift is based on measurements at +25°C, at high (T_H) and low (T_L) temperatures. Drift calculations are made for the high (T_H-25°C) and low (+25°C-T_L) ranges, and the larger of the two values is given as a specification representing worstcase drift.

Gain Drift, Offset Drift, Reference Drift and Total Bipolar Drift are calculated in parts per million per °C as follows:

$$\text{Gain Drift} = \frac{\Delta \text{ FSR}/\Delta^{\circ}\text{C}}{\text{FSR}} \times 10^6$$

$$\text{Offset Drift} = \frac{\Delta \text{ Offset}/\Delta^{\circ}\text{C}}{\text{FSR}} \times 10^6$$

$$\text{Reference Drift} = \frac{\Delta V_{REF}/\Delta^{\circ}\text{C}}{V_{REF}} \times 10^6$$

$$\text{Total Bipolar Drift} = \frac{\Delta V_O/\Delta^{\circ}\text{C}}{\text{FSR}} \times 10^6$$

NOTE: FSR = Full Scale Output Voltage - Zero Scale Output Voltage

Δ FSR = FSR (T_H) - FSR (+25°C) or FSR (+25°C) - FSR (T_L)

V_O = Steady-state response to any input code.

Total Bipolar Drift is the variation of output voltage with temperature, in the bipolar mode of operation. It represents the net effect of drift in Gain, Offset, Linearity and Reference Voltage. Total Bipolar Drift values are calculated, based on measurements as explained above. Gain and Offset need not be calibrated to zero at +25°C. The specified limits for TBD apply for any input code and for any power supply setting within the specified operating range.

Accuracy

LINEARITY ERROR (Short for "Integral Linearity Error". Also, sometimes called "Integral Nonlinearity" and "Nonlinearity".) - The maximum deviation of the actual transfer characteristic from an ideal straight line. The ideal line is positioned according to end-point linearity for D/A converter products from Harris Semiconductor, i.e. the line is drawn between the end-points of the actual transfer characteristic (codes 00...0 and 11...1).

DIFFERENTIAL LINEARITY ERROR - The difference between one LSB and the output voltage change corresponding to any two consecutive codes. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity.

MONOTONICITY - The property of a D/A converter's transfer function which guarantees that the output derivative will not change sign in response to a sequence of increasing (or decreasing) input codes. That is, the only output response to a code change is to remain constant, increase for increasing code, or decrease for decreasing code.

TOTAL ERROR - The net output error resulting from all internal effects (primarily non-ideal Gain, Offset, Linearity and Reference Voltage). Supply voltages may be set to any values within the specified operating range. Gain and offset errors must be calibrated to zero at +25°C. Then the specified limits for Total Error apply for any input code and for any temperature within the specified operating range.

Power Supply Sensitivity

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in -Vs, or +Vs supplies. It is specified under DC conditions and expressed as full scale range percent of change divided by power supply percent change.

$$P.S.S. = \frac{\frac{\Delta \text{ Full Scale Range} \times 100}{\text{Full Scale Range (Nominal)}}}{\frac{\Delta \text{ Vs} \times 100}{\text{Vs (Nominal)}}}$$

Glitch

A glitch on the output of a D/A converter is a transient spike resulting from unequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale, i.e. the major carry code transition from 011...1 to 100...0 or vice versa. For example, if turn ON is greater than OFF for 011...1 to 100...0, an intermediate state of 000...0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably. (Measured as one half the product of duration and amplitude.)

Decoupling and Grounding

For best accuracy and high frequency performance, the grounding and decoupling scheme shown in Figure 1 should be used. Decoupling capacitors should be connected close to the HI-569XV (preferably to the device pins) and should be tantalum or electrolytic bypassed with ceramic types for best high frequency noise rejection.

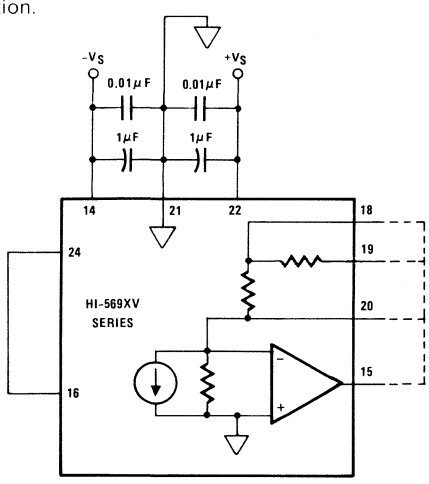


FIGURE 1.

Reference Supply

An internal 6.3 Volt reference is provided on board all HI-569XV models. This voltage (pin 24) is accurate to ±0.8% and must be connected to the reference input (pin 16) for specified operation. This reference may be used externally, provided current drain is limited to 2.5mA. An exteral buffer amplifier is recommended if this reference is to be used to drive other system components. Otherwise, variations in the load driven by the reference will result in gain variations of the HI-569XV. All gain adjustments should be made under constant load conditions.

Output Voltage Ranges

HI-569XV

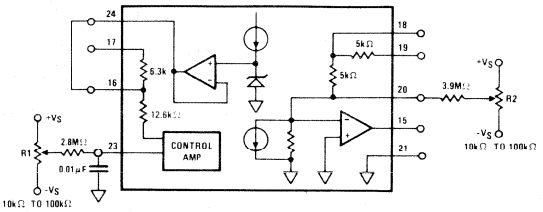


FIGURE 2.

RANGE CONNECTIONS

	RANGE	CONNECT PIN 15	CONNECT PIN 17	CONNECT PIN 19
Unipolar	0 to +5V	18	N.C.	20
	0 to +10V	18	N.C.	N.C.
Bipolar	±2.5V	18	20	20
	±2.5V	18	20	N.C.
	±10V	19	20	15

Gain and Offset Calibration

UNIPOLAR CALIBRATION

Step 1: Offset
- Turn all bits OFF (11...1)
- Adjust R_2 for zero volts out

Step 2: Gain
- Turn all bits ON (00...0)
- Adjust R_1 for FS-1LSB
- That is:
  - 4.9988 for 0 to +5V range
  - 9.9976 for 0 to +10V range

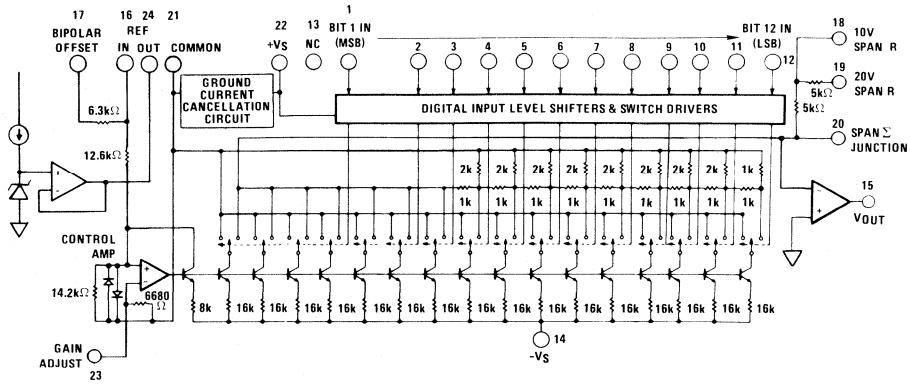
BIPOLAR CALIBRATION

Step 1: Offset
- Turn all bits OFF (11...1)
- Adjust R2 for Negative FS
- That Is:
  - -10V for ±10V range
  - -5V for ±5V range
  - -2.5V for ±2.5 range

Step 2: Gain
- Turn all bits ON (00...0)
- Adjust R1 for positive FS-1LSB
- That is:
  - +9.9951V for ±10V range
  - +4.9976V for ±5V range
  - +2.4988V for ±2.5V range

This Bipolar procedure adjusts the output range end points. The maximum error at zero (half scale) will not exceed the Linearity error. See the "Accuracy" specifications.

Functional Block Diagram



Die & Package Characteristics

Transistor Count	280
Die Size	219 x 123 mils
Thermal Impedance;	
θ_{ja}	49°C/W
θ_{jc}	12°C/W
Tie Substrate to:	Ground
Process	Bipolar-DI

HI-DAC16B/ DAC16C

16-Bit D to A Converter

Features

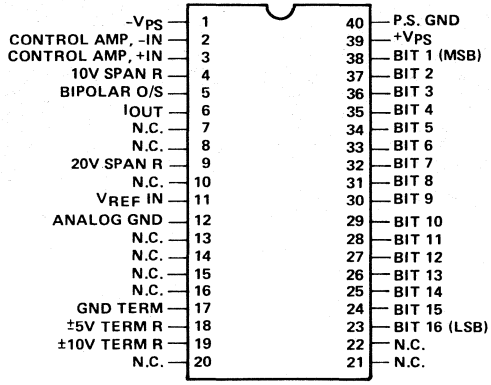
- 16 BIT RESOLUTION
- MONOLITHIC DI BIPOLAR CONSTRUCTION
- FAST SETTLING TIME — 1 μs TO .003%FS
- LOW DIFF. NONLIN. DRIFT — ± 0.3ppm/°C
- LOW GAIN DRIFT — ± 1ppm/°C
- ON-CHIP SPAN & OFFSET RESISTORS
- TTL/5V-CMOS COMPATIBLE
- LOW UNIPOLAR OFFSET — ≤ 1/2LSB@ +25°C
- LOW UNIPOLAR OFFSET T.C. — ± 0.2ppm/°C
- EXCELLENT STABILITY

Applications

- HIGH RESOLUTION CONTROL SYSTEMS
- HIGH FIDELITY AUDIO RECONSTRUCTION
- PRECISION FUNCTION GENERATION AND INSTRUMENTATION

Pinout

TOP VIEW



Description

The HARRIS HI-DAC16 is a 16-bit, current output D/A converter. Single chip construction includes thin-film application resistors for use with an external op amp. These permit standard output voltage ranges of 0 to +5V, 0 to +10V, ±2.5V, ±5V and ±10V. The HI-DAC16B is monotonic to 15 bits; and the HI-DAC16C to 14 bits.

Reference and span resistors have adjacent placement on the chip for optimum match and thermal tracking. Futhermore, this layout feature helps minimize the superposition error caused by self-heating of the span resistor, reducing it to less than 1/10LSB. This and other design innovations have produced exceptionally stable operation over temperature. Typical temperature coefficients are ± 1ppm/°C for gain error and 0.3ppm/°C for differential non-linearity error.

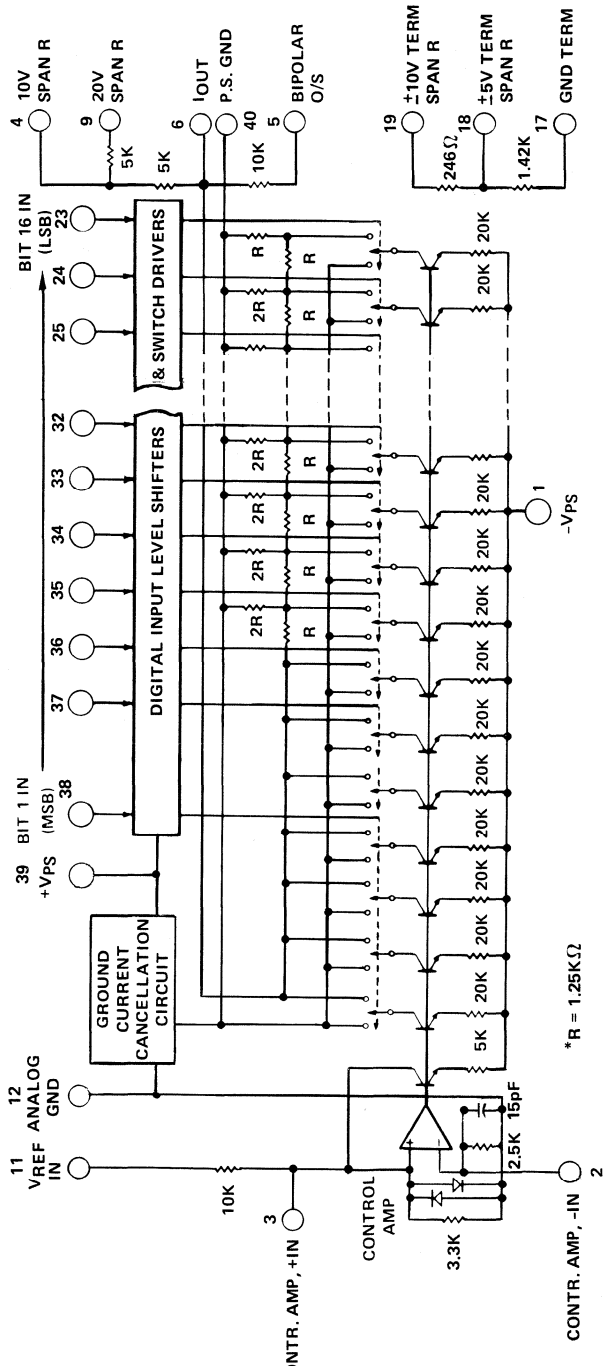
The internal architecture is an extension of the earlier HI-562 with several major improvements. All code dependent ground currents are steered to a separate non-critical path, namely, power supply ground. This feature allows the precision ground of the converter to be sensed with virtually zero voltage drop referred to system ground. The result is the complete elimination of non-linearities due to code dependent ground currents while yielding an extremely low unipolar offset of less than 1/2LSB. Because of this separation, the user may route the precision ground some distance to the system ground without degrading converter accuracy.

The HARRIS HI-DAC16 delivers a stable, accurate output without sacrifice in speed. Settling time to within ±0.003% is one microsecond. Overall performance of this monolithic device should be attractive for applications such as high fidelity audio and high-resolution control systems.

Two accuracy grades are offered, and typical power dissipation is 465mW. Package is a 40 pin ceramic DIP. For further information, see Application Note 539.

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Functional Diagram



Absolute Maximum Ratings (Referred to Ground)

Power Supply Inputs	$V_{ps}+$	+20V	Junction Temperature	175°C
	$V_{ps}-$	−20V	Operating Temperature Range	
Reference Inputs	V_{REF} (Hi)	$\pm V_{ps}$		
Digital Inputs	Bits 1 to 16	−1V, +12V	HI-DAC 16B/C	0°C to +75°C
Outputs		$\pm V_{ps}$	Storage Temperature Range	−65°C to +150°C

Electrical Specifications (T_A = +25°C, V_{ps} = ±15V, V_{ref} = +10V, unless otherwise specified)

PARAMETER	CONDITIONS	HI-DAC16B MIN	HI-DAC16B TYP	HI-DAC16B MAX	HI-DAC16C MIN	HI-DAC16C TYP	HI-DAC16C MAX	UNITS
INPUT CHARACTERISTICS								
Digital Inputs	Bit ON "Logic 1" Bit OFF "Logic 0"							
Input Voltage								
Logic "1"	Full Temperature Range	2.0			2.0			V
Logic "0"				0.8			0.8	V
Input Current								
Logic "1"			20	500		20	500	nA
Logic "0"		-50			-50			μA
Reference Input								
Input Resistance			10			10		kΩ
Input Voltage			10			10		V
TRANSFER CHARACTERISTICS								
Resolution	Full Temperature Range		16			16		Bits
Nonlinearity	25°C		±0.0023			±0.0045		%FSR(3)
	Full Temperature Range			±0.0045			±0.009	
Differential Nonlinearity	25°C		±0.0015			±0.003		%FSR
	Full Temperature Range			±0.003			±0.006	
Relative Accuracy (5)	With 100Ω(1%) Trim Resistors							
Unipolar Gain Error	All Bits ON		±0.1	±0.25		±0.1	±0.25	
Bipolar Offset Error	All Bits OFF		±0.15	±0.43		±0.15	±0.43	%FSR
Unipolar Offset Error			±0.002	±0.05		±0.002	±0.05	
Adjustment Range	See Operating Instructions							
Gain	Using Trim Potentiometers			±3			±3	%FSR
Bipolar Offset	as shown in Figure 1			±0.43			±0.43	
Temperature Stability	Drift specified with internal span resistors for voltage output							
Gain Drift (2)	Full Temperature Range		±1	±5		±1	±5	ppm of FSR/°C
Offset Drift (2)								
Unipolar Offset	All Bits OFF		±0.2			±0.2		
Bipolar Offset			±0.5			±0.5		
Differential Nonlinearity	Full Temperature Range		±0.3			±0.3		
Settling Time (2) to ±0.003%FS	All Bits ON-to-OFF or OFF-to-ON		1.0			1.0		μs

PARAMETER	CONDITIONS	HI-DAC16B			HI-DAC16C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Glitch (2)	From 0111 . . .1 to 100 . . . 0 or 100 . . . 0 to 011 . . . 1		1300			1300		mV–ns
Power Supply (2) Rejection Ratio, PSRR (3)								
$V_{ps}+$			1.5			1.5		ppm of FSR/% V_{ps}
$V_{ps}-$			1.5			1.5		
OUTPUT CHARACTERISTICS								
Output Current								
Unipolar		-1.6	-2	-2.4	-1.6	-2	-2.4	mA
Bipolar		±0.8	±1	±1.2	±0.8	±1	±1.2	
Resistance			2.5k			2.5k		
Capacitance			10			10		pF
Output Voltage Ranges	Using external op amp and internal scaling resistors. See Figure 1 and Table 1 for connections							
Unipolar			0 to +5			0 to +5		V
			0 to +10			0 to +10		
Bipolar			±2.5			±2.5		
			±5			±5		
			±10			±10		
Compliance Limit (2)		-3		+10	-3		+10	V
Compliance Voltage (2)	Full Temperature Range		±1			±1		V
Output Noise	0.1 to 5MHz (All bits ON)		30			30		μVRMS
POWER REQUIREMENTS								
$V_{ps}+$ (7)	Full Temperature Range	13.5	+15	16.5	13.5	+15	16.5	V
$V_{ps}-$		-13.5	-15	-16.5	-13.5	-15	-16.5	
$I_{ps}+$ (4)	All Bits ON or OFF		+13	+18		+13	+18	mA
$I_{ps}-$ (4)	Full Temperature Range	-25	-18		-25	-18		
Power Dissipation			465			465		mW

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impared. Functional operation under any of these conditions is not necessarily implied.
2. See Definitions.
3. FSR is "full scale range" and is 20V for ±10V range, 10V for ±5V range, etc., or 2mA (±20%) for current output.
4. After 30 seconds warm-up.
5. Using an external op amp with internal span resistors and specified external trim resistors in place of potentiometers R_1 and R_2. Errors are adjustable to zero using R_1 and R_2 potentiometers. (See Operating Instructions Figure 2.)

Definition of Specifications

DIGITAL INPUTS

The HI-DAC 16B/C accepts digital input codes in binary format and may be user connected for any one of three binary codes. Straight Binary, Two's Complement, or Offset Binary. (See Operation Instructions).

DIGITAL INPUT	ANALOG OUTPUT		
	Straight Binary	Offset Binary	Two's Complement *
MSB LSB			
000...000	Zero	-FS 9(Full Scale)	Zero
100...000	½FS	Zero	−FS
111...111	+FS − 1 LSB	+FS − 1 LSB	Zero − 1 LSB
011...111	½FS − 1 LSB	Zero − 1 LSB	+FS − 1 LSB
*Invert MSB with external inverter to obtain Two's Complement Coding			

ACCURACY

INTEGRAL NONLINEARITY – The maximum deviation of the actual transfer characteristic from an ideal straight line. The ideal line is positioned according to "end-point linearity" for D/A converter products from Harris Semiconductor, i.e. the line is drawn between the end-points of the actual transfer characteristic (codes 00...0 and 11...1).

DIFFERENTIAL NONLINEARITY – The difference between one LSB and the output voltage change corresponding to any two consecutive codes. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity.

MONOTONICITY – The property of a D/A converter's transfer function which guarantees that the output derivative will not change sign in response to a sequence of increasing (or decreasing) input codes. That is, the only output response to a code change is to remain constant, increase for increasing code, or decrease for decreasing code.

SETTLING TIME

Settling time is the time required for the output to settle to within the specified error band for any input code transition. It is usually specified for a full scale or major carry transition.

DRIFT

GAIN DRIFT – The change in full scale analog output over the specified temperature range expressed in parts per million of full scale per °C (ppm of FSR/°C). Gain error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Gain drift is calculated for both high (T_H −25°C) and low ranges (+25°C−T_L) by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst case drift.

OFFSET DRIFT – The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Offset error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Offset Drift is calculated for both high (T_H −25°C) and low (+25°C −T_L) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst-case drift.

POWER SUPPLY SENSITIVITY

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in −15V, or +15V supplies. It is specified under DC conditions and expressed as parts per million of full scale range per percent of change in power supply (ppm of FSR/%).

COMPLIANCE

Compliance Voltage is the maximum output voltage range that can be tolerated and still maintain its specified accuracy. Compliance Limit implies functional operation only and makes no claims to accuracy.

GLITCH

A glitch on the output of a D/A converter is a transient spike resulting from unequal internal ON–OFF switching times. Worst case glitches usually occur at half-scale or the major carry code transition from 011...1 to 100...0 or vice versa. For example, if turn ON is greater than turn OFF for 011...1 to 100...0, an intermediate state of 000...0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably. (Calculated as the product of duration and amplitude.)

Operating Instructions

UNIPOLAR AND BIPOLAR VOLTAGE OUTPUT CONNECTIONS

FIGURE 1

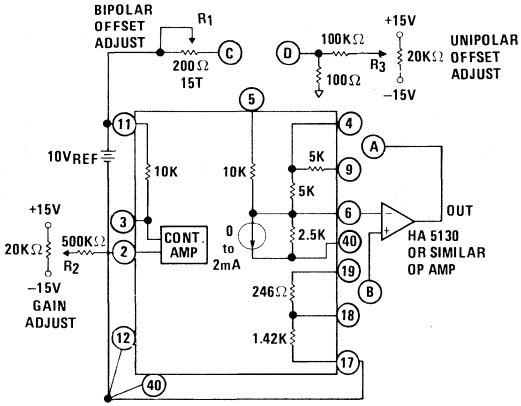


TABLE 1

	OUTPUT RANGE	CONNECTIONS PIN5 to	PIN4 to	PIN9 to	PIN B to
UNIPOLAR MODE	0 to +10V	D	A	N.C.	19
	0 to +5V	D	A	PIN6	*
BIPOLAR MODE	±10V	C	N.C.	A	19
	±5V	C	A	N.C.	18
	±2.5V	C	A	6	*

*Connect an external 1.1K ohm resistor to ground.

GAIN AND ZERO CALIBRATION

The HI-DAC16B/C input reference resistor, bipolar offset resistor and span resistors are optimized for excellent tracking over temperature. LASER trimming of the reference circuit resistors corrects the unipolar Gain and Offset errors to high accuracy. The remaining error can be adjusted with trimming potentiometers. The bipolar Gain and Offset errors are greater since the LASER correction is done in the unipolar mode, however these too are easily adjusted. Figure 1 illustrates the connections for unipolar and bipolar operation. Trimming potentiometers R_1, R_2, and R_3 are required for adjustment.

UNIPOLAR CALIBRATION

Step 1: Offset
- Turn all bits OFF (00..0)
- Adjust R_3 for zero volts output

Step 2: Gain
- Turn all bits ON (11..1)
- Adjust R_2 for an output of FS-1LSB
  That is, adjust for:

  9.999847 for +10V range
  4.999924 for +5V range

BIPOLAR CALIBRATION

Step 1: Offset
Turn all bits OFF (00..0)
Adjust R_1 for an output of
−10V for ± 10V range
−5V for ± 5V range
−2.5V for ± 2.5V range

Step 2: Gain
Turn all bits ON (11..1)
Adjust R_2 for FS-1LSB output
That is, adjust for:

9.999695 for ±10V range
4.999847 for ± 5V range
2.499924 for ± 2.5V range

Other Considerations

GROUNDS

The HI-DAC16 has two ground terminals, pin 12 (REF GND) and pin 40 (PWR GND). These should not be tied together near the package unless that point is also the system signal ground to which all returns are connected. (If such a point exists, then separate paths are required to pins 12 and 40).

The current through pin 12 is near-zero DC*, but pin 40 carries up to 1.75mA of code - dependent current from bits 1, 2, and 3. The general rule is to connect pin 12 directly to the system signal, or analog ground. Connect pin 40 to the local digital or power ground. Then, of course, a single path must connect the analog/signal and digital/power grounds.

Other Considerations (Continued)

*Current cancellation is a two-step process in which code-dependent variations are eliminated, then the resulting DC current is supplied internally. First, an auxiliary 13-bit R-2R Ladder is driven by the complement of the DAC's input code. Together the main and auxiliary ladders draw a continuous 3.25mA from the internal ground node, regardless of input code. Part of this DC current is supplied by the zener voltage reference, and the remainder is sourced from the positive supply via a current mirror which is laser trimmed for zero current through the external terminal (pin 12).

LAYOUT

Connections to pin 6 (I_{OUT}) on the HI–DAC16 are most critical for high speed performance. Output capacitance of the DAC is only 10pF, so a small additional capacitance will alter the op amp's stability and affect settling time. Connections to pin 6 should be short and few. Component leads should be short on the side connecting to pin 6.

BYPASS CAPACITORS

Power supply bypass capacitors on the op amp will serve the HI–DAC16 also. If no op amp is used, a 0.01μF ceramic capacitor from each supply terminal to pin 40 is sufficient, since supply current variations are small.

THERMAL EFFECTS

A consideration when using the DAC16 is Temperature Stability. In applications where full scale shift could be a problem, the use of a heat sink and/or a cooling fan is suggested. This will decrease the magnitude of the total variation by lowering the effective thermal resistance between the package and its environment. The device should be kept in a stable isothermal environment, and a warm-up time consistent with accuracy requirements should be provided.

SELECTING AN OPERATIONAL AMPLIFIER

The HI-DAC16 is a high resolution, high accuracy DAC. Many applications will require an op-amp used as a current-to-voltage converter at the DAC output. (Careful consideration should be given the choice of this amplifier as a poor selection can seriously degrade the inherent qualities of the DAC.)

The HA-5130 is an excellent choice to maintain high accuracy with an average Offset Drift of only 0.4 μV/°C leading to an error over temperature of 30 μV (0.0003% FSR for a 10V FS). Initial offset and bias current are 10 μV and 3nA respectively, while input noise current of 0.2pA/$\sqrt{Hz}$. Settling time is adequate for most audio applications. (11 μs typ. to 0.1%).

COMPOSITE AMPLIFIER

It is desirable at times to have an output amplifier which combines the qualities of those op-amps available to the designer. For instance one may wish to combine the excellent front-end characteristics of the HA-5130 with the speed of a device such as the HA-2540 (t_{settle} =250ns to 0.1%). In these instances there is the option of the composite amplifier. The basic configuration is shown in Figure 2.

COMPOSITE AMPLIFIER

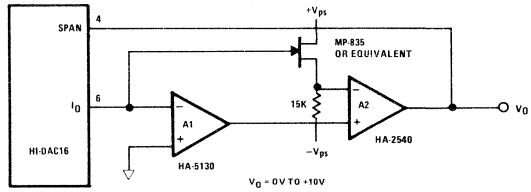


FIGURE 2

The composite amplifier may be used to achieve a compromise depending on the requirements of a design. Trade-offs in performance can be made and the following equations apply:

Offset; $$V_{OFF} = \frac{V_{OFF2}}{A_{01}} + V_{OFF1}$$

Bias; $$I_{BIAS} = I_{BIAS2} + I_{BIAS1}$$

Gain; $$\frac{V_0}{V_1} = A_V(S) = A_{V2}(S)\,[1 + A_{V1}(S)]$$

The amplifier A_2 should be of wide bandwidth and fast settling time.

Die Characteristics

Transistor Count		190
Die Size:		215 x 125 mils
Thermal Constants;	θ_{ja}	41°C/W
	θ_{jc}	11°C/W
Tie Substrate to:		Analog Ground
Process:		Bipolar - DI

ANALOG

Sample and Hold Amplifiers

7

ABSOLUTE MAXIMUM RATINGS

As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Specifications" are the only conditions recommended for satisfactory operation.

Ordering Information

HARRIS PRODUCT CODE EXAMPLE

H A 1 — 2420 — 2

PREFIX:
H (HARRIS)

FAMILY:
A : Analog
C : Communications
D : Digital
F : Filters
I : Interface
M : Memory
V : Analog High Voltage
Y : Analog Hybrids

PACKAGE:
1 : Dual-In-Line Ceramic
3 : Dual-In-Line Plastic
4 : Leadless Chip Carriers (LCC)
4P : Plastic Leaded Chip Carriers (PLCC)
5 : LCC Hybrid
7 : Mini-DIP, Ceramic
0 : Chip Form

PART NUMBER

TEMPERATURE:
1 : 0°C to +200°C *
2 : -55°C to +125°C
4 : -25°C to +85°C
5 : 0°C to +75°C
6 : 100% +25°C Probe (Dice Only)
7 : Dash-7 High Reliability Commercial Product 0°C to +75°C
8 : Dash-8 Program
9 : -40°C to +85°C

* Special High Temperature Testing Available on Certain Product Types. Consult Factory for Availability.

Standard Products Packaging Availability†

PACKAGE	PLASTIC DIP	CERAMIC DIP					SURFACE MOUNT LCC	SURFACE MOUNT PLCC
TEMPERATURE	-5	-2	-4	-5	-7	-8	-8	-5
DEVICE NUMBER								
SAMPLE AND HOLD								
HA-2420		B1				*	*	
HI-2425	N			B1	B1			AA
HI-5320		B1		B1	B1	B1	T	
HI-5330		B1	B1	B1		*	*	

* Available as MIL-STD-883 Only.
† Letter codes in this chart indicate available packages as shown in Packaging Section 11.

Selection Guide

SAMPLE AND HOLD

PART NUMBER	FEATURES	TEMPERATURE RANGE -55°C TO +125°C	TEMPERATURE RANGE 0°C TO +75°C	TEMPERATURE RANGE -25°C TO +85°C	PACKAGE	ACQUISITION TIME (TO 0.01%) TYP., +25°C	CHARGE TRANSFER TYP., +25°C	APERTURE TIME TYP., +25°C	GAIN BANDWIDTH PRODUCT TYP., +25°C	PAGE
HA-2420 HA-2425	Low Charge Transfer Low Droop Rate	X	X		14 Pin Cerdip, Epoxy DIP, PLCC	3.2µs	10pC	30ns	2.5MHz	7-3
HA-5320	High Speed Precision Complete-Includes Hold Capacitor	X	X		14 Pin Cerdip, LCC	1µs	0.1pC	25ns	2.0MHz	7-10
HA-5330	High Speed Precision Complete-Includes Hold Capacitor	X	X	X	14 Pin Cerdip	0.5µs	0.05pC	20ns	4.5MHz	7-17

HA-2420/25

Fast Sample and Hold

Features

- Maximum Acquisition Time (10V Step to 0.1%) ... 4μs
  (10V Step to 0.01%) 6μs
- Low Droop Rate (C_H = 1000pF) ..... 5μV/ms (Typ.)
- Gain Bandwidth Product ..... 2.5MHz (Typ.)
- Low Effective Aperture Delay Time ..... 30ns (Typ.)
- TTL Compatible Control Input
- ±12V to ±15V Operation

Applications

- 12-Bit Data Acquisition
- Digital to Analog Deglitcher
- Auto Zero Systems
- Peak Detector
- Gated Operational Amplifier

Description

The HA-2420/2425 is a monolithic circuit consisting of a high performance operational amplifier with its output in series with an ultra-low leakage analog switch and MOSFET input unity gain amplifier.

With an external holding capacitor connected to the switch output, a versatile, high performance sample-and-hold or track-and-hold circuit is formed. When the switch is closed, the device behaves as an operational amplifier, and any of the standard op amp feedback networks may be connected around the device to control gain, frequency response, etc. When the switch is opened the output will remain at its last level.

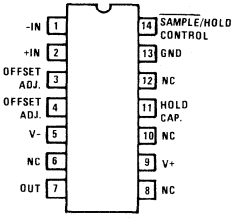
Performance as a sample-and-hold compares very favorably with other monolithic, hybrid, modular, and discrete circuits. Accuracy to better than 0.01% is achievable over the temperature range. Fast acquisition is coupled with superior droop characteristics, even at high temperatures. High slew rate, wide bandwidth, and low acquisition time produce excellent dynamic characteristics. The ability to operate at gains greater than 1 frequently eliminates the need for external scaling amplifiers.

The device may also be used as a versatile operational amplifier with a gated output for applications such as analog switches, peak holding circuits, etc. For more information, please see Application Note 517.

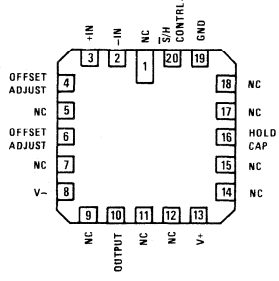
The HA-2420/25 is offered in a 14 pin Ceramic or Plastic DIP and a 20 pad Ceramic LCC or 20 pad PLCC. The MIL-STD-883 data sheet for this device is available on request.

Pinouts

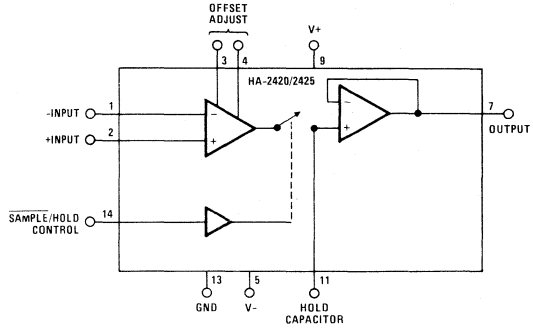
14 PIN CERAMIC/PLASTIC DIP
TOP VIEW



20 PAD LCC/PLCC
TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 40V
Differential Input Voltage..... ±24V
Digital Input Voltage (Sample and Hold Pin) ..... +8V, -15V
Output Current ..... Short Circuit Protected
Junction Temperature ..... +175°C

Operating Temperature Range

HA-2420-2 ..... $-55°C \leq T_A \leq +125°C$
HA-2425-5/-7 ..... $0°C \leq T_A \leq +75°C$
Storage Temperature Range ..... $-65°C \leq T_A \leq +150°C$

Electrical Specifications

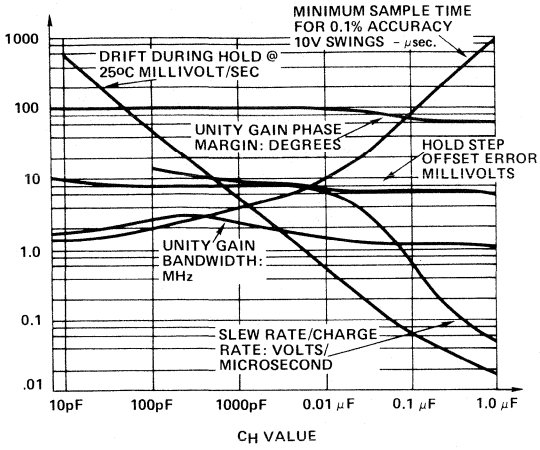
Test Conditions (Unless Otherwise Specified) $V_{SUPPLY} = \pm 15.0V$; $C_H = 1000pF$; Digital Input: $V_{IL} = +0.8V$ (Sample), $V_{IH} = +2.0V$ (Hold), Unity Gain Configuration (Output tied to -Input)

PARAMETER	TEMP	HA-2420-2			HA-2425-5/-7			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Input Voltage Range	Full	±10	-	-	±10	-	-	V
Offset Voltage	+25°C	-	2	4	-	3	6	mV
	Full	-	3	6	-	4	8	mV
Bias Current	+25°C	-	40	200	-	40	200	nA
	Full	-	-	400	-	-	400	nA
Offset Current	+25°C	-	10	50	-	10	50	nA
	Full	-	-	100	-	-	100	nA
Input Resistance	+25°C	5	10	-	5	10	-	MΩ
Common Mode Range	Full	±10	-	-	±10	-	-	V
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Notes 1, 4)	Full	25K	50K	-	25K	50K	-	V/V
Common Mode Rejection (Note 2)	Full	-80	-90	-	-74	-90	-	dB
Hold Mode Feedthrough Attenuation (Note 3)	Full	-	-76	-	-	-76	-	dB
Gain Bandwidth Product (Note 3)	+25°C	-	2.5	-	-	2.5	-	MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 1)	Full	±10	-	-	±10	-	-	V
Output Current	+25°C	±15	-	-	±15	-	-	mA
Full Power Bandwidth (Notes 3, 4)	+25°C	-	100	-	-	100	-	kHz
Output Resistance (D.C.)	+25°C	-	0.15	-	-	0.15	-	Ω
TRANSIENT RESPONSE								
Rise Time (Notes 3, 5)	+25°C	-	75	100	-	75	100	ns
Overshoot (Notes 3, 5)	+25°C	-	25	40	-	25	40	%
Slew Rate (Notes 3, 6)	+25°C	3.5	5	-	3.5	5	-	V/μs
DIGITAL INPUT CHARACTERISTICS								
Digital Input Current ($V_{IN} = 0V$)	Full	-	-	-0.8	-	-	-0.8	mA
Digital Input Current ($V_{IN} = +5.0V$)	Full	-	-	20	-	-	20	μA
Digital Input Voltage (Low)	Full	-	-	0.8	-	-	0.8	V
Digital Input Voltage (High)	Full	2.0	-	-	2.0	-	-	V
SAMPLE AND HOLD CHARACTERISTICS								
Acquisition Time to 0.1% 10V Step (Note 3)	+25°C	-	2.3	4	-	2.3	4	μs
Acquisition Time to 0.01% 10V Step (Note 3)	+25°C	-	3.2	6	-	3.2	6	μs
Aperture Time (Note 9)	+25°C	-	30	-	-	30	-	ns
Effective Aperture Delay Time	+25°C	-	30	-	-	30	-	ns
Aperture Uncertainty	+25°C	-	5	-	-	5	-	ns
Drift Current (Notes 3, 7)	+25°C	-	5	-	-	5	-	pA
HA1-2420, HA4-2420	Full	-	1.8	10	-	-	-	nA
HA1-2425	Full	-	-	-	-	0.1	1.0	nA
HA3-2425, HA4P2425	Full	-	-	-	-	7.5	10.0	nA
Hold Step Error (Note 7)	+25°C	-	10	20	-	10	20	mV
POWER SUPPLY CHARACTERISTICS								
Supply Current (+)	+25°C	-	3.5	5.5	-	3.5	5.5	mA
Supply Current (-)	+25°C	-	2.5	3.5	-	2.5	3.5	mA
Power Supply Rejection	Full	-80	-90	-	-74	-90	-	dB

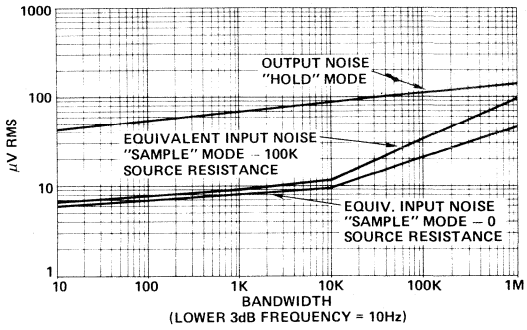
NOTES:
1. $R_L = 2k\Omega$.
2. $V_{CM} = \pm 10VDC$.
3. $A_V = \pm 1$, $R_L = 2k\Omega$, $C_L = 50pF$.
4. $V_{OUT} = 20V$ peak-to-peak.
5. $V_{OUT} = 200mV$ peak-to-peak.
6. $V_{OUT} = 10.0V$ peak-to-peak.
7. $V_{IN} = 0V$.
8. $f_{IN} \leq 100kHz$.
9. Derived from computer simulation only; not tested.

Performance Curves V_{SUPPLY} = ±15VDC, T_A = +25°C, C_H = 1000pF Unless Otherwise Specified

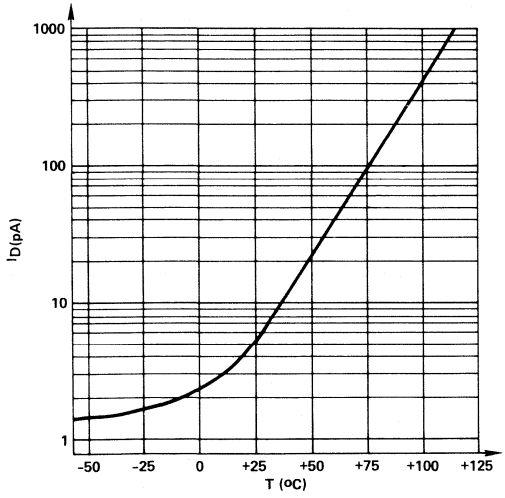
TYPICAL SAMPLE AND HOLD PERFORMANCE AS A FUNCTION OF HOLDING CAPACITOR



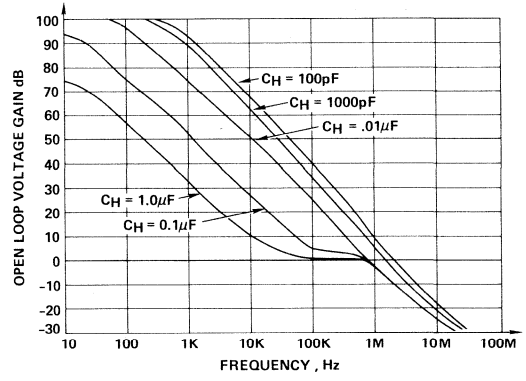
BROADBAND NOISE CHARACTERISTICS



DRIFT CURRENT vs. TEMPERATURE

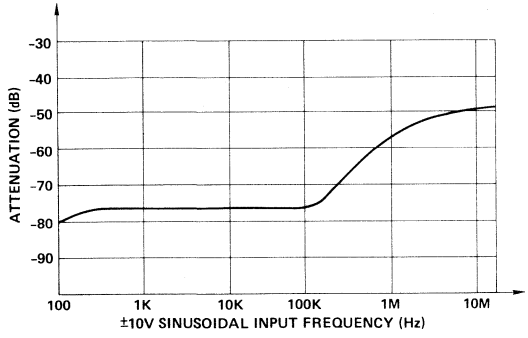


OPEN LOOP FREQUENCY RESPONSE

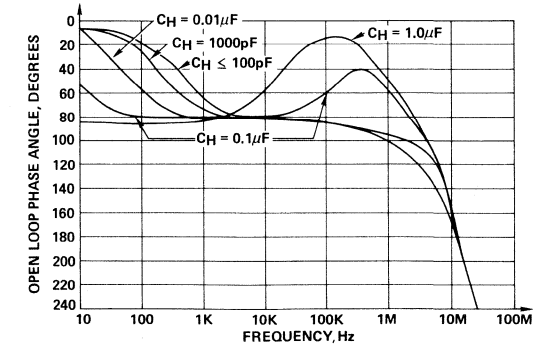


HOLD MODE FEED THROUGH ATTENUATION

C_H = 1000pF



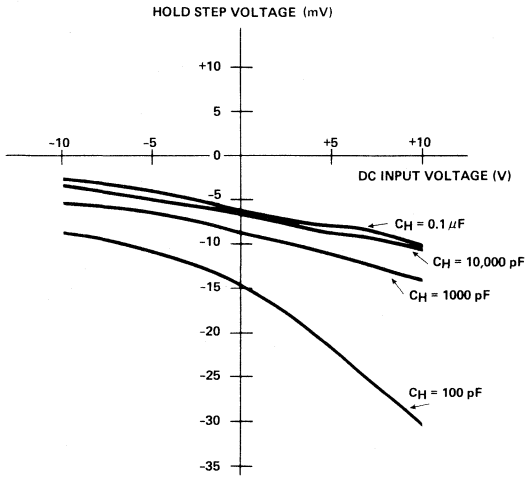
OPEN LOOP PHASE RESPONSE



7 SAMPLE & HOLD AMPLIFIERS

Offset and Gain Adjustment

HOLD STEP vs. INPUT VOLTAGE



OFFSET ADJUSTMENT

The offset voltage of the HA-2420/2425 may be adjusted using a 100kΩ trim pot, as shown in Figure 6. The recommended adjustment procedure is:

1. Apply zero volts to the sample-and-hold input, and a square wave to the $\overline{S}$/H control.
2. Adjust the trim pot for zero volts output in the hold mode.

GAIN ADJUSTMENT

The linear variation in pedestal voltage with sample-and-hold input voltage causes a -0.06% gain error (C_H = 1000pF). In some applications (D/A deglitcher, A/D converter) the gain error can be adjusted elsewhere in the system, while in other applications it must be adjusted at the sample-and-hold. The two circuits shown below demonstrate how to adjust gain error at the sample-and-hold.

The recommended procedure for adjusting gain error is:

1. Perform offset adjustment.
2. Apply the nominal input voltage that should produce a +10V output.
3. Adjust the trim pot for +10V output in the hold mode.
4. Apply the nominal input voltage that should produce a -10V output.
5. Measure the output hold voltage ($V_{-10\ NOMINAL}$). Adjust the trim pot for an output hold voltage of

$$\frac{(V_{-10\ NOMINAL}) + (-10V)}{2}$$

INVERTING CONFIGURATION

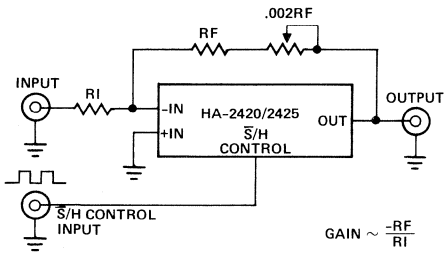


FIGURE 2.

NONINVERTING CONFIGURATION

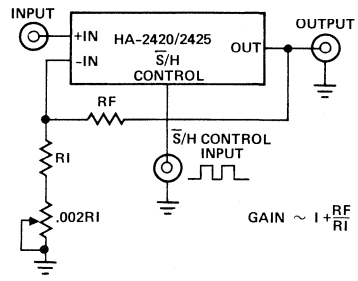


FIGURE 3.

Test Circuits

HOLD STEP ERROR AND DRIFT CURRENT

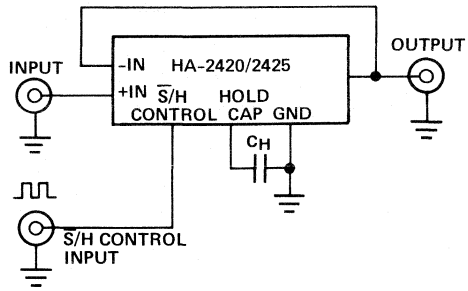
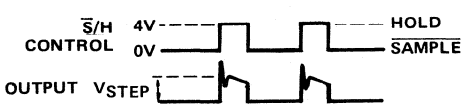


FIGURE 4.

HOLD STEP ERROR TEST

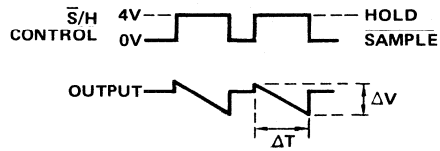
1. With a D.C. input voltage, observe the following waveforms:



2. Set rise/fall times of S/H Control to approximately 20ns.

DRIFT CURRENT TEST

1. With a D.C. input voltage, observe the following waveforms:



2. Measure the slope of the output during hold, $\Delta V/\Delta t$, and compute drift current from: $I_D = C_H \Delta V/\Delta t$.

HOLD MODE FEEDTHROUGH ATTENUATION

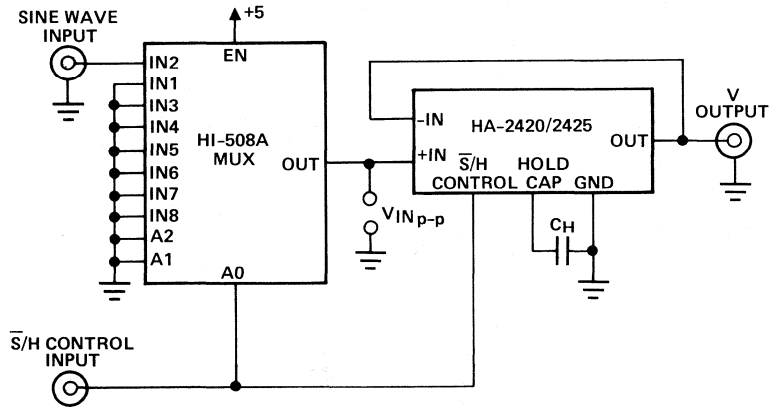


FIGURE 5.

NOTE: Compute hold mode feedthrough attenuation from the formula:

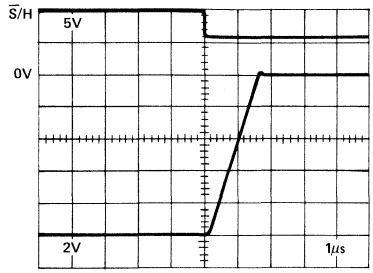
$$\text{Feedthrough Attenuation} = 20 \text{ Log } \frac{V_{OUT\ HOLD}}{V_{IN\ HOLD}}$$

Where $V_{OUT\ HOLD}$ = Peak-to-Peak value of output sinewave during the hold mode.

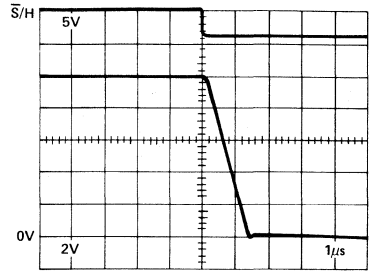
7 SAMPLE & HOLD AMPLIFIERS

Acquisition Times (C_H = 1000pF)

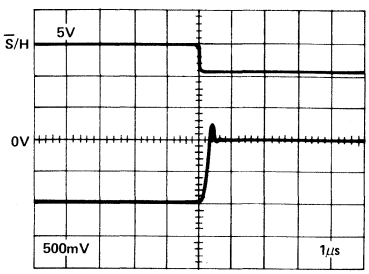
-10 TO 0V



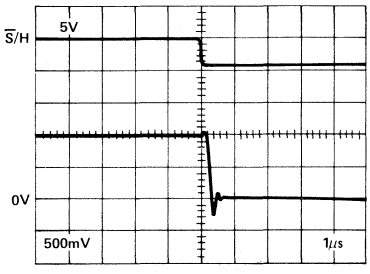
+10V TO 0V



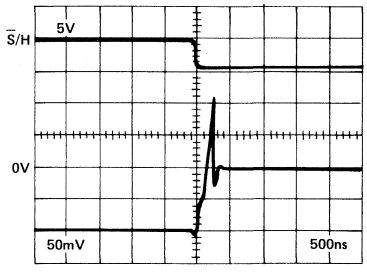
-1V TO 0V



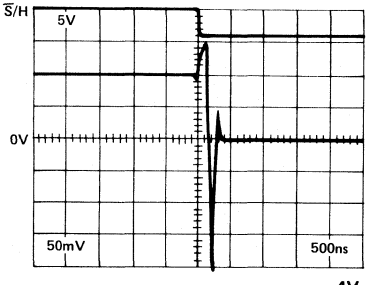
+1V TO 0V



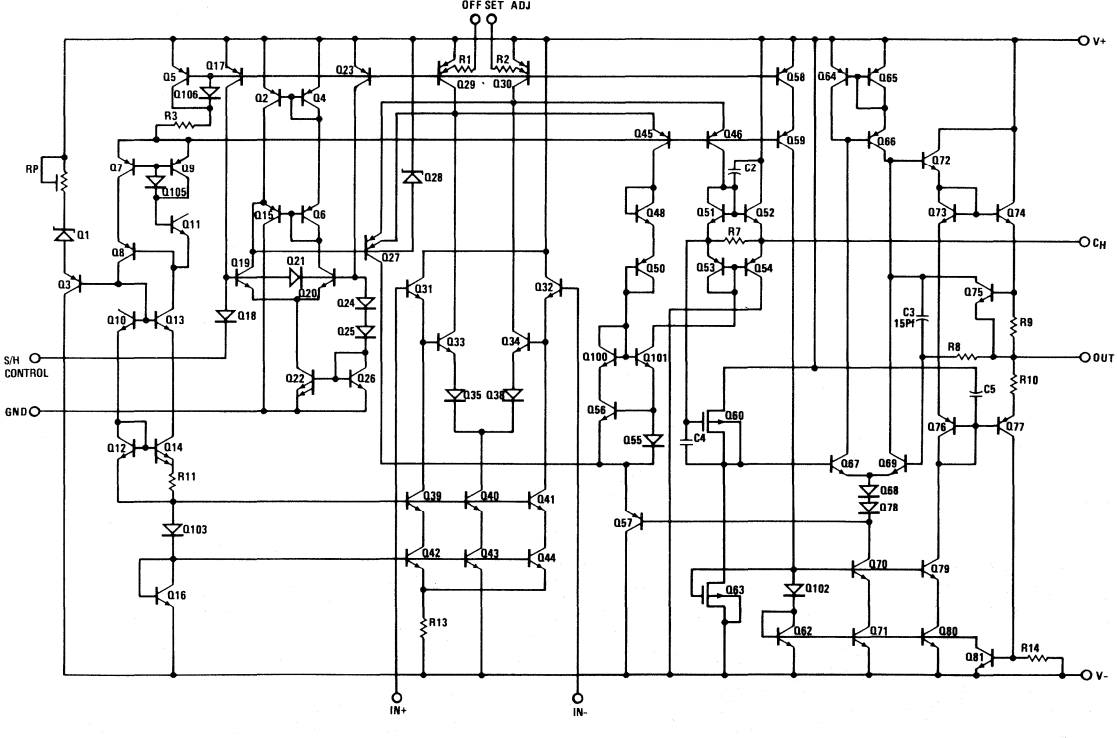
-100mV TO 0V



+100mV TO 0V



Schematic



Applications

BASIC SAMPLE-AND-HOLD
TOP VIEW

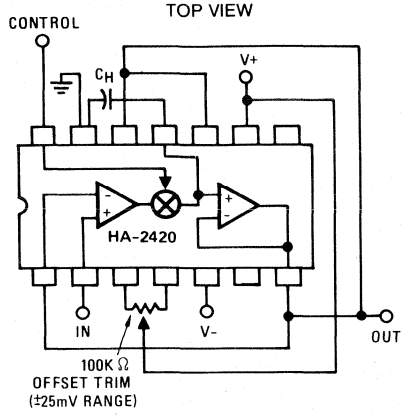


FIGURE 6.

GUARD RING LAYOUT
BOTTOM VIEW

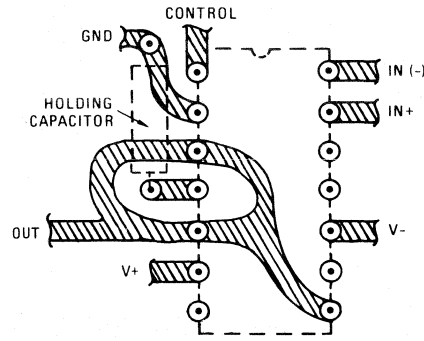


FIGURE 7.

NOTES:

1. Figure 6 shows a typical unity gain circuit, with Offset Zeroing. All of the other normal op amp feedback configurations may be used with the HA-2420/2425. The input amplifier may be used as a gated amplifier by utilizing Pin 11 as the output. This amplifier has excellent drive capabilities along with exceptionally low switch leakage.
2. The method used to reduce leakage paths on the P.C. board and the device package is shown in Figure 7. This guard ring is recommended to minimize the drift during hold mode.
3. The holding capacitor should have extremely high insulation resistance and low dielectric absorption. Polystyrene (below +85°C), Teflon, or Parlene types are recommended.

   For more applications, consult Harris Application Note 517, or factory applications group.

Glossary of Terms:

ACQUISITION TIME:

The time required following a "sample" command, for the output to reach its final value within ±0.1% or ±0.01%. This is the minimum sample time required to obtain a given accuracy, and includes switch delay time, slewing time and settling time.

APERTURE TIME:

The time required for the sample-and-hold switch to open, independent of delays through the switch driver and input amplifier circuitry. The switch opening time is that interval between the conditions of 10% open and 90% open.

EFFECTIVE APERTURE DELAY TIME (EADT):

The difference between propagation time from the analog input to the S/H switch, and digital delay time between the Hold command and opening of the switch.

EADT may be positive, negative or zero. If zero, the $\overline{S}/H$ amplifier will output a voltage equal to V_{IN} at the instant the Hold command was received. For negative EADT, the output in Hold (exclusive of pedestal and droop errors) will correspond to a value of V_{IN} that occurred before the Hold command.

APERTURE UNCERTAINTY:

The range of variation in Effective Aperture Delay Time. Aperture Uncertainty (also called Aperture Delay Uncertainty, Aperture Time Jitter, etc.) sets a limit on the accuracy with which a waveform can be reconstructed from sample data.

DRIFT CURRENT:

The net leakage current from the hold capacitor during the hold mode. Drift current can be calculated from the droop rate using the formula:

$$I_D\ (pA) = C_H\ (pF) \times \frac{\Delta V}{\Delta T}\ (Volts/sec)$$

Die Characteristics

Transistor Count 78
Die Dimensions ..... 97 x 61 x 19 mils
Substrate Potential ..... $-V_{SUPPLY}$
Process ..... Bipolar DI

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
Ceramic DIP	94	39
Ceramic LCC	88	28

HARRIS

HA-5320

High Speed Precision Monolithic Sample and Hold Amplifier

Features

- Gain, D.C. ..... 2 x 10^6 V/V
- Aquisition Time 1.0μs (0.01%)
- Droop Rate ..... 0.08μV/μs (+25°C)
  17μV/μs (Full Temperature)
- Aperture Time 25ns
- Hold Step Error (See Glossary) 1.0mV
- Internal Hold Capacitor
- Fully Differential Input
- TTL Compatible

Applications

- Precision Data Acquisition Systems
- Digital to Analog Converter Deglitcher
- Auto Zero Circuits
- Peak Detector

Description

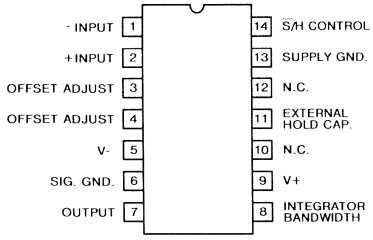
The HA-5320 was designed for use in precision, high speed data acquisition systems.

The circuit consists of an input transconductance amplifier capable of providing large amounts of charging current, a low leakage analog switch, and an output integrating amplifier. The analog switch sees virtual ground as its load; therefore, charge injection on the hold capacitor is constant over the entire input/output voltage range. The pedestal voltage resulting from this charge injection can be adjusted to zero by use of the offset adjust inputs. The device includes a hold capacitor. However, if improved droop rate is required at the expense of acquisition time, additional hold capacitance may be added externally.

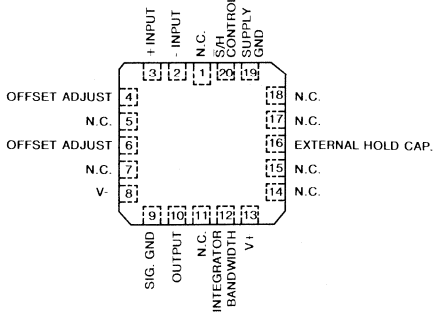
This monolithic device is manufactured using the Harris Dielectric Isolation Process, minimizing stray capacitance and eliminating SCR's. This allows higher speed and latch-free operation. The HA-5320 is available in a Ceramic 14-pin DIP, and a Ceramic 20-pin LCC package. For further information, please see Application Note 538.

Pinouts

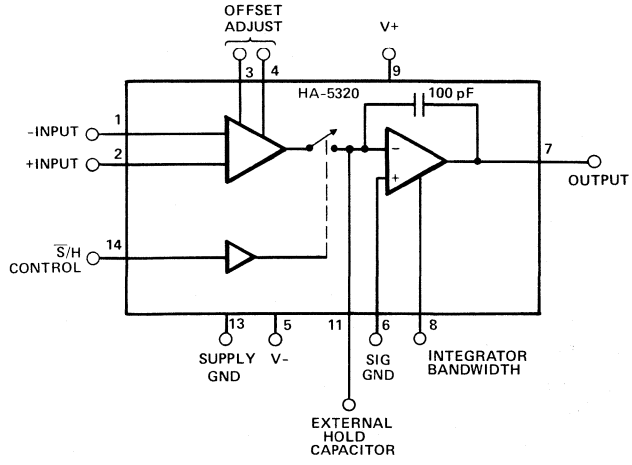
14 PIN CERAMIC DIP
TOP VIEW



20 PIN CERAMIC LCC



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Terminals 40V
Differential Input Voltage ..... ±24V
Digital Input Voltage ..... +8V, -15V
Output Current, Continuous ..... ±20mA (Note 2)
Junction Temperature ..... +175°C

Operating Temperature Range

HA-5320-2/-8 ..... $-55^{\circ}C \leq T_A \leq +125^{\circ}C$
HA-5320-5 ..... $0^{\circ}C \leq T_A \leq +75^{\circ}C$
Storage Temperature Range ..... $-65^{\circ}C \leq T_A \leq +150^{\circ}C$

Electrical Specifications

Test Conditions (Unless Otherwise Specified) $V_{SUPPLY} = \pm 15.0V$; C_H = Internal; Digital Input: $V_{IL} = +0.8V$ (Sample), $V_{IH} = +2.0V$ (Hold), Unity Gain Configuration (Output tied to -Input)

PARAMETER	TEMP	HA-5320-2/-8			HA-5320-5/-7			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Input Voltage Range	Full	±10	-	-	±10	-	-	V
Input Resistance	+25°C	1	5	-	1	5	-	MΩ
Input Capacitance	+25°C	-	-	3	-	-	3	pF
Offset Voltage	+25°C	-	0.2	-	-	0.5	-	mV
	Full	-	-	2.0	-	-	1.5	mV
Bias Current	+25°C	-	70	200	-	100	300	nA
	Full	-	-	200	-	-	300	nA
Offset Current	+25°C	-	30	100	-	30	300	nA
	Full	-	-	100	-	-	300	nA
Common Mode Range	Full	±10	-	-	±10	-	-	V
CMRR (Note 3)	+25°C	80	90	-	72	90	-	dB
Offset Voltage T.C.	Full	-	5	15	-	5	20	µV/°C
TRANSFER CHARACTERISTICS								
Gain, D.C.	+25°C	10^6	$2x10^6$	-	$3x10^5$	$2x10^6$	-	V/V
Gain Bandwidth Product ($A_V = +1$)	+25°C							
(Note 5) $C_H = 100pF$	-	-	2.0	-	-	2.0	-	MHz
$C_H = 1000pF$	-	-	0.18	-	-	0.18	-	MHz
OUTPUT CHARACTERISTICS								
Output Voltage	Full	±10	-	-	±10	-	-	V
Output Current	+25°C	±10	-	-	±10	-	-	mA
Full Power Bandwidth (Note 4)	+25°C	-	600	-	-	600	-	kHz
Output Resistance (Hold Mode)	+25°C	-	1.0	-	-	1.0	-	Ω
Total Output Noise, D.C. to 10MHz								
Sample	+25°C	-	125	200	-	125	200	μV_{RMS}
Hold	+25°C	-	125	200	-	125	200	μV_{RMS}
TRANSIENT RESPONSE								
Rise Time (Note 5)	+25°C	-	100	-	-	100	-	ns
Overshoot (Note 5)	+25°C	-	15	-	-	15	-	%
Slew Rate (Note 6)	+25°C	-	45	-	-	45	-	V/µs

Electrical Specifications (Continued)

PARAMETER	TEMP	HA-5320-2/-8 MIN	HA-5320-2/-8 TYP	HA-5320-2/-8 MAX	HA-5320-5/-7 MIN	HA-5320-5/-7 TYP	HA-5320-5/-7 MAX	UNITS
DIGITAL INPUT CHARACTERISTICS								
Input Voltage (High), V_{IH}	Full	2.0	-	-	2.0	-	-	V
Input Voltage (Low), V_{IL}	Full	-	-	0.8	-	-	0.8	V
Input Current (V_{IL} = 0V)	Full	-	-	10	-	-	4	µA
Input Current (V_{IH} = +5V)	Full	-	-	0.1	-	-	0.1	µA
SAMPLE AND HOLD CHARACTERISTICS								
Acquisition Time to 0.1% (Note 7)	+25°C	-	0.8	1.2	-	0.8	1.2	µs
Acquisition Time to 0.01% (Note 7)	+25°C	-	1.0	1.5	-	1.0	1.5	µs
Aperture Time (Note 8)	+25°C	-	25	-	-	25	-	ns
Effective Aperture Delay Time (See Glossary)	+25°C	-50	-25	0	-50	-25	0	ns
Aperture Uncertainty	+25°C	-	0.3	-	-	0.3	-	ns
Droop Rate	+25°C	-	0.08	0.5	-	0.08	0.5	µV/µs
	Full	-	17	100	-	1.2	100	µV/µs
Drift Current (Note 9)	+25°C	-	8	50	-	8	50	pA
	Full	-	1.7	10	-	0.12	10	nA
Charge Transfer (Note 9)	+25°C	-	0.1	0.5	-	0.1	0.5	pC
Hold Mode Settling Time 0.01%	Full	-	165	350	-	165	350	ns
Hold Mode Feedthrough ($10V_{p-p}$, 100kHz)	Full	-	2	-	-	2	-	mV
POWER SUPPLY CHARACTERISTICS								
Positive Supply Current (Note 10)	+25°C	-	11	13	-	11	13	mA
Negative Supply Current (Note 10)	+25°C	-	-11	-13	-	-11	-13	mA
Power Supply Rejection V+	Full	80	-	-	80	-	-	dB
(Note 11) V-	Full	65	-	-	65	-	-	dB

NOTES

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Internal Power Dissipation may limit Output Current below 20mA.
3. V_{CM} = ±5V D.C.
4. $V_O = 20V_{p-p}$; R_L = 2kΩ; C_L = 50pF; unattenuated output.
5. $V_O = 200mV_{p-p}$; R_L = 2kΩ; C_L = 50pF.
6. V_O = 20V Step; R_L = 2kΩ; C_L = 50pF.
7. V_O = 10V Step; R_L = 2kΩ; C_L = 50pF.
8. Derived from computer simulation only; not tested.
9. V_{IN} = 0V, V_{IH} = +3.5V, t_r < 20ns (V_{IL} to V_{IH}).
10. Specified for a zero differential input voltage between +IN and -IN. Supply current will increase with differential input (as may occur in the Hold mode) to approximately ±28mA at 20V.
11. Based on a one volt delta in each supply, i.e. 15V ±0.5V D.C.

Applying the HA-5320

The HA-5320 has the uncommitted differential inputs of an op amp, allowing the Sample and Hold function to be combined with many conventional op amp circuits. See the Harris Application Note 517 for a collection of circuit ideas.

LAYOUT

A printed circuit board with ground plane is recommended for best performance. Bypass capacitors (0.01 to 0.1μF, ceramic) should be provided from each power supply terminal to the Supply Ground terminal on pin 13.

The ideal ground connections are pin 6 (SIG. Ground) directly to the system Signal Ground, and pin 13 (Supply Ground) directly to the system Supply Common.

HOLD CAPACITOR

The HA-5320 includes a 100pF MOS hold capacitor, sufficient for most high speed applications (the Electrical Specifications section is based on this internal capacitor). Additional capacitance may be added between pins 7 and 11. This external hold capacitance will reduce droop rate at the expense of acquisition time, and provide other trade-offs as shown in the Performance Curves.

If an external hold capacitor C_H is used, then a noise bandwidth capacitor of value 0.1 C_H should be connected from pin 8 to ground. Exact value and type are not critical.

The hold capacitor C_H should have high insulation resistance and low dielectric absorption, to minimize droop errors. Polystyrene dielectric is a good choice for operating temperatures up to +85°C. Teflon® and glass dielectrics offer good performance to +125°C and above.

The hold capacitor terminal (pin 11) remains at virtual ground potential. Any PC connection to this terminal should be kept short and "guarded" by the ground plane, since nearby signal lines or power supply voltages will introduce errors due to drift current.

®Teflon is a registered Trademark of Dupont Corporation.

Applications

Figure 1 shows the HA-5320 connected as a unity gain noninverting amplifier — its most widely used configuration. As an input device for a fast successive — approximation A/D converter, it offers very high throughput rate for a monolithic IC sample/hold amplifier. Also, the HA-5320's hold step error is adjustable to zero using the Offset Adjust potentiometer, to deliver a 12-bit accurate output from the converter.

The application may call for an external hold capacitor C_H as shown. As mentioned earlier, 0.1C_H is then recommended at pin 8 to reduce output noise in the Hold mode.

The HA-5320 output circuit does not include short circuit protection, and consequently its output impedance remains low at high frequencies. Thus, the step changes in load current which occur during an A/D conversion are absorbed at the S/H output with minimum voltage error. A momentary short circuit to ground is permissible, but the output is not designed to tolerate a short of indefinite duration.

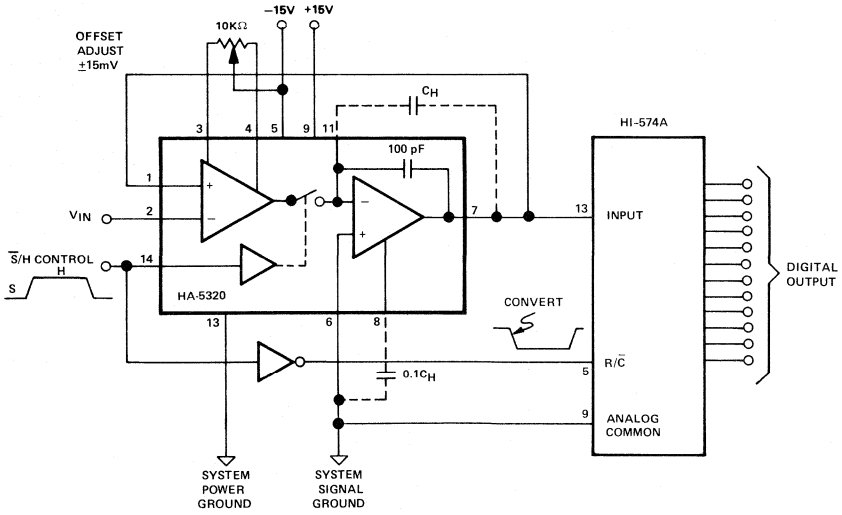


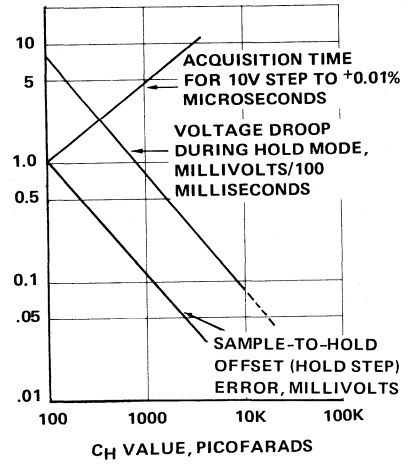
FIGURE 1.

TYPICAL HA-5320 CONNECTIONS; NONINVERTING UNITY GAIN MODE

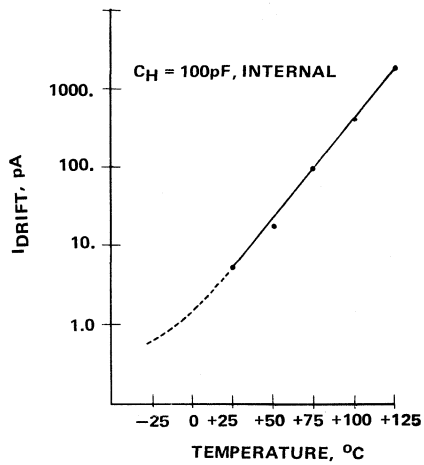
NOTE: Pin Numbers Refer to DIP Package Only.

Performance Curves $V_{SUPPLY} = \pm 15VDC$

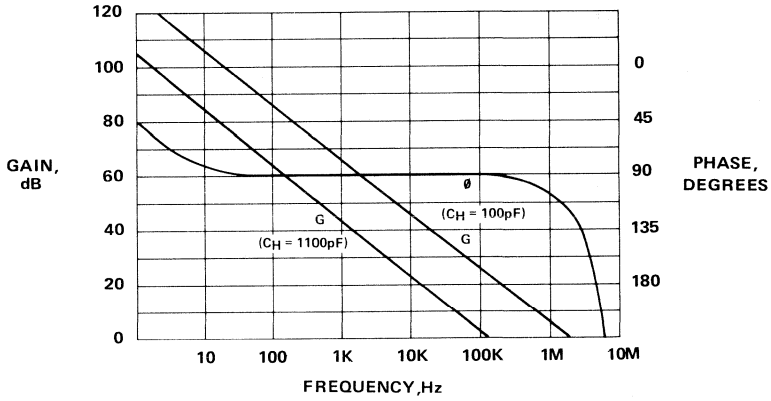
TYPICAL SAMPLE AND HOLD PERFORMANCE AS FUNCTION OF HOLDING CAPACITOR



DRIFT CURRENT vs. TEMPERATURE

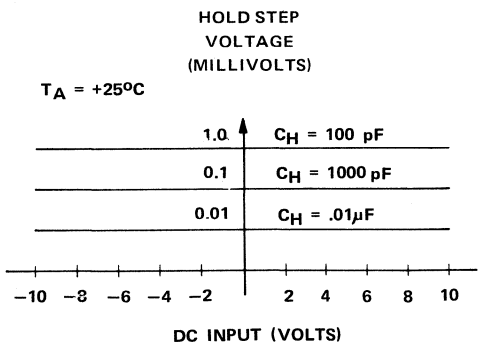


OPEN LOOP GAIN AND PHASE RESPONSE

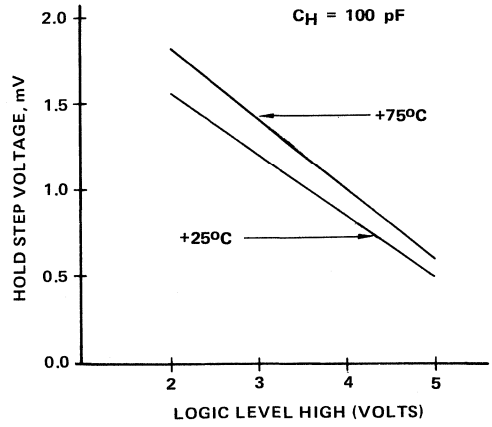


TYPICAL SAMPLE-TO-HOLD OFFSET (HOLD STEP) ERROR

HOLD STEP vs. INPUT VOLTAGE

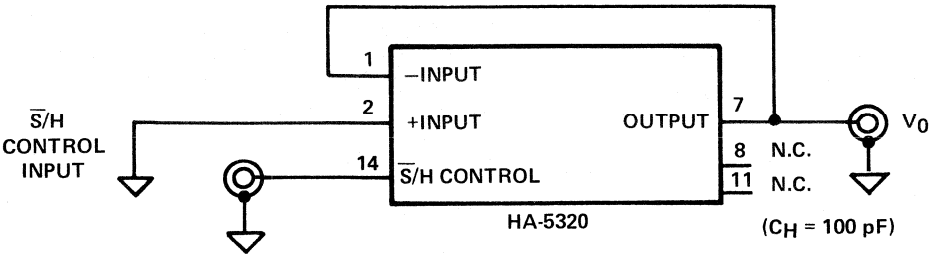


HOLD STEP vs. LOGIC (V_{IH}) VOLTAGE



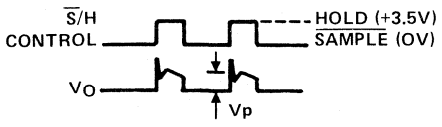
Test Circuits

CHARGE TRANSFER AND DRIFT CURRENT



CHARGE TRANSFER TEST

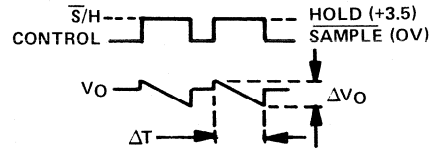
1. Observe the "hold step" voltage V_p:



2. Compute charge transfer: $Q = V_p C_H$

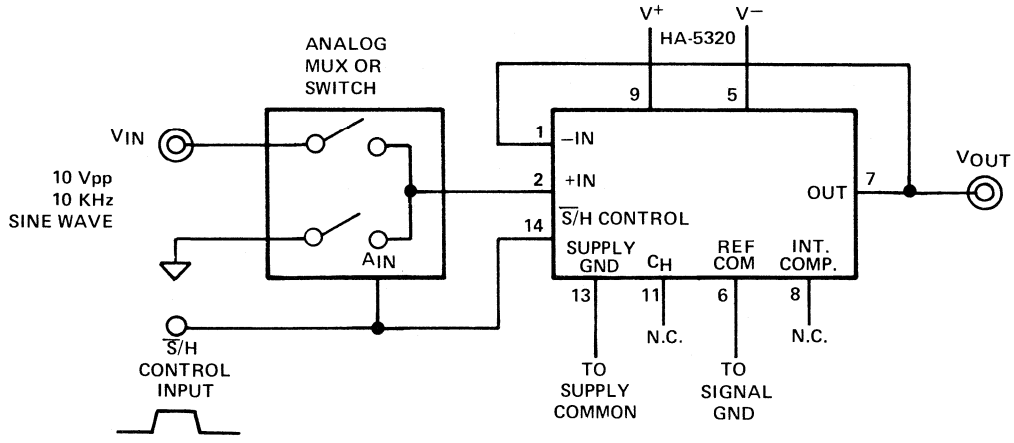
DRIFT CURRENT TEST

1. Observe the voltage "droop", $\Delta V_O/\Delta T$:



2. Measure the slope of the output during hold, $\Delta V_O/\Delta T$, and compute drift current: $I_D = C_H \Delta V_O/\Delta T$.

HOLD MODE FEED THROUGH ATTENUATION



Feedthrough in dB = 20 Log $\frac{V_{OUT}}{V_{IN}}$ where:

V_{OUT} = $Volts_{p-p}$, Hold Mode,
V_{IN} = $Volts_{p-p}$.

Glossary of Terms

ACQUISITION TIME:

The time required following a "sample" command, for the output to reach its final value within ±0.1% or ±0.01%. This is the minimum sample time required to obtain a given accuracy, and includes switch delay time, slewing time and settling time.

CHARGE TRANSFER:

The small charge transferred to the holding capacitor from the inter-electrode capacitance of the switch when the unit is switched to the HOLD mode. Charge transfer is directly proportional to sample-to-hold offset pedestal error, where:

$$\text{Charge Transfer (pC)} = C_H \text{ (pF)} \times \text{Offset Error (V)}$$

APERTURE TIME:

The time required for the sample-and-hold switch to open, independent of delays through the switch driver and input amplifier circuitry. The switch opening time is the interval between the conditions of 10% open and 90% open.

HOLD STEP ERROR:

Hold Step Error is the output error due to Charge Transfer (see above). It may be calculated from the specified parameter, Charge Transfer, using the following relationship:

$$\text{HOLD STEP (V)} = \frac{\text{CHARGE TRANSFER (pC)}}{\text{HOLD CAPACITANCE (pF)}}$$

See Performance Curves.

EFFECTIVE APERTURE DELAY TIME (EADT):

The difference between propagation time from the analog input to $\overline{S}$/H switch, and digital delay time between the Hold command and opening of the switch.

EADT may be positive, negative or zero. If zero, the $\overline{S}$/H amplifier will output a voltage equal to V_{IN} at the instant the Hold command was received. For negative EADT, the output in Hold (exclusive of pedestal and droop errors) will correspond to a value of V_{IN} that occurred before the Hold command.

APERTURE UNCERTAINTY:

The range of variation in Effective Aperture Delay Time. Aperture Uncertainty (also called Aperture Delay Uncertainty, Aperture Time Jitter, etc.) sets a limit on the accuracy with which a waveform can be reconstructed from sample data.

DRIFT CURRENT:

The net leakage current from the hold capacitor during the hold mode. Drift current can be calculated from the droop rate using the formula:

$$I_D \text{ (pA)} = C_H \text{ (pF)} \times \frac{\Delta V}{\Delta T} \text{ (Volts/sec)}$$

Die Characteristics

Transistor Count	175
Die Dimensions	90.2 x 143.7 x 19 mils
Substrate Potential	$-V_{SUPPLY}$
Process	Bipolar DI

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
Ceramic DIP	75	15
Ceramic LCC	76	19

HA-5330

Very High Speed Precision Monolithic Sample and Hold

Features

- Very Fast Acquisition.....350ns (0.1%)
  500ns (0.01%)
- Low Droop Rate 0.01μV/μs
- Very Low Offset.....0.2mV
- High Slew Rate.....90V/μs
- Wide Supply Range..... $\pm$11V to $\pm$18V
- Internal Hold Capacitor
- Fully Differential Input
- TTL/CMOS Compatible

Applications

- Precision Data Acquisition Systems
- D/A Converter Deglitching
- Auto-Zero Circuits
- Peak Detectors

Description

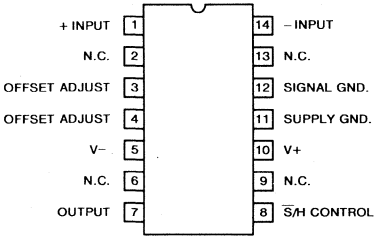
The HA-5330 is a very fast sample and hold amplifier designed primarily for use with high speed A/D converters. It utilizes the Harris Dielectric Isolation process to achieve a 500ns acquisition time to 12-bit accuracy and a droop rate of 0.01μV/μs. The circuit consists of an input transconductance amplifier capable of producting large amounts of charging current, a low leakage analog switch, and an integrating output stage which includes a 90pF hold capacitor.

The analog switch operates into a virtual ground, so charge injection on the hold capacitor is constant and independent of V_{IN}. Charge injection is held to a low value by compensation circuits and, if necessary, the resulting 0.5mV hold step error can be adjusted to zero via the Offset Adjust terminals. Compensation is also used to minimize leakage currents which cause voltage droop in the Hold mode.

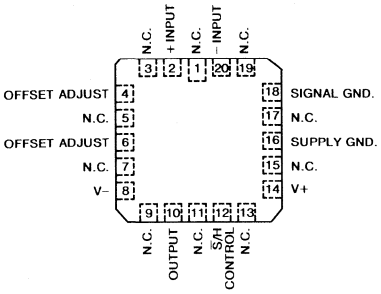
The HA-5330 will operate at reduced supply voltages (to $\pm$11V) with a reduced signal range. This monolithic device is available in a 14 pin Ceramic DIP and a 20 pad LCC package. The MIL-STD-883 data sheet for this device is available on request.

Pinouts

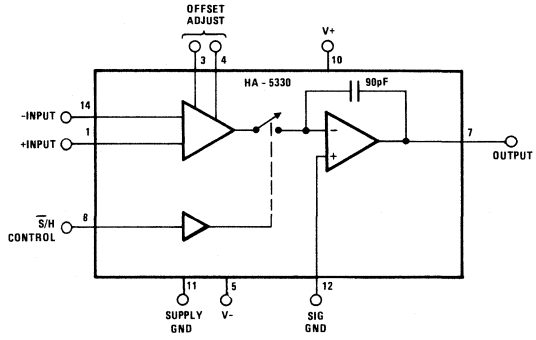
14 PIN CERAMIC DIP
TOP VIEW



20 PAD (LCC)
TOP VIEW



Functional Diagram



CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

Voltage between V+ and SUPPLY/SIG GND ..... +20V
Voltage between V- and SUPPLY/SIG GND ..... -20V
Voltage between SUPPLY GND and SIG GND ..... ±2.0V
Differential Input Voltage ..... ±24V
Voltage between $\overline{S}$/H Control and SUPPLY/SIG GND ..... +8V, -6V
Output Current, Continuous ..... ±17mA (Note 2)
Junction Temperature ..... +175°C

Operating Temperature Range

HA-5330-2 ..... -55°C to +125°C
HA-5330-4 ..... -25°C to +85°C
HA-5330-5 ..... 0°C to +75°C
Storage Temperature Range ..... -65°C to +150°C

Electrical Specifications

Test Conditions Unless Otherwise Specified: V_{SUPPLY} = ±15V; $\overline{S}$/H Control V_{IL} = +0.8V (Sample), V_{IH} = +2.0V (Hold); SIG GND = SUPPLY GND, Unity Gain Configuration (Output tied to -Input)

PARAMETER	TEMP	HA-5330-2, -4			HA-5330-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Input Voltage Range	Full	±10	—	—	±10	—	—	V
Input Resistance (Note 3)	+25°C	5	15	—	5	15	—	MΩ
Input Capacitance	+25°C	—	3	—	—	3	—	pF
Offset Voltage	+25°C	—	0.2	—	—	0.2	—	mV
	Full	—	—	2.0	—	—	1.5	mV
Offset Voltage Temperature Coefficient	Full	—	1	10	—	1	10	μV/°C
Bias Current	+25°C	—	±20	—	—	±20	—	nA
	Full	—	—	±500	—	—	±300	nA
Offset Current	+25°C	—	20	—	—	20	—	nA
	Full	—	—	500	—	—	300	nA
Common Mode Range	Full	±10	—	—	±10	—	—	V
CMRR (Note 4)	Full	86	100	—	86	100	—	dB
TRANSFER CHARACTERISTICS								
Gain, DC	Full	2×10^6	2×10^7	—	2×10^6	2×10^7	—	V/V
Gain Bandwidth Product (Note 5)	+25°C	—	4.5	—	—	4.5	—	MHz
OUTPUT CHARACTERISTICS								
Output Voltage	Full	±10	—	—	±10	—	—	V
Output Current	Full	±10	—	—	±10	—	—	mA
Full Power Bandwidth (Note 6)	+25°C	—	1.4	—	—	1.4	—	MHz
Output Resistance								
Hold Mode	+25°C	—	0.2	—	—	0.2	—	Ω
Sample Mode	+25°C	—	10^{-5}	0.001	—	10^{-5}	0.001	Ω
Total Output Noise, DC to 4.0MHz								
Sample Mode	+25°C	—	230	—	—	230	—	μV RMS
Hold Mode	+25°C	—	190	—	—	190	—	μV RMS

Die Characteristics

Transistor Count 205
Die Dimensions ..... 99 x 166 x 19 mils
Substrate Potential ..... SIG. GND
Process ..... Bipolar DI

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
Ceramic DIP	75	15
Ceramic LCC	76	19

Electrical Specifications (Continued)

PARAMETER	TEMP	HA-5330-2, -4			HA-5330-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TRANSIENT RESPONSE								
Rise Time (Note 5)	+25°C	—	70	—	—	70	—	ns
Overshoot (Note 5)	+25°C	—	10	—	—	10	—	%
Slew Rate (Note 7)	+25°C	—	90	—	—	90	—	V/μs
DIGITAL INPUT CHARACTERISTICS								
Input Voltage (High), V_{IH}	Full	2.0	—	—	2.0	—	—	V
Input Voltage (Low), V_{IL}	Full	—	—	0.8	—	—	0.8	V
Input Current (V_{IL} = 0V)	Full	—	10	40	—	10	40	μA
Input Current (V_{IH} = +5V)	Full	—	10	40	—	10	40	μA
SAMPLE/HOLD CHARACTERISTICS								
Acquistion Time (Note 8)								
(0.1%)	+25°C	—	350	—	—	350	—	ns
	Full	—	—	500	—	—	500	ns
(0.01%)	+25°C	—	500	—	—	500	—	ns
	Full	—	—	900	—	—	900	ns
Aperture Time (Note 3)	+25°C	—	20	—	—	20	—	ns
Effective Aperture Delay Time (See Glossary)	+25°C	-50	-25	0	-50	-25	0	ns
Aperture Uncertainty	+25°C	—	0.1	—	—	0.1	—	ns
Droop Rate (Note 9)	+25°C	—	0.01	—	—	0.01	—	μV/μs
	Full	—	—	100	—	—	10	μV/μs
Hold Step Error (Note 10)	+25°C	—	0.5	—	—	0.5	—	mV
Hold Mode Settling Time (0.01%)	+25°C	—	100	200	—	100	200	ns
Hold Mode Feedback 20V_{p-p}, 100kHz	Full	—	-88	—	—	-88	—	dB
POWER SUPPLY CHARACTERISTICS								
Positive Supply Current	Full	—	18	22	—	18	24	mA
Negative Supply Current	Full	—	19	23	—	19	25	mA
Power Supply Rejection, V+, V- (Note 11)	Full	86	100	—	86	100	—	dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Internal Power Dissipation may limit Output Current below ±17mA.
3. Derived from computer simulation only; not tested.
4. V_{CM} = ±10V DC.
5. V_i = 200mV Step; R_L = 2K; C_L = 50pF
6. Full power bandwidth based on slew rate measurement using $FPBW = \frac{SLEW\ RATE}{2\pi\ Vpeak}$
7. V_0 = 20V Step; R_L = 2K; C_L = 50pF.
8. V_0 = 10V Step; R_L = 2K; C_L = 50pF.
9. This parameter is measured at ambient temperature extremes in a high speed test environment. Consequently, steady state heating effects from internal power dissipation are not included.
10. V_{IN} = 0V; V_{IH} = +3.5V; t_r = 22ns (V_{IL} to V_{IH}). See graph.
11. Based on a three volt delta in each supply, i.e. 15V = ±1.5V DC.

Applying the HA-5330

The HA-5330 has the uncommitted differential inputs of an op amp, allowing the Sample/Hold function to be combined with many conventional op amp circuit ideas. See the Harris Application Note 517 for a collection of circuit ideas.

Layout

A printed circuit board with ground plane is recommended for best performance. Bypass capacitors (0.01 to 0.1μF, ceramic) should be provided from each power supply terminal to the Supply GND Terminal on pin 11.

Applications

The HA-5330 is configured as a unity gain noninverting amplifier by simply connecting the output (pin 7) to the inverting input (pin 14). As an input device for a fast successive - approximation A/D converter, it offers an extremely high throughput rate. Also, the HA-5330's pedestal error is adjustable to zero by using an Offset Adjust potentiometer (10K to 50K) center tapped to V-.

The ideal ground connections are pin 11 (Supply Ground) directly to the system Supply Common, and pin 12 (Signal Ground) directly to the system Signal Ground (Analog Ground).

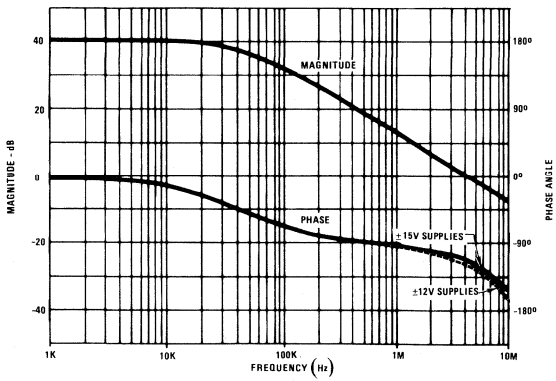
Hold Capacitor

The HA-5330 includes a 90pF MOS hold capacitor, sufficient for most high speed applications (the Electrical Specifications section is based on the internal capacitor).

Output Stage

The HA-5330 output circuit does not include short circuit protection, and consequently its output impedance remains low at high frequencies. Thus, the step changes in load current which occur during an A/D conversion are absorbed at the $\overline{S}$/H output with minimum voltage error. A momentary short circuit to ground is permissible, but the output is not designed to tolerate a short of indefinite duration.

MAGNITUDE AND PHASE RESPONSE
(Closed Loop Gain = 100)



Glossary of Terms

Acquisition Time:

The time required following a "sample" command, for the output to reach its final value within ±0.1% or ±0.01%. This is the minimum sample time required to obtain a given accuracy, and includes switch delay time, slewing time and settling time.

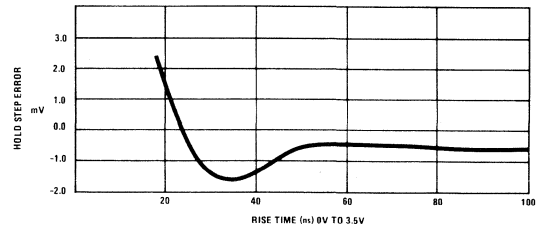
Aperture Time:

The time required for the sample-and-hold switch to open, independent of delays through the switch driver and input amplifier circuitry. The switch opening time is that interval between the conditions of 10% open and 90% open.

Hold Step Error:

Hold step error is the output shift due to charge transfer from the sample to the hold mode. It is also referred to as "offset step" or "pedestal error".

HOLD STEP ERROR vs. S/H CONTROL RISE TIME



Effective Aperture Delay Time (EADT):

The difference between propagation time from the analog input to the $\overline{S}$/H switch, and digital delay time between the Hold command and opening of the switch.

EADT may be positive, negative or zero. If zero, the $\overline{S}$/H amplifier will output a voltage equal to V_{IN} at the instant the Hold command was received. For negative EADT, the output in Hold (exclusive of pedestal and droop errors) will correspond to a value of V_{IN} that occurred before the Hold command.

Aperture Uncertainty:

The range of variation in Effective Aperture Delay Time. Aperture Uncertainty (also called Aperture Delay Uncertainty, Aperture Time Jitter, etc.) sets a limit on the accuracy with which a waveform can be reconstructed from sample data.

ANALOG

Telecommunications

8

ABSOLUTE MAXIMUM RATINGS

As with all semiconductors, stresses listed under "Absolute Maximum Ratings " may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Specifications" are the only conditions recommended for satisfactory operation.

Ordering Information

HARRIS PRODUCT CODE EXAMPLE

H C 3 — 5502A — 5

PREFIX:
H (HARRIS)

FAMILY:
A : Analog
C : Communications
D : Digital
F : Filters
I : Interface
M : Memory
V : Analog High Voltage
Y : Analog Hybrids

PACKAGE:
1 : Dual-In-Line Ceramic
2 : Metal Can
3 : Dual-In-Line Plastic
4 : Leadless Chip Carriers (LCC)
4P : Plastic Leaded Chip Carriers (PLCC)
7 : Mini-DIP, Ceramic
0 : Chip Form

PART NUMBER

TEMPERATURE:
1 : 0°C to +200°C *
2 : -55°C to +125°C
4 : -25°C to +85°C
5 : 0°C to +75°C
6 : 100% +25°C Probe (Dice Only)
7 : Dash-7 High Reliability Commercial Product 0°C to +75°C
8 : Dash-8 Program HA2-2520-8 (Example Only)
9 : -40°C to +85°C

* Special High Temperature Testing Available on Certain Product Types. Consult Factory for Availability.

Standard Products Packaging Availability†

PACKAGE	PLASTIC DIP 3-		CERAMIC DIP 1-					SURFACE MOUNT LCC 4-	SURFACE MOUNT PLCC 4P	
TEMPERATURE	**-5**	**-7**	**-2**	**-5**	**-7**	**-8**	**-9**	**-8**	**-5**	**-7**
DEVICE NUMBER										
TELECOM										
HC-5502A	R	R		G	G		G		AB	AB
HC-5502B	R	R		G	G		G		AB	AB
HC-5504	R	R		G	G		G		AB	AB
HC-5504B	R	R		G	G		G		AB	AB
HC-5512				C2	C2					
HC-5512A				C2	C2					
HC-5512D			C2			C2	C2	T		
HC-55536				B1			B1			
HC-55564			B1	B1	B1	*	B1	*		
HC-5560	Q									
HF-10			E	E	E	E	E	T		

* Available as MIL-STD-883 Only.
† Letter codes in this chart indicate available packages as shown in Packaging Section 11.

Glossary of Telecom Terms

BORSCHT: Acronym for functions provided by a subscriber line interface circuit. Includes Battery feed, Overvoltage protection, Ringing, Supervision, Coding, Hybrid and Test functions.

CHIP POWER DOWN: Ability to minimize device power dissipation by shutting down majority of power consuming circuitry, putting the device in an "idle" state. Not to be confused with Power Denial, which minimizes power dissipation across the 2w loop.

DC/DC CONVERTER: Converts one DC voltage to another. Commonly used in transmission equipment where different DC voltages are required throughout a system.

FAULT CURRENTS: These are loop currents that flow during loop fault conditions, i.e., shorts in the line. Integrated on the SLIC is a fault current limit circuit which protects the SLIC from excessive power.

FREQUENCY RESPONSE: A measure of the variation of the transmission performance of the SLIC with respect to frequency variations.

IDLE CHANNEL NOISE (ICN): Noise measurements must characterize the annoyance to a user of unwanted signals. ICN is a measure of these unwanted signals under idle (no signal) channel conditions.

INSERTION LOSS OR TRANS HYBRID GAIN VARIATION: Simply the gain or loss of a signal through the SLIC from 2w to 4w and from 4w to 2w.

LEVEL LINEARITY OR GAIN TRACKING: A measure of the linearity of gain over a range of signal levels at a particular frequency. (Dynamic range usually +3dBm to -55dBm).

LINE POLARITY REVERSAL: Refers to 2w side tip and ring lines. Tip lines normally more positive with respect to the ring line. Reverse polarity is used for signaling purposes on trunk lines.

LONGITUDINAL CURRENT REJECTION: Ability of SLIC to suppress currents induced in the subscriber loop by power lines, antennae, etc.

LOOP CURRENT LIMIT: This is the maximum current the SLIC will allow in the subscriber loop. It is controlled by sensing loop current across the feed resistors, and adjusting the DC bias voltage at ring feed accordingly.

LOW FREQUENCY LONGITUDINAL BALANCE: Measure of degree of match of tip to ground and ring to ground impedance in the presence of large longitudinal currents at power line frequencies (50, 60 Hz).

OVERLOAD LEVEL: Upper limit of the SLICs dynamic range where speech signals just start to clip. This parameter sets the maximum speech power level the device can handle.

PROGRAMMABLE DC FEED: Ability to control the tip feed and ring feed output DC bias voltages that establish loop current.

PSRR: Measures the SLICs ability to reject noise in the power supply. SLIC must not allow the noise to couple into the speech paths.

SURGE PROTECTION: Adequate protection of the SLIC must be provided against lightning, low frequency induction, and power contact surges. The combination of split feed resistors, a diode bridge and ability of the feed amplifiers to reject longitudinal currents afford adequate protection to the SLIC.

TRANS HYBRID LOSS: A measure of the SLICs ability to separate the bidirectional speech transmission path into distinct transmit and receive paths on the 4w side.

2W LONGITUDINAL BALANCE: A measure of the degree of balance of tip to ground and ring to ground. Mismatches result in degradation of longitudinal current suppression in on-hook and off-hook conditions.

Telecom Line Card Glossary

RING RELAY: Allows switching of AC ringing signal from ring generator to drive subscriber telephone ringer via tip or ring side.

RING RELAY DRIVER: SLIC output to drive ring relay coil.

SNUBBER NETWORK: RC network across ring relay contacts to reduce effects of inductive kickbacks to SLIC.

DC ISOLATION CAPACITOR: Blocks DC loop current from transformer.

ZENER DIODE: Secondary protection for RX and TX amplifiers.

AC HYBRID TRANSFORMER: Provides 2wire-4wire and 4wire-2wire conversion of voice signals.

BALANCING NETWORK: Provides 2wire line impedance matching and transhybrid balance.

DC FEED RESISTORS: Four 150Ω resistors that provide 600Ω of 2wire impedance and provide sense mechanism for SLIC to detect switch hook, ground key and ring trip. Also provides some high voltage protection to SLIC by dividing in half any voltage transient.

TX/RX AMPLIFIERS: Amplifies voice signal lost in hybrid transformer. Also provides impedance conversion from 2wire-4wire and 4wire-2wire.

SUPERVISION NETWORK: Monitors SLICs switch hook, ringtrip, and ground key detection functions, and flags controller.

CONTROLLER: Stores ring command, ring trip, switch hook information, etc., until system CPU or line circuit can react.

HC-5502A

SLIC
Subsciber Line Interface Circuit

Features

- Monolithic Integrated Device
- DI High Voltage Process
- Compatible With Worldwide PBX Performance Requirements
- Controlled Supply of Battery Feed Current for Short Loops (30mA)
- Internal Ring Relay Driver
- Low Power Consumption During Standby
- Switch Hook, Ground Key and Ring Trip Detection Functions
- Selective Denial of Power to Subscriber Loops

Applications

- Solid State Line Interface Circuit for Analog and Digital PBX Systems
- Direct Inward Dial (DID) Trunks
- Voice Messaging PBX's

Description

The Harris SLIC incorporates many of the BORSHT function on a single IC chip. This includes DC battery feed, a ring relay driver, supervisory and hybrid functions. This device is designed to maintain transmission performance in the presence of externally induced longitudinal currents. Using the unique Harris dielectric isolation process, the SLIC can operate directly with a wide range of station battery voltages.

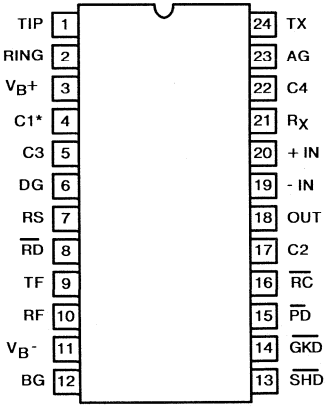
The SLIC also provides selective denial of power. If the PBX system becomes overloaded during an emergency, the SLIC will provide system protection by denying power to selected subscriber loops.

The Harris SLIC is ideally suited for the design of new digital PBX systems, by eliminating bulky hybrid transformers.

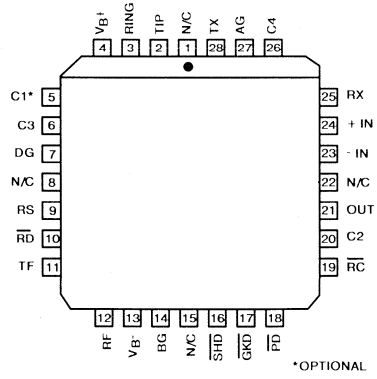
SLIC is available in either a 24 pin Dual-in-Line Plastic or Ceramic package, and a 28 pin PLCC package. The SLIC is also available as unpackaged die.

Pinouts

HC-5502A
(CERAMIC/PLASTIC DIP)
TOP VIEW

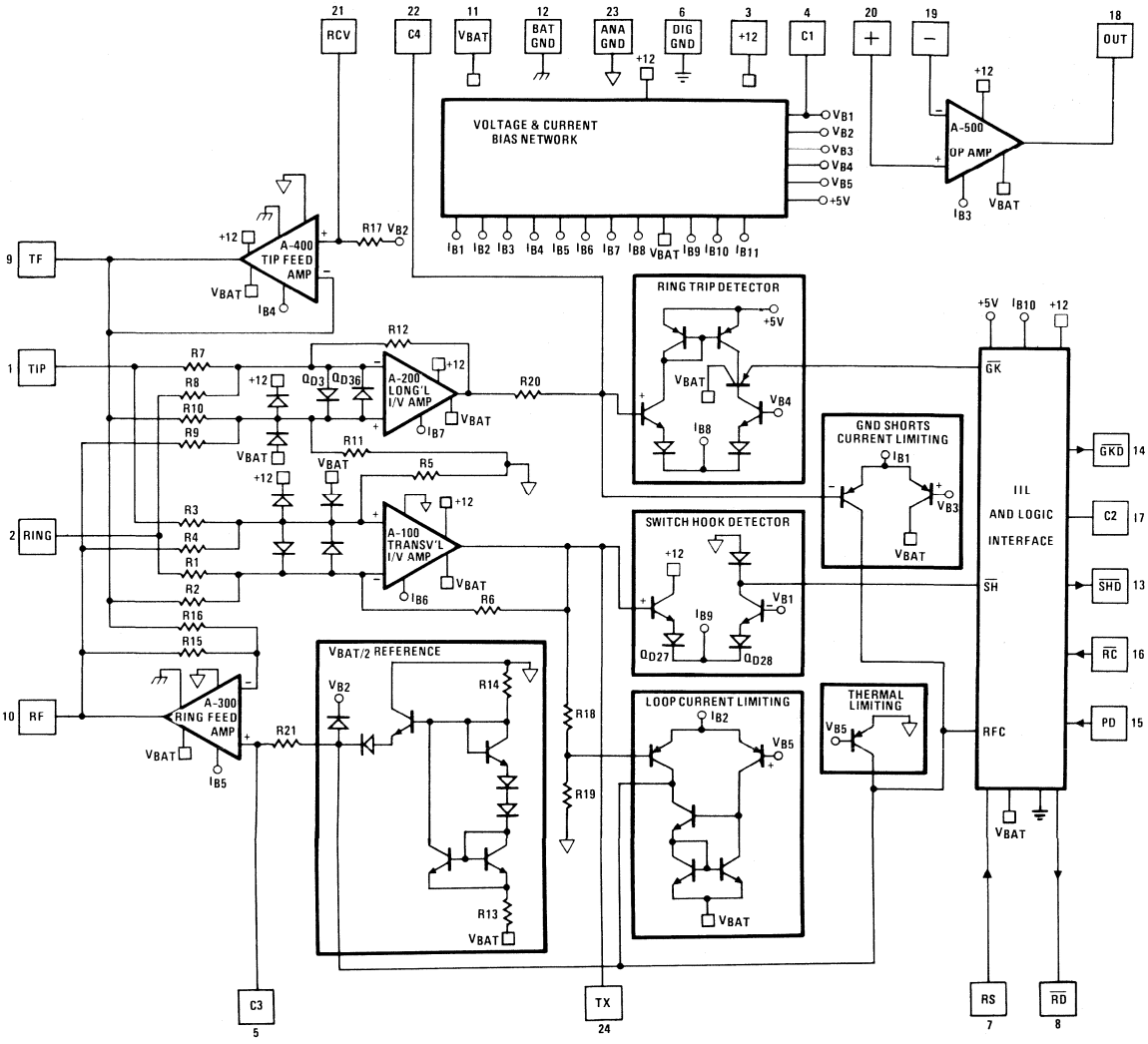


HC4P5502A
(PLCC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Schematic



HC-5502A SLIC FUNCTIONAL SCHEMATIC.

Die Characteristics

Transistor Count	181	
Diode Count	27	
Die Dimensions	169 x 112	
Substrate Potential	Unconnected	
Process	Bipolar-DI	
Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
Ceramic DIP	51	16
Plastic DIP	52	24

Absolute Maximum Ratings (Note 1)

Maximum Continuous Supply Voltages ($V_{B}-$) ..... -60 to +0.5 V
($V_{B}+$) .... -0.5 to +15 V
($V_{B}+ - V_{B}-$) 75V
Relay Drive Voltage (V_{RD}) ..... -0.5 to +15V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C

Recommended Operating Conditions

Relay Driver Voltage (V_{RD}) ..... +5 to +12V
Positive Supply Voltage ($V_{B}+$) ..... 10.8 to 13.2V
Negative Supply Voltage($V_{B}-$) ..... -42 to -58V
Minimum High Level Logic Input Voltage 2.4V
Maximum Low Level Logic Input Voltage 0.6V
Loop Resistance (R_L) ..... 200 to 1200 Ohms
Operating Temperature Range
HC-5502A-5,-7 ..... 0°C to +75°C
HC-5502A-9 ..... -40°C to +85°C

Electrical Specifications

$V_{B}-$ = -48V, $V_{B}+$ = +12V, AG = BG = DG = 0V, Unless Otherwise Noted, Typical Parameters +25°C. Min-Max Parameters are Over Operating Temperature Range.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
On Hook Power Dissipation	$I_{Long} = 0$	-	135	174	mW
Off Hook Power Dissipation	R_{LINE} = 600 Ohms, $I_{Long} = 0$	-	450	580	mW
Off Hook IB+	R_{LINE} = 600 Ohms, $I_{Long} = 0$ @ -40°C	-	-	5.0	mA
Off Hook IB+	R_{LINE} = 600 Ohms, $I_{Long} = 0$ @ +25°C	-	-	4.3	mA
Off Hook IB-	R_{LINE} = 600 Ohms, $I_{Long} = 0$	-	-	38	mA
Off Hook Loop Current	R_{LINE} = 1200 Ohms, $I_{Long} = 0$	-	21	-	mA
Off Hook Loop Current	R_{LINE} = 1200 Ohms, $V_{B}-$ = -42V, $I_{Long} = 0$ T_A = 25°C	17.5	-	-	mA
Off Hook Loop Current	R_{LINE} = 200 Ohms, $I_{Long} = 0$	25.5	30	34.5	mA
Fault Currents					
TIP to Ground		-	14	-	mA
RING to Ground		-	47	-	mA
TIP to RING		-	30	-	mA
TIP and RING to Ground		-	47	-	mA
Ring Relay Drive V_{OL}	I_{OL} = 62mA	-	0.2	0.5	V
Ring Relay Driver Off Leakage	V_{RD} = +12V, RC = 1 = HIGH, T_A = 25°C	-	-	100	µA
Ring Rrip Detection Period	R_{LINE} = 600 Ohms, T_A = +25°C	-	2	3	Ring Cycles
Switch Hook Detection Threshold	$\overline{SHD} = V_{OL}$	10	-	-	mA
	$\overline{SHD} = V_{OH}$	-	-	5	mA
Ground Key Detection Threshold	$\overline{GKD} = V_{OL}$	20	-	-	mA
	$\overline{GKD} = V_{OH}$	-	-	10	-
Loop Current During Power Denial		-	±2	-	mA
Dial Pulse Distortion		0	-	5	ms
Receive Input Impedance		-	90	-	kOhms
Transmit Output Impedance		-	5	20	Ohms
Two Wire Return Loss	(Return Loss Referenced to 600Ω +2.16µF)				
SRL LO		-	15.5	-	dB
ERL		-	24	-	dB
SRL HI		-	31	-	dB
Longitudinal Balance	1V Peak-Peak 200Hz - 3400Hz $0°C \leq T_A \leq 75°C$				
2 Wire Off Hook		58	65	-	dB
2Wire On Hook		60	63	-	dB
4 Wire Off Hook		50	58	-	dB
Low Frequency Longitudinal Balance	R.E.A. Method, $0°C \leq T_A \leq 75°C$	-	-	23	dBrnC
		-	-	-67	dBm0p

NOTES: 1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceaiblity of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Electrical Specifications (Continued)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Insertion Loss	@1kHz, OdBm Input Level				
2 Wire - 4 Wire		-	±0.05	±0.2	dB
4 Wire - 2 Wire		-	±0.05	±0.2	dB
Frequency Response	200 - 3400Hz Referenced to Absolute Loss at 1kHz and OdBm Signal Level $0^oC \leq T_A \leq 75^oC$	-	±0.02	±0.05	dB
Idle Channel Noise	$0^oC \leq T_A \leq 75^oC$	-			
2 Wire - 4 Wire		-	1	5	dBrnC
		-	-89	-85	dBm0p
4 Wire - 2 Wire		-	1	5	dBrnC
		-	-89	-85	dBm0p
Absolute Delay	$0^oC \leq T_A \leq 75^oC$				
2 Wire - 4 Wire		-	-	2	µs
4 Wire - 2 Wire		-	-	2	µs
Trans Hybrid Loss	Balance Network Set Up for 600 Ohm Termination at 1kHz	36	40	-	dB
Overload Level	$0^oC \leq T_A \leq 75^oC$				
2 Wire - 4 Wire		1.75	-	-	Vpeak
4 Wire - 2 Wire		1.75	-	-	Vpeak
Level Linearity	at 1kHz, $0^oC \leq T_A \leq 75^oC$				
2 Wire - 4 Wire	+3 to -40dBm	-	-	±0.05	dB
	-40 to -50dBm	-	-	±0.1	dB
	-50 to -55dBm	-	-	±0.3	dB
4 Wire - 2 Wire	+3 to -40dBm	-	-	±0.05	dB
	-40 to -50dBm	-	-	±0.1	dB
	-50 to -55dBm	-	-	±0.3	dB
Power Supply Rejection Ratio	$0^oC \leq T_A \leq 75^oC$				
V_B+ to 2 Wire	30 - 60Hz, $R_{LINE} = 600\Omega$	15	-	-	dB
V_B+ to Transmit		15	-	-	dB
V_B- to 2 Wire		15	-	-	dB
V_B- to Transmit		15	-	-	dB
V_B+ to 2 Wire	200 - 16kHz	30	-	-	dB
V_B+ to Transmit	$R_{LINE} = 600\Omega$	30	-	-	dB
V_B- to 2 Wire		30	-	-	dB
V_B- to Transmit		30	-	-	dB
Logic Input Current (RS, $\overline{RC}$, $\overline{PD}$)	$OV \leq VIN \leq 5V$	-	-	±100	µA
Logic Inputs					
Logic '0' V_{IL}		-	-	0.8	Volts
Logic '1' V_{IH}		2.0	-	5.5	Volts
Logic Outputs					
Logic '0' V_{OL}	I_{LOAD} 800µA	-	0.1	0.5	Volts
Logic '1' V_{OH}	ILOAD 80µA	2.7	5.0	5.5	Volts

Uncommitted Op Amp Specifications

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		-	±5	-	mV
Input Offset Current		-	±10	-	nA
Input Bias Current		-	20	-	nA
Differential Input Resistance		-	1	-	MΩ
Output Voltage Swing	RL = 10K	-	±5	-	Vpeak
Output Resistance	$A_{VCL} = 1$	-	10	-	Ω
Small Signal GBW		-	1	-	MHz

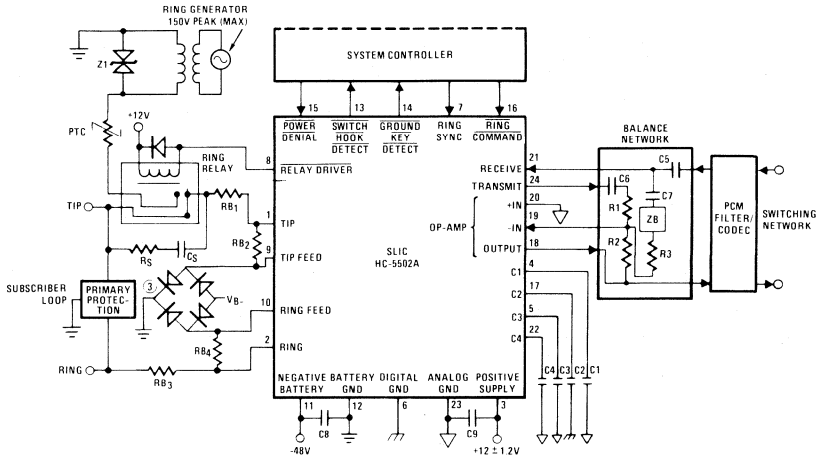
Pin Assiginments HC-5502A

28 PIN PLCC	24 PIN DIP	SYMBOL	DESCRIPTION
2	1	TIP	An analog input connected to the TIP (more positive) side of the subscriber loop through a 150Ω feed resistor and a ring relay. Functions with the Ring terminal to receive voice signals from the telephone and for Loop Monitoring Purposes.
3	2	RING	An analog input connected to the RING (more negative) side of the subscriber loop through a 150Ω feed resistor. Functions with the Tip terminal to receive voice signals from the telephone and for loop monitoring purposes.
4	3	V_B+	Positive Voltage Source - Most positive supply. V_B+ is typically 12 volts with an operational range of 10.8 to 13.2 volts.
5	4	C1	Capacitor #1 - Optional Capacitor used to improve power supply rejection. This pin should be left open if unused.
6	5	C3	Capacitor #3 - An external capacitor to be connected between this terminal and analog ground. Required for proper operation of the loop current limiting function, and for filtering V_B- supply. Typical value is 0.3µF, 30V.
7	6	DG	Digital Ground - To be connected to zero potential and serves as a reference for all digital inputs and outputs on the SLIC.
9	7	RS	Ring Synchronization Input - A TTL - compatible clock input. The clock is arranged such that a positive transition occurs on the negative going zero crossing of the ring voltage source, ensuring that the ring relay is activated and deactivated when the instantaneous ring voltage is near zero. If synchronization is not required, tie to +5V.
10	8	$\overline{RD}$	Relay Driver - A low active open collector logic output. When enabled, the external ring relay is energized.
11	9	TF	Tip Feed - A low inpedance analog output connected to the TIP terminal through a 150Ω feed resistor. Functions with the RF terminal to provide loop current, feed voice signals to the telephone set, and sink longitudinal current.
12	10	RF	Ring Feed - A low impedance analog output connected to the RING terminal through a 150Ω feed resistor. Functions with the TF terminal to provide loop current, feed voice singals to the telephone set, and sink longitudinal currents.
13	11	V_B-	Negative Voltage Source - Most negative supply. V_B- is typically -48 volts with an operational range of -42 to -58 volts. Frequently referred to as "battery".
14	12	BG	Battery Ground - To be connected to zero potential. All loop current and some quiescent current flows into this ground terminal.
16	13	$\overline{SHD}$	Switch Hook Detection - A low active LS TTL - compatible ligic output. This output is enabled for loop currents exceeding 10mA and disabled for loop currents less than 5mA.
17	14	$\overline{GKD}$	Ground Key Detection - A low active LS TTL - compatible logic output. This output is enabled if the DC current into the ring lead exceeds the DC current out of the tip lead by more than 20mA, and disabled if this current difference is less than 10mA.
18	15	$\overline{PD}$	Power Denial - A low active TTL - Compatible logic input. When enabled the switch hook detect ($\overline{SHD}$) and ground key detect ($\overline{GKD}$) are not necessarily valid, and the relay driver, ($\overline{RD}$) output is disabled.
19	16	$\overline{RC}$	Ring Command - A low active TTL - Compatible logic input. When enabled, the relay driver ($\overline{RD}$) output goes low on the next rising edge of the ring sync (RS) input, as long as the SLIC is not in the power denial state ($\overline{PD}$ = 0) or the subecriber is not already off- hook ($\overline{SHD}$ = 0).
20	17	C2	Capacitor #2 - An external capacitor to be connected between this terminal and digital ground. Prevents false ground key indications from occuring durring ring trip detection. Typical value is 0.15µF, 10V. This capacitor is ont used if ground key function is not required.
21	18	OUT	The analog output of the spare operational amplifier.
23	19	-IN	The inverting analog input of the spare operational amplifier.
24	20	+IN	The non-inverting analog input of the spare operational amplifier.
25	21	RX	Receive Input, Four Wire Side - A high inpedance analog input which is internally biased. Capacitive coupling to this input is required. AC signals appearing at this input differentially drive the Tip feed and Ring feed amplifiers, which in turn drive tip and ring through 300 Ohms of feed resistance on each side of the line.
26	22	C4	Capacitor #4 - An external capacitor to be connected between this terminal and analog ground. This capacitor prevents false ground key indication and false ring trip detection from occurring when longitudinal currents are induced onto the subscriber loop from near proximity power lines and other noise sources. This capacitor is also required for the proper operation of ring trip detection. Typical value is 0.5µF, to 1.0µF, 20V. This capicitor should be nonpolarized.
27	23	AG	Analog Ground - To be connected to zero potential and serves as a reference for the transmit output (TX) and receive input (RX) terminals.
28	24	TX	Transmit Output, Four Wire Side - A low impedance analog output which represents the differential voltage across Tip and Ring. Transhybrid balancing must be preformed (using the SLIC microcircuit's spare op amp) beyond this output to completely implement two to four wire conversion. This output is unbalanced and referenced to analog ground. Since the DC level of this output varies with loop current, capacitive coupling to the next stage is essential.
1,8,15,22		NC	No Internal Connection.

NOTE: All grounds (AG, BG, & DG) must be applied before VB+ or VB-. Fallure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first.

Applications Diagram

TYPICAL LINE CIRCUIT APPLICATION WITH THE MONOLITHIC SLIC



TYPICAL COMPONET VALUES

C1 = 0.5µF (Note 1)
C2 = 0.15µF, 10V
C3 = 0.3µF,30V
C4 = 0.5µV to 1.0µF, ±10%, 20V (Should be nonpolarized)
C5 = 0.5µF, 20V
C6 = C7 = 0.5µF (10% Match Required) (Note 2), 20V
C8 = 0.01µF, 100V
C9 = 0.01µF, 20V, ±20%

R1 → R3 = 100kΩ (0.1% Match Required, 1% absolute value), ZB = 0 for 600Ω Terminations (Note 2)
$RB_1 = RB_2 = RB_3 = RB_4 = 150\Omega$ (0.1% Match Required, 1% absolute value)
$R_S = 1k\Omega$, $C_S = 0.1\mu F$, 200V typically, depending on V_{Ring} and line length.
Z1 = 150V to 200V transient protector. PTC used as ring ballast.

NOTE 1: C1 is an optional capacitor used to improve +12V supply rejection. This pin must be left open if unused.

NOTE 2: To obtain the specified transhybrid loss it is necessary for the three legs of the balance network, C6-R1 and R2 and C7-ZB-R3, to match in impedance to within 0.3%. Thus, if C6 and C7 and 1µF each, a 20% match is adequate. It should be noted that the transmit output to C6 see's a -10.5 to -21 volt step when the loop is closed and that too large a value for C6 may produce an excessively long transient at the op amp output to the PCM Filter/CODEC.

A 0.5µF and 100kΩ gives a time constant of 50msec. The uncommitted op amp output is internally clamped to stay within ±5.5V and also has current limiting protection.

NOTE 3: Secondary protection diode bridge recommended is MDA 220 or equivalent.

ADDITIONAL INFORMATION IS CONTAINEDIN APPLICATION NOTE 549, "THE HC-550X TELEPHONE SLICs" BY GEOFF PHILLIPS

Overvoltage Protection and Longitudinal Current Protection

The SLIC device, in conjunction with an external protection bridge, will withstand high voltage lightning surges and power line crosses.

High voltage surge conditions are as specified in Table 1.

The SLIC will withstand longitudinal currents up to a maximum or 30mA RMS, 15mA RMA per leg, without any performance degradation.

TABLE 1

PARAMETER	TEST CONDITION	PEFORMANCE (MAX)	UNITS
Longitudinal Surge	10µs Rise/ 1000µs/Fall	±1000 (Plastic) ±500 (Ceramic)	V Peak V Peak
Metallic Surge	10µs Rise/ 1000µ Fall	±1000 (Plastic) ±500 (Ceramic)	V Peak V Peak
T/GND R/GND	10µs Rise/ 1000µs Fall	±1000 (Plastic) ±500 (Ceramic)	V Peak V Peak
50/60Hz Current T/GND R/GND	700V rms Limited to 10A rms	11	Cycles

HARRIS

HC-5502B

PREVIEW

SLIC
Subsciber Line Interface Circuit

Features

- Pin For Pin Replacement For The HC-5502A With Low Voltage +5V (VB+) Capability
- Monolithic Integrated Device
- DI High Voltage Process
- Compatible With Worldwide PBX Performance Requirements
- Controlled Supply of Battery Feed Current for Short Loops (30mA)
- Internal Ring Relay Driver
- Low Power Consumption During Standby
- Switch Hook, Ground Key and Ring Trip Detection Functions
- Selective Denial of Power to Subscriber Loops

Applications

- Solid State Line Interface Circuit for Analog and Digital PBX Systems
- Direct Inward Dial (DID) Trunks
- Voice Messaging PBX's

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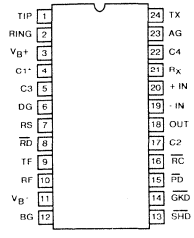
The SLIC also provides selective denial of power. If the PBX system becomes overloaded during an emergency, the SLIC will provide system protection by denying power to selected subscriber loops.

The Harris SLIC is ideally suited for the design of new digital PBX systems, by eliminating bulky hybrid transformers.

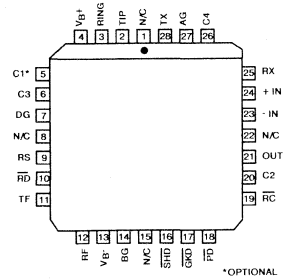
SLIC is available in either a 24 pin Dual-in-Line Plastic or Ceramic package, and a 28 pin PLCC package. The SLIC is also available as unpackaged die.

Pinouts

HC-5502B
(CERAMIC/PLASTIC DIP)
TOP VIEW

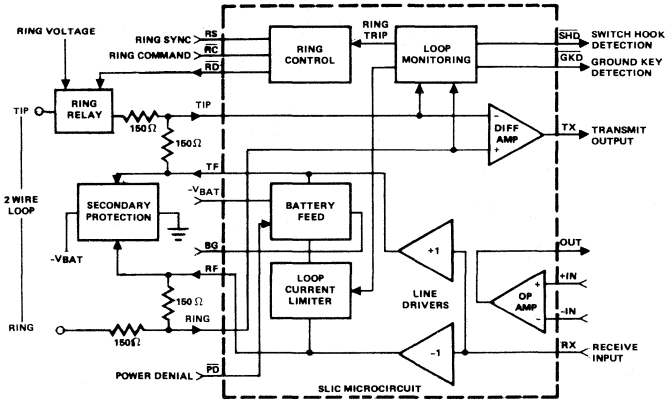


HC-5502B
(PLCC)
TOP VIEW



*OPTIONAL

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

HARRIS

HC-5504

SLIC
Subscriber Line Interface Circuit

Features

- Monolithic Integrated Device
- DI High Voltage Process
- Compatible With Workdwide PBX Performance Requirements
- Controlled Supply of Battery Feed Current for Short Loops (41mA)
- Internal Ring Relay Driver
- Allows Interfacing With Negative Superimposed Ringing Systems
- Low Power Consumption During Standby
- Switch Hook Ground Key and Ring Trip Detection Functions
- Selective Denial of Power to Subscriber Loops

Applications

- Solid State Line Interface Circuit for Analog and Digital PBX Systems
- Direct Inward Dial (DID) Trunks
- Voice Messaging PBXs

Description

The Harris SLIC incorporates many of the BORSHT functions on a single IC chip. This includes DC battery feed, a ring relay driver, supervisory and hybrid functions. This device is designed to maintain transmission performance in the presence of externally induced longitudinal currents.

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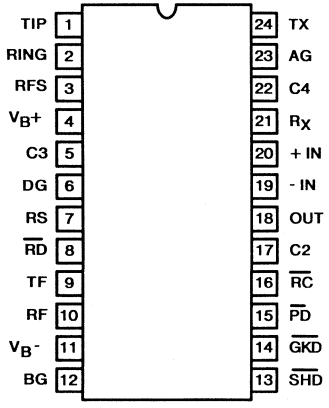
The Harris SLIC is ideally suited for the design of new PBX systems, by eliminating bulky hybrid transformers.

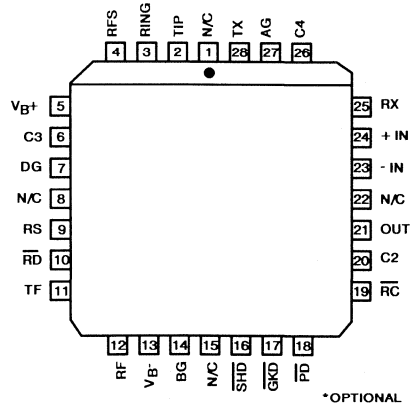
SLIC is available in either a 24 pin Dual-in-Line Plastic or Ceramic package. The SLIC is also available in die form and a 28 pin PLCC package.

Pinouts

HC-5504
(CERAMIC/PLASTIC DIP)
TOP VIEW

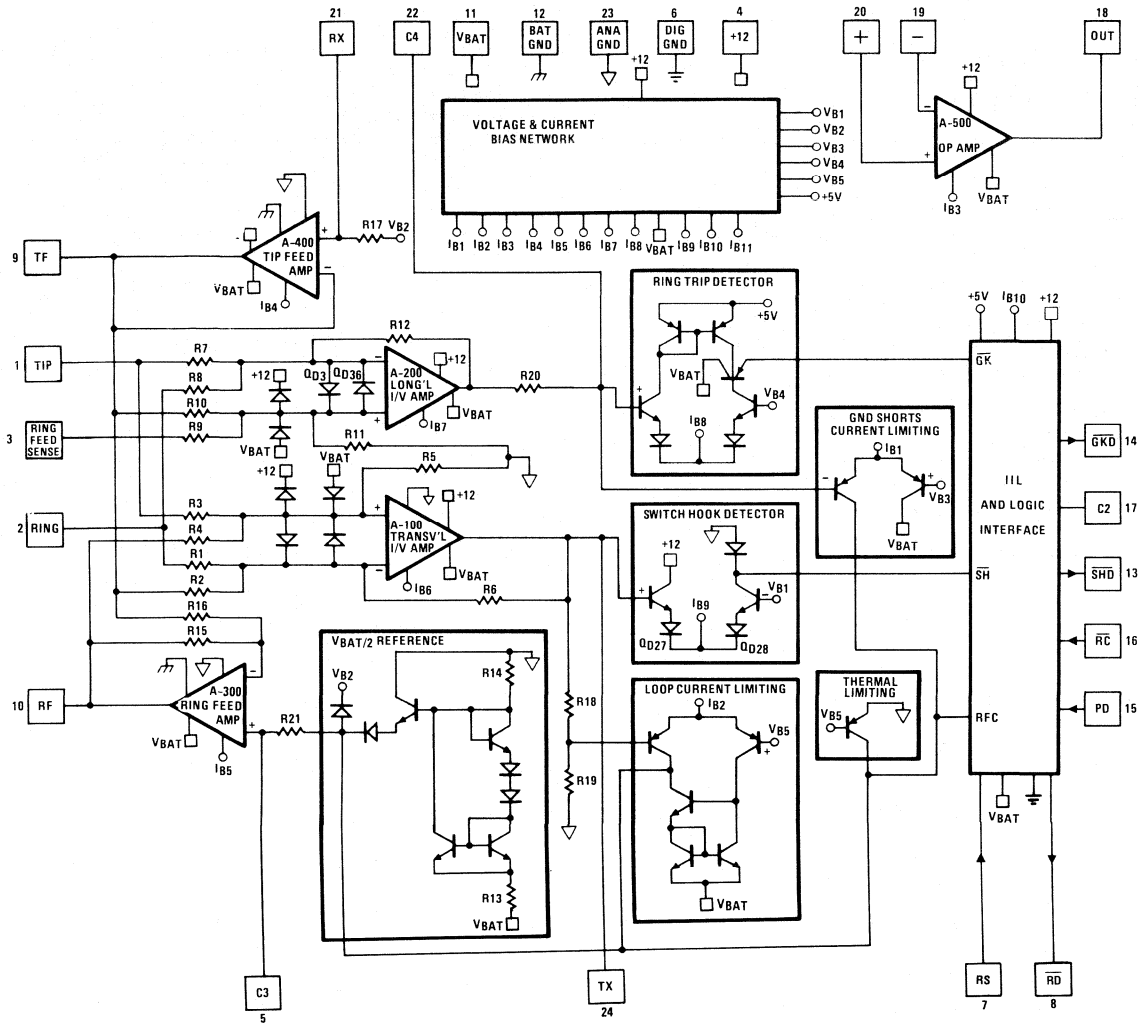


HC4P5504
(PLCC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Schematic



HC-5504 SLIC FUNCTIONAL SCHEMATIC.

Die Characteristics

Transistor Count	181
Diode Count	27
Die Dimensions	169 x 112
Substrate Potential	Unconnected
Process	Bipolar-DI

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
Ceramic DIP	51	16
Plastic DIP	52	24

Absolute Maximum Ratings (Note 1)

Maximum Continuous Supply Voltages (V_B-) ..... -60 to +0.5 V
(V_B+) .... -0.5 to +15 V
($V_B+ - V_B-$) ..... +75V
Relay Drive Voltage (V_{RD}) ..... -0.5 to +15V
Storage Temperature Range ..... -65°C to 150°C
Junction Temperature ..... 175°C

Recommended Operating Conditions

Relay Driver Voltage (V_{RD}) ..... +5 to +12V
Positive Supply Voltage (V_B+) ..... 10.8 to 13.2V
Negative Supply Voltage(V_B-) ..... -42 to -58V
Minimum High Level Logic Input Voltage 2.4V
Maximum Low Level Logic Input Voltage 0.6V
Loop Resistance (R_L) ..... 200 to 1200 Ohms
Operating Temperature Range
HC-5504-5,-7 ..... 0°C to +75°C
HC-5504-9 ..... -40°C to +85°C

Electrical Specifications

Unless Otherwise Specified, V_B- = -48V, V_B+ = +12V, AG = BG = DG = 0V, Typical Parameters +25°C. Min-Max Parameters are Over Operating Temperature Range.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
On Hook Power Dissipation	$I_{Long} = 0$	-	135	174	mW
Off Hook Power Dissipation	$R_{LINE} = 600$ Ohms, $I_{Long} = 0$	-	390	490	mW
Off Hook IB+	$R_{LINE} = 600$ Ohms, $I_{Long} = 0$ @ -40°C	-	-	5.0	mA
Off Hook IB+	$R_{LINE} = 600$ Ohms, $I_{Long} = 0$ @ +25°C	-	-	4.3	mA
Off Hook IB-	$R_{LINE} = 600$ Ohms, $I_{Long} = 0$	-	35	40	mA
Off Hook Loop Current	$R_{LINE} = 1200$ Ohms, $I_{Long} = 0$	-	21	-	mA
Off Hook Loop Current	$R_{LINE} = 1200$ Ohms, $V_B- = -42V$, $I_{Long} = 0$ $T_A = +25°C$	17.5	-	-	mA
Off Hook Loop Current	$R_{LINE} = 200$ Ohms, $I_{Long} = 0$	36	41	48	mA
Fault Currents					
TIP to Ground		-	14	-	mA
RING to Ground		-	63	-	mA
TIP to RING		-	41	-	mA
TIP and RING to Ground		-	63	-	mA
Ring Relay Drive V_{OL}	$I_{OL} = 62$mA	-	0.2	0.5	V
Ring Relay Driver Off Leakage	$V_{RD} = +12V$, RC = 1 = HIGH, $T_A = 25°C$	-	-	100	µA
Ring Rrip Detection Period	$R_{LINE} = 600$ Ohms	-	2	3	Ring Cycles
Switch Hook Detection Threshold	$\overline{SHD} = V_{OL}$	10	-	-	mA
	$\overline{SHD} = V_{OH}$	-	-	5	mA
Ground Key Detection Threshold	$\overline{GKD} = V_{OL}$	20	-	-	mA
	$\overline{GKD} = V_{OH}$	-	-	10	-
Loop Current During Power Denial		-	±2	-	mA
Dial Pulse Distortion		0	-	5	ms
Receive Input Impedance		-	90	-	kOhms
Transmit Output Impedance		-	5	20	Ohms
Two Wire Return Loss	(Return Loss Referenced to 600Ω +2.16µF)				
SRL LO		-	15.5	-	dB
ERL		-	24	-	dB
SRL HI		-	31	-	dB
Longitudinal Balance	1V Peak-Peak 200Hz - 3400Hz $0°C \leq T_A \leq +75°C$				
2 Wire Off Hook		58	65	-	dB
2Wire On Hook		60	63	-	dB
4 Wire Off Hook		50	58	-	dB
Low Frequency Longitudinal Balance	R.E.A. Method, $0°C \leq T_A \leq +75°C$	-	-	23	dBrnC
		-	-	-67	dBm0p

NOTES: 1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceablity of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Electrical Specifications (Continued)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Insertion Loss	@1kHz, OdBm Input Level				
2 Wire - 4 Wire		-	±0.05	±0.2	dB
4 Wire - 2 Wire		-	±0.05	±0.2	dB
Frequency Response	200 - 3400Hz Referenced to Absolute Loss at 1kHz and OdBm Signal Level $0^oC \leq T_A \leq 75^oC$	-	±0.02	±0.05	dB
Idle Channel Noise	$0^oC \leq T_A \leq 75^oC$	-			
2 Wire - 4 Wire		-	1	5	dBrnC
		-	-89	-85	dBm0p
4 Wire - 2 Wire		-	1	5	dBrnC
		-	-89	-85	dBm0p
Absolute Delay	$0^oC \leq T_A \leq 75^oC$				
2 Wire - 4 Wire		-	-	2	µs
4 Wire - 2 Wire		-	-	2	µs
Trans Hybrid Loss	Balance Network Set Up for 600 Ohm Termination at 1kHz	36	40	-	dB
Overload Level	$0^oC \leq T_A \leq 75^oC$				
2 Wire - 4 Wire		1.75	-	-	Vpeak
4 Wire - 2 Wire		1.75	-	-	Vpeak
Level Linearity	at 1kHz, $0^oC \leq T_A \leq 75^oC$				
2 Wire - 4 Wire	+3 to -40dBm	-	-	±0.05	dB
	-40 to -50dBm	-	-	±0.1	dB
	-50 to -55dBm	-	-	±0.3	dB
4 Wire - 2 Wire	+3 to -40dBm	-	-	±0.05	dB
	-40 to -50dBm	-	-	±0.1	dB
	-50 to -55dBm	-	-	±0.3	dB
Power Supply Rejection Ratio	$0^oC \leq T_A \leq 75^oC$				
V_B+ to 2 Wire	30 - 60Hz, $R_{LINE} = 600\Omega$	15	-	-	dB
V_B+ to Transmit		15	-	-	dB
V_B- to 2 Wire		15	-	-	dB
V_B- to Transmit		15	-	-	dB
V_B+ to 2 Wire	200 - 16kHz	30	-	-	dB
V_B+ to Transmit	$R_{LINE} = 600\Omega$	30	-	-	dB
V_B- to 2 Wire		30	-	-	dB
V_B- to Transmit		30	-	-	dB
Logic Input Current (RS, $\overline{RC}$, $\overline{PD}$)	$OV \leq VIN \leq 5V$	-	-	±100	µA
Logic Inputs					
Logic '0' V_{IL}		-	-	0.8	Volts
Logic '1' V_{IH}		2.0	-	5.5	Volts
Logic Outputs					
Logic '0' V_{OL}	I_{LOAD} 800µA	-	0.1	0.5	Volts
Logic '1' V_{OH}	ILOAD 80µA	2.7	5.0	5.5	Volts

Uncommitted Op Amp Specifications

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		-	±5	-	mV
Input Offset Current		-	±10	-	nA
Input Bias Current		-	20	-	nA
Differential Input Resistance		-	1	-	MΩ
Output Voltage Swing	RL = 10K	-	±5	-	Vpeak
Output Resistance	$A_{VCL} = 1$	-	10	-	Ω
Small Signal GBW		-	1	-	MHz

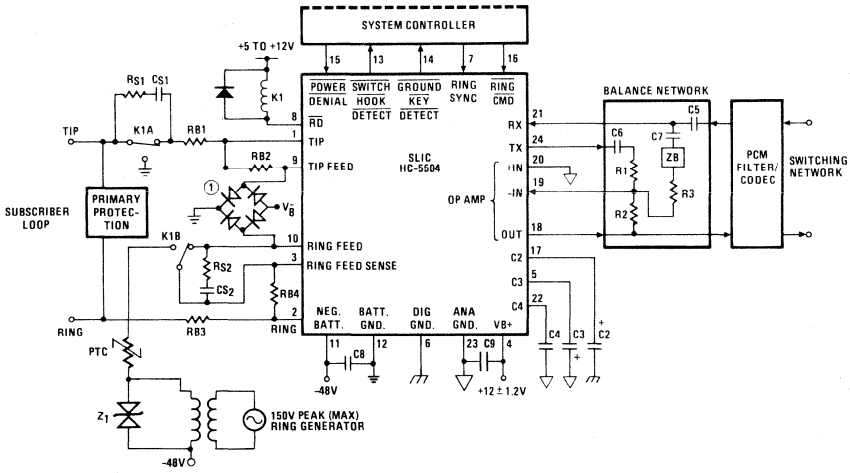
Pin Assiginments HC-5504

28 PIN PLCC	24 PIN DIP	SYMBOL	DESCRIPTION
2	1	TIP	An analog input connected to the TIP (more positive) side of the subscriber loop through a 150Ω feed resistor and a ring relay. Functions with the Ring terminal to receive voice signals from the telephone and for loop monitoring purposes.
3	2	RING	An analog input connected to the RING (more negative) side of the subscriber loop through a 150Ω feed resistor. Functions with the Tip terminal to receive voice signals from the telephone and for loop monitoring purposes.
4	3	RFS	Senses ring side of loop for ground key and ring trip detection. During ringing, the ring signal is inserted into the line at this node and RF is isolated from RFS via a relay.
5	4	V_B+	Positive Voltage Source - Most positive supply. V_B+ is typically 12 volts with an operational range of 10.8 to 13.2 volts.
6	5	C3	Capacitor #3 - An external capacitor to be connected between this terminal and analog ground. Required for proper operation of the loop current limiting function, and for filtering V_B-. Typical value is 0.3μF, 30V.
7	6	DG	Digital Ground - To be connected to zero potential and serves as a reference for all digital inputs and outputs on the SLIC microcircuit.
9	7	RS	Ring Synchronization Input - A TTL - compatible clock input. The clock is arranged such that a positive pulse (50 -500μs) occurs on the zero crossing of the ring voltage source, as it appears at the RFS terminal. For Tip side injected systems,the RS pulse should occur on the negative going zero crossing and for Ring injected systems, on the positive going zero crossing. This ensures that the ring relay activates and deactivates when the instantaneous ring voltage is near zero. If synchronization is not required, the pin should be tied to +5V.
10	8	$\overline{RD}$	Relay Driver - A low active open collector logic output. When enabled, the external ring relay is energized.
11	9	TF	Tip Feed - A low inpedance analog output connected to the TIP terminal through a 150Ω feed resistor. Functions with the RF terminal to provide loop current, feed voice signals to the telephone set, and sink longitudinal current.
12	10	RF	Ring Feed - A low impedance analog output connected to the RING terminal through a 150Ω feed resistor. Functions with the TF terminal to provide loop current, feed voice singals to the telephone set, and sink longitudinal currents.
13	11	V_B-	Negative Voltage Source - Most negative supply. V_B- is typically -48 volts with an operational range of -42 to -58 volts. Frequently referred to as "battery".
14	12	BG	Battery Ground - To be connected to zero potential. All loop current and some quiescent current flows into this ground terminal.
16	13	$\overline{SHD}$	Switch Hook Detection - A low active LS TTL - compatible logic output. This output is enabled for loop currents exceeding 10mA and disabled for loop currents less than 5mA.
17	14	$\overline{GKD}$	Ground Key Detection - A low active LS TTL - compatible logic output. This output is enabled if the DC current into the ring lead exceeds the DC current out of the tip lead by more than 20mA, and disabled if this current difference is less than 10mA.
18	15	$\overline{PD}$	Power Denial - A low active TTL - Compatible logic input. When enabled, the switch hook detect ($\overline{SHD}$) and ground key detect ($\overline{GKD}$) are not necessarily valid, and the relay driver ($\overline{RD}$) output is disabled.
19	16	$\overline{RC}$	Ring Command - A low active TTL - Compatible logic input. When enabled, the relay driver ($\overline{RD}$) output goes low on the next high level of the ring sync (RS) input, as long as the SLIC is not in the power denial state ($\overline{PD}$ = 0) or the subecriber is not already off- hook ($\overline{SHD}$ = 0).
20	17	C2	Capacitor #2 - An external capacitor to be connected between this terminal and digital ground. Prevents false ground key indications from occuring durring ring trip detection. Typical value is 0.15μF, 10V. This capacitor is not used if ground key function is not required and (Pin 17) may be left open or connected to digital ground.
21	18	OUT	The analog output of the spare operational amplifier. The output voltage swing is typically ±5V.
23	19	-IN	The inverting analog input of the spare operational amplifier.
24	20	+IN	The non-inverting analog input of the spare operational amplifier.
25	21	RX	Receive Input, Four Wire Side - A high inpedance analog input which is internally biased. Capacitive coupling to this input is required. AC signals appearing at this input differentially drive the Tip feed and Ring feed terminals, which in turn drive tip and ring through 300 Ohms of feed resistance on each side of the line.
26	22	C4	Capacitor #4 - An external capacitor to be connected between this terminal and analog ground. This capacitor prevents false ground key indication and false ring trip detection from occurring when longitudinal currents are induced onto the subscriber loop from near proximity power lines and other noise sources. This capacitor is also required for the proper operation of ring trip detection. Typical value is 0.5μF, to 1.0μF, 20V. This capicitor should be nonpolarized.
27	23	AG	Analog Ground - To be connected to zero potential and serves as a reference for the transmit output (TX) and receive input (RX) terminals.
28	24	TX	Transmit Output, Four Wire Side - A low impedance analog output which represents the differential voltage across Tip and Ring. Transhybrid balancing must be preformed (using the SLIC microcircuit's spare op amp) beyond this output to completely implement two to four wire conversion. This output is unbalanced and referenced to analog ground. Since the DC level of this output varies with loop current, capacitive coupling to the next stage is essential.
1,8,15,22		NC	No Internal Connection.

NOTE: All grounds (AG, BG, & DG) must be applied before VB+ or VB-. Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first.

Applications Diagram

TYPICAL LINE CIRCUIT APPLICATION WITH THE MONOLITHIC SLIC



TYPICAL COMPONET VALUES

C2 = 0.15µF, 10V
C3 = 0.3µF, 30V
C4 = 0.5µF to 1.0µF, 10%, 20V (Should be nonpolarized)
C5 = 0.5µF, 20V
C6 = C7 = 0.5µF (10% Match Required) (Note 2)
C8 = 0.01µF, 100V
C9 = 0.01µF, 20V, ±20%

R1 = R2 = R3 = 100k (0.1% Match Required, 1% absolute value) ZB = 0 for 600Ω Terminations (Note 2)
$RB_1 = RB_2 = RB_3 = RB_4$ = 150Ω (0.1% Match Required, 1% absolute value)
$R_{S1} = R_{S2}$ =1kΩ, typically.
$C_{S1} = C_{S2}$ = 0.1µF, 200V typically, depending on V_{RING} and line length.
Z_1 = 150V to 200V transient protection.
PTC used as ring generator ballast.

NOTE 1: Secondary protection diode bridge recommended is an MDA 220 or equivalent.

NOTE 2: To obtain the specified transhybrid loss it is necessary for the three legs of the balance network, C6-R1 and R2 and C7-ZB-R3, to match in impedance to within 0.3%. Thus, if C6 and C7 and 1µF each, a 20% match is adequate. It should be noted that the transmit output to C6 see's a -22V step when the loop is closed. Too large a value for C6 may produce an excessively long transient at the op amp output to the PCM Filter/CODEC.

A 0.5µF and 100kΩ gives a time constant of 50msec. The uncommitted op amp output is internally clamped to stay within ±5.5V and also has current limiting protection.

ADDITIONAL INFORMATION IS CONTAINED IN APPLICATION NOTE 549, "THE HC-550X TELEPHONE SLICs" BY GEOFF PHILLIPS

Overvoltage Protection and Longitudinal Current Protection

The SLIC device, in conjunction with an external protection bridge, will withstand high voltage lightning surges and power line crosses.

High voltage surge conditions are as specified in Table 1.

The SLIC will withstand longitudinal currents up to a maximum or 30mA RMS, 15mA RMA per leg, without any performance degradation.

TABLE 1

PARAMETER	TEST CONDITION	PEFORMANCE (MAX)	UNITS
Longitudinal Surge	10µs Rise/ 1000µs/Fall	±1000 (Plastic) ±500 (Ceramic)	V Peak V Peak
Metallic Surge	10µs Rise/ 1000µ Fall	±1000 (Plastic) ±500 (Ceramic)	V Peak V Peak
T/GND R/GND	10µs Rise/ 1000µs Fall	±1000 (Plastic) ±500 (Ceramic)	V Peak V Peak
50/60Hz Current T/GND R/GND	700V rms Limited to 10A rms	11	Cycles

8 TELECOM-MUNICATIONS

HARRIS

HC-5504B

PREVIEW

SLIC
Subscriber Line Interface Circuit

Features

- **Pin for Pin Replacement for the HC-5504 With Added Low Voltage +5V (VB+) Capability**
- **Monolithic Integrated Device**
- **DI High Voltage Process**
- **Compatible With Workdwide PBX Performance Requirements**
- **Controlled Supply of Battery Feed Current for Short Loops (41mA)**
- **Internal Ring Relay Driver**
- **Allows Interfacing With Negative Superimposed Ringing Systems**
- **Low Power Consumption During Standby**
- **Switch Hook Ground Key and Ring Trip Detection Functions**
- **Selective Denial of Power to Subscriber Loops**

Applications

- **Solid State Line Interface Circuit for Analog and Digital PBX Systems**
- **Direct Inward Dial (DID) Trunks**
- **Voice Messaging PBXs**

Description

The Harris SLIC incorporates many of the BORSHT functions on a single IC chip. This includes DC battery feed, a ring relay driver, supervisory and hybrid functions. This device is designed to maintain transmission performance in the presence of externally induced longitudinal currents.

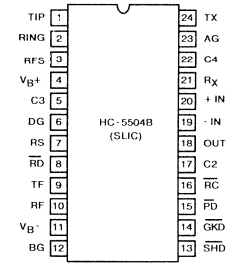
The SLIC also provides selective denial of power. If the PBX system becomes overloaded during an emergency, the SLIC will provide system protection by denying power to selected subscriber loops.

The Harris SLIC is ideally suited for the desigbn of new PBX systems, by eliminating bulky hybrid transformers.

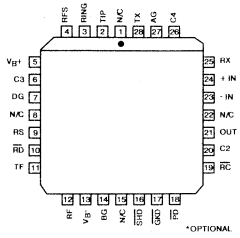
SLIC is available in either a 24 pin Dual-in-Line Plastic or Ceramic package. The SLIC is also available in die form and a 28 pin PLCC package.

Pinouts

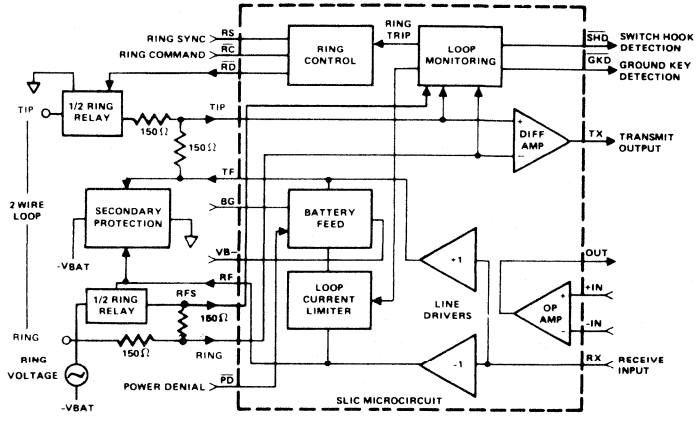
HC-5504B
(CERAMIC/PLASTIC DIP)
TOP VIEW



HC4P5504B
(PLCC)
TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

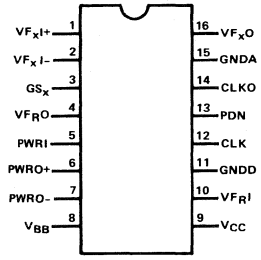
PCM Monolithic Filter

Features

- Exceeds All D3/D4 and CCITT Specifications
- +5V, -5V Power Supplies
- Low Power Consumption:
  - ▸ 45mW (600Ω 0dBm Load)
  - ▸ 30mW (Power Amps Disabled)
- Power Down Mode: 0.5mW
- 20dB Gain Adjust Range
- No External Anti-Aliasing Components
- Sin x/x Correction in Receive Filter
- 50/60Hz Rejection in Transmit Filter
- TTL and CMOS Compatible Logic
- All Inputs Protected Against Static Discharge Due to Handling

Pinout

HC-5512/5512A (CERAMIC DIP)
TOP VIEW



Description

The HC-5512/HC-5512A filter is a monolithic circuit containing both transmit and receive filters specifically designed for PCM CODEC filter applications in 8kHz sampled systems. The HC-5512A has tighter gain specification than the HC-5512.

The filter is manufactured using double-poly silicon gate CMOS technology. Switched capacitor integrators are used to simulate classical LC ladder filters which exhibit low component sensitivity.

Transmit Filter Stage

The transmit filter is a fifth order elliptic low pass filter in series with a fourth order Chebyshev high pass filter. It provides a flat response in the passband and rejection of signals below 200Hz and above 3.4kHz.

Receive Filter Stage

The receive filter is a fifth order elliptic low pass filter designed to reconstruct the voice signal from the decoded/demultiplexed signal which, as a result of the sampling process, is a stairstep signal having the inherent sin x/x frequency response. The receive filter approximates the function required to compensate for the degraded frequency response and restore the flat passband response.

Both PCM filters are ideally suited for use with the HC-5502A, HC-5504, CVSD and PCM CODECS.

Functional Diagram

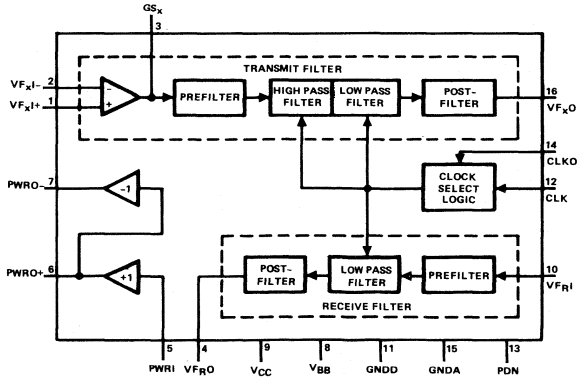


FIGURE 1.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

Absolute Maximum Ratings

Supply Voltages ..... ±7V
Power Dissipation 1W/Package
Input Voltage ..... ±7V
Output Short-Circuit Duration ..... Continuous
Junction Temperature ..... 175°C

Operating Temperature Range
HC-5512/12A-5, -7 ..... 0°C to +75°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering, 10s) ..... 300°C

D.C. Electrical Specifications Unless otherwise specified, typical parameters @ 25°C, Min-Max parameters are over operating temperature range, V_{CC} = 5.0V ± 5%, V_{BB} = -5.0V ± 5%, clock frequency is 1.544MHz. V_{CC} = 5.0V, V_{BB} = -5.0V. Digital interface voltages measured with respect to digital ground, GNDD. Analog voltages measured with respect to analog ground, GNDA.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER DISSIPATION						
I_{CC0}	V_{CC} Standby Current	PDN = V_{DD}, Power Down Mode		50	100	μA
I_{BB0}	V_{BB} Standby Current	PDN = V_{DD}, Power Down Mode		50	100	μA
I_{CC1}	V_{CC} Operating Current	PWRI = V_{BB}, Power Amp Inactive		3.0	4.0	mA
I_{BB1}	V_{BB} Operating Current	PWRI = V_{BB}, Power Amp Inactive		3.0	4.0	mA
I_{CC2}	V_{CC} Operating Current	Note 1		4.6	6.4	mA
I_{BB2}	V_{BB} Operating Current	Note 1		4.6	6.4	mA
DIGITAL INTERFACE						
I_{INC}	Input Current, CLK	$V_{BB} \le V_{IN} \le V_{CC}$	-10		10	μA
I_{INP}	Input Current, PDN	$V_{BB} \le V_{IN} \le V_{CC}$	-100			μA
I_{IN0}	Input Current, CLK0	$V_{BB} \le V_{IN} \le V_{CC}$ -0.5V	-10		-0.1	μA
V_{IL}	Input Low Voltage, CLK, PDN		0		0.8	V
V_{IH}	Input High Voltage, CLK, PDN		2.2		V_{CC}	V
V_{IL0}	Input Low Voltage, CLK0		V_{BB}		V_{BB}+0.5	V
V_{II0}	Input Intermediate Voltage, CLK0		-0.8		0.8	V
V_{IH0}	Input High Voltage, CLK0		V_{CC}-0.5		V_{CC}	V
TRANSMIT INPUT OP AMP						
$IB_x I$	Input Leakage Current, $VF_x I$	$V_{BB} \le VF_x I \le V_{CC}$	-100		100	nA
$RI_x I$	Input Resistance, $VF_x I$	$V_{BB} \le VF_x I \le V_{CC}$	10			MΩ
$VOS_x I$	Input Offset Voltage, $VF_x I$	$-2.5V \le V_{IN} \le +2.5V$	-20		20	mV
V_{CM}	Common-Mode Range, $VF_x I$		-2.5		2.5	V
CMRR	Common-Mode Rejection Ratio	$-2.5V \le V_{IN} \le 2.5V$	60			dB
PSRR	Power Supply Rejection of V_{CC} or V_{BB}		60			dB
R_{OL}	Open Loop Output Resistance, GS_x			1		kΩ
R_L	Minimum Load Resistance, GS_x		10			kΩ
C_L	Maximum Load Capacitance, GS_x				100	pF
$VO_x I$	Output Voltage Swing, GS_x	$R_L \ge 10k$	±2.5			V
A_{VOL}	Open Loop Voltage Gain, GS_x	$R_L \ge 10k$	5,000			V/V
F_c	Open Loop Unity Gain Bandwidth, GS_x			2		MHz

A.C. Electrical Specifications Unless otherwise specified, typical parameters @ 25°C. Min-Max parameters are over operating temperature range. All parameters are specified for a signal level of 0 dBm0 at 1kHz. The 0 dBm0 level is assumed to be 1.54 Vrms measured at the output of the transmit or receive filter.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TRANSMIT FILTER (Transmit filter input op amp set to the non-inverting unity gain mode, with VF_xI = 1.09 Vrms unless otherwise noted.)						
RL_x	Minimum Load Resistance, VF_xO	$-3.2V < V_{OUT} < 3.2V$	10			kΩ
CL_x	Load Capacitance, VF_xO				100	pF
RO_x	Output Resistance, VF_xO			1	3	Ω
PSRR1	V_{CC} Power Supply Rejection, VF_xO	f = 1 kHz, VF_xI+ = 0 Vrms	30			dB
PSRR2	V_{BB} Power Supply Rejection, VF_xO	Same as Above	35			dB
GA_x	Absolute Gain	f = 1 kHz (HC-5512A)	2.9	3.0	3.1	dB
		f = 1 kHz (HC-5512)	2.875	3.0	3.125	dB
GR_x	Gain Relative to GA_x	Below 50 Hz			−35	dB
		50 Hz		−41	−35	dB
		60 Hz		−35	−30	dB
		200 Hz (HC-5512A)	−1.5		0	dB
		200 Hz (HC-5512)	−1.5		0.05	dB
		300 Hz to 3 kHz (HC-5512A)	−0.125		0.125	dB
		300 Hz to 3 kHz (HC-5512)	−0.15		0.15	dB
		3.3 kHz	−0.35		0.03	dB
		3.4 kHz	−0.70		−0.1	dB
		4.0 kHz		−15	−14	dB
		4.6 kHz and Above			−32	dB
DA_x	Absolute Delay at 1 kHz				230	μs
DD_x	Differential Envelope Delay from 1 kHz to 2.6 kHz				60	μs
DP_x1	Single Frequency Distortion Products				−48	dB
DP_x2	Distortion at Maximum-Signal Level	0.16 Vrms, 1 kHz Signal Applied to VF_xI+, Gain = 20 dB, R_L = 10k			−45	dB
NC_x1	Total C Message Noise at VF_xO			2	5	dBrnc0
NC_x2	Total C Message Noise at VF_xO	Gain Setting Op Amp at 20 dB, Non-Inverting, Note 3 T_A = 0°C to 70°C		3	6	dBrnc0
GA_xT	Temperature Coefficient of 1 kHz Gain			0.0004		dB/°C
GA_xS	Supply Voltage Coefficient of 1 kHz Gain	V_{CC} = 5.0V ± 5% V_{BB} = −5.0V ± 5%		0.01		dB/V
CT_{RX}	Crosstalk, Receive to Transmit $20 \log \frac{VF_xO}{VF_RO}$	Receive Filter Output = 2.2 Vrms VF_xI+ = 0 Vrms, f = 0.2 kHz to 3.4 kHz Measure VF_xO			−70	dB
GR_xL	Gaintracking Relative to GA_x	Output Level = +3 dBm0	−0.1		0.1	dB
		+2 dBm0 to −40 dBm0	−0.05		0.05	dB
		−40 dBm0 to −55 dBm0	−0.1		0.1	dB

A.C. Electrical Specifications Unless otherwise specified, typical parameters @ 25°C. Min-Max parameters are over operating temperature range. All parameters are specified for a signal level of 0 dBm0 at 1kHz. The 0 dBm0 level is assumed to be 1.54 Vrms measured at the output of the transmit or receive filter.

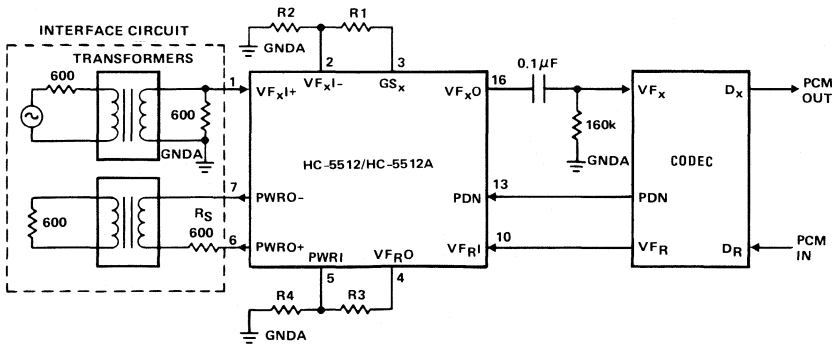
Symbol	Parameter	Conditions	Min	Typ	Max	Units
RECEIVE FILTER (Unless otherwise noted, the receive filter is preceded by a sin x/x filter with an input signal level of 1.54 Vrms.)						
IB_R	Input Leakage Current, VF_RI	$-3.2V \le V_{IN} \le 3.2V$	−100		100	nA
RI_R	Input Resistance, VF_RI		10			MΩ
RO_R	Output Resistance, VF_RO			1	3	Ω
CL_R	Load Capacitance, VF_RO				100	pF
RL_R	Load Resistance, VF_RO		10			kΩ
PSRR3	Power Supply Rejection of V_{CC} or V_{BB}, VF_RO	VF_RI Connected to GNDA f = 1 kHz	35			dB
VOS_RO	Output DC Offset, VF_RO	VF_RI Connected to GNDA	−200		200	mV
GA_R	Absolute Gain	f = 1 kHz (HC-5512A) f = 1 kHz (HC-5512)	−0.1 −0.125	0 0	0.1 0.125	dB dB
GR_R	Gain Relative to Gain at 1 kHz	Below 300 Hz 300 Hz to 3.0 kHz (HC-5512A) 300 Hz to 3.0 kHz (HC-5512) 3.3 kHz 3.4 kHz 4.0 kHz 4.6 kHz and Above	 −0.125 −0.15 −0.35 −0.7		0.125 0.125 0.15 0.03 −0.1 −14 −32	dB dB dB dB dB dB dB
DA_R	Absolute Delay at 1 kHz				100	μs
DD_R	Differential Envelope Delay 1 kHz to 2.6 kHz				100	μs
DP_R1	Single Frequency Distortion Products	f = 1 kHz			−48	dB
DP_R2	Distortion at Maximum Signal Level	2.2 Vrms Input to Sin x/x Filter, f = 1 kHz, R_L = 10k			−45	dB
NC_R	Total C-Message Noise at VF_RO			3	5	dBrnc0
GA_RT	Temperature Coefficient of 1 kHz Gain			0.0004		dB/°C
GA_RS	Supply Voltage Coefficient of 1 kHz Gain			0.01		dB/V
CT_{XR}	Crosstalk, Transmit to Receive $20 \log \frac{VF_RO}{VF_XO}$	Transmit Filter Output = 2.2 Vrms VF_RI = 0 Vrms, f = 0.3 kHz to 3.4 kHz Measure VF_RO			−70	dB
GR_RL	Gaintracking Relative to GA_R	Output Level = +3 dBm0 +2 dBm0 to −40 dBm0 −40 dBm0 to −55 dBm0 Note 5	−0.1 −0.05 −0.1		0.1 0.05 0.1	dB dB dB

A.C. Electrical Specifications Unless otherwise specified, typical parameters @ 25°C. Min-Max parameters are over operating temperature range. All parameters are specified for a signal level of 0 dBm0 at 1kHz. The 0 dBm0 level is assumed to be 1.54 Vrms measured at the output of the transmit or receive filter.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RECEIVE OUTPUT POWER AMPLIFIER						
IBP	Input Leakage Current, PWRI	$-3.2V \leq V_{IN} \leq 3.2V$	0.1		3	μA
RIP	Input Resistance, PWRI		10			MΩ
ROP1	Output Resistance, PWRO +, PWRO –	Amplifiers Active		1		Ω
CLP	Load Capacitance, PWRO +, PWRO –				500	pF
GA_P+	Gain, PWRI to PWRO +	$R_L = 600\Omega$ Connected Between		1		V/V
GA_P-	Gain, PWRI to PWRO –	PWRO + and PWRO –, Input Level = 0 dBm0 (Note 4)		–1		V/V
GR_PL	Gaintracking Relative to 0 dBm0	$V = 2.05$ Vrms, $R_L = 600\Omega$ (Notes 4, 5)	– 0.1		0.1	dB
	Output Level	$V = 1.75$ Vrms, $R_L = 300\Omega$ (Notes 4, 5)	– 0.1		0.1	dB
S/D_P	Signal/Distortion	$V = 2.05$ Vrms, $R_L = 600\Omega$ (Notes 4, 5)			– 45	dB
		$V = 1.75$ Vrms, $R_L = 300\Omega$ (Notes 4, 5)			– 45	dB
VOSP	Output DC Offset, PWRO + PWRO –	PWRI Connected to GNDA	– 50		50	mV
PSRR5	Power Supply Rejection of V_{CC} or V_{BB}	PWRI Connected to GNDA	45			dB

Note 1: Maximum power consumption will depend on the load impedance connected to the power amplifier. The specification listed assumes 0 dBm is delivered to 600Ωconnected from PWRO+ to PWRO–.
Note 2: Voltage input to receive filter at 0V, VF_RO connected to PWRI, 600Ω from PWRO+ to PWRO–. Output measured from PWRO+ to PWRO–.
Note 3: The 0dBm0 level for the filter is assumed to be 1.54 Vrms measured at the output of the XMT or RCV filter.
Note 4: The 0dBm0 level for the power amplifiers is load dependent. For R_L = 600Ω to GNDA the 0dBm0 level is 1.43 Vrms measured at the amplifier output for R_L = 300Ωthe 0dBm0 level is 1.22Vrms.
Note 5: VF_RO connected to PWRI, input signal applied to VF_RI.

Interface Circuit



Note 1: Transmit voltage gain = $\frac{R1 + R2}{R2} \times \sqrt{2}$ (The filter itself introduces a 3dB gain) (R1 +R2 ≥ 10k).

Note 2: Receive gain = $\frac{R4}{R3 + R4}$
(R3 +R4 ≥ 10k)

Note 3: In the configuration shown, the receive filter power amplifiers will drive a 600Ω T to R termination to a signal level of 8.5dBm. An alternative arrangement, using a transformer winding ratio equivalent to 1.414:1 and 300Ω resistor, R_S, will provide a maximum signal level of 10.1dBm across a 600Ω termination impedance.

FIGURE 2.

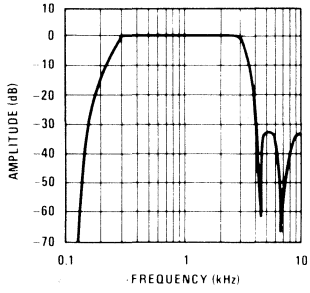
Pin Assignments

Pin No.	Name	Function
1	VF_xI+	The non-inverting input to the transmit filter stage.
2	VF_xI-	The inverting input to the transmit filter stage.
3	GS_x	The output used for gain adjustments of the transmit filter.
4	VF_RO	The low power receive filter output. This pin can directly drive the receive port of an electronic hybrid.
5	PWRI	The input to the receive filter differential power amplifier.
6	PWRO+	The non-inverting output of the receive filter power amplifier. This output can directly interface conventional transformer hybrids.
7	PWRO–	The inverting output of the receive filter power amplifier. This output can be used with PWRO+ to differentially drive a transformer hybrid.
8	V_{BB}	The negative power supply pin. Recommended input is –5V.
9	V_{CC}	The positive power supply pin. The recommended input is 5V.
10	VF_RI	The input pin for the receive filter stage.

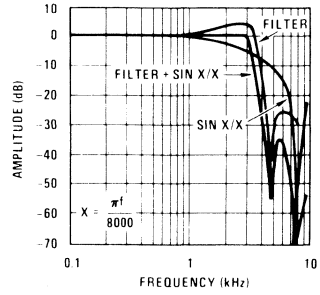
Pin No.	Name	Function
11	GNDD	Digital ground input pin. All digital signals are referenced to this pin.
12	CLK	Master input clock. Input frequency can be selected as 2.048 MHz, 1.544 MHz or 1.536 MHz.
13	PDN	The input pin used to power down the HC-5512/12A during idle periods. Logic 1 (V_{CC}) input voltage causes a power down condition. An internal pull-up is provided.
14	CLK0	This input pin selects internal counters in accordance with the CLK input clock frequency: **CLK** **Connect CLK0 to:** 2048 kHz V_{CC} 1544 kHz GNDD 1536 kHz V_{BB} An internal pull-up is provided.
15	GNDA	Analog ground input pin. All analog signals are referenced to this pin. Not internally connected to GNDD.
16	VF_xO	The output of the transmit filter stage.

Typical Performance Characteristics

Transmit Filter Stage



Receive Filter Stage



Die Characteristics

Transistor Count 815
Die Dimensions ..... 179.9 x 129.1
Substrate Potential ..... +V
Process ..... SAJI CMOS

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
Ceramic DIP	75	15
Ceramic LCC	76	19

Functional Description

The HC-5512/12A monolithic filter contains four main sections; Transmit Filter, Receive Filter, Receive Filter Power Amplifier, and Frequency Divider/ Select Logic *(Figure 1)*. A brief description of the operation for each section is provided below.

Transmit Filter

The input stage of the transmit filter is a CMOS operational amplifier which provides an input resistance of greater than 10MΩ , a voltage gain of greater than 5,000, low power consumption (less than 3mW), high power supply rejection, and is capable of driving a 10kΩ load in parallel with up to 100pF. The inputs and output of the amplifier are accessible for added flexibility. Noninverting mode, inverting mode, or differential amplifier mode operation can be implemented with external resistors. It can also be connected to provide a gain of up to 20dB without degrading the overall filter performance.

The input stage is followed by a prefilter which is a two-pole RC active low pass filter designed to attenuate high frequency noise before the input signal enters the switched-capacitor high pass and low pass filters.

A high pass filter is provided to reject 200Hz or lower noise which may exist in the signal path. The low pass portion of the switched-capacitor filter provides stopband attenuation which exceeds the D3 and D4 specifications as well as the CCITT G712 recommendations.

The output stage of the transmit filter, the postfilter, is also a two-pole RC active low pass filter which attenuates clock frequency noise by at least 40dB. The output of the transmit filter is capable of driving a ±3.2V peak to peak signal into a 10kΩ load in parallel with up to 100pF.

Receive Filter

The input stage of the receive filter is a prefilter which is similar to the transmit prefilter. The prefilter attenuates high frequency noise that may be present on the receive input signal. A switched capacitor low pass filter follows the prefilter to provide the necessary passband flatness, stopband rejection and sin x/x gain correction. A postfilter which is similar to the transmit postfilter follows the low pass stage. It attenuates clock frequency noise and provides a low output impedance capable of directly driving an electronic subscriber-line-interface circuit.

Receive Filter Power Amplifiers

Two power amplifiers are also provided to interface to transformer coupled line circuits. These two amplifiers are driven by the output of the receive postfilter through gain setting resistors, R3, R4 *(Figure 2)*. The power amplifiers can be deactivated, when not required, by connecting the power amplifier input (pin 5) to the negative power supply V_{BB}. This reduces the total filter power consumption by approximately 10mW-20mW depending on output signal amplitude.

Power Down Control

A power down mode is also provided. A logic 1 power down command applied on the PDN pin (pin 13) will reduce the total filter power consumption to less than 1mW. If the PWRI pin (pin 5) is connected to V_{BB}, the power amplifier output will enter a high impedance (tri-state) mode. Otherwise, the power amplifier output will be clamped to V_{BB}.

Frequency Divider and Select Logic Circuit

This circuit divides the external clock frequency down to the switching frequency of the low pass and high pass switched capacitor filters. The divider also contains a TTL-CMOS interface circuit which converts the external TTL clock level to the CMOS logic level required for the divider logic. This interface circuit can also be directly driven by CMOS logic. A frequency select circuit is provided to allow the filter to operate with 2.048MHz, 1.544MHz or 1.536MHz clock frequencies. By connecting the frequency select pin CLK0 (pin 14) to V_{CC}, a 2.048MHz clock input frequency is selected. Digital ground selects 1.544MHz and V_{BB} selects 1.536MHz.

Applications Information

Gain Adjust

(Figure 2) shows the signal path interconnections between the HC-5512/12A and a single channel CODEC. The transmit RC coupling components have been chosen both for minimum passband droop and to present the correct impedance to the CODEC during sampling.

Optimum noise and distortion performance will be obtained for the HC-5512/12A filter when operated with system peak overload voltages of ±2.5V to ±3.2V at VF_XO. When interfacing to a PCM CODEC with a peak overload voltages outside this range, further gain or attenuation may be required.

A gain stage following the transmit filter output and an attenuation stage following the CODEC output are required.

Board Layout

Care must be taken in PCB layout to minimize power supply and ground noise. Analog ground (GNDA) of each filter should be connected to digital ground (GNDD) at a single point, which should be bypassed to both power supplies. Further power supply decoupling adjacent to each filter and CODEC is recommended. Ground loops should be avoided, both between GNDA and GNDD and between the GNDA traces of adjacent filters and CODECs.

HARRIS

HC-5512D

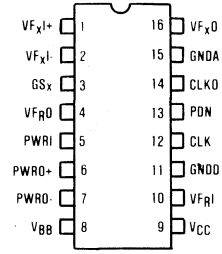
PCM or CVSD Monolithic Filter

Features

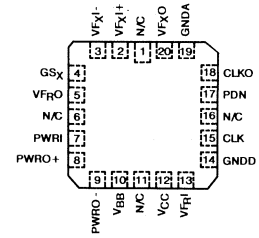
- +5V, -5V Power Supplies
- Low Power Consumption:
  45mW (600Ω 0dBm Load)
  30mW (Power Amps Disabled)
- Power Down Mode: 0.5mW
- No External Anti-Aliasing Components
- Sin x/x Correction in Receive Filter
- 50/60Hz Rejection in Transmit Filter
- TTL and CMOS Compatible Logic
- All Inputs Protected Against Static Discharge Due to Handling
- HC-5512D-2/-8
  Temperature Range..... -55°C to +125°C

Pinouts

HC-5512D (CERAMIC)
TOP VIEW



HC4-5512D (LCC)
TOP VIEW



Description

The HC-5512D filter is a monolithic circuit containing both transmit and receive filters originally designed for PCM CODEC filtering applications in 8kHz sampled systems.

The filter lends itself well as a cost effective replacement of a discrete audio input/output filter for CVSD/PCM/ADPCM/PAM speech filtering. Other applications include telephone line cards, modems and multiplexers.

The HC-5512D is a wider specification version of the HC-5512 that meets high-rel requirements and most D3/D4 and CCITT specifications. To meet the Harris high-rel Dash -8 program (-55°C to+125°C), the HC-5512D undergoes a manufacturing process which requires more test, burn-in and inspection than the HC-5512.

The filter is manufactured using double-poly silicon gate CMOS technology. Switched capacitor integrators are used to simulate classical LC ladder filters which exhibit low component sensitivity.

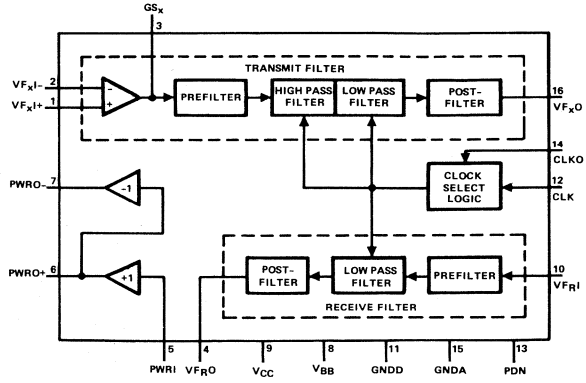
Transmit Filter Stage

The transmit filter is a fifth order elliptic low pass filter in series with a fourth order Chebyshev high pass filter. It provides a flat response in the passband and rejection of signals below 200Hz and above 3.4kHz.

Receive Filter Stage

The receive filter is a fifth order elliptic low pass filter designed to reconstruct the voice signal from the decoded/demultiplexed signal which, as a result of the sampling process, is a stairstep signal having the inherent sin x/x frequency response. The receive filter approximates the function required to compensate for the degraded frequency response and restore the flat passband response.

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow standard IC Handling Procedures.

Absolute Maximum Ratings

Supply Voltages ..... ±7V
Input Voltage ..... ±7V
Output Short-Circuit Duration ..... Continuous
Junction Temperature ..... 175°C

Operating Temperature Range
HC-5512D-2, -8 ..... -55°C to +125°C
HC-5512D -9 ..... -40°C to +85°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C

DC Electrical Specifications

Unless Otherwise Noted, T_A = Operating temperature range for min-max parameters, V_{CC} + 5.0V ±5%, Clock Frequency is 1.544MHz. Typical parameters are specified at T_A = + 25°C, V_{CC} = + 5.0V, V_{BB} = -5.0V. Digital interface voltages measured with respect to digital ground, GNDD. Analog voltages measured with respect to analog ground, GNDA.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
POWER DISSIPATION						
I_{CC0}	V_{CC} Standby Current	PDN = V_{DD}, Power Down Mode		50	200	µA
I_{BB0}	V_{BB} Standby Current	PDN = V_{DD}, Power Down Mode	-200	-50		µA
I_{CC1}	V_{CC} Operating Current	PWRI = V_{BB}, Power Amp Inactive		3.0	7.0	mA
I_{BB1}	V_{BB} Operating Current	PWRI = V_{BB}, Power Amp Inactive	-7.0	-3.0		mA
I_{CC2}	V_{CC} Operating Current	Note 1		4.6	9.0	mA
I_{BB2}	V_{BB} Operating Current	Note 1	-9.0	-4.6		mA
DIGITAL INTERFACE						
I_{INC}	Input Current, CLK	$V_{BB} \leq V_{IN} \leq V_{CC}$	-10		10	µA
I_{INP}	Input Current, PDN	$V_{BB} \leq V_{IN} \leq V_{CC}$	-100		100	µA
I_{IN0}	Input Current, CLK0	$V_{BB} \leq V_{IN} \leq V_{CC}$ - 0.5V	-10		0	µA
V_{IL}	Input Low Voltage, CLK, PDN		0		0.8	V
V_{IH}	Input High Voltage, CLK, PDN		2.2		V_{CC}	V
V_{IL0}	Input Low Voltage, CLK0		V_{BB}		V_{BB} +0.5	V
V_{II0}	Input Intermediate Voltage, CLK0		-0.8		0.8	V
V_{IH0}	Input High Voltage, CLK0		V_{CC} -0.5		V_{CC}	V
TRANSMIT INPUT OP AMP						
$IB_X I$	Input Leakage Current, $VF_X I$	$V_{BB} \leq VF_X I \leq V_{CC}$	-100		100	nA
$RI_X I$	Input Resistance, $VF_X I$	$V_{BB} \leq VF_X I \leq V_{CC}$	10			MΩ
$VOS_X I$	Input Offset Voltage, $VF_X I$	-2.5V ≤ V_{IN} ≤ +2.5V	-20		20	mV
V_{CM}	Common Mode Range, $VF_X I$		-2.5		2.5	V
CMRR	Common Mode Rejection Ratio	-2.5V ≤ V_{IN} ≤ +2.5V	60			dB
PSRR+	Power Supply Rejection of V_{CC}		60			dB
PSRR-	Power Supply Rejection of VBB		60			dB
R_{OL}	Open Loop Output Resistance, GS_X			1		kΩ
R_L	Minimum Load Resistance, GS_X		10			kΩ
C_L	Maximum Load Capacitance, GS_X				100	pF
$VO_X I$	Output Voltage Swing, GS_X	$R_L \geq 10k$	-2.5		2.5	V
A_{VOL}	Open Loop Voltage Gain, GS_X	$R_L \geq 10k$	3000			V/V
F_C	Open Loop Unity Gain Bandwidth, GS_X			2		MHz

A.C. Electrical Specifications Unless otherwise specified, typical parameters @ 25°C. Min-Max parameters are over operating temperature range. All parameters are specified for a signal level of 0 dBm0 at 1kHz. The 0 dBm0 level is assumed to be 1.54 Vrms measured at the output of the transmit or receive filter.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
TRANSMIT FILTER (Transmit filter input op amp set to the noninverting unity gain mode, with VFxI = 1.09Vrms unless otherwise noted)						
RL_X	Minimum Load Resistance	$-3.2V < V_{OUT} < 3.2V$	10			kΩ
CL_X	Load Capacitance, VF_XO				100	pF
RO_X	Output Resistance, VF_XO			1	3	Ω
PSRR1	V_{CC} Power Supply Rejection, VF_XO	f = 1kHz, VF_XI^+ = 0Vrms	30			dB
PSRR2	V_{BB} Power Supply Rejection, VF_XO	Same as above	35			dB
GA_X	Absolute Gain	f = 1kHz	2.8	3.0	3.2	dB
GR_X	Gain Relative to GA_X	Below 50Hz			-35	dB
		50Hz		-41	-35	dB
		60Hz		-35	-30	dB
		200Hz	-1.5		0.15	dB
		300Hz to 3kHz	-0.15		0.15	dB
		3.3kHz	-0.35		0.15	dB
		3.4kHz	-1.0		0.0	dB
		4.0kHz		-15	-10	dB
		4.6kHz and Above			-30	dB
DA_X	Absolute Delay at 1kHz				230	μs
DD_X	Differential Envelope Delay from 1kHz to 2.6kHz				60	μs
DP_X1	Single Frequency Distortion Products				-40	dB
DP_X2	Distortion at Maximum Signal Level Level	0.16Vrms, 1kHz Signal Applied to VF_XI^+, Gain = 20dB, R_L = 10k			-40	dB
NC_X1	Total C Message Noise at VF_XO with V_{IN} = 0				10	dBrnC0
NC_X2	Total C Message Noise at VF_XO with V_{IN} = 0	Gain Setting Op Amp at 20dB, Non-Inverting			10	dBrnC0
GA_XT	Temperature Coefficient of 1kHz Gain			0.0004		dB/°C
GA_XS	Supply Voltage Coefficient of 1kHz Gain			0.01		dB/V
CTR_X	Crosstalk, Receive to Transmit $20 \log \frac{VF_XO}{VF_RO}$	Receive Filter Output = 2.2Vrms VF_XI^+ = 0Vrms, f = 0.2kHz to 3.4kHz Measure VF_XO			-60	dB
GR_XL	Gaintracking Relative to GA_X	Output Level = +3dBm0 to -45dBm0	-0.1		0.1	dB
		-50dBm0	-0.15		0.15	dB
		-55dBm0	-0.25		0.25	dB

A.C. Electrical Specifications Unless otherwise specified, typical parameters @ 25°C. Min-Max parameters are over operating temperature range. All parameters are specified for a signal level of 0 dBm0 at 1kHz. The 0 dBm0 level is assumed to be 1.54 Vrms measured at the output of the transmit or receive filter.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RECEIVE FILTER (Unless otherwise noted, the receive filter is preceded by a sin x/x filter with an input signal level of 1.54Vrms.)						
IB_R	Input Leakage Current, VF_RI	$-2.5V \leq V_{IN} \leq 2.5V$	-100		100	nA
RI_R	Input Resistance, VF_RI		10			MΩ
RO_R	Output Resistance, VF_RO			1	3	Ω
CL_R	Load Capacitance, VF_RO				100	pF
RL_R	Load Resistance, VF_RO		10			kΩ
PSRR3	Power Supply Rejection of V_{CC} or V_{BB}, VF_RO	VF_RI Connected to GNDA f = 1kHz	35			dB
VOS_RO	Output DC Offset, VF_RO	VF_RI Connected to GNDA	-200		200	mV
GA_R	Absolute Gain	f = 1kHz	-0.2	0	0.2	dB
GR_R	Gain Relative to Gain at 1kHz	Below 300Hz			0.125	dB
		300Hz to 3.0kHz	-0.15		0.15	dB
		3.3kHz	-0.5		0.15	dB
		3.4kHz	-1.0		0.0	dB
		4.0kHz			-10	dB
		4.6kHz and Above			-30	dB
DA_R	Absolute Delay at 1kHz				100	μs
DD_R	Differential Envelope Delay 1kHz to 2.6kHz				100	μs
DP_R1	Single Frequency Distortion Products	f = 1kHz			-40	dB
DP_R2	Distortion at Maximum Signal Level	2.2Vrms Input to Sin x/x Filter, f = 1kHz, R_L = 10k			-40	dB
NC_R	Total C-Message Noise at VF_RO				10	dBrnC0
GA_RT	Temperature Coefficient of 1kHz Gain			0.0004		dB/°C
GA_RS	Supply Voltage Coefficient of 1kHz Gain			0.01		dB/V
CT_{XR}	Crosstalk, Transmit to Receive $20 \log \frac{VF_RO}{VF_XO}$	Transmit Filter Output = 2.2Vrms VF_RI = 0Vrms, f = 0.3kHz to 3.4kHz Measure VF_RO			-60	dB
GR_RL	Gaintracking Relative to GA_R	Output Level = +3dBm0 to -45dBm0	-0.1		0.1	dB
		-50 dBm0	-0.15		0.15	dB
		-55 dBm0	-0.25		0.25	dB
		Note 3				

8 TELECOM-MUNICATIONS

A.C. Electrical Specifications Unless otherwise specified, typical parameters @ 25°C. Min-Max parameters are over operating temperature range. All parameters are specified for a signal level of 0 dBm0 at 1kHz. The 0 dBm0 level is assumed to be 1.54 Vrms measured at the output of the transmit or receive filter.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RECEIVE OUTPUT POWER AMPLIFIER						
IBP	Input Leakage Current, PWRI	$-2.5V \leq V_{IN} \leq 2.5V$	0.1		3	μA
RIP	Input Resistance, PWRI		10			MΩ
ROP1	Output Resistance, PWRO + PWRO-	Amplifiers Active		1		Ω
CLP	Load Capacitance, PWRO + PWRO-				500	pF
GAp+	Gain, PWRI to PWRO+	R_L = 600Ω Connected Between		1		V/V
GAp-	Gain, PWRI to PWRO-	PWRO+ and PWRO-		-1		V/V
		Input Level = 0dBm0 (Note 2)				
GRpL	Gaintracking Relative to 0dBm0	V = 2.05Vrms, R_L = 600Ω	-0.1		0.1	dB
	Output Level	V = 1.75Vrms, R_L = 300Ω (Notes 2,3)	-0.1		0.1	dB
S/Dp	Signal/Distortion	V = 2.05Vrms, R_L = 600Ω			-45	dB
		V = 1.75Vrms, R_L = 300Ω (Notes 2,3)			-45	dB
VOSP	Output DC Offset, PWRO + PWRO-	PWRI Connected to GNDA	-50		50	mV
PSRR5	Power Supply Rejection of V_{CC} or V_{BB}	PWRI Connected to GNDA	45			dB

NOTES:
1. Maximum power consumption will depend on the load impedance connected to the power amplifier. The specification listed assumes 0dBm is delivered to 600Ω connected from PWRO+ to PWRO-.
2. The 0dBm0 level for the power amplifiers is load dependent. For R_L = 600Ω to GNDA the 0dBm0 level is 1.43Vrms measured at the amplifier output. For R_L = 300Ω the 0dBm0 level is 1.22Vrms.
3. VF_RO connected to PWRI, input signal applied to VF_RI.

Typical Performance Specifications

TRANSMIT FILTER STAGE

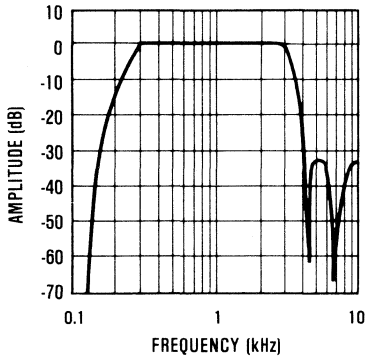


FIGURE 2.

RECEIVE FILTER STAGE

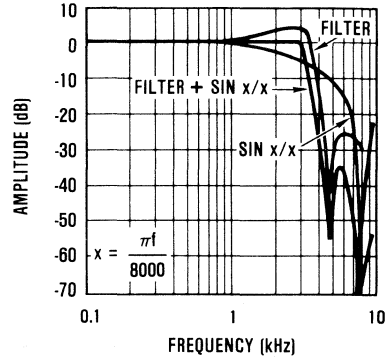


FIGURE 3.

Pin Assignments

PIN # 16-PIN DIP	PIN # 20-PIN LCC	SYMBOL	DESCRIPTION
1	2	VF_XI+	The non-inverting input to the transmit filter stage.
2	3	VF_XI-	The inverting input to the transmit filter stage.
3	4	GS_X	The output used for gain adjustments of the transmit filter.
4	5	VF_RO	The low power receive filter output. This pin can directly drive the receive port of an electronic hybrid.
5	7	PWRI	The input to the receive filter differential power amplifier.
6	8	PWRO+	The non-inverting output of the receive filter power amplifier. This output can directly interface conventional transformer hybrids.
7	9	PWRO-	The inverting output of the receive filter power amplifier. This output can be used with PWRO+ to differentially drive a transformer hybrid.
8	10	V_{BB}	The negative power supply pin. Recommended input is -5V.
9	12	V_{CC}	The positive power supply pin. Recommended input is 5V.
10	13	VF_RI	The input pin for the receive filter stage.
11	14	GNDD	Digital ground input pin. All digital signals are referenced to this pin
12	15	CLK	Master input clock. Input frequency can be selected as 2.048MHz, 1.544MHz or 1.536MHz.
13	17	PDN	The input pin used to power down the HC-5512D during idle periods. Logic 1 (V_{CC}) input voltage causes a power down condition. An internal pull-up is provided.
14	18	CLK0	This input pin selects internal counters in accordance with the CLK input clock frequency: **CLK — Connect CLK0 to:** 2048kHz — VCC 1544kHz — GNDD 1536kHz — VBB An internal pull-up is provided.
15	19	GNDA	Analog ground input pin. All analog signals are referenced to this pin. Not internally connected to GNDD.
16	20	VFxO	The output of the transmit filter stage.
	1, 6, 11, 16	NC	No internal connection is made to these pins.

Die Characteristics

Transistor Count 815
Die Dimensions ..... 180 x 129
Substrate Potential ..... +V
Process ..... SAJI CMOS

Thermal Constants ($^oC/W$)	θ_{ja}	θ_{jc}
Ceramic DIP	75	15
Ceramic LCC	76	19

Functional Description

The HC-5512D monolithic filter contains four main sections; Transmit Filter, Receive Filter, Receive Filter Power Amplifier, and Frequency Divider/Select Logic (Figure 1). A brief description of the operation for each section is provided below.

Transmit Filter

The input stage of the transmit filter is a CMOS operational amplifier which provides an input resistance of greater than 10MΩ, a voltage gain of greater than 3,000, low power consumption (less than 3mW), high power supply rejection, and is capable of driving a 10kΩ load in parallel with up to 100pF. The inputs and output of the amplifier are accessible for added flexibility. Non-inverting mode, inverting mode, or differential amplifier mode operation can be implemented with external resistors. It can also be connected to provide a gain of up to 20dB without degrading the overall filter performance.

The input stage is followed by a prefilter which is a two-pole RC active low pass filter designed to attenuate high frequency noise before the input signal enters the switched-capacitor high pass and low pass filters.

A high pass filter is provided to reject 200Hz or lower noise which may exist in the signal path. The low pass portion of the switched-capacitor filter provides stopband attenuation.

The output stage of the transmit filter, the postfilter, is also a two-pole RC active low pass filter which attenuates clock frequency noise by at least 40dB. The output of the transmit filter is capable of driving a ±2.5V peak to peak signal into a 10kΩ load in parallel with up to 100pF.

Receive Filter

The input stage of the receive filter is a prefilter which is similar to the transmit prefilter. The prefilter attenuates high frequency noise that may be present on the receive input signal. A switched capacitor low pass filter follows the prefilter to provide the necessary passband flatness, stopband rejection and sin x/x gain correction. A postfilter which is similar to the transmit postfilter follows the low pass stage. It attenuates clock frequency noise and provides a low output impedance capable of directly driving an electronic subscriber-line-interface circuit.

Receive Filter Power Amplifiers

Two power amplifiers are also provided to interface to transformer coupled line circuits in PCM applications. These two amplifiers are driven by the output of the receive postfilter through gain setting resistors, R3 and R4 (Figure 4). The power amplifiers can be deactivated, when not required, by connecting the power amplifier input (pin 5) to the negative power supply V_{BB}. This reduces the total filter power consumption by approximately 10mW-20mW depending on output signal amplitude.

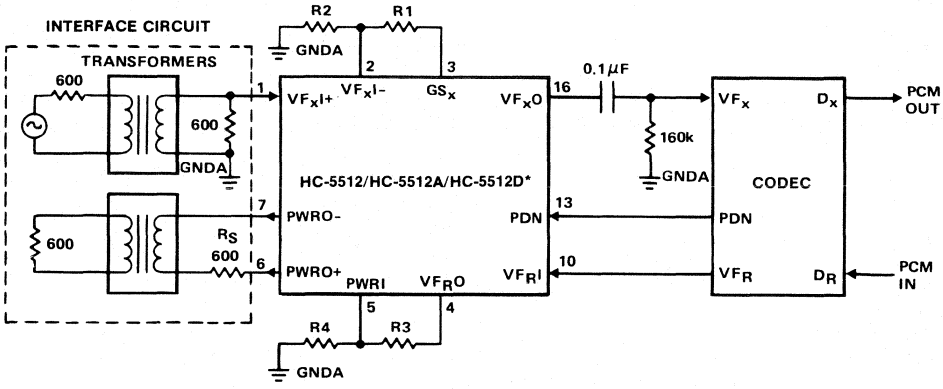
Power Down Control

A power down mode is also provided. A logic 1 power down command applied on the PDN pin (pin 13) will reduce the total filter power consumption to less than 1mW. If the PWRI pin (pin 5) is connected to VBB, the power amplifier output will enter a high impedance (three-state) mode. Otherwise, the power amplifier output will be clamped to V_{BB}.

Frequency Divider and Select Logic Circuit

This circuit divides the external clock frequency down to the switching frequency of the low pass and high pass switched capacitor filters. The divider also contains a TTL-CMOS interface circuit which converts the external TTL clock level to the CMOS logic level required for the divider logic. This interface circuit can also be directly driven by CMOS logic. A frequency select circuit is provided to allow the filter to operate with 2.048MHz, 1.544MHz or 1.536MHz clock frequencies. By connecting the frequency select pin CLKO (pin 14) to VCC, a 2.048MHz clock input frequency is selected. Digital ground selects 1.544MHz and VBB selects 1.536MHz.

Interface Circuit



Note 1. Transmit voltage gain = $\frac{R1 + R2}{R2} \times \sqrt{2}$ (The filter itself introduces a 3dB gain) (R1 + R2 ≥ 10k).

Note 2. Receive gain $\frac{R4}{R3 + R4}$
(R3 + R4 ≥ 10k)

Note 3. In the configuration shown, the receive filter power amplifiers will drive a 600Ω T to R termination to a signal level of 8.5dBm. An alternative arrangement, using a transformer winding ratio equivalent to 1.414:1 and 300Ω resistor, R_S, will provide a maximum signal level of 10.1dBm across a 600Ω termination impedance.

*Note 4. The HC-5512D may be used in some PCM telephone applications, it does meet most CCITT and D3/D4 specifications for PCM telephone transmission systems.

FIGURE 4.

Interface Circuit for HC-55564 CVSD

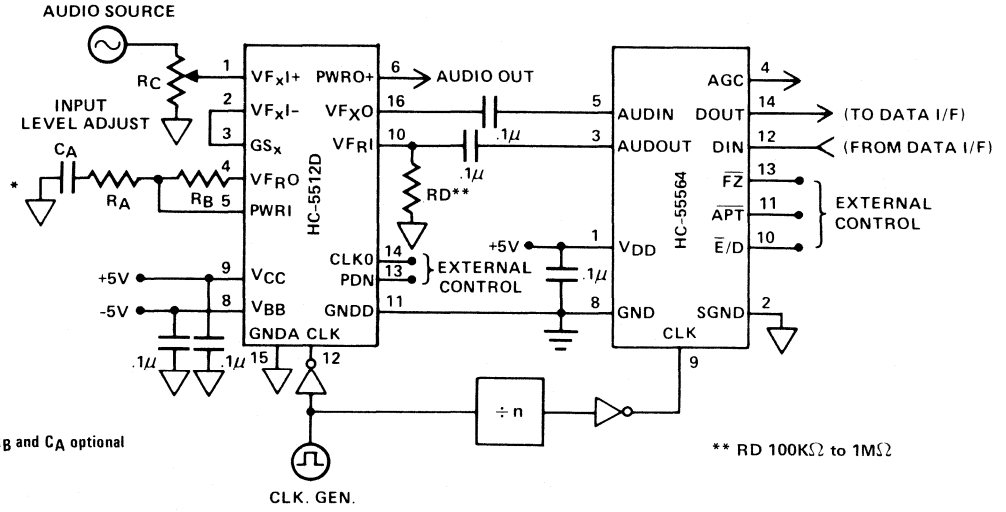


FIGURE 5.

Applications Information

Gain Adjust

Figure 4 shows the signal path interconnections between the HC-5512D and a single channel CODEC. The transmit RC coupling components have been chosen both for minimum passband droop and to present the correct impedance to the CODEC during sampling.

Figure 5 shows the signal path interconnections between the HC-5512D and the HC-55564 CVSD. For the circuit shown, the audio signal into the CVSD should be 1Vp-p over the 3.2kHz band to obtain a flat response. R_A, R_B and C_A form a simple lead/lag filter at the output of the HC-5512D receive filter which introduces a pole and a zero at 3.3kHz to help compensate against the filters' inherent sin x/x characteristic. (See Figure 3). Note that the transmit side of the filter provides an inherent +3dB voltage gain, and the resistor RD, at VFRI causes a voltage loss from audio out to VFRI, owing to the 100kΩ output impedance of the CVSD at audio out. Generally, the higher the RD value used, the more thermal noise introduced to the circuit.

Optimum noise and distortion performance will be obtained for the HC-5512D filter when operated with system peak overload voltages of ±2.5V to ±3.2 at VF_XO and VF_RO. When interfacing to a PCM CODEC or CVSD with a peak overload voltage outside this range, further gain or attenuation may be required.

For example, the HC-5512/12A/12D filter can be used with the CODEC which has a 5.5V peak overload voltage, or with the HC-55564 CVSD which has a 4.0V peak overload voltage. A gain stage following the transmit filter output and an attenuation stage following the CODEC or CVSD output are required in this case.

Board Layout

Care must be taken in PCB layout to minimize power supply and ground noise. Analog ground of each filter and each CVSD should be connected to digital ground at a single point, which should be bypassed to both power supplies. Further power supply decoupling adjacent to each filter and CODEC, and each filter and CVSD is recommended. Ground loops should be avoided between GNDA and GNDD, between the GNDA traces of adjacent filters and CODECs, and between the analog ground traces of adjacent filters and CVSDs.

HC-55536

Continuous Variable Slope Delta Demodulator (CVSD)

Features

- ALL DIGITAL
- REQUIRES FEWER EXTERNAL PARTS
- LOW POWER DRAIN: 1.5mW FROM SINGLE 3.0-7.0V SUPPLY
- TIME CONSTANTS DETERMINED BY CLOCK FREQUENCY; NO CALIBRATION OR DRIFT PROBLEMS; AUTOMATIC OFFSET ADJUSTMENT
- FILTER RESET BY DIGITAL CONTROL
- AUTOMATIC OVERLOAD RECOVERY
- AUTOMATIC "QUIET" PATTERN GENERATION

Applications

- VOICE DECODER FOR DIGITAL SYSTEMS AND SPEECH SYNTHESES
- VOICE MAIN
- AUDIO MANIPULATIONS; DELAY LINES, ECHO GENERATION/SUPPRESSION, SPECIAL EFFECTS, ETC.
- PAGERS/SATELLITES

Description

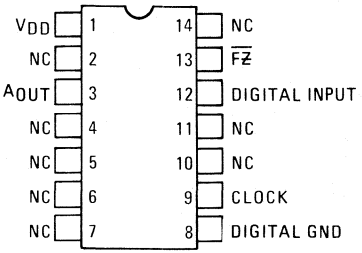
The HC-55536 is a CMOS integrated circuit used to convert serial NRZ digital data to an analog (voice) signal. Conversion is by delta demodulation, using the Continuously Variable Slope (CVSD) method of demodulation.

While signals are compatible with other CVSD circuits, the internal design is unique. The analog loop filters have been replaced by digital filters which use very low power and require no external timing components. This digital approach allows inclusion of many desirable features, which otherwise would be difficult to inplement. The device is usable from 9K bits/sec. to above 64K bits/sec.,and may be easily configured with the HC-55564 CVSD for a complete transmit/receive voice channel.

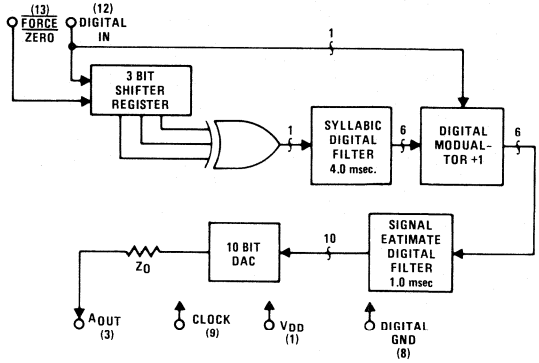
The HC-55536 is available in a 14 pin ceramic DIP package.

Pinout

HC-55536 (CERAMIC DIP)
TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow standard IC Handling Procedures.

Absolute Maximum Ratings

Voltage at Any Pin ..... GND -0.3V to V_{DD} +0.3V
Maximum V_{DD} Voltage ..... +7.0V
Minimum V_{DD} Voltage ..... +3.0V
Operating V_{DD} Range ..... +3.0V to +7.0V
Junction Temperature ..... 175°C

Operating Temperature Ranges
HC-55536-5 ..... 0°C to +75°C
HC-55536-9 ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C

Electrical Specifications

Unless Otherwise Specified: V_{DD} = +5.0V; Bit Range = 16K Bits/sec; typical parameters are at +25°C. Min-Max parameters are over operating temperature.

PARAMETER	MIN	TYP	MAX	UNIT	NOTE
Clock Sampling Rate	9	16	64	Kbps	(1)
Clock Duty Cycle	30		70	%	
Supply Voltage	+3.0		+7.0	V	
Supply Current		0.3	1.5	mA	
Logic "1" Input, V_{IH}	3.5	4.5		V	(2)
Logic "0" Input , V_{IL}			1.5	V	(2)
Audio Output Voltage		0.5	1.2	V_{rms}	(3)
Audio Output Impedance		150		kΩ	(4)
Syllabic Filter Time Constant		4.0		ms	(5)
L.P. Signal estimate Filter Time Conatant		1.0		ms	(5)
Step Size Ratio		24		dB	(6)
Resolution		0.1		%	(7)
Minimum Step Size		0.2		%	(8)
Signal/Noise Ratio	25			dB	
Quieting Pattern Amplitude		10		mV_{p-p}	(9)
Clamping Threshold		0.75		F.S.	(11)

NOTES:

1. There is one NRZ data bit per clock period. Clock must be phased with digital data such that a positive clock transition occurs in the middle of each received data bit. Clock may be run at greater than 64Kbps or less than 9Kbps.
2. Logic inputs are CMOS compatible at supply voltage and are diode protected. Digital data input is NRZ at clock rate and changes with negative clock transitions.
3. This output includes a DC bias of $V_{DD}/2$; therefore, an AC coupling capacitor is required unless the output filter also includes this bias.
4. Presents approximately 150KΩ in series with recovered audio voltage. Zero-signal reference is $V_{DD}/2$.
5. Note that filter time cinstants are inversely proportional to clock rate. Both filters approximate single pole responses.
6. Step size compression ratio of the syllabic filter is defined as the ratio of the filter output, with an equal 1-0 bit density input to the filter, to its minimum output.
7. Minimum quantization voltage level expressed as a percentage of supply voltage.
8. The minimum step size between levels is twice the resolution.
9. The"quieting" pattern or idle-channel audio output steps at ½ the bit rate, changing state on negative clock transitions.
10. The recovered signal will be clamped, and the computation will be inhibited, when the recovered singal reaches three-quarters of full-scale value, and will unclamp when it falls below this value (positive or negative).

FIG. 1. Illustrates the frequency response of the HC-55536 for varying input levels. To prevent slope overload (slew rate limiting) do not exceed the 0dB boundary. The frequency response is directly proportional to the sampling rate. The output levels were measured after filtering.

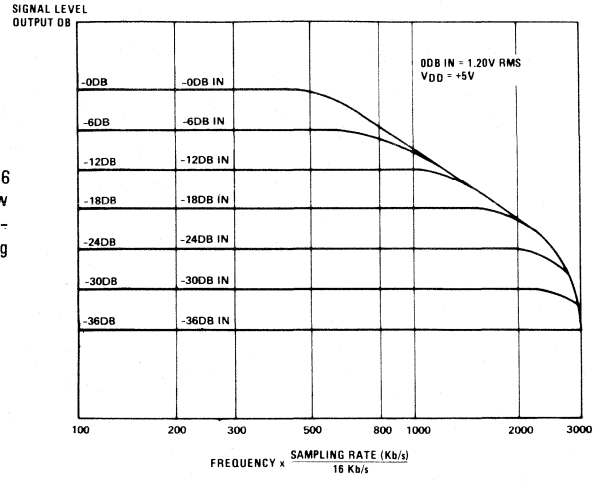


FIGURE 1 - TRANSFER FUNCTION FOR CVSD AT 16Kbps

Die Characteristics

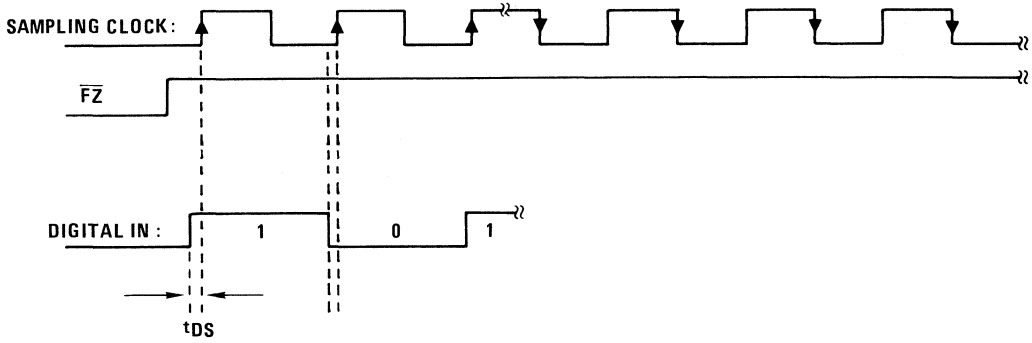
Transistor Count		1790
Die Dimensions		154 x 93
Substrate Potential		+V
Process		SAJI CMOS
Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
Ceramic DIP, HC-55536	75	15

Pin Description

PIN NO. 14-LEAD DIP	SYMBOL	DESCRIPTION
1	V_{DD}	Positive supply voltage.
2	N.C.	No internal connection is made to this pin.
3	Audio Out	Recovered audio out. Presents approximately 150KΩ source with DC offset of $V_{DD}/2$ should be externally AC couples.
4	N.C.	No internal connection is made to this pin.
5	N.C.	No internal connection is made to this pin.
6, 7	N.C.	No internal connection is made to these pins.
8	Digital GND.	Logic Ground.
9	Clock	Sampling rote clock must be synchronized with the digital input data such that the data is valid at the positive clock transition.
10	N.C.	No internal connection is made to this pin.
11	N.C.	No internal connection is made to this pin.
12	Digital In	Input for the received serial NRZ digital data.
13	$\overline{FZ}$	Active low logic input. Activating this input resets the internal logic and forces the recovered audio output into the "quieting" condition.
14	N.C.	No internal connection is made to this pin.

NOTE: No active input should be left in a "floating condition".

Timing Waveforms



tDS : DATA SET UP TIME 100ns TYPICAL

FIGURE 2 – CVSD TIMING DIAGRAM

HC-55564

Continuously Variable Slope Delta-modulator (CVSD)

Features

- All Digital
- Requires Few External Parts
- Low Power Drain: 1.5mW Typical From Single 3.0V-7V Supply
- Time Constants Determined by Clock Frequency; No Calibration or Drift Problems; Automatic Offset Adjustment
- Half Duplex Operation Under Digital Control
- Filter Reset Under Digital Control
- Automatic Overload Recovery
- Automatic "Quiet" Pattern Generation
- AGC Control Signal Available

Applications

- Voice Transmission Over Data Channels (Modems)
- Voice/Data Multiplexing (Pair Gain)
- Voice Encryption/Scrambling
- Voicemail
- Audio Manipulations: Delay Lines, Time Compression, Echo Generation/Suppression, Special Effects, Etc.
- Pagers/Satellites
- Data Aquisition Systems
- Voice I/O For Digital Systems and Speech Synthesis Requiring Small Size, Low Weight, and Ease of Reprogrammability

Description

The HC-55564 is a half duplex modulator/demodulator CMOS integrated circuit used to convert voice signals into serial NRZ digital data and to reconvert that data into voice. The conversion is by delta-modulation, using the Continuously Variable Slope (CVSD) method of modulation/de-modulation.

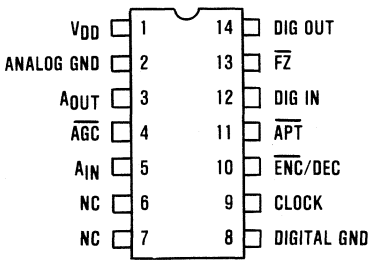
While the signals are compatible with other CVSD circuits, the internal design is unique. The analog loop filters have been replaced by very low power digital filters which require no external timing components. This approach allows inclusion of many desirable features which would be difficult to implement using other approaches.

The fundamental advantages of delta-modulation, along with its simplicity and serial data format, provide an efficient (low data rate/low memory requirements) method for voice digitization. The device may be easily configured with the HC-5512/12A/12D PCM/CVSD filter.

The HC-55564 is usable from 9K bits/sec to above 64Kbps. The unit is available in a 14 pin Ceramic DIP, in commercial 0°C to +75°C and industrial -40°C to +85°C, temperature ranges, including the Harris High Rel Dash 7 program and MIL-STD-883. Application Notes 607 and 576 are available.

Pinout

HC-55564
TOP VIEW



Functional Diagram

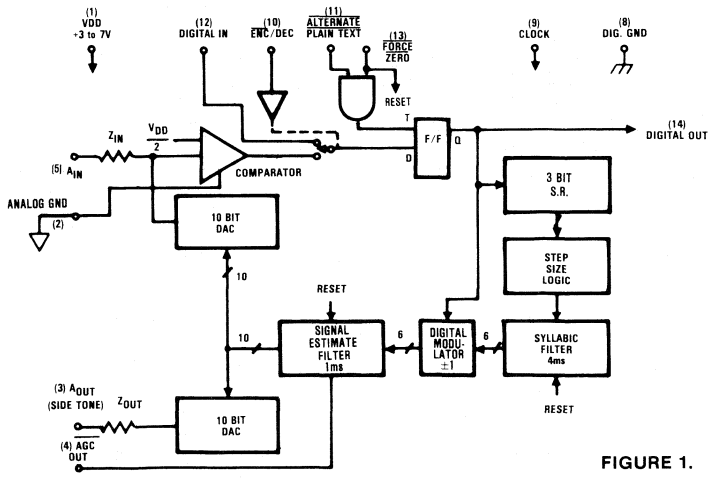


FIGURE 1.

Pin Assignments

PIN # 14-PIN DIP	SYMBOL	DESCRIPTION
1	V_{DD}	Positive supply voltage. Voltage range is +3.0V to +7.0V.
2	Analog Gnd	Analog Ground connection to D/A ladders and comparator.
3	A_{OUT}	Audio Out recovered from 10 bit DAC. May be used as side tone at the transmitter. Presents approximately 150 kilohm source with DC offset of $V_{DD}/2$. Within ±2dB of Audio Input. Should be externally AC coupled.
4	$\overline{AGC}$	Automatic Gain Control output. A logic low level will appear at this output when the recovered signal excursion reaches one-half of full scale value. In each half cycle full scale is $V_{DD}/2$. The mark-space ratio is proportional to the average signal level.
5	A_{IN}	Audio Input to comparator. Should be externally AC coupled. Presents approximately 280 kilohms in series with $V_{DD}/2$.
6,7	NC	No internal connection is made to these pins.
8	Digital Gnd	Logic ground. 0V reference for all logic inputs and outputs
9	Clock	Sampling rate clock. In the decode mode, must be synchronized with the digital input data such that the data is valid at the positive clock transition. In the encode mode, the digital data is clocked out on the negative going clock transition. The clock rate equals the data rate.
10	$\overline{Encode}$/ Decode	A single CVSD can provide half-duplex operation. The encode or decode function is selected by the logic level applied to this input. A low level selects the encode mode, a high level the decode mode.
11	$\overline{APT}$	Alternate Plain Text input. Activating this input causes a digital quieting pattern to be transmitted, however; internally the CVSD is still functional and a signal is still available at the A_{OUT} port. Active low.
12	Digital In	Input for the received digital NRZ data.
13	$\overline{FZ}$	Force Zero input. Activating this input resets the internal logic and forces the digital output and the recovered audio output into the "quieting" condition. An alternating 1-0 pattern appears at the digital output at ½ the clock rate. When this is decoded by a receive CVSD, a 10mVp-p inaudible signal appears at audio output. Active low.
14	Digital Out	Output for transmitted digital NRZ data.

NOTE: No active input should be left in a "floating condition."

Absolute Maximum Ratings

Voltage at Any Pin ..... GND -0.3V to V_{DD} +0.3V
Maximum V_{DD} Voltage ..... +7.0V
Minimum V_{DD} Voltage ..... +3.0V
Operating V_{DD} Range ..... +3.0V to +7.0V
Junction Temperature ..... 175°C

Operating Temperature Ranges
HC-55564-5, -7 ..... 0°C to +75°C
HC-55564-9 ..... -40°C to +85°C
HC-55564-2 ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C

Electrical Specifications

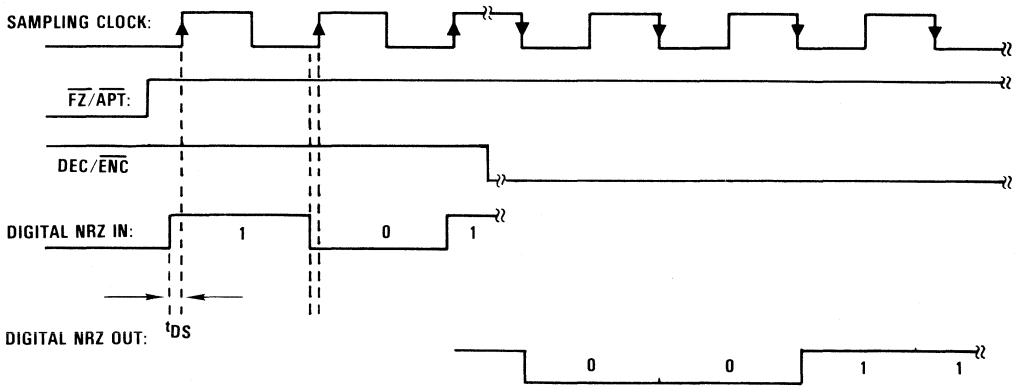
Unless Otherwise Specified, typical parameters are at +25°C, min-max are over operating temperature ranges, V_{DD} = +5.0V, Sampling Rate = 16Kbps, AG = DG = 0V, A_{IN} = 1.2Vrms.

SYMBOL	PARAMETER	MIN	TYPICAL	MAX	UNITS	CONDITIONS
CLK	Sampling Rate	9	16	64	Kbps	Note 1
I_{DD}	Supply Current		0.3	1.5	mA	
V_{IH}	Logic '1' Input	3.5			V	Note 2
V_{IL}	Logic '0' Input			1.5	V	Note 2
V_{OH}	Logic '1' Output	4.0			V	Note 3
V_{OL}	Logic '0' Output			0.4	V	Note 3
	Clock Duty Cycle	30		70	%	
A_{IN}	Audio Input Voltage		0.5	1.2	Vrms	AC coupled. Note 4
A_{OUT}	Audio Output Voltage		0.5	1.2	Vrms	AC coupled. Note 5
Z_{IN}	Audio Input Impedance		280		kΩ	Note 6
Z_{OUT}	Audio Output Impedance		150		kΩ	Note 6
A_{E-D}	Transfer Gain	-2.0		+2.0	dB	No Load. Audio In to Audio Out.
A_E	Encode Gain		.34		dB	
A_D	Decode Gain		1.23		dB	
t_{SF}	Syllabic Filter Time Constant		4.0		mS	Note 7
t_{SE}	Signal Estimate Filter Time Constant	1.0			mS	Note 7
	Resolution		0.1		%	Note 8
	Minimum Step Size		0.2		%	Note 9
V_{QP}	Quieting Pattern Amplitude		10		mVp-p	$\overline{FZ}$ = 0V or $\overline{APT}$ = 0V, or A_{IN} = 0V. Note 10, 13
V_{ATH}	AGC Threshold		0.5		F.S.	Note 11
V_{CTH}	Clamping Threshold		0.75		F.S.	Note 12

NOTES:

1. There is one NRZ (Non-Return Zero) data bit per clock period. Data is clocked out on the negative clock edge. Data is clocked into the CVSD on the positive going edge (see Figure 2). Clock may be run at less than 9Kbps and greater than 64Kbps.
2. Logic inputs are CMOS compatible at supply voltage and are diode protected. Digital data input is NRZ at clock rate.
3. Logic outputs are CMOS compatible at supply voltage and will withstand short-circuits to V_{DD} or ground. Digital data output is NRZ and changes with negative clock transitions. Each output will drive one LS TTL load.
4. Recommended voice input range for best voice performance. Should be externally AC coupled.
5. May be used for side-tone in encode mode. Should be externally AC coupled. Varies with aduio input level by ±dB.
6. Presents series impedance with audio signal. Zero signal reference is approximatey $V_{DD}/2$.
7. Note that filter time constants are inversely proportional to clock rate. Both filters approximate single pole responses.
8. Minimum quantization voltage level expressed as a percentage of supply voltage.
9. The minimum step size between levels is twice the resolution.
10. The "quieting" pattern or idle-channel audio output steps at one-half the bit rate, changing state on negative clock transitions.
11. A logic "0" will appear at the AGC output pin when the recovered signal reaches one-half of full-scale value (positive or negative), i.e. at $V_{DD}/2$ ±25% of V_{DD}.
12. The recovered signal will be clamped, and the computation will be inhibited, when the recovered signal reaches three-quarters of full-scale value, and will unclamp when it falls below this value (positive or negative).
13. Typical encoding threshold for quieting pattern generation is 6.5mVrms at 1kHz input signal, 16kHz clock. The threshold varies inversly with input frequency and proportionally with clock frequency.

Timing Waveforms



t_{DS}: DATA SET UP TIME, 100ns TYPICAL

FIGURE 2. CVSD TIMING DIAGRAM

Die Characteristics

Transistor Count 1896
Die Dimensions ..... 154 x 93
Substrate Potential ..... +V
Process ..... SAJI CMOS

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
Ceramic DIP	75	15
Ceramic LCC	76	19

Interface Circuit for HC-55564 CVSD

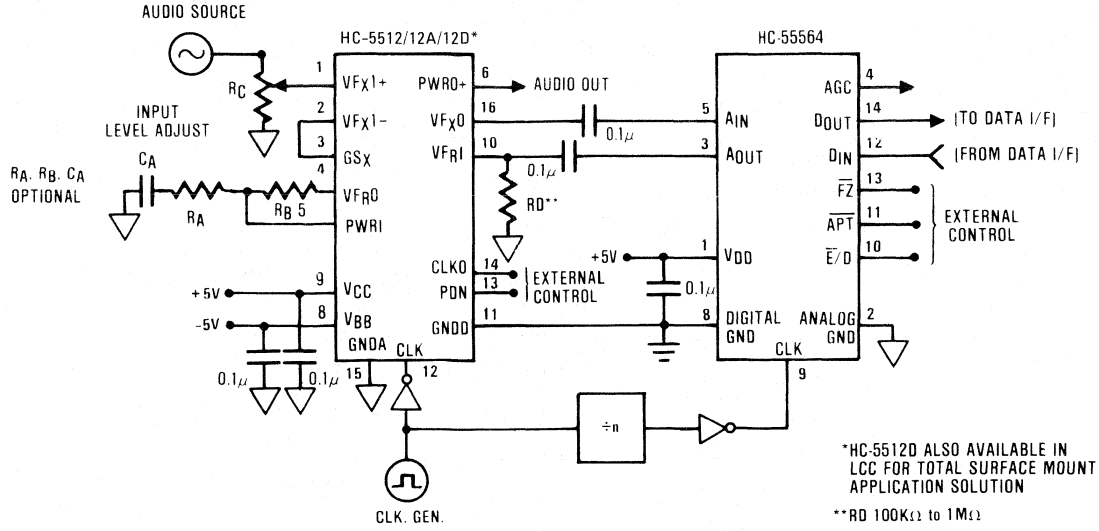
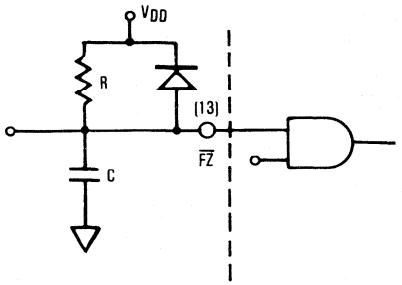


FIGURE 3.

CVSD Hookup for Evaluation

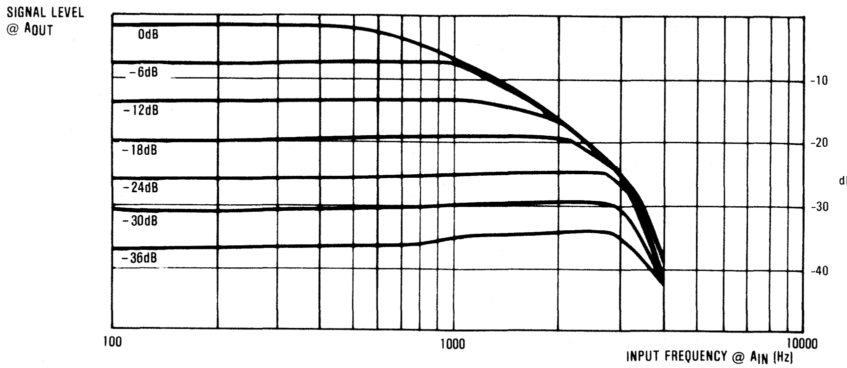
The circuit in Figure 3 is sufficient to evaluate the voice quality of the CVSD, since when encoding the feedback signal at the audio output pin is the reconstructed audio input signal. CVSD design considerations are as follows;

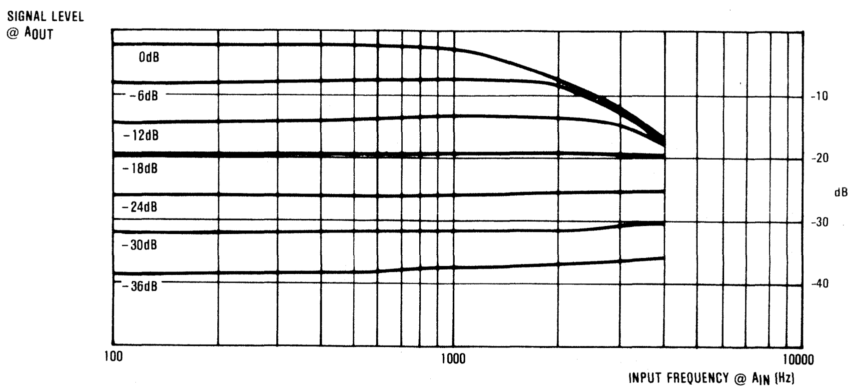
1) Care should be taken in layout to maintain isolation between analog and digital signal paths for proper noise consideration.
2) Power supply decoupling is necessary as close to the device as possible. A 0.1uf should be sufficient.
3) Ground, then power, must be present before any input signals are applied to the CVSD. Failure to observe this may cause a latchup condition which may be destructive. Latchup may be removed by cycling the power off/on. A power-up reset circuit may be used that strobes Force Zero (Pin 13) during power-up as follows:

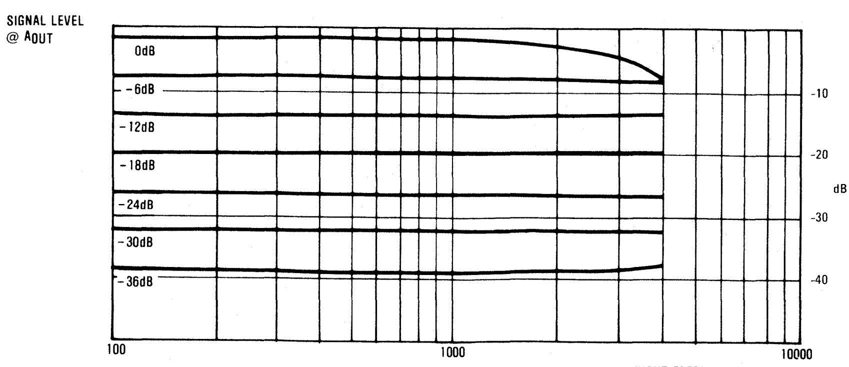


4) Analog (signal) ground (Pin 2) should be externally tied to Pin 8 and power ground. It is recommended that the A_{IN} and A_{OUT} ground returns connect only to Pin 2.
5) Digital inputs and outputs are compatible with standard CMOS logic using the same supply voltage. All unused logic inputs must be tied to the appropriate logic level for desired operation. TTL outputs will require 1K Ohm pull-up resistors. Pins 4 and 14 will each drive CMOS logic or one low power TTL input.
6) Since the Audio Out pins are internally DC biased to $V_{DD}/2$, AC coupling is required. In general, a value of $0.1\mu f$ is sufficient for AC coupling of the CVSD audio pins to a filter circuit.
7) The AGC output may be externally integrated to drive an AGC pre-amp, or it could drive an LED indicator through a buffer to indicate proper speaking volume.

Figures 4, 5, and 6 illustrate the typical frequency response of the HC-55564 for varying input levels and for varying sampling rates. To prevent slope overload (slew limiting), the 0dB boundry should not be exceeded. The frequency response is directly proportional to the sampling clock rate. The flat bandwidth at 0dB doubles for every 16kHz increase in sampling rate. The output levels were measured in the encode mode, without filtering, from A_{IN} to A_{OUT}, at V_{DD} = +5V. 0dB = 1.2Vrms.







The following typical performance distortion graphs were realized with the test configuration of Figure 7. The measurement vehicle for Total Harmonic Distortion (THD) was an HP-339A distortion measurement set, and for 2nd and 3rd harmonic distortion, an HP-3582A spectrum analyzer. All measurement conditions were at VDD = +5V, and 2nd and 3rd harmonic distortion measurements were C-message filtered. 0dB = 1.2Vrms.

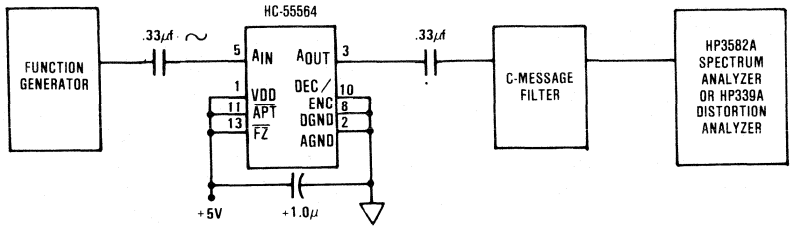


FIGURE 7. TEST AND MEASUREMENT CIRCUIT

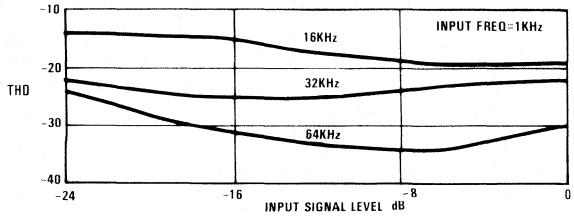
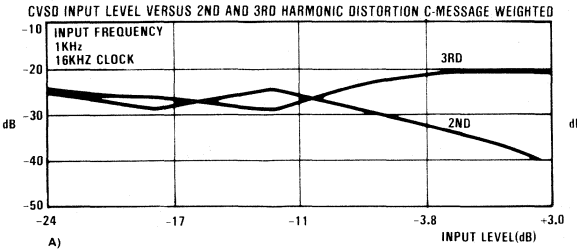
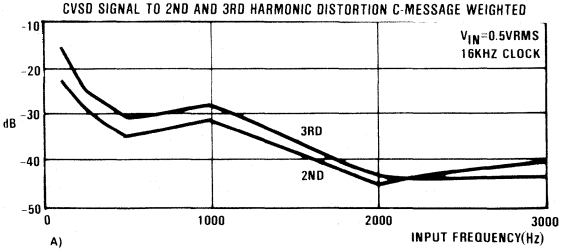
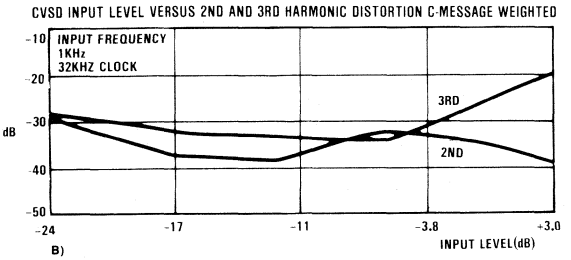
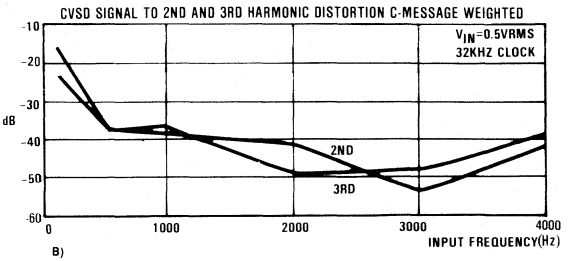


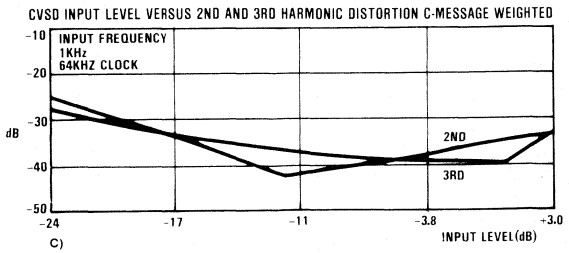
FIGURE 8. CVSD SIGNAL LEVEL VERSUS TOTAL HARMONIC DISTORTION











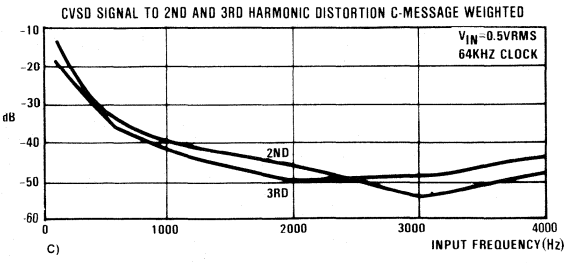


FIGURE 9A, B, C. CVSD INPUT LEVEL VERSUS 2ND AND 3RD HARMONIC DISTORTION

FIGURE 10A, B, C. CVSD INPUT FREQUENCY VERSUS 2ND AND 3RD HARMONIC DISTORTION

HARRIS

HF-10

Universal Active Filter

Features

- Industry Standard Pinout
- Low Crosstalk ..... -60dB
- Low Clock Feed Through 2mVrms
- Low Standby Current 500μA
- Clock to Center Frequency Ratio Accuracy $\pm$2%
- Filter Cutoff Frequency Stability Directly Dependent on External Clock Quality
- Separate High-pass (or Notch or All-Pass), Band-Pass, Low-pass Outputs
- f_O x Q Range up to 50kHz Minimum
- Operates to f_O = 20KHz Minimum
- Specifications Guaranteed for T_A from -55°C to +125°C

Applications

- General Purpose Audio-Band Filtering
- Real-Time Programming
  - ▶ Prototyping ▶ Dynamic Reconfiguration
- High Q Applications
- Precision Filtering at Low Q
- Precision Oscillators
- Extended Temperature
- Voice Response Systems
  - ▶ Modems ▶ Tone Generators
- Data Acquisition Systems
- Building Block for Precision Higher-Order Filters (Directly Cascadable)

Description

The HF-10 consists of two fully independent second order switched capacitor CMOS filter sections. Each second order section is a modified state-variable filter. In each section there are three operational amplifiers and an additional "summing node". The extra summing node is a direct benefit of the switched capacitor design approach. This provides increased versatility as compared to the classical continuous-time active filter. The transfer function of each section is tailored by the user's choice of feedback configuration, external resistor values, and external clock rate.

The HF-10 topology is very useful since it produces three different, but related, transfer functions simultaneously. Each transfer function has the same pole locations but different zero locations. One of the outputs is either a notch, all-pass, or high-pass signal, depending on the feedback configuration chosen by the user; the other outputs are band-pass and low-pass signals. The center frequency of the complex pole pair, f_O, is determined by the external clock frequency and the state of the "50/100/CL" input. This value can also be scaled by a function of the external resistor values depending on the feedback configuration. The other important filter characteristics, such as gain, Q, etc. are determined by functions of external resistor values. Any of the classical filter configurations (Butterworth, Bessel, Cauer/Elliptic, Chebyshev, etc.) can be realized.

The second order sections can be used separately with the constraint that the clock input for each section be driven by signals of the same level (i.e., either TTL or CMOS logic levels), and that the two clock signals share the same digital ground. If it is desired that a fourth order function be realized, the two sections can be cascaded. The "L Sh" (level shift) input is used in conjunction with the clock inputs to allow compatibility with either TTL or CMOS clock levels.

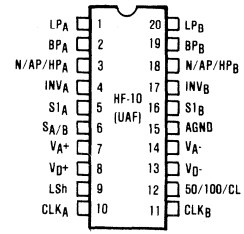
The HF-10 can be powered-down by connecting the "50/100/CL" input to V_D-. This disables the reference current generators for the operational amplifiers and the clock level shifters.

The HF-10 provides a number of advantages over other universal active filters: higher accuracy at frequency extremes; superior clock feedthrough supression; significantly lower crosstalk; better performance over -55°C to +125°C; drives smaller impedance to higher peak output voltage; and capable of precision oscillator applications (phase is continuous when frequency is changed).

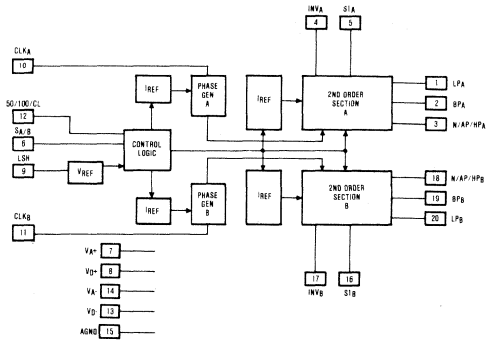
The device is available in a 20 pin ceramic package with temperature ranges of 0°C to +75°C and -55°C to +125°C. Application Note 578 is available.

Pinout

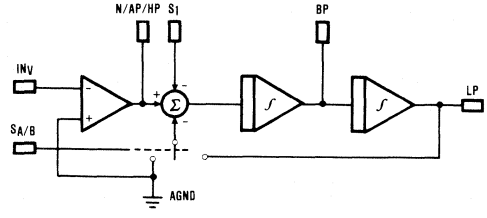
TOP VIEW



System Block Diagram



Filter Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Absolute Maximum Ratings

Supply Voltages ..... ±6.5 Volts
Power Dissipation 300mW
Lead Temperature (Soldering, 10 Sec.) ..... 300°C
Output Loading ..... RLOAD > 3.5kΩ
CLOAD <100pF
Junction Temperature ..... 175°C

Operating Temperature Ranges
HF-10-2, -8 ..... -55°C to +125°C
HF-10-5, -7 ..... 0°C to +75°C
HF-10-9 ..... -40°C to +85°C
Storage Temperature ..... -65°C to +150°C

Electrical Specifications (Complete Filter) ±4.5V < V_S < ±5.5V, (Note 1) Refer to Figure 1.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Range	f_o XQ < 50kHz	50		20K	Hz
Clock to Center Frequency Ratio					
f_{CLK}/f_o = 50	Pin 12 = V_D+, Q = 10 f_o XQ < 50kHz			±2%	
f_{CLK}/f_o = 100	Pin 12 = AGND, Q = 10 f_o XQ < 50kHz			±2%	
Q Range	f_o XQ < 50kHz	0.5		100	
Q Accuracy (Q Deviation from an Ideal Continuous Filter)					
f_{CLK}/f_o = 50	Pin 12 = V_D+, Q ≤ 20 f_o XQ < 50kHz			±4%	
f_{CLK}/f_o = 100	Pin 12 = AGND, Q ≤ 20 f_o XQ < 50kHz			±3%	
f_o XQ Product		50K			Hz
f_o Temperature Coefficient					
f_{CLK}/f_o = 50	T_A = 25°C Pin 12 = V_D+, f_o XQ < 50kHz External Clock Temperature Independent			±100	ppm/°C
f_{CLK}/f_o = 100	Pin 12 = AGND, f_o XQ < 50kHz External Clock Temperature Independent			±100	ppm/°C
Q Temperature Coefficient	T_A = 25°C f_o XQ < 50kz, Q Setting Resistors Temperature Independent			±500	ppm/°C
Crosstalk	INV_A = 0dBm @ 1kHz INV_B = 0V		-60		dB
Clock Feedthrough	See Figure 2		2	5	mVrms
Clock Frequency	Min @ f_{CLK}/f_o = 50, Max @ f_{CLK}/f_o = 100	2.5		2048	kHz
Power Supply Current	T_A = 25°C		13		mA
Standby Current	Pin 12 = V_A-		500		μA

Electrical Specifications (Internal Operational Amplifiers) ±4.5V < V_S < ±5.5V, (Note 1) Refer to Figure 1

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Voltage Swing (Pins 1, 2, 3, 18, 19, 20)	R_{LOAD} = 3.5KΩ	±3.5			V
Op Amp Gain-BW Product		2.5	3.8		MHz
Op Amp Slew Rate		5	15		V/μs
Power Supply Rejection Ratio (PSRR)	DC Only	40			dB

NOTE 1. Unless Otherwise Specified, typical parameters are at +25°C, min-max parameters are over operating temperature range.

Die Characteristics

Transistor Count 464
Die Dimensions ..... 88 x 127
Substrate Potential ..... +V
Process ..... SAJI CMOS

Thermal Constants (°C)	θ_{ja}	θ_{jc}
Ceramic DIP	81	24
Ceramic LCC	76	19

Pin Assignments

SYMBOL	DESCRIPTION
LP, BP, N/AP/HP (A or B)	Low-pass, band-pass, notch or all-pass or high-pass outputs of each second order section.
INV (A or B)	Inverting input of the summing op amp of each filter.
S1 (A or B)	Inverting summing input pin used in most filter configurations.
$S_{A/B}$	Activates a switch connecting one of the inputs of the filter's second summer to either analog ground ($S_{A/B}$ low to V_A-) or to the low-pass output of the circuit ($S_{A/B}$ high to V_A+). This allows flexibility in the various modes of operation of the I. C.
V_A+, V_D+*	Analog positive supply and digital positive supply. These pins are internally connected through the I.C. substrate and therefore, V_A+ and V_D+ should be derived from the same power supply source. They have been brought out separately so they can be bypassed by separate capacitors, if desired. They can be externally tied together and bypassed by a single capacitor.
V_A-, V_D-*	Analog and digital negative supply, respectively. The same comments as for V_A+, V_D+ apply here, except V_A- and V_D- are not tied together internally.
L Sh	Level shift pin. Accommodates various clock levels with dual or single supply operation. With dual ±5V supplies, the HF-10 can be driven with CMOS clock levels (±5V), and the "L Sh" pin should be tied either to the system ground or to the negative supply pin. If the same supplies as above are used and TTL clock levels, derived from a 0V to 5V supply, are used, the "L Sh" pin should be tied to the system ground. For single supply operation (0V and 10V), the V_D- and V_A- pins should be connected to the system ground, the AGND pin should be biased at 5V, and the "L Sh" pin should also be tied to the system ground. This will accommodate both CMOS and TTL clock levels.
CLK (A or B)	Clock inputs for each switched capacitor filter building block. Should both be of the same level (TTL or CMOS). The level shift (L Sh) pin description discusses how to accommodate their levels. The duty cycle of the clock should preferably be close to 50%, especially when clock frequencies above 200kHz are used. This allows the maximum time for the op amps to settle, yielding optimum filter operation.
50/100/CL	By tying this pin to V_D+, a 50:1 clock to filter center frequency operation is obtained. Tying at mid-supplies (i.e., analog ground with dual supplies) allows the filter to operate at a 100:1 clock to center frequency ratio. When tied to VD-, a simple current limiting circuit is triggered to limit the overall supply current. The filtering action is then aborted. This pin also acts as a power up reset when pulled to V_D- after power is applied.
AGND	Analog ground pin. Should be connected to the system ground for dual supply operation or biased at mid-supply for single supply operation. The Non-inverting inputs of the filter op amps are connected to the AGND pin so a "clean" ground is mandatory.

NOTE: All pins are protected against static discharge.

*To initiate the internal power-on reset feature of the HF-10, V+ and V- should be brought up at the same time, or V- should be brought up first. An alternative to power supply sequencing is to strobe Pin 12 (50/100/CL) to V- after power is applied, regardless of power supply sequencing. This will also initiate the power-on reset feature of the HF-10.

Typical Filter Configuration

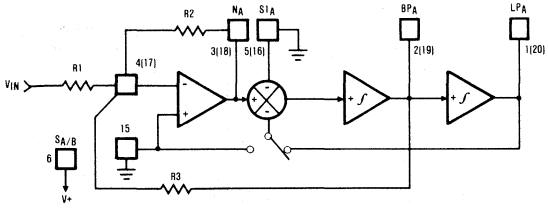


FIGURE 1.

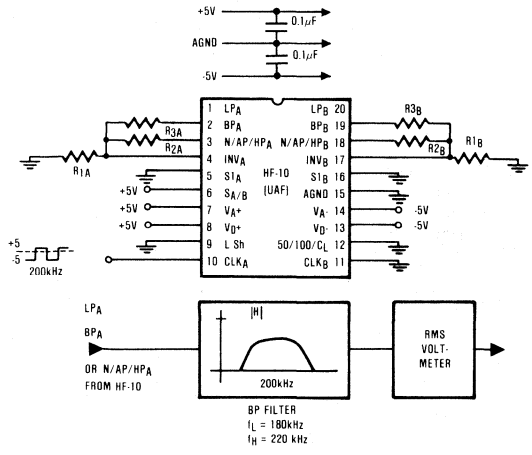


FIGURE 2. MEASURING CHANNEL A CLOCK FEEDTHROUGH

HC-5560

PCM Transcoder

Features

- Single 5V Supply ..... 10mA Typ.
- Mode Selectable Coding Including:
  - AMI (T1, T1C)
  - B8ZS (T1)
  - B6ZS (T2)
  - HDB3 (PCM30)
- North American and European Compatibility
- Simultaneous Encoding and Decoding
- Asynchronous Operation
- Loop Back Control
- Transmission Error Detection
- Alarm Indication Signal
- Replaces CD22103, MJ1440, MJ1471 and TCM2201 Transcoders

Applications

- North American and European PCM Transmission Lines where Pseudo Ternary Line Code Substitution Schemes are Desired
- Any Equipment that Interfaces T1, T1C, T2 or PCM30 Lines Including Multiplexers, Channel Service Units, (CSUs) Echo Cancellors, Digital Cross-Connects (DSXs), T1 Compressors, etc.

Description

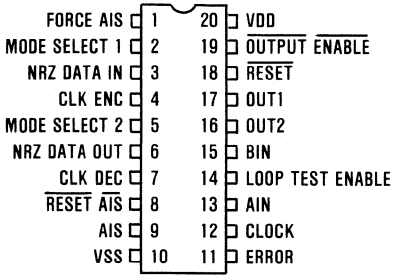
The HC-5560 digital line transcoder provides encoding and decoding of pseudo ternary line code substitution schemes. Unlike other industry standard transcoders, the HC-5560 provides four worldwide compatible mode selectable code substitution schemes, including HDB3 (High Density Bipolar 3), B6ZS, B8ZS (Bipolar with 6 or 8 Zero Substitution), and AMI (Alternate Mark Inversion).

The HC-5560 is fabricated in CMOS and operates from a single 5V supply. All inputs and outputs are TTL compatible. The HC-5560 is available in 20 pin dual-in-line plastic packages over the commercial temperature range, 0°C to +70°C.

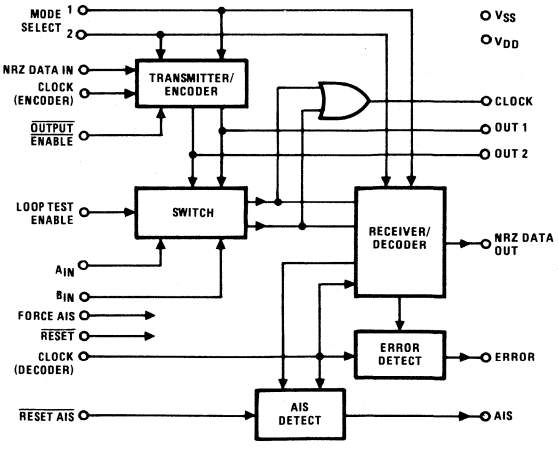
Application Note #573,"The HC-5560 Digital Line Transcoder," by D.J. Donovan is available.

Pinout

HC-5560
TOP VIEW



Functional Diagram



Functional Description

The HC-5560 TRANSCODER can be divided into six sections: transmission (coding), reception (decoding), error detection, all ones detection, testing functions, and output controls.

The transmitter codes a non-return to zero (NRZ) binary unipolar input signal (NRZ Data In) into two binary unipolar return to zero (RZ) output signals (Out 1, Out 2). These output signals represent the NRZ data stream modified according to the selected encoding scheme (i.e., AMI, B8ZS, B6ZS, HDB3) and are externally mixed together (usually via a transistor or transformer network) to create a ternary bipolar signal for driving transmission lines.

The receiver accepts as its input the ternary data from the transmission line that has been externally split into two binary unipolar return to zero signals (A_{in} and B_{in}). These signals are decoded, according to the rules of the selected line code into one binary unipolar NRZ output signal (NRZ Data Out).

The encoder and decoder sections of the chip perform independently (excluding loopback condition) and may operate simultaneously.

The Error output signal is active high for one cycle of CLK DEC upon the detection of any bipolar violation in the received A_{in} and B_{in} signals that is not part of the selected line coding scheme. The bipolar violation is not removed, however, and shows up as a pulse in the NRZ Data Out signal. In addition, the Error output signal monitors the received A_{in} and B_{in} signals for a string of zeros that violates the maximum consecutive zeros allowed for the selected line coding scheme (i.e., 15 for AMI, 8 for B8ZS, 6 for B6ZS, and 4 for HDB3). In the event that an excessive amount of zeros is detected, the Error output signal will be active high for one cycle of CLK DEC during the zero that exceeds the maximum number. In the case that a high level should simultaneously appear on both received input signals A_{in} and B_{in} a logical one is assumed and appears on the NRZ Data Out stream with the Error output active.

An input signal received at inputs A_{in} and B_{in} that consists of all ones (or marks) is detected and signaled by a high level at the Alarm Indication Signal (AIS) output. This is also known as Blue Code. The AIS output is set to a high level when less than three zeros are received during one period of $\overline{\text{Reset AIS}}$ immediately followed by another period of $\overline{\text{Reset AIS}}$ containing less than three zeros. The AIS output is reset to a low level upon the first period of $\overline{\text{Reset AIS}}$ containing 3 or more zeros.

A logic high level on LTE enables a loopback condition where Out 1 is internally connected to A_{in} and Out 2 is internally connected to B_{in} (this disables inputs A_{in} and B_{in} to external signals). In this condition, NRZ Data In appears at NRZ Data Out (delayed by the amount of clock cycles it takes to encode and decode the selected line code). A decode clock must be supplied for this operation.

The output controls are $\overline{\text{Output Enable}}$ and Force AIS. These pins allow normal operation, force Out 1 and Out 2 to zero, or force Out 1 and Out 2 to output all ones (AIS condition).

Pin Assignments

PIN NO.	FUNCTION	DESCRIPTION
1	Force AIS	Pin 19 must be at logic '0' to enable this pin. A logic '1' on this pin forces Out 1 and Out 2 to all ones. A logic '0' on this pin allows normal operation.
2,5	Mode Select 1, Mode Select 2	**MS1 MS2 functions as** 0 0 AMI 0 1 B8ZS 1 0 B6ZS 1 1 HDB3
3	NRZ Data In	Input data to be encoded into ternary form. The data is clocked by the negative going edge of CLK ENC.
4	CLK ENC	Clock encoder, clock for encoding data at NRZ Data In.
6	NRZ Data Out	Decoded data from ternary inputs A_{in} and B_{in}.
7	CLK DEC	Clock decoder, clock for decoding ternary data on inputs A_{in} and B_{in}.
8,9	$\overline{\text{Reset AIS}}$, AIS	Logic '0' on $\overline{\text{Reset AIS}}$ resets a decoded zero counter and either resets AIS output to zero provided 3 or more zeros have been decoded in the preceding $\overline{\text{Reset AIS}}$ period or sets AIS to '1' if less than 3 zeros have been decoded in the preceding two $\overline{\text{Reset AIS}}$ periods. A period of $\overline{\text{Reset AIS}}$ is defined from the bit following the bit during which $\overline{\text{Reset AIS}}$ makes a high to low transition to the bit during which $\overline{\text{Reset AIS}}$ makes the next high to low transition.
10	V_{SS}	Ground reference.
11	Error	A logic '1' indicates that a violation of the line coding scheme has been decoded.
12	Clock	"OR" function of A_{in} and B_{in} for clock regeneration when pin 14 is at logic '1', "OR" function of Out 1 and Out 2 when pin 14 is at logic '0'.
13,15	A_{in}, B_{in}	Inputs representing the recieved PCM signal. A_{in}='1' represents a positive going '1' and B_{in}='1' represents a negative going '1'. A_{in} and B_{in} are sampled by the positive going edge of CLK DEC. A_{in} and B_{in} may be interchanged.
14	LTE	Loop Test Enable, this pin selects between normal and loop back operation. A logic '0' selects normal operation where encode and decode are independent and asynchronous. A logic '1' selects a loop back condition where Out 1 is internally connected to A_{in} and Out 2 is internally connected to B_{in}. A decode clock must be supplied.
16,17	Out 1, Out 2	Outputs representing the ternary encoded NRZ Data In signal for line transmission. Out 1 and Out 2 are in return to zero form and are clocked out on the positive going edge of CLK ENC. The length of Out 1 and Out 2 is set by the length of the positive clock pulse.
18	$\overline{\text{Reset}}$	A logic '0' on this pin resets all internal registers to zero. A logic '1' allows normal operation of all internal registers.
19	$\overline{\text{Output Enable}}$	A logic '1' on this pin forces outputs Out 1 and Out 2 to zero. A logic '0' allows normal operation.
20	V_{DD}	Power to chip.

Static Electrical Specifications

Unless Otherwise Specified. Typical parameters at +25°C.
Min-Max parameters are over operating temperature range. V_{DD} = +5V.

SPECIFICATION	SYMBOL	MIN	TYP	MAX	UNITS
Quiescent Device Current	I_{DD}			100	uA
Operating Device Current			10		mA
Out 1, Out 2 Low (Sink) Current (V_{OL} = 0.4V)	I_{OL1}	3.2			mA
All Other Outputs Low (Sink) Current (V_{OL} = 0.8V)	I_{OL2}	2			mA
All outputs High (Source) Current (V_{OH} = 4.0V)	I_{OH}	2			mA
Input Low Current	I_{IL}			10	uA
Input High Current	I_{IH}			10	uA
Input Low Voltage	V_{IL}			0.8	V
Input High Voltage	V_{IH}	2.4			V
Input Capacitance	C_{IN}			8	pF

Dynamic Electrical Specifications

Unless otherwise Specified. Typical parameters at +25°C.
Min-Max parameters are over operating temperature range. V_{DD} = +5V.

SPECIFICATION	SYMBOL	MIN	TYP	MAX	UNITS	FIG.
CLK ENC, CLK DEC Input Frequency	f_{cl}			8.5	MHz	
CLK ENC, CLK DEC Rise Time (1.544 MHz)	t_{rcl}		10	60	ns	1,2
Fall Time	t_{fcl}		10	60	ns	1,2
Rise Time (2.048 MHz)	t_{rcl}		10	40	ns	1,2
Fall Time	t_{fcl}		10	40	ns	1,2
Rise Time (6.3212 MHz)	t_{rcl}		10	30	ns	1,2
Fall Time	t_{fcl}		10	30	ns	1,2
Rise Time (8.448 MHz)	t_{rcl}		5	10	ns	1,2
Fall Time	t_{fcl}		5	10	ns	1,2
NRZ-Data In to CLK ENC Data Setup Time	t_S	20			ns	1
Data Hold Time	t_H	20			ns	1
A_{IN}, B_{IN} to CLK DEC Data Setup Time	t_S	55			ns	2
Data Hold Time	t_H	5			ns	2
CLK ENC to Out 1, Out 2	t_{DD}		23	80	ns	1
Out 1, Out 2 Pulse Width (CLK ENC Duty Cycle = 50%)						
f_{cl} = 1.544 MHz	t_w		324		ns	1
f_{cl} = 2.048 MHz	t_w		224		ns	1
f_{cl} = 6.3212 MHz	t_w		79		ns	1
f_{cl} = 8.448 MHz	t_w		58		ns	1
CLK DEC to NRZ-Data Out.	t_{DD}		25	54	ns	2
Setup Time CLK DEC to $\overline{\text{Reset AIS}}$	t_{s2}	35			ns	3
Hold Time of $\overline{\text{Reset AIS}}$ = '0'	t_{h2}	20			ns	3
Setup Time $\overline{\text{Reset AIS}}$ = '1' to CLK DEC	t_{s2}	0			ns	3
$\overline{\text{Reset AIS}}$ to AIS output	t_{pd5}			42	ns	3
CLK DEC to Error output	t_{pd4}			62	ns	3

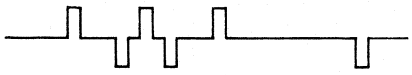
Line Code Descriptions

AMI, Alternate Mark Inversion, is used primarily in North American T1 (1.544 MHz) and T1C (3.152 MHz) carriers. Zeros are coded as the absence of a pulse and one's are coded alternately as positive or negative pulses. This type of coding reduces the average voltage level to zero to eliminate DC spectral components, thereby eliminating DC wander. To simplify timing recovery, logic 1's are encoded with 50% duty cycle pulses.

e.g.

PCM Code 0 0 0 1 0 1 1 1 0 1 0 0 0 0 0 1

AMI Code



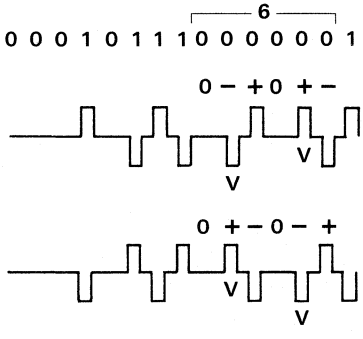
To facilitate timing maintenance at regenerative repeaters along a transmission path, a minimum pulse density of logic 1's is required. Using AMI, there is a possibility of long strings of zeros and the required density may not always exist, leading to timing jitter and therefore higher error rates.

A method for insuring minimum logic 1 density by substituting bipolar code in place of strings of 0's is called BNZS or Bipolar with N Zero Substitution. B6ZS is used commonly in North American T2 (6.3212MHz) carriers. For every string of 6 zeros, bipolar code is substituted according to the following rule;

> If the immediate preceding pulse is of (−) polarity, then code each group of 6 zeros as 0 −+ 0+−, and if the immediate preceding pulse is of (+) polarity, code each group of 6 zeros as 0+− 0−+. One can see the consecutive logic 1 pulses of the same polarity violate the AMI coding scheme.

e.g.

PCM Code 0 0 0 1 0 1 1 1 0 0 0 0 0 0 1



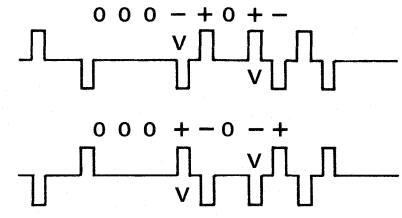
V = Violation

B8ZS is used commonly in North American T1 (1.544 MHz) and T1C (3.152 MHz) carriers. For every string of 8 zeros, bipolar code is substituted according to the following rules;

1. If the immediate preceding pulse is of (−) polarity, then code each group of 8 zeros as 000−+ 0+−.
2. If the immediate preceding pulse is of (+) polarity then code each group of 8 zeros as 000+− 0−+.

e.g.

PCM Code 1 0 10 0 0 0 0 0 0 0 1 1 0



V = Violation

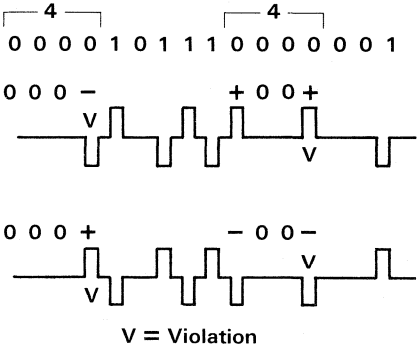
The BNZS coding schemes, in addition to eliminating DC wander, minimize timing jitter and allow a line error monitoring capability.

Another coding scheme is HDB3, high density bipolar 3 used primarily in Europe for 2.048 MHz and 8.448 MHz carriers. This code is similar to BNZS in that it substitutes bipolar code for 4 consecutive zeros according to the following rule;

1. If the polarity of the immediate preceding pulse is (−) and there have been an odd (even) number of logic 1 pulses since the last substitution, each group of 4 consecutive zeros is coded as 000−(+00+).
2. If the polarity of the immediate preceding pulse is (+) then the substitution is 000+(−00−) for odd (even) number of logic 1 pulses since the last substitution.

e.g.

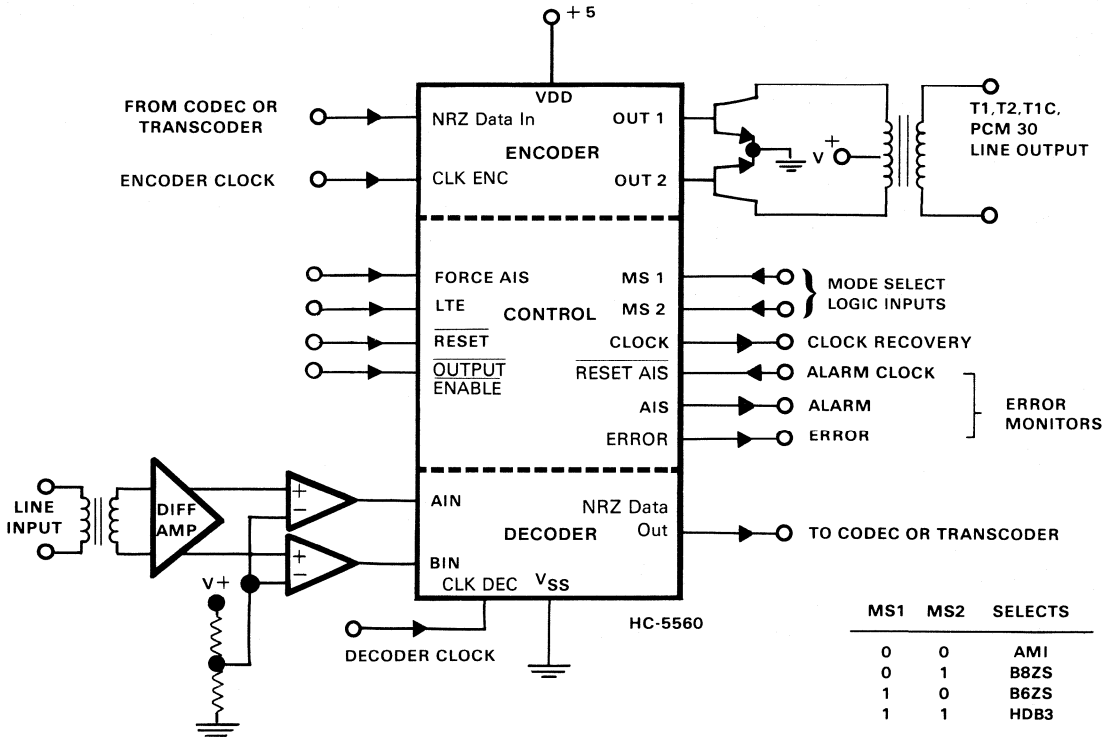
PCM Code 0 0 0 0 1 0 1 1 1 0 0 0 0 0 0 1



V = Violation

The 3 in HDB3 refers to the coding format that precludes strings of zeros greater than 3. Note that violations are produced only in the fourth bit location of the substitution code and that successive substitutions produce alternate polarity violations.

Application Diagram



MS1	MS2	SELECTS
0	0	AMI
0	1	B8ZS
1	0	B6ZS
1	1	HDB3

Die Characteristics

Transistor Count 4322
Die Dimensions ..... 119 x 133
Substrate Potential ..... +V
Process ..... SAJI CMOS

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
Plastic DIP, HC-5560	67	25

Timing Waveforms

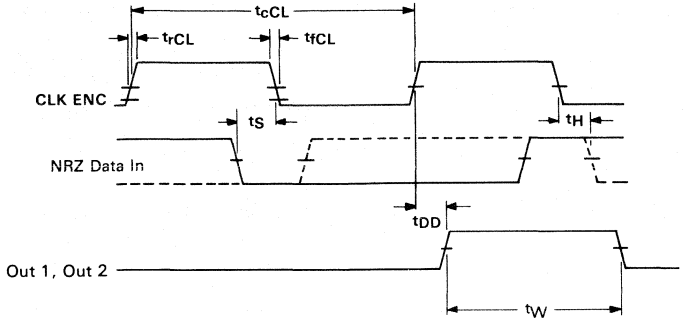


FIGURE 1. TRANSMITTER (CODER) TIMING WAVEFORMS

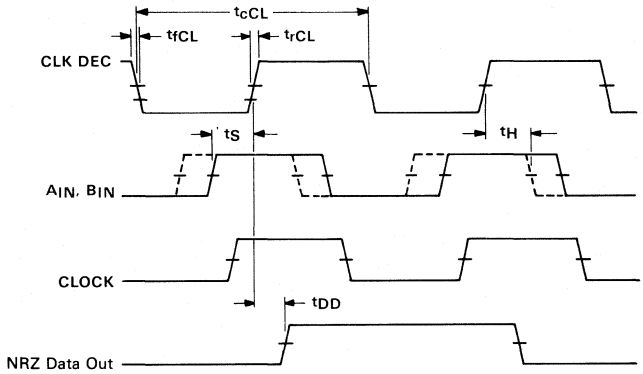


FIGURE 2. RECEIVER (DECODER) TIMING WAVEFORMS

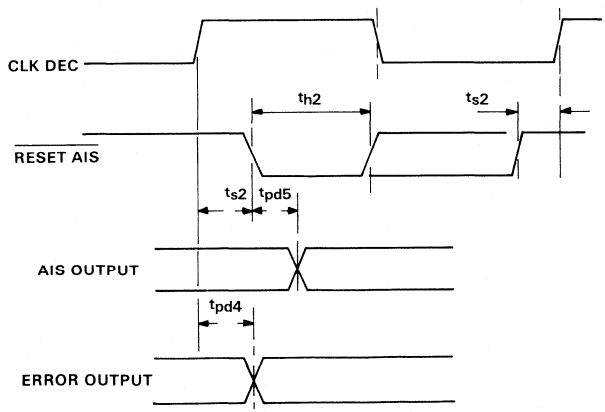


FIGURE 3. $\overline{\text{RESET AIS}}$ INPUT, AIS OUTPUT, ERROR OUTPUT

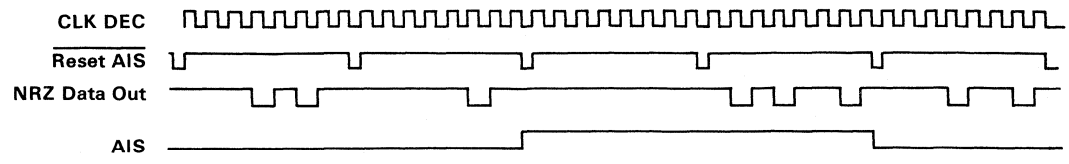


FIGURE 4.

Two consecutive periods of Reset AIS, each containing less than three zeros, sets AIS to a logic '1' and remains in a logic '1' state until a period of Reset AIS contains three or more zeros.

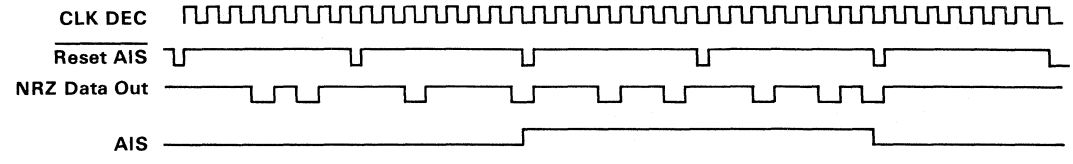


FIGURE 5.

Zeros which occur during a high to low transition of Reset AIS are counted with the zeros that occured before the high to low transition.

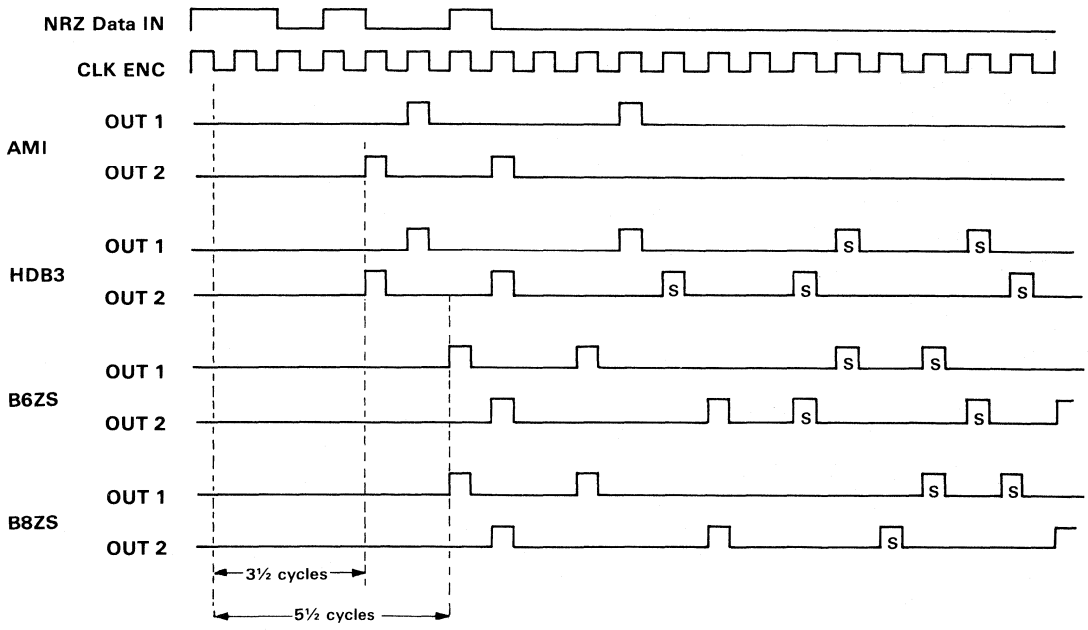


FIGURE 6. ENCODE TIMING AND DELAY

Data is clocked on the negative edge of CLK ENC and appears on Out 1, and Out 2. Out 1 and Out 2 are interchangable. Bipolar violations and all other pulses inserted by the line coding scheme to encode strings of zeros are labled with an "S".

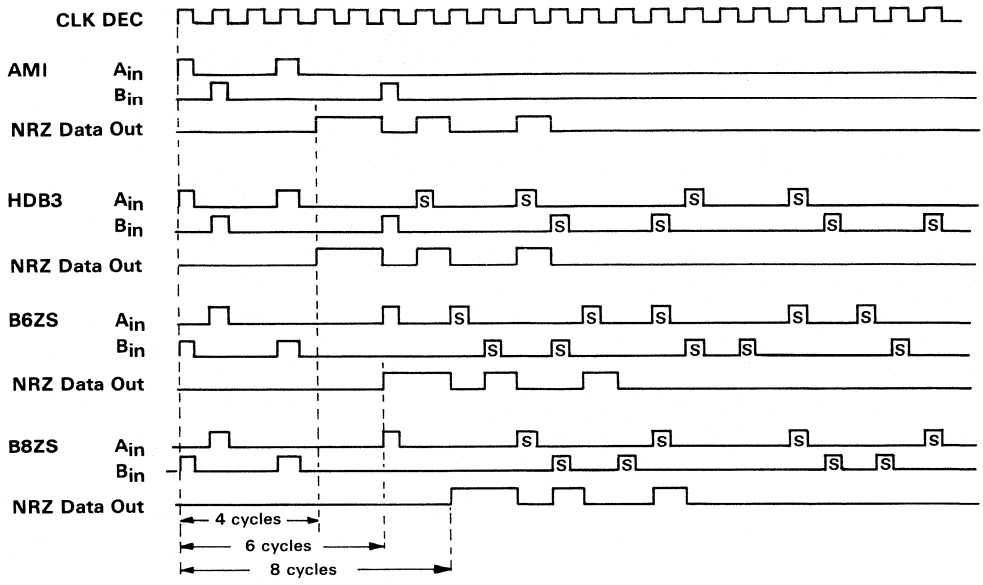


FIGURE 7. DECODE TIMING AND DELAY

Data that appears on A_{in} and B_{in} is clocked by the positive edge of CLK DEC, decoded and zeros are inserted for all valid line code substitutions. The data then appears in non-return to zero form at output NRZ Data Out. A_{in} and B_{in} are interchangable.

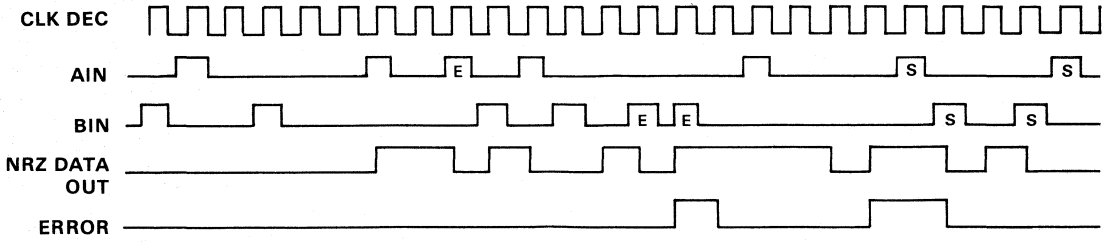


FIGURE 8.

The ERROR signal indicates bipolar violations that are not part of a valid substitution.

ANALOG

Harris Quality and Reliability

9

Introduction

Success in the integrated circuit industry requires building products which are not only acceptable to the requirements of today's market but are continually evolving to meet the challenges of the future. This demands actions which are based on improvement and aimed at perfection.

Harris Semiconductor's commitment to supply top value in integrated circuits has made quality improvement a mandate for every person in our workforce - from circuit designer to manufacturing operator, from the hourly employee to the corporate executive. Quality, reliability, and performance are all measures of value in integrated circuits that have significantly increased in importance in today's market. Price is no longer the only determinant in the success of a supplier. See Figure 1.

To succeed in today's integrated circuit market, quality cannot be an add-on or after-the-fact consideration. Quality must begin with the development of capable process technology and product designs. It continues in the manufacturing process only via effective controls at each operation. It culminates in the delivery of products which meet or exceed the expectations of the customer. Our company's quality methodology is evolving. In 1981 we embarked on a program to move from Stage I. We are currently in the transition from Stage II to Stage III as more and more people in our organization become involved in quality activities. Quality is not the responsibility of one person, it is everyone's job. The traditional "quality" tasks of screening, inspection and testing are giving way to more effective and efficient methods. We are putting new tools in the hands of our employees. Here's a sample of how our quality systems are changing to meet the needs of today's marketplace. See Table 1.

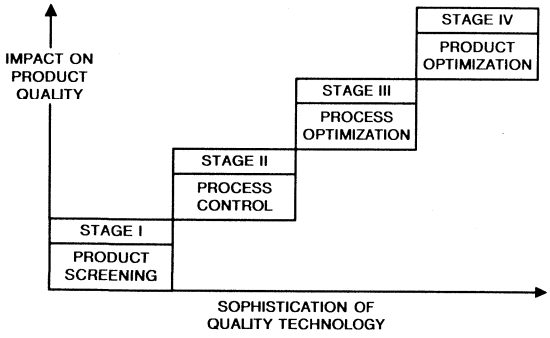


FIGURE 1. STAGES OF STATISTICAL QUALITY TECHNOLOGY

TABLE 1. APPROACH AND IMPACT OF STATISTICAL QUALITY TECHNOLOGY

STAGE		APPROACH	IMPACT
I	Product Screening	• Stress and Test • Defective Prediction	• Limited Quality • Costly • After-The-Fact
II	Process Control	• Statistical Process Control • Just-In-Time Manufacturing	• Identifies Variability • Reduces Costs • Real Time
III	Process Optimization	• Design of Experiments • Process Simulation	• Minimizes Variability • Before-The-Fact • Limited by Process Capability
IV	Product Optimization	• Design for Producibility • Product Simulation	• Insensitive to Variability • Designed-In Quality • Optimal Results

Designing for Success—Feeding Back the Results

Assuring quality and reliability in integrated circuits begins with good product and process design and this has always been a strength in Harris Semiconductor's quality approach. We have a very long lineage of high reliability, high performance products that have been born out of our commitment to design excellence. Today as before, all Harris products are designed to meet the stringent quality and reliability requirements of the most demanding end equipment applications, from military and space to industrial and telecommunications. The application of new tools and methods has allowed us to continuously upgrade the design process.

Each new design is evaluated throughout the development cycle to validate the capability of the new product to meet the end market performance, quality, and reliability objectives.

This validation process has four major components:

1. Design simulation/optimization
2. Layout verification
3. Product demonstration
4. Reliability assessment

Harris designers have an extensive set of very powerful Computer-Aided Design (CAD) tools to create and optimize product designs as outlined in Table 2.

TABLE 2. HARRIS I.C. DESIGN TOOLS

	PRODUCTS	
DESIGN STEP	ANALOG	DIGITAL
Functional Simulation	Slice	Silos Proteous Socrates
Parametric Simulation	Slice Monte Carlo	Slice
Schematic Capture	Note 1	Daisey SDA-Mass Comp
Functional Checking	Note 1	SDA-LVS
Rules Checking	Calma-DRC	Harris Dash
Parasitic Extraction	Note 1	SDA-LVS

NOTE 1. Tools are in Development.

From schematic generation to layout rules checking, the application of these CAD tools allows our designers to optimize product capabilities. These tools afford the designer ample opportunity to evaluate alternative approaches, check tradeoffs, and eliminate errors. The result is better product designs.

The second aspect of design validation is characterization and reliability testing. New products are manufactured in our normal production lines, not in pilot lines, allowing full characterization of the product as it will be produced when offered to the market. Harris has accumulated a large reliability data base on its processes. New product conformance to the reliability objectives is verified on samples during the pre-production phase prior to product introduction. The results of these tests are added to the reliability data base. Design rules used to design and layout products are refined based on analysis of the reliability test results (Table 3). Feedback from our past results and experiences helps us continually improve and update the quality of our design.

TABLE 3. NEW PROCESS AND NEW PRODUCTION SITE QUALIFICATION

TESTS	SAMPLE SIZE
High Temp Operating Life Test	850 Units Out of 8 Wafer Lots
85°C/85% Relative Humidity	110 Units Out of 2 Assembly Lots
Autoclave (Plastic Only)	55 Units
Temperature Cycle	50 Units Out of 2 Assembly Lots
Thermal Shock	50 Units Out of 2 Assembly Lots
Construction Analysis	100 Units Out of 4 Wafer Lots
ESD Characterization	20 Units Out of 4 Wafer Lots
Absolute Max. Rating Tests	20 Units Out of 4 Lots
Electrical Characterization	110 Units Out of 4 Lots

Controlling and Improving the Manufacturing Process—SPC/DOX

Statistical process control (SPC) is the basis for quality control and improvement at Harris Semiconductor. Harris SPD manufacturing people use over 1000 Shewhart control charts to determine the normal variations in processes, materials, and products. Critical process variables are measured and control limits are plotted on the control charts. Appropriate action is taken if the control charts indicate that an operation is outside the process control limits or indicates a trend toward the limit. These same control charts are powerful tools for use in reducing variations in processing, materials, and products. See Table 4.

The job does not stop there. Processes which operate in statistical control are not always capable of meeting engineering requirements. The conventional way of dealing with this in the semiconductor industry has been to implement 100% screening or inspection steps to remove defects. Harris still uses screening and inspection to "grade" products and to satisfy specific screening requirements imposed by customers by offering burn-in, multiple temperature test insertions, environmental screening, and visual inspection as value-added testing options.

TABLE 4. SUMMARIZING CONTROL CHART APPLICATIONS

FAB			
• Diffusion - Junction Depth - Sheet Resistivities - Oxide Thickness - Implant Dose Calibration - Uniformity	• Thin Film - Film Thickness - Uniformity - Refractive Index	• PR - Critical Dimension - Resist Thickness - Etch Rates - Film Composition	• Measurement Equipment - Critical Dimension - Film Thickness - 4 Point Probe - Ellipsometer
ASSEMBLY			
• Pre -Seal - Die Prep Visuals - Yields - Die Attach Heater Block - Die Shear - Wire Pull - Saw Blade Wear	• Post -Seal - Internal Package Moisture - Tin Plate Thickness - Solder Thickness - Leak Tests - Module Rm. Solder Pot Temp.	• Measurement - XRF - Radiation Counter - PIND Defect Rate - GM-Force Measurement	- Thermocouples
TEST			
	- Handlers/Test Systems - Defect Parato Charts - Lot % Defective - ESD Failures per Month	- Monitor Failures - Lead Strengthening Quality - After Burn-In PDA	
OTHER			
• IQC - Vendor Performance - Material Criteria - Quality Levels	• Environment - Water Quality - Clean Room Control	• IQC Measurement/Analysis - XRF - ADE - 4 Point Probe - Chemical Analysis Equipment	

We feel these techniques are insufficient to meet the demands of today's market for high reliability and perfect quality performance. Inspection and screening have limited capability in reducing product defects to the levels expected by today's marketplace, and screening operations occasionally introduce defects into product populations. Also, screening and inspection activities have associated expense which adds to product cost. Harris engineers use Design of Experiments (DOX), a scientifically disciplined mechanism for evaluating and implementing improvements in product processes, materials, equipment, and facilities. These improvements are aimed at reducing the number of defects by studying the key variables controlling the process and optimizing the procedures or design to yield the best result. This is a long haul approach to achieving quality perfection. It takes time, but better product results from the efforts and the basic causes of product nonconformance can be eliminated.

SPC, DOX, and design for manufacturability, coupled with our 100% screening flows, make a product assurance program that results in the quality and reliability performance demanded by today's marketplace. Harris AOQ results for our catalog products during the last half of 1987 were 200ppm (see Figure 2). Our goal is to be at or below 100ppm by the middle of 1988. Harris reliability results for all process and products are approximately 160 FITS. Our goal is to maintain this outstanding performance for all products we offer. We have the tools and the people to do it.

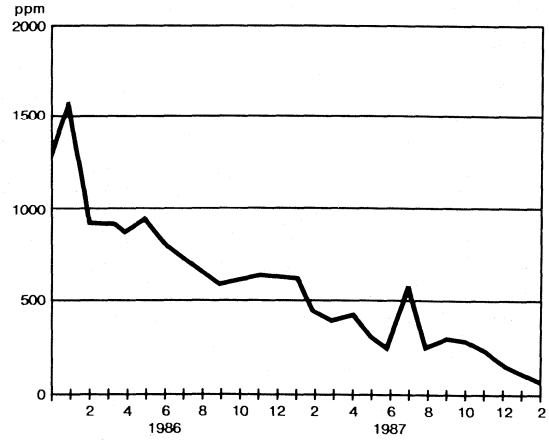


FIGURE 2. DEFECTIVE PARTS PER MILLION

The Role of the Quality Organization

The emphasis on building quality into the design and manufacturing processes of a product has resulted in a significant change in the role of the Quality organization. In addition to facilitating the development of SPC and DOX programs and working with manufacturing to establish control charts, Quality professionals are involved in the measurement of equipment capability, standa rdization of inspection equipment, procedures for chemical controls, analysis of inspection data and feedback to the manufacturing areas, coordination of efforts for product improvement, upgrades of environmental or raw materials quality, and development of quality improvement programs with vendors. The Quality organization's role is changing from one of policing quality to one of facilitating quality in other organizations. It does this through auditing, sampling, consulting, and managing QIT projects. The Quality organization assists top management in formulating quality policy and establishing overall quality programs and objectives. Many of the conventional quality functions are still performed by the Quality organization to support specific market requirements (e.g., Group A and B testing for military products). But true to the philosphy that quality is everyone's job, much of the traditional on-line measurement and control of quality characteristics is where it belongs, with the people who make the product what it is. The Quality organization is there to assist in the deployment of quality techniques and to monitor progress.

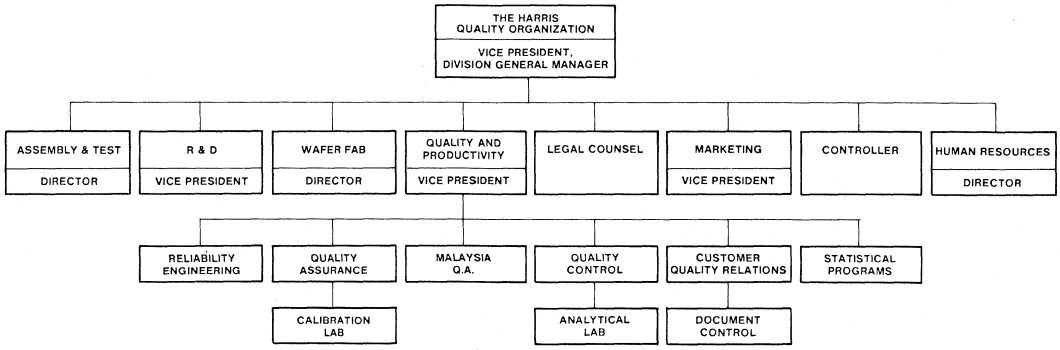


FIGURE 3. THE HARRIS QUALITY ORGANIZATION

TABLE 5. ON-LINE MANUFACTURING/QC FUNCTIONS

AREA	FUNCTION	MANUFACTURING CONTROLS	QA/AC MONITOR AUDIT
Wafer Fab	• JAN Self-Audit		X
	• Environmental		
	- Room/Hood Particulates	X	X
	- Temperature/Humidity	X	X
	- Water Quality		X
	• Product		
	- Junction Depth	X	
	- Sheet Resistivities	X	
	- Defect Density	X	X
	- Critical Dimensions	X	X
	- Visual Inspection	X	X
	- Lot Acceptance		X
	• Process		
	- Film Thickness	X	X
	- Implant Dosages	X	
	- Capacitance Voltage Changes	X	X
	- Conformance to Specification	X	X
	• Equipment		
	- Repeatability	X	X
	- Profiles	X	X
	- Calibration		X
	- Preventive Maintenance	X	X
Wafer Fab	• JAN Self-Audit		X
	• Environmental		
	- Room/Hood Particulates	X	X
	- Temperature/Humidity	X	X
	- Water Quality		X
	• Product		
	- Documentation Check		X
	- Dice Inspection	X	X
	- Wire Bond Pull Strength/Controls	X	X
	- Pre-Seal Visual	X	X
	- Fine/Gross Leak	X	X
	- PIND	X	
	- Lead Finish Visuals, Thickness Die Shear	X	X
	- Solderability		X
	• Process		
	- Operator Quality Performance		X
	- Saw Controls	X	
	- Die Attach Temperatures	X	X
	- Seal Temperature Profile	X	X
	- Temp Cycle Chamber Temperature	X	X
	- ESD Protection	X	X
	- Plating Bath Controls	X	
	- Mold Parameters	X	X
Test	• JAN Self-Audit		X
	• Temperature/Humidity	X	X
	• ESD Controls	X	
	• Temperature Test Calibration	X	
	• Test System Calibration	X	
	• Test Procedures		X
	• Control Unit Compliance		
	• Lot Acceptance Conformance	X	
	• Group A Lot Acceptance		X
Probe	• JAN Self-Audit		X
	• Wafer Repeat Correlation	X	
	• Visual Requirements	X	X
	• Documentation	X	X
	• Process Performance	X	X
Burn-In	• JAN Self-Audit		X
	• Functionality Board Check	X	
	• Oven Temperature Controls	X	
	• Procedural Conformance		X

TABLE 5. ON-LINE MANUFACTURING/QC FUNCTIONS (CONTINUED)

AREA	FUNCTION	MANUFACTURING CONTROLS	QA/AC MONITOR AUDIT
Brand	• JAN Self-Audit		X
	• ESD Controls	X	X
	• Brand Permanency	X	X
	• Temperature/Humidity	X	X
	• Procedural Conformance		X
QCI Inspection	• JAN Self-Audit		X
	• Solderability Bath		X
	• Group D Conformance		X

Training

The foundation of a successful transition from the conventional quality program to a more effective one is extensive training of the personnel involved in manu facturing the products. Early in 1984, Harris SPD began a comprehensive development program in statistical methods. Through the University of Tennessee, private consultants, and internally developed training programs, Harris has completed the training of nearly 2,000 engineers, supervisors, and operators/technicians.

Over 940 operators, more than 98 supervisors, and some 751 engineers have been trained in SPC methods, providing them with tools to improve the overall level of uniformity of Harris products. More than 256 engineers have received training in DOX methods, learning to evaluate changes in process operations, set up new processes, select or accept new equipment, evaluate materials, select vendors, compare two or more pieces of equipment, and compare two or more process techniques.

Over the past four years, Harris SPD has also deployed a comprehensive training program for hourly operators and supervisors in job requirements and functional skills. All hourly manufacturing employees participate. Nearly 600 hourly SPD employees are certified in an average of ten job skills. About 20,000 man hours per year are expended in SPD employee training and certification. Harris SPD maintains a full time training staff to develop and manage its training programs (see Table 6).

TABLE 6. TABLE OF TRAINING PROGRAMS

COURSE	AUDIENCE	LENGTH	TOPICS COVERED
SPC	Manufacturing Operators	8 Hours	Basic Philosophy, Statistical Calculations Graphing Techniques, Pareto Charts, Control Charts
SPC	Manufacturing Supervisors	21 Hours	Basic Philosophy, Statistical Calculations Graphing Techniques, Pareto Charts, Control Charts, Testing for Inspector Agreement, Cause and Effect Diagrams, 1 and 2 Sample Methods
SPC	Engineers and Managers	48 Hours	Basic Philosophy, Graphical Methods, Control Charts, Rational Subgroubing, Variance Components, 1 and 2 Sample Methods, Pareto Charts, Cause and Effect Diagrams
DOX (Design of Experiments)	Engineers and Managers	88 Hours	Factorial Designs, Fractional Factorial Designs, Blocking Designs, Variance Components, Computer Usage, Normal Probability Plotting
RSM (Response Surface Methods)	Engineers and Managers	40 Hours	Steepest Ascent, Central Composite Designs, Box-Behnken Designs, Computer Usage, Contour Plotting, Second Order Response Surfaces
Continuous Improvement Methods	Manufacturing Supervisors	12 Hours	Basic Philosophy, Pareto Analysis, Imagineering, Run Charts, Cause and Effect Diagrams, Histograms, Ideas of Control Charts

Vendors

The quality of materials used in manufacturing is very important to making quality integrated circuits. Since the introduction of statistical process control in our factory, the impact of incoming materials and chemicals is more visible and measurable. To achieve the highest quality and the most economical results from a statistically controlled manufacturing operation, incoming materials must also be statistically controlled.

To upgrade the quality and consistency of incoming materials, and to learn more about the characteristics of the materials, Harris has initiated and coordinated an aggressive program aimed at certifying major vendors and ens uring they have SPC programs in place. SPC seminars are held for vendors in all material categories (silicon, chemicals, thin film materials, photoresists, gases, and piece parts). Those who have attended are now certified or working toward certification. See Table 7.

TABLE 7. INCOMING QUALITY CONTROL MATERIAL QUALITY CONFORMANCE

MATERIAL	INCOMING INSPECTIONS	VENDOR DATA REQUIREMENTS
Silicon	• Resistivity • Crystal Orientation • Dimensions • Edge Conditions • Taper • Thickness • Total Thickness Variation • Backside Criteria • Oxygen • Carbon	• Equipment Capability Control Charts - Oxygen - Resistivity • Control Charts for - Enhanced Gettering - Total Thickness Variation - Total Indicated Reading - Particulates • Certificate of Analysis for all Critical Parameters
Chemicals/Photo-resists/Gases	• Chemicals - Assay - Major Contaminants • Molding Compounds - Spiral Flow - Thermal Characteristics • Gases - Impurities • Photoresists - Viscosity - Film Thickness - Solids - Pinholes	• Certificate of Analysis on all Critical Parameters • Control Charts - Assay - Contaminants - Water - Selected Parameters • Control Charts - Assay - Contaminants • Control Charts on - Photospeed - Thickness - UV Absorbance - Filterability - Water - Contaminants
Thin Film Materials	• Assay • Selected Contaminants	• Control Charts - Assay - Contaminants - Dimensional Characteristics • Certificate of Analysis for all Critical Parameters
Assembly Materials	• Visual Inspection • Dimension Checks • Lead Integrity • Glass Composition • Bondability • Intermetallic Layer Adhesion • Ionic Contaminants • Thermal Characteristics • Lead Coplanarity • Metal Thickness • Hermeticity	• Certificate of Analysis • Process Control Charts on Outgoing Product Checks and In-Line Process Controls

Prior to certification, Harris and its vendors work closely on correlating measurement techniques, clarifying specific material parameters, and negotiating specifications governing the Harris quality requirements. The use of real-time SPC procedures in the vendor's manufacturing operation is an indispensable prerequisite to certification. Our goal is for the supplier's factory to become an extension of the Harris manufacturing line. In addition to periodic incoming inspection on lots, Harris Quality personnel review control charts supplied with materials, review operations, and carry out regularly scheduled audits of the vendors.

All of the data is used to formulate "The Vendor History." Materials inspection data, vendor conformance to corrective action, and the use of SPC procedures are compiled in a quantitative Vendor Quality Rating (VQR). Active participation by our vendors in defining requirements, and constant feedback by Harris on quality performance, has instilled the quality ownership into the vendor's manufacturing operation. Our incoming lot defect rates are 2.4%, compared to 9.7% before we initiated this program. Our goal is to reduce the incoming reject rate to 1.5% by the end of June 1989.

Manufacturing Science—CAM, JIT

In addition to deploying SPC and DOX as key tools to control the product and processes, Harris is deploying other management mechanisms in the factory. Upon first examination, these tools appear to be directed more at schedules and capacity. However, they have a significant impact on quality results.

- **Computer Aided Manufacturing (CAM)**
  CAM is a computer based inventory and productivity management tool. The CAM systems allow personnel to quickly identify production line problems and take corrective action. In addition, CAM improves scheduling and allows Harris to more quickly respond to fluctuating customer requirements. It is also an important tool in managing work in process (WIP) and inventories.

  Through the use of CAM, significant improvements have been made in a number of areas. Wafer lot tracking has greatly improved, facilitating a number of process improvements through correlation of yields to process variables. In several places CAM has greatly improved capacity utilization through better planning and scheduling. Queues have been reduced; cycle times have been shortened, in one case by as much as a factor of 2.

  The most significant advantage has been the reduction in WIP inventory levels, in one area by as much as a factor of 5. This results in fewer lots in the area. By reducing inventory and time in the area, quality improves. In wafer fab, defect rates are reduced because wafers spend less time sitting in production area waiting to be processed. Less inventory also raises morale and brings a more orderly flow to the area. CAM facilitates all of these advantages.

- **Just In Time (JIT)**
  A key adjunct to the CAM activity is Just In Time (JIT) material management. This is more than an inventory reduction technique. In many cases it involves reorganization of facilities and people. The essential concept is to form work units that are responsible for doing the whole job rather than bits of it. For example, a photoresist flow consists of several steps which were previously organized in the classical departmentalized way. The inspection and etch areas were in a different serial manner location from the deposition and alignment areas. Work piled up at the slowest operation (inspection). Quality problems detected at inspection were decoupled in space and time from the areas producing them by 20 to 30 feet and at least one day. Rework rates were very high. Scrap was unacceptable.

  The area was reorganized into GT (group technology) cells, a basic concept in JIT (see Figure 4). The inspection and alignment areas were physically coupled and people were organized into teams. The whole job (finished defect free wafers) was assigned to the GT cell. Rework rates decreased 70%. Scrap rates decreased 45%. And probe yields increased by 50%. This is only one of hundreds of examples of how JIT has improved our factory performance.

PHOTORESIST AREA (BEFORE & AFTER JIT WAS IMPLEMENTED)

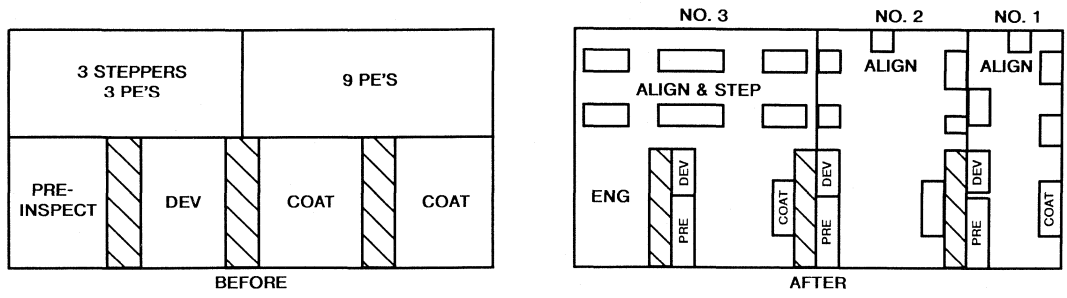


FIGURE 4. GROUP TECHNOLOGY CELL

Measurement

Analytical Services Laboratories

All Engineering, Manufacturing, and Product Assurance functions are supported by the Analytical Services Laboratory. This laboratory maintains capability in chemical and physical analysis. The principal capabilities of this lab are:

SPECTROSCOPIC METHODS: Colorimetry, Optical Emission, Ultraviolet Visible, Fourier Transform-Infrared, Flame Atomic Absorption, Furnace Organic Carbon Analyzer, Mass Spectrometer.

CHROMATOGRAPHIC METHODS: Gas Chromatography, Ion Chromatography.

THERMAL METHODS: Differential Scanning Colorimetry, Thermogravimetric Analysis, Thermomechanical Analysis.

PHYSICAL METHODS: Profilometry, Microhardness, Rheometry.

CHEMICAL METHODS: Volumetric, Gravimetric, Specific Ion Electrodes.

ELECTRON MICROSCOPE: Transmission Electron Microscopy, Scanning Electron Microscope.

X-RAY METHODS: Energy Dispersive X-ray Analysis (SEM), Wavelength Dispersive X-ray Analysis (SEM), X-ray Fluorescence Spectrometry, X-ray Diffraction Spectrometry.

SURFACE ANALYSIS METHODS: Scanning Auger Microprobe, Electron Spectroscope/Chemical Analysis, Secondary Ion Mass Spectrometry, Ion Scattering Spectrometry, Ion Microprobe.

The Analytical Services Lab provides analysis support for process development, failure analysis, product evaluation, and qualification. Finally, the lab serves as a reference source for correlation and calibration of process control measurements as well as assisting in developing improved process measurement methodology.

Calibration Laboratories

Another important resource in the product assurance system is Harris Semiconductor's Calibration Lab. This area is responsible for calibrating the electronic, electrical, electro/mechanical, and optical equipment used in both the production and engineering areas. The accuracy of instruments used at Harris in calibration is traceable to the National Bureau of Standards. The lab maintains a system which conforms to the current revision of MIL-STD45662, "Calibration System Requirements."

Each instrument requiring calibration is given a calibration interval based upon stability, purpose, and degree of use. The equipment is labeled with an identification tag which describes the last calibration date and the next required calibration. The Calibration Lab reports on a regular basis to each user department, and equipment out of calibration is taken out of service until calibration is performed. The Quality organization performs periodic audits to assure proper control in the using areas.

Failure Analysis

Harris Semiconductor products have an outstanding reputation for reliability and quality. Our records show that less than 1/10 of 1% of all products shipped in calendar year 1986 were returned for quality or reliability defects. Of these, more than half were determined to be damaged by EOS or ESD. Harris Semiconductor operates a fully staffed and equipped failure analysis lab to assist the customer, should products be found which fail to meet requirements for reliability or quality. Formal documentation of failure analysis results is provided by the Harris reliability organization, including failure mechanism and corrective action. The table below summarizes the dominant failure mechanisms of each of Harris Semiconductor's product groups. This data is used in formulating reliability predictions and in guiding process and product design improvements. Should formal failure analysis of any products be required, simply contact your local field sales representative for help.

TABLE 8. HIGH TEMPERATURE OPERATING LIFE

PROCESS DESCRIPTION	TESTED QUANTITY (UNITS)	NO. OF FAILURES (UNITS)	DEVICE HOURS @ STRESS TEMPERATURE	FAILURE RATE (FIT*) @ $T_A = 55^oC$ (60% CONF. LEVEL)
Scaled SAJI IV	4,404	26	5,013,762	35
SAJI V/VI	425	7	311,792	47
Standard Linear, DI with Nichrome Resistors	2,563	6	3,182,671	62
Standard Linear, DI with Nichrome Resistors	2,887	1	3,602,273	17
DI, Aluminum & Silicon Gate Linear CMOS	4,256	0	7,101,794	3
Comb. Std. Linear and MOS, High Frequency	455	0	458,728	6
Comb. Std. Linear and MOS	154	0	155,021	25
Local Oxidized SAJI VII	1,565	1	3,599,306	47

*FIT = One Failure in 10^9 Device Hours.

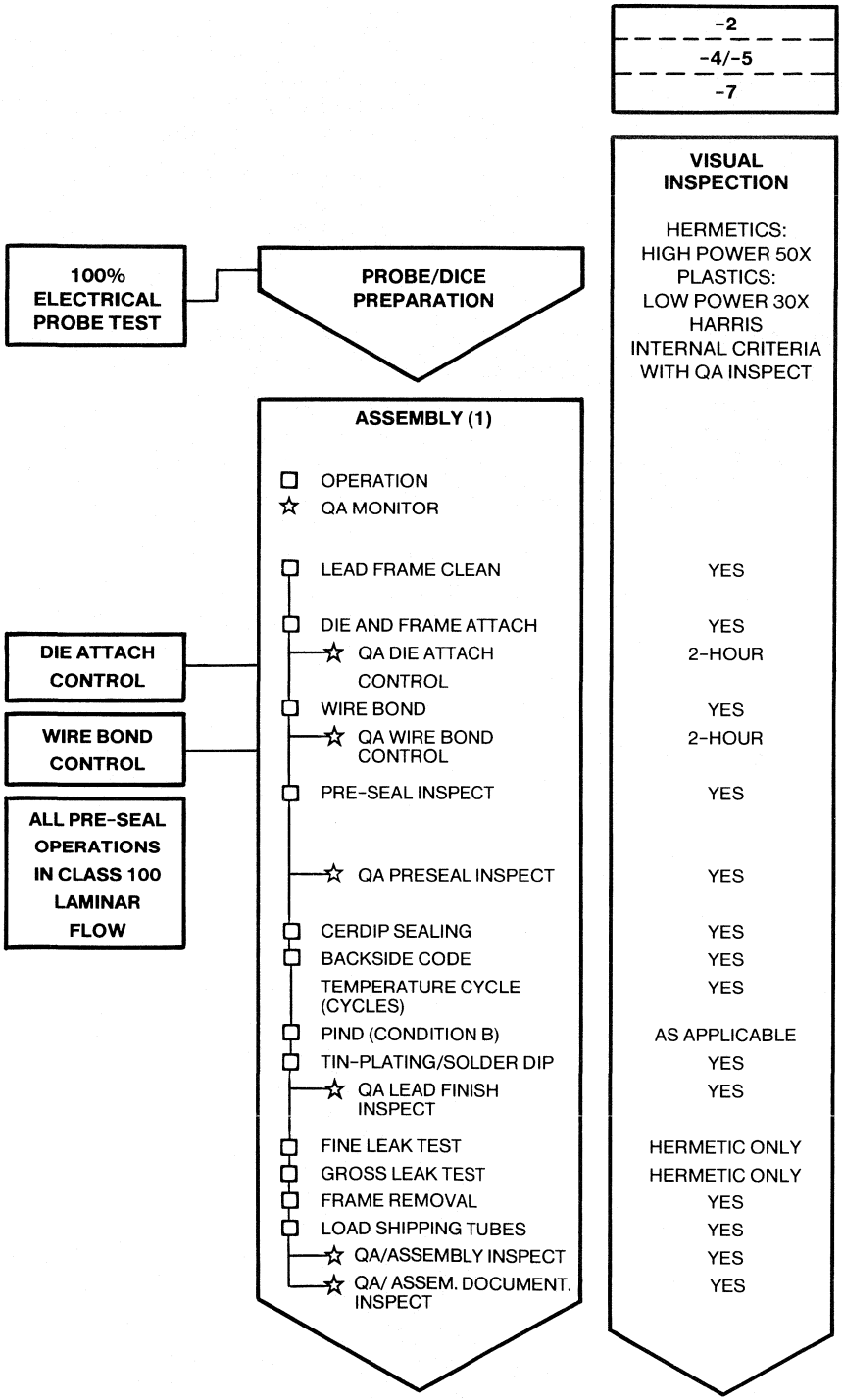
Applications Support

To obtain top system performance, it is not sufficient just to select high-quality components. It is necessary to apply those in ways which do not compromise the maximum ratings of the product or utilize them beyond their design capabilities. To assist customers in properly applying Harris Semiconductor products, Harris maintains a full staff of applications engineers in the field. The Harris field applications engineers (FAEs) assist customers in system design problems, product test problems, and utilization of Harris Semiconductor products in a wide variety of application situations. To obtain help from the Harris FAEs, simply contact your local field sales representative

Special Testing

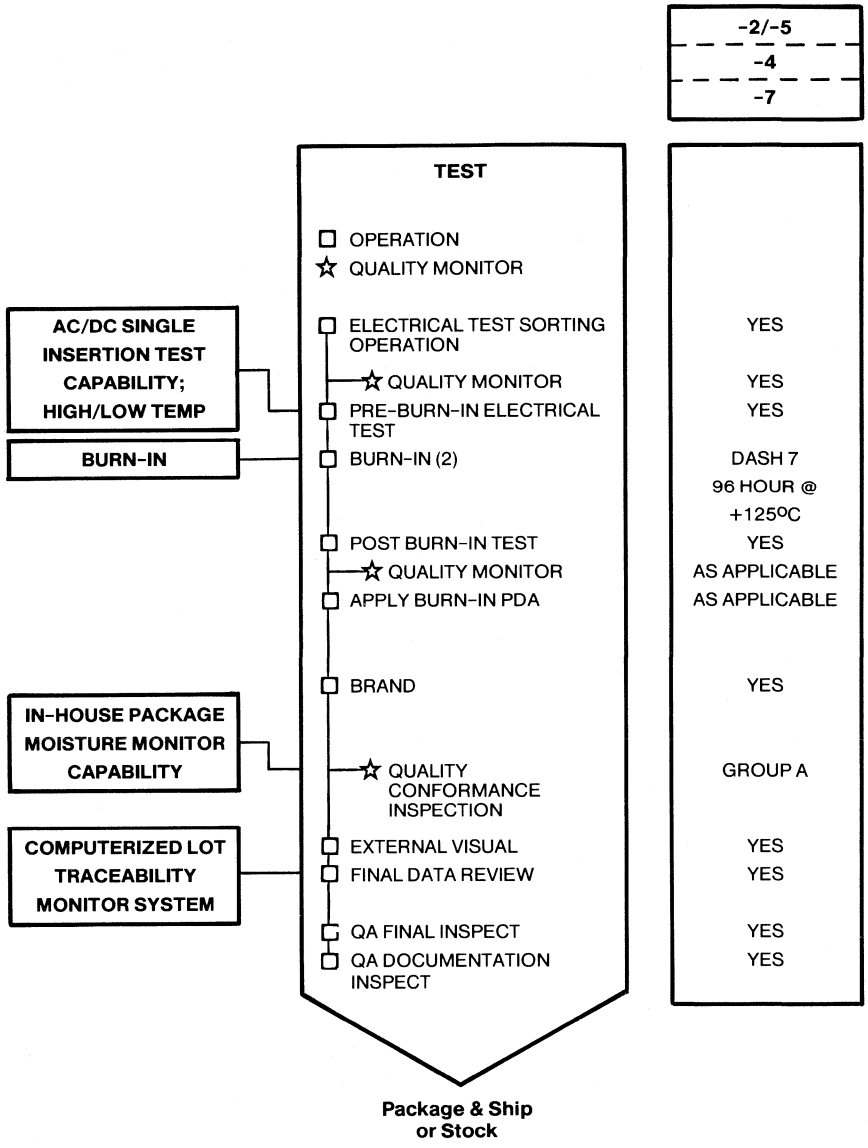
Harris Semiconductor offers several standard screen flows to support a customer's need for additional testing and reliability assurance. These flows include environmental stress testing, burn-in, and electrical testing at temperatures other than +25^{o}C. The flows shown below indicate the Harris standard screening processes. In addition, Harris can supply products tested to customer specifications both for electrical requirements and for non-standard environmental stress screening. Consult your field sales representative for details.

Harris Semiconductor
Commercial/Industrial Processing Flows



(1) Example for a Cerdip Package Part

Harris Semiconductor
Commercial/Industrial Processing Flows
(Continued)



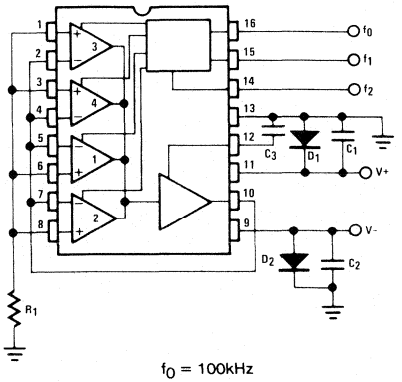
(2) Burn-In test temperatures can be increased and time reduced per regression tables in Mil-Std-883, Method 1015.

Burn-In Drawing Index

Burn-In Drawing Index (Continued)

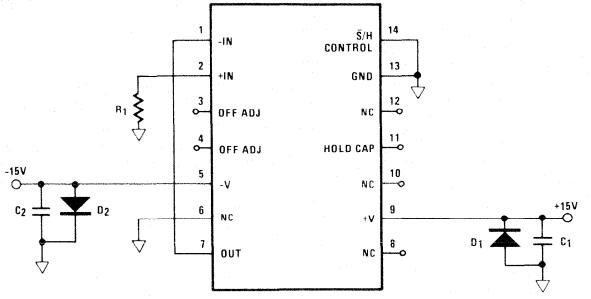
		Drawing Number
HI-1818A/1828A	Low Resistance Single 8/Differential 4 Channel CMOS Analog Multiplexers	73, 74, 75, 76
HI-200	Dual SPST CMOS Analog Switch	38, 39
HI-201	Quad SPST CMOS Analog Switch	40
HI-201HS	High Speed Quad SPST CMOS Switch	41
HI-300 thru 307	CMOS Analog Switches	42-49
HI-381/384	CMOS Analog Switches	50, 51, 52, 53
HI-387/390	CMOS Analog Switches	54, 55
HI-5040 thru 5051	CMOS Analog Switches	77
HI-5046A/5047A	CMOS Analog Switches	77
HI-506/507	Single 16/Differential 8 Channel CMOS Analog Multiplexers	57
HI-506A/507A	Single 16/Differential 8 Channel CMOS Analog Multiplexers with Active Overvoltage Protection	56, 57
HI-508/509	Single 8/Differential 4 Channel CMOS Analog Multiplexers	58, 59, 60, 61
HI-508A/509A	Single 8/Differential 4 Channel CMOS Analog Multiplexers with Active Overvoltage Protection	58, 59, 60,61
HI-516	16 Channel/Differential 8 Channel CMOS High Speed Analog Multiplexer	62, 63
HI-518	8 Channel/Differential 4 Channel CMOS High Speed Analog Multiplexer	64, 65
HI-524	4 Channel Wideband and Video Multiplexer	66, 67
HI-539	Monolithic, 4 Channel, Low Level, Differential Multiplexer	60, 61
HI-546/547	Single 16/Differential 8 Channel CMOS Analog Multiplexers with Active Overvoltage Protection	56, 57
HI-548/549	Single 8/Differential 4 Channel CMOS Analog Multiplexers with Active Overvoltage Protection	58, 59, 60, 61
HI-562A	12-Bit High Speed Monolithic Digital-to-Analog Converter	68, 69
HI-565A	High Speed Monolithic Digital-to-Analog Converter with Reference	70
HI-574A	Fast, Complete 12-Bit A/D Converter with Microprocessor Interface	71, 72
HI-674A	12μs, Complete 12-Bit A/D Converter with Microprocessor Interface	71, 72
HI-774	8.5μs, Complete 12-Bit A/D Converter with Microprocessor Interface	71, 72
HI-5618A/5618B	8-Bit High Speed Digital-to-Analog Converters	78
HI-5660/5660A	High Speed Monolithic Digital-to-Analog Converter	79
HI-5687	Wide Temperature Range Monolithic 12-Bit Digital-to-Analog Converter	80, 81, 82
HI-5697V	High Speed, 12-Bit Low Cost Monolithic Digital-to-Analog Converter	83, 84

1 HA-2400/04/05; HA-2406



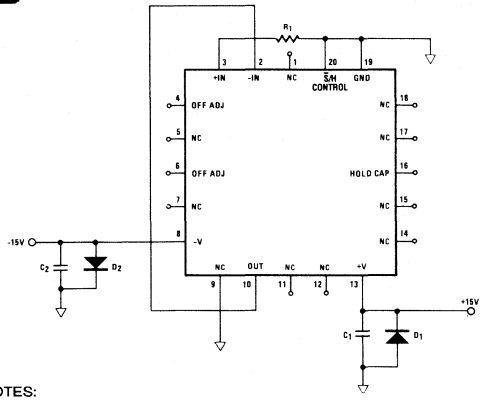
NOTES:
R_1 = 100kΩ
$C_1 = C_2$ = 0.1µF (one per row)
C_3 = 0.001µF
$D_1 = D_2$ = IN4002 or equivalent (one per board)
$|(V+) - (V-)|$ = 30V
f_0 = 100kHz
f_1 = 50kHz
f_2 = 25kHz

2 HA-2420/2425



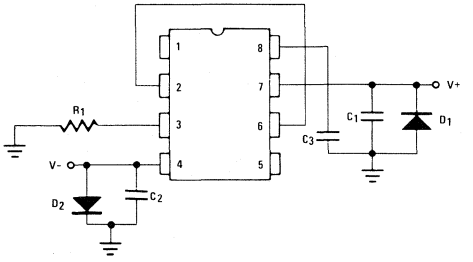
NOTES:
R_1 = 100kΩ ± 5% (per socket)
$C_1 = C_2$ = 0.1µF (one per row) or (0.01µF (one per socket)
$D_1 = D_2$ = IN4002 or equivalent (per board)

3 HA-2420/2425



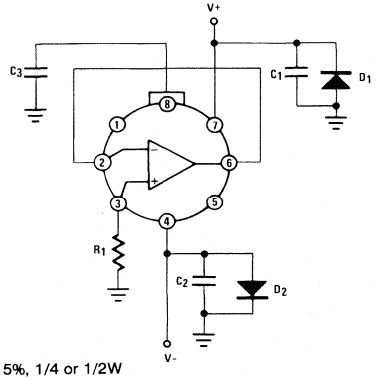
NOTES:
R_1 = 100kΩ ± 5% (per socket)
$C_1 = C_2$ = 0.1µF (one per row) or 0.01µF (one per socket)
$D_1 = D_2$ = IN4002 or equivalent (per board)

4 HA-2500/02/05; HA-2510/12/15; HA-2520/22/25; HA-2529 (CERAMIC MINI-DIP)



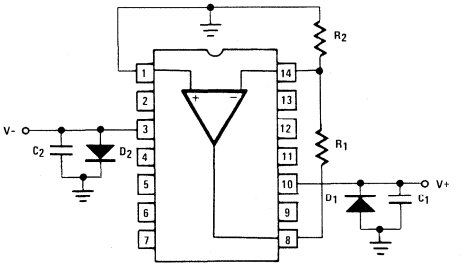
NOTES:
R_1 = 1MΩ ± 5%, 1/4 or 1/2W
$C_1 = C_2 = C_3$ = 0.01µF, ±10%
$D_1 = D_2$ = IN4002 or equivalent
$|(V+) - (V-)|$ = 30V

5 HA-2500/02/05; HA-2510/12/15; HA-2520/22/25; HA-2529; HA-5160/62 (TO-99 METAL CAN)



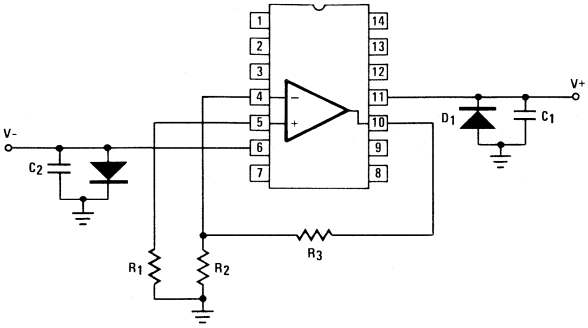
NOTES:
R_1 = 1MΩ ± 5%, 1/4 or 1/2W
$C_1 = C_2 = C_3$ = 0.01µF ± 10%
$D_1 = D_2$ = IN4002 or equivalent
$|(V+) - (V-)|$ = 30V

6 HA1-2539 (CERAMIC DIP)



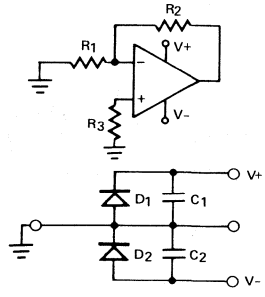
NOTES:
$C_1 = C_2$ = 0.1µF (per row) or 0.01µF (per socket)
$D_1 = D_2$ = IN4002 (one pair per board)
R_1 = 10kΩ
R_2 = 1kΩ
$|(V+) - (V-)|$ = 30V

7 HA-2540; HA-5190/5195 (CERAMIC DIP)



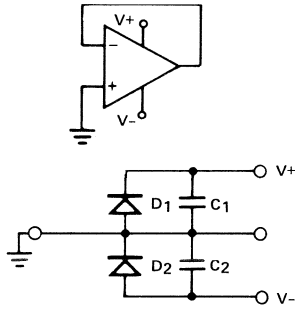
$R_1 = R_2 = 1k\Omega$
$R_3 = 10k\Omega$
$C_1 = C_2 = 0.1\mu F$ per socket
$D_1 = D_2$ = IN4002 or equivalent (per board)
$|(V+) - (V-)| = 30V$

8 HA-2541; HA-2542 (CERAMIC DIP OR TO-8 CAN)



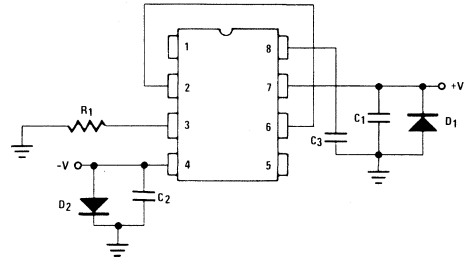
NOTES:
$R_1 = R_3 = 1k\Omega \pm 5\%$ (per socket)
$R_2 = 10k\Omega \pm 5\%$
$C_1 = C_2 = 0.01\mu F$
$D_1 = D_2$ = IN4002
$|(V+) - (V-)| = 30V$

9 HA-2544; HA-5170; HA-5180 (CERAMIC MINI-DIP OR TO-99 CAN)



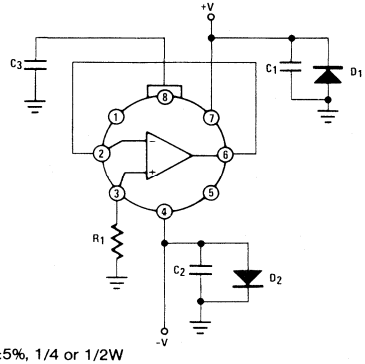
NOTES:
$C_1 = C_2 = 0.01\mu F$
$D_1 = D_2$ = IN4002
$|(V+) - (V-)| = 30V$

10 HA-2600/02/05; HA-2620/22/25 (CERAMIC MINI-DIP)



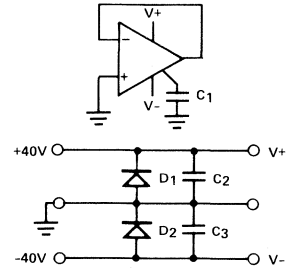
NOTES:
$R_1 = 1M\Omega \pm 5\%$, 1/4 or 1/2W
$C_1 = C_2 = C_3 = 0.01\mu F \pm 10\%$
$D_1 = D_2$ = IN4002 or equivalent
$|(V+) - (V-)| = 30V$

11 HA-2600/02/05; HA-2620/22/25 (TO-99 METAL CAN)



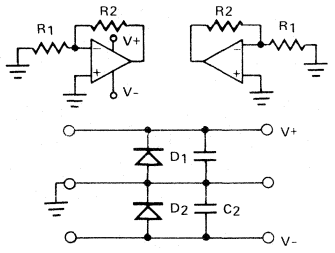
NOTES:
$R_1 = 1M\Omega \pm 5\%$, 1/4 or 1/2W
$C_1 = C_2 = C_3 = 0.01\mu F \pm 10\%$
$D_1 = D_2$ = IN4002 or equivalent
$|(V+) - (V-)| = 30V$

12 HA-2640/2645 (CERAMIC MINI-DIP OR TO-99 CAN)



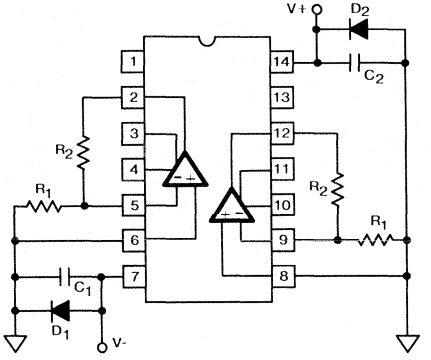
NOTES:
$C_1 = 0.01\mu F$
$C_2 = C_3 = 0.01\mu F$ (Min)
D_1, D_2 = IN4002

13 HA-2650/2655 (CERAMIC MINI-DIP OR TO-99 CAN)



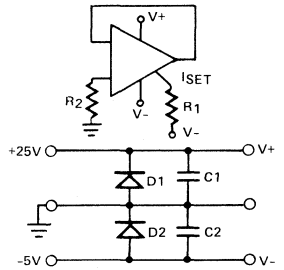
NOTES:
$R_1 = R_2 = 2k\Omega$
$C_1 = C_2 = 0.01\mu F$
$D_1 = D_2 = IN4002$
$|(V+) - (V-)| = 30V$

14 HA-2650/2655 (14 PIN CERAMIC DIP)



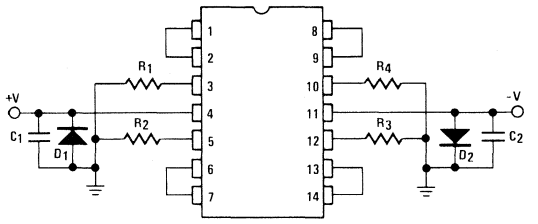
NOTES:
$R_1 = 1k\Omega \pm 5\%$
$R_2 = 10k\Omega \pm 5\%$
$C_1 = C_2 = 0.01\mu F$ (per row or per board)
$D_1 = D_2 = IN4002$ or equivalent
$|(V+) - (V-)| = 30V$

15 HA-2720/2725



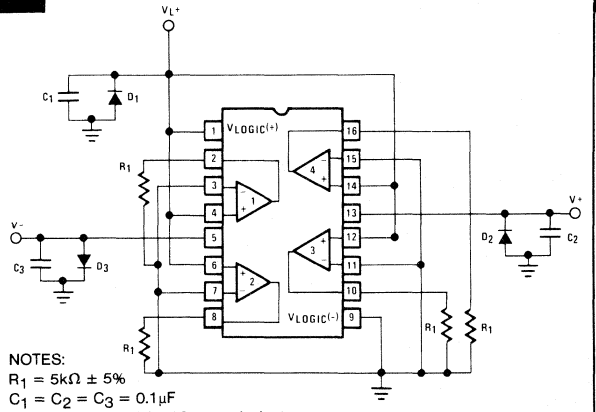
NOTES:
$R_1 = 2M\Omega$
$R_2 = 1M\Omega$
$C_1 = C_2 = 0.01\mu F$ (Min)
$D_1 = D_2 = IN4002$
$|(V+) - (V-)| = 30V$

16 HA-4741; HA-5134



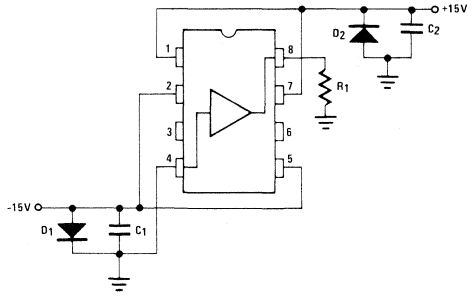
NOTES:
$R_1 = R_2 = R_3 = R_4 = 1M\Omega$
$C_1 = C_2 = 0.1\mu F$
$D_1 = D_2 = IN4002$ or equivalent
$|(V+) - (V-)| = 30V$

17 HA-4900/02/05



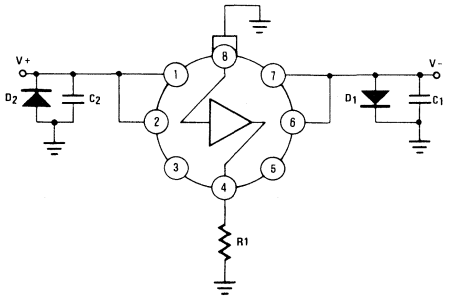
NOTES:
$R_1 = 5k\Omega \pm 5\%$
$C_1 = C_2 = C_3 = 0.1\mu F$
$D_1 = D_2 = D_3 = IN4002$ or equivalent
$V_{L+} = +5V$
$|(V+) - (V-)| = 30V$

18 HA-5002 (CERAMIC MINI-DIP)



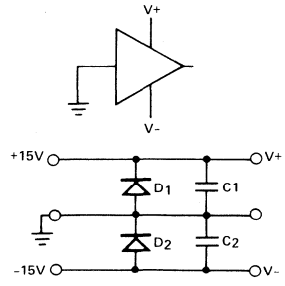
NOTES:
$R_1 = 1k\Omega \pm 5\%$
$C_1 = C_2 = 0.1\mu F$ (per row or per board)
$D_1 = D_2 = IN4002$ or equivalent

19 HA-5002 (TO-99 METAL CAN)



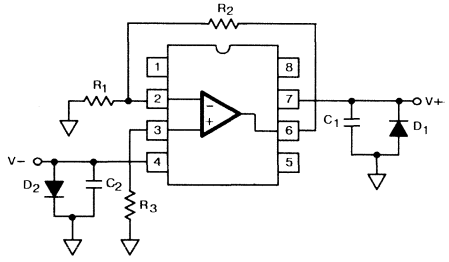
NOTES:
R_1 = 1kΩ ± 5%
$C_1 = C_2$ = 0.1µF (per row or per board)
$D_1 = D_2$ = IN4002 or equivalent
| (V+) - (V-) | = 30V

20 HA-5033



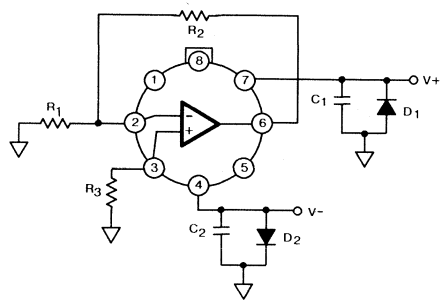
NOTES:
$C_1 = C_2$ = 0.01µF
$D_1 = D_2$ = IN4002

21 HA-5101; HA-5111; HA-5141; HA-5151 (CERAMIC MINI-DIP)



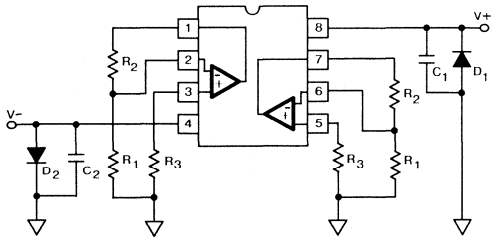
NOTES:
R_1 = 1kΩ ± 3%
R_2 = 10kΩ ± 3%
R_3 = 1kΩ ± 5%
$C_1 = C_2$ = 0.1µF (per row or per board)
$D_1 = D_2$ = IN4002 or equivalent
| (V+) - (V-) | = 30V

22 HA-5101; HA-5111; HA-5141; HA-5151 (TO-99 METAL CAN)



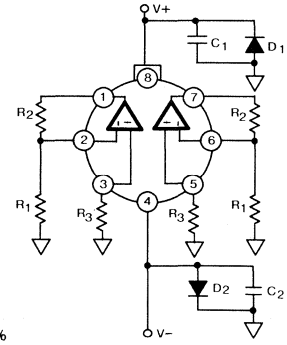
NOTES:
R_1 = 1kΩ ± 3%
R_2 = 10kΩ ± 3%
R_3 = 1kΩ ± 5%
$C_1 = C_2$ = 0.1µF (per row or per board)
D_1, D_2 = IN4002 or equivalent
| (V+) - (V-) | = 30V

23 HA-5102; HA-5112; HA-5142; HA-5152 (CERAMIC MINI-DIP)



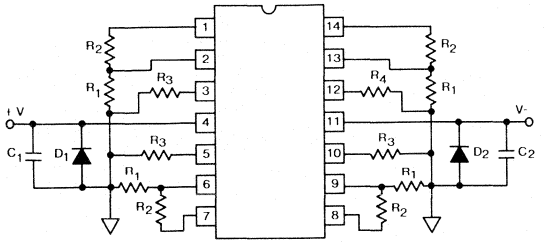
NOTES:
R_1 = 1kΩ ± 3%
R_2 = 10kΩ ± 3%
R_3 = 1kΩ ± 5%
$C_1 = C_2$ = 0.1µF (per row or per board)
D_1, D_2 = IN4002 or equivalent
| (V+) - (V-) | = 30V

24 HA-5102; HA-5112; HA-5142; HA-5152 (TO-99 METAL CAN)



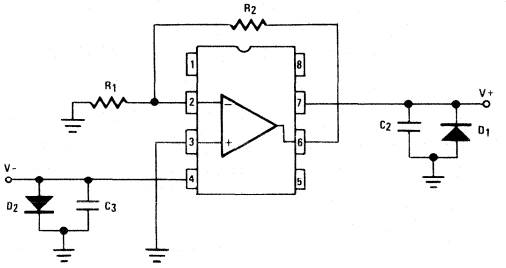
NOTES:
R_1 = 1kΩ ± 3%
R_2 = 10kΩ ± 3%
R_3 = 1kΩ ± 5%
$C_1 = C_2$ = 0.1µF (per row or per board)
D_1, D_2 = IN4002 or equivalent
| (V+) - (V-) | = 30V

25 HA-5104; HA-5114



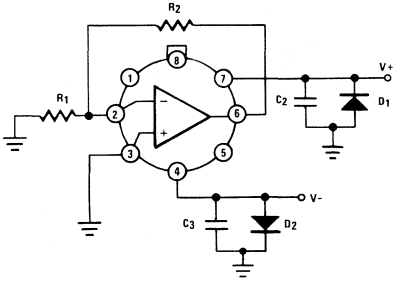
NOTES:
R_1 = 1kΩ ± 3%
R_2 = 10kΩ ± 3%
R_3 = 1kΩ ± 5%
$C_1 = C_2$ = 0.1µF (one per row)
$D_1 = D_2$ = IN4002 or equivalent
$|(V+) - (V-)| = 30V$

26 HA-5127; HA-5130/5135; HA-5137; HA-5147; HA-5177 (CERAMIC MINI-DIP)



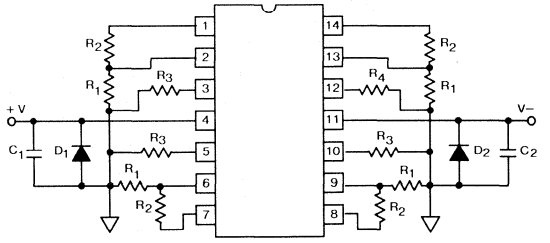
NOTES:
R_1 = 1kΩ ± 5%
R_2 = 10kΩ ± 5%
$C_2 = C_3$ = 0.1µF (per row or per board)
$D_1 = D_2$ = IN4002 or equivalent
$|(V+) - (V-)| = 30V$

27 HA-5127; HA-5130/5135; HA-5137; HA-5147; HA-5177 (TO-99 METAL CAN)



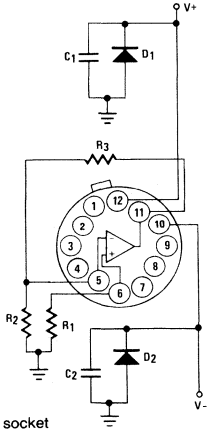
NOTES:
R_1 = 1kΩ ± 5%
R_2 = 10kΩ ± 5%
$C_2 = C_3$ = 0.1µF (per row or per board)
$D_1 = D_2$ = IN4002 or equivalent
$|(V+) - (V-)| = 30V$

28 HA-5144; HA-5154



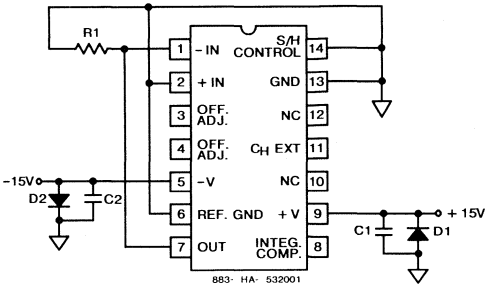
NOTES:
R_1 = 1kΩ ± 3%
R_2 = 10kΩ ± 3%
R_3 = 1kΩ ± 5%
$C_1 = C_2$ = 0.01µF (Min)
$D_1 = D_2$ = IN4002
$|(V+) - (V-)| = 30V$

29 HA-5190/5195 (TO-8 METAL CAN)



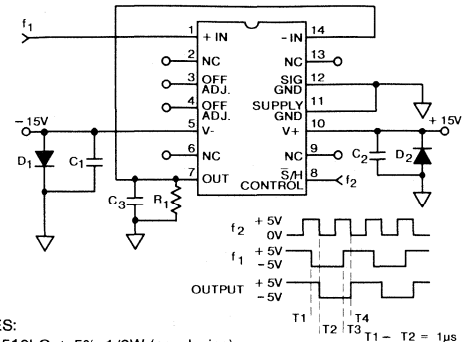
NOTES:
$R_1 = R2$ = 1kΩ
R_3 = 10kΩ
$C_1 = C_2$ = 0.1µF per socket
$D_1 = D_2$ = IN4002 or equivalent (per board)
$|(V+) - (V-)| = 30V$

30 HA-5320



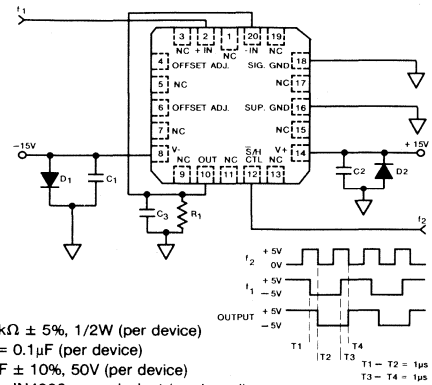
NOTES:
R_1 = 10kΩ
$D_1 = D_2$ = IN4002
$C_1 = C_2$ = 0.01µF

31 HA-5330



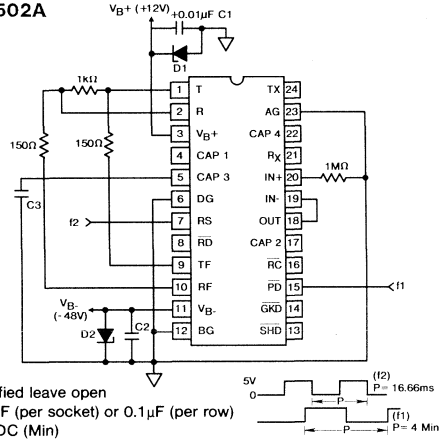
NOTES:
R_1 = 510kΩ ± 5%, 1/2W (per device)
$C_1 = C_2$ = 0.1µF (per device)
C_3 = 47pF ± 10%, 50V (per device)
$D_1 = D_2$ = IN4002 or equivalent (per board)
f2 = 250kHz, TTL levels, 50% duty cycle
f1 = 125kHz, +5V to -5V, 50% duty cycle

32 HA-5330 (LCC)



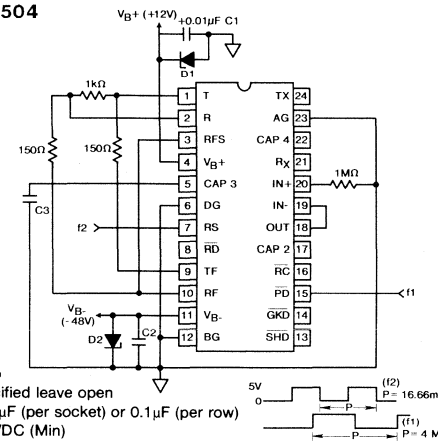
NOTES:
R_1 = 510kΩ ± 5%, 1/2W (per device)
$C_1 = C_2$ = 0.1µF (per device)
C_3 = 47pF ± 10%, 50V (per device)
$D_1 = D_2$ = IN4002 or equivalent (per board)
f2 = 250kHz, TTL levels, 50% duty cycle
f1 = 125kHz, +5V to -5V, 50% duty cycle

33 HC-5502A



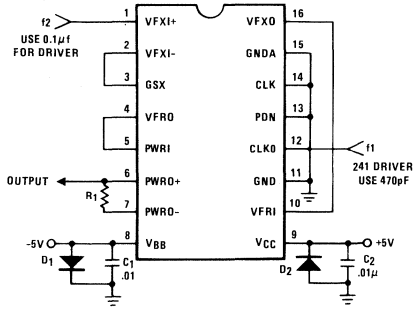
NOTES:
All resistors 10%
All pins not specified leave open
$C_1 = C_2$ = 0.01µF (per socket) or 0.1µF (per row)
C_3 = 0.3µF; 30VDC (Min)
f1 = 1/240Hz, 0-5V square wave, TTL level, 50% duty cycle
f2 = 60Hz, 0-5V square wave, TTL level, 50% duty cycle
$D_1 = D_2$ = transient protection

34 HC-5504



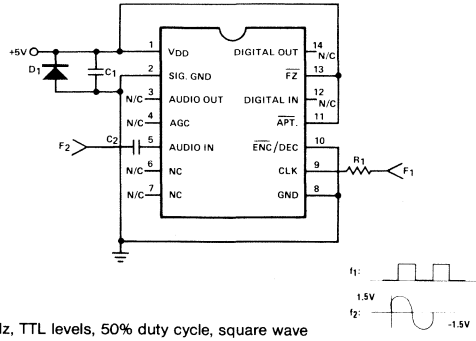
NOTES:
All resistors 10%
All pins not specified leave open
$C_1 = C_2$ = 0.01µF (per socket) or 0.1µF (per row)
C_3 = 0.3µF; 30VDC (Min)
f1 = 1/240Hz, 0-5V square wave, TTL level, 50% duty cycle
f2 = 60Hz, 0-5V square wave, TTL level, 50% duty cycle
$D_1 = D_2$ = transient protection

35 HC-5512; HC-5512A; HC-5512D



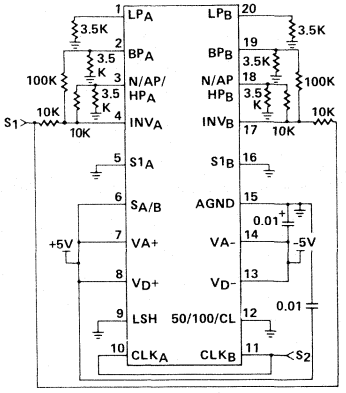
NOTES:
f1 = TTL, 50% duty cycle
f1 = 100kHz
f2 = 2.0V_{p-p} at ≃100Hz
C_1, C_2 = 0.01µF
D_1, D_2 = IN4002
R_1 = 600Ω

36 HC-55564



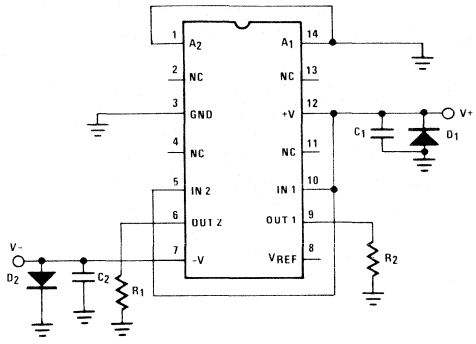
NOTES:
f1 = 16kHz, TTL levels, 50% duty cycle, square wave
f2 ≃ 200Hz (approximate), 3V_{p-p}
Sine wave (or triangle wave)
C_1 = 0.01µF
C_2 = 0.1µF
D_1 = IN4002
R_1 = 10kΩ ± 10%, 1/4W

37 HF-10



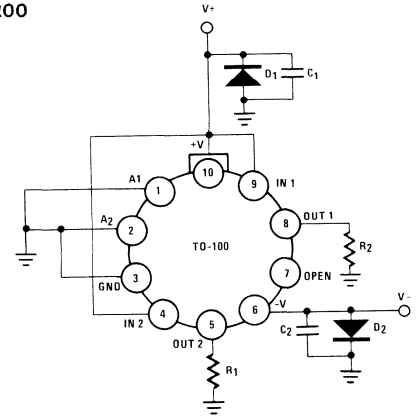
NOTES:
S_1 = 1kHz, 5.0V_{p-p} sine wave
S_2 = 100kHz, clock, +5V to GND
All caps are in µF

38 HI-200



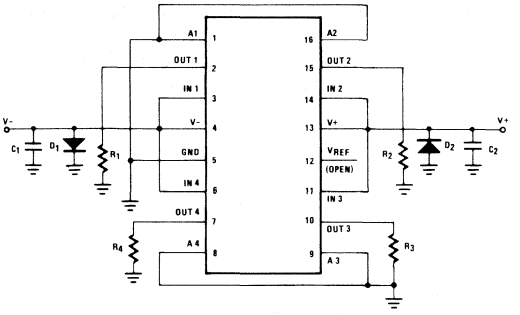
NOTES:
$R_1 = R_2 = 10k\Omega$
$C_1 = C_2 = 0.1\mu F$ (one per row)
$D_1 = D_2$ = IN4002 or equivalent
| (V+) - (V-) | = 30V

39 HI-200



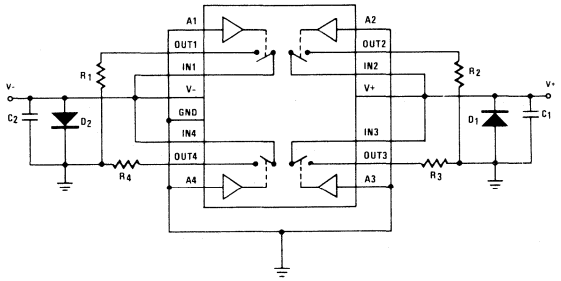
NOTES:
$R_1 = R_2 = 10k\Omega$
$C_1 = C_2 = 0.1\mu F$ (one per row)
$D_1 = D_2$ = IN4002 or equivalent
| (V+) - (V-) | = 30V

40 HI-201



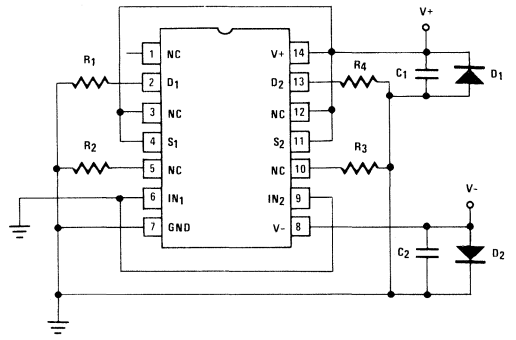
NOTES:
$R_1 = R_2 = R_3 = R_4 = 10k\Omega$
$C_1 = C_2 = 0.1\mu F$
$D_1 = D_2$ = IN4002 or equivalent
| (V+) - (V-) | = 30V

41 HI-201HS



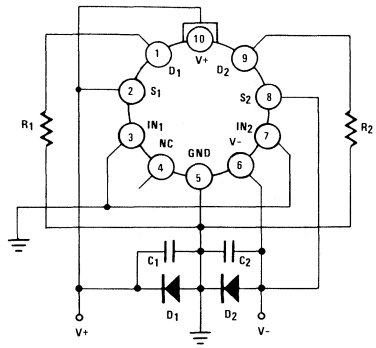
NOTES:
$R_1 = R_2 = R_3 = R_4 = 10k\Omega \pm 5\%$, 1/4 or 1/2W
$C_1 = C_2 = 0.1\mu F$ (one per row) or 0.01µF (one per socket)
$D_1 = D_2$ = IN4002 or equivalent (one per board)
| (V+) - (V-) | = 30V

42 HI-300; HI-305



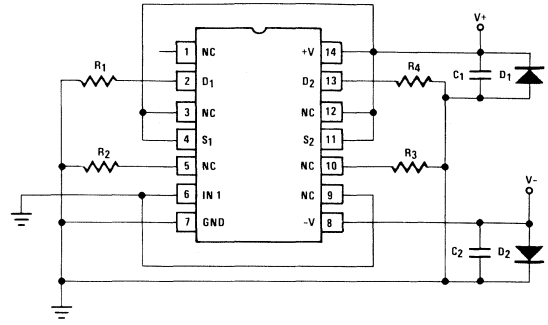
NOTES:
$R_1 = R_2 = R_3 = R_4 = 10k\Omega \pm 5\%$, 1/4 or 1/2W
$C_1 = C_2 = 0.01\mu F$ (per socket) or 0.1µF (per row)
$D_1 = D_2$ = IN4002 (per board)
| (V+) - (V-) | = 30V

43 HI-300



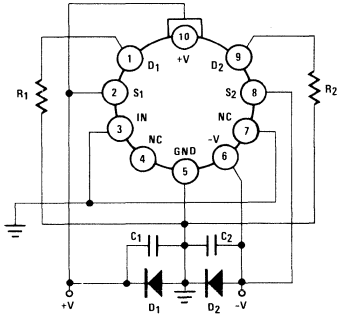
NOTES:
$R_1 = R_2 = 10k\Omega \pm 5\%$, 1/4 or 1/2W
$C_1 = C_2 = 0.01\mu F$ (per socket) or $0.1\mu F$ (per row)
$D_1 = D_2$ = IN4002 (per board)
$|(V+) - (V-)| = 30V$

44 HI-301



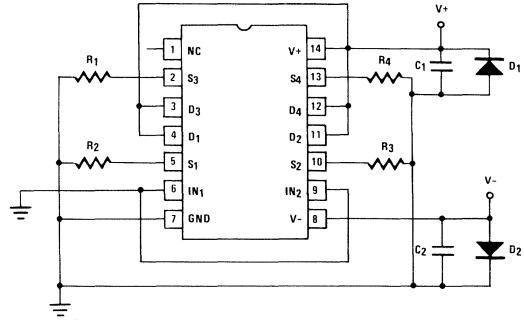
NOTES:
$R_1 = R_2 = R_3 = R_4 = 10k\Omega \pm 5\%$ (per socket)
$C_1 = C_2 = 0.01\mu F$ (per socket) or $0.1\mu F$ (per row)
$D_1 = D_2$ = IN4002 equivalent (per board)
$|(V+) - (V-)| = 30V$

45 HI-301; HI-305



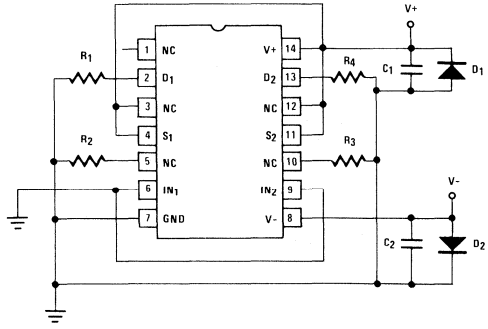
NOTES:
$R_1 = R_2 = 10k\Omega \pm 5\%$ (per socket)
$C_1 = C_2 = 0.01\mu F$ (per socket) or $0.1\mu F$ (per row)
$D_1 = D_2$ = IN4002 equivalent (per board)
$|(V+) - (V-)| = 30V$

46 HI-302; HI-303



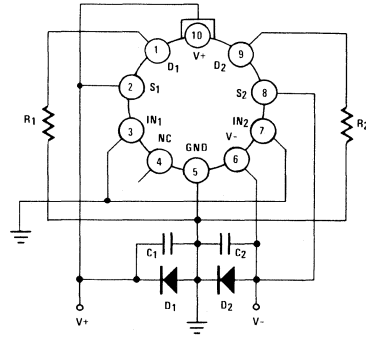
NOTES:
$R_1 = R_2 = R_3 = R_4 = 10k\Omega \pm 5\%$, 1/4 or 1/2W
$C_1 = C_2 = 0.01\mu F$ (per socket) or $0.1\mu F$ (per row)
$D_1 = D_2$ = IN4002 (per board)
$|(V+) - (V-)| = 30V$

47 HI-304



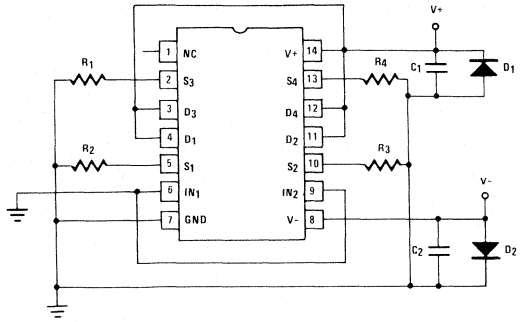
NOTES:
$R_1 = R_2 = 10k\Omega \pm 5\%$ (per socket)
$C_1 = C_2 = 0.01\mu F$ (per socket) or $0.1\mu F$ (per row)
$D_1 = D_2$ = IN4002 or equivalent (per board)
$|(V+) - (V-)| = 30V$

48 HI-304



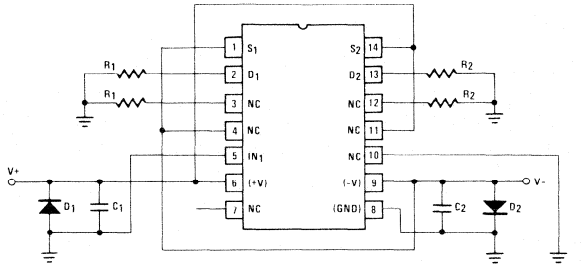
NOTES:
$R_1 = R_2 = 10k\Omega \pm 5\%$ (per socket)
$C_1 = C_2 = 0.01\mu F$ (per socket) or $0.1\mu F$ (per row)
$D_1 = D_2$ = IN4002 or equivalent (per board)
$|(V+) - (V-)| = 30V$

49 HI-306; HI-307



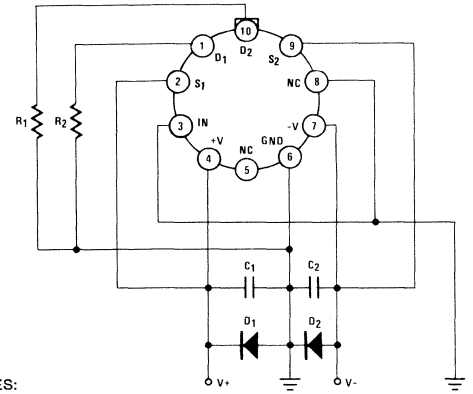
NOTES:
$R_1 = R_2 = R_3 = R_4 = 10k\Omega \pm 5\%$, 1/4 or 1/2W
$C_1 = C_2 = 0.01\mu F$ (per socket) or $0.1\mu F$ (per board)
$D_1 = D_2$ = IN4002 (per board)
$|(V+) - (V-)| = 30V$

50 HI-381



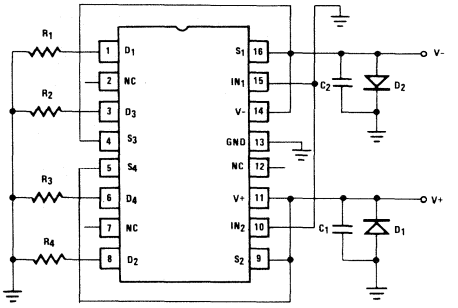
NOTES:
$R_1 = R_2 = 10k\Omega \pm 5\%$ (per socket)
$C_1 = C_2 = 0.01\mu F$ (per socket) or $0.1\mu F$ (per row)
$D_1 = D_2$ = IN4002 equivalent (per board)
$|(V+) - (V-)| = 30V$

51 HI-381



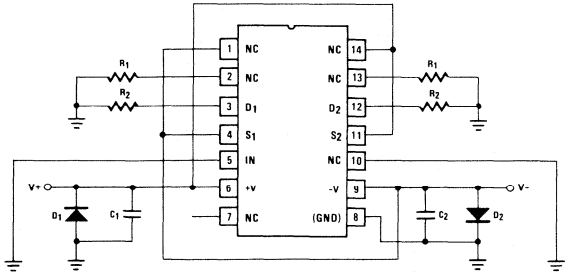
NOTES:
$R_1 = R_2 = 10k\Omega \pm 5\%$ (per socket)
$C_1 = C_2 = 0.01\mu F$ (per socket) or $0.1\mu F$ (per row)
$D_1 = D_2$ = IN4002 equivalent (per board)
$|(V+) - (V-)| = 30V$

52 HI-384



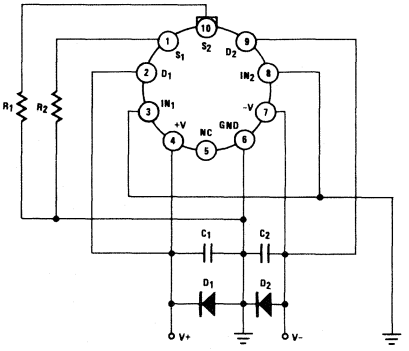
NOTES:
$R_1 = R_2 = R_3 = R_4 = 10k\Omega \pm 5\%$, 1/4 or 1/2W
$C_1 = C_2 = 0.01\mu F$ (per socket) or $0.1\mu F$ (per row)
$D_1 = D_2$ = IN4002 or equivalent (per board)
$|(V+) - (V-)| = 30V$

53 HI-387



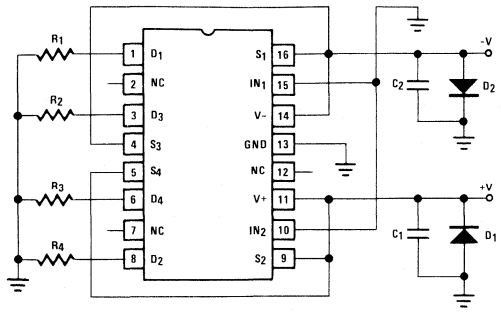
NOTES:
$R_1 = R_2 = 10k\Omega \pm 5\%$ (per socket)
$C_1 = C_2 = 0.01\mu F$ (per socket) or $0.1\mu F$ (per row)
$D_1 = D_2$ = IN4002 or equivalent (per board)
$|(V+) - (V-)| = 30V$

54 HI-387



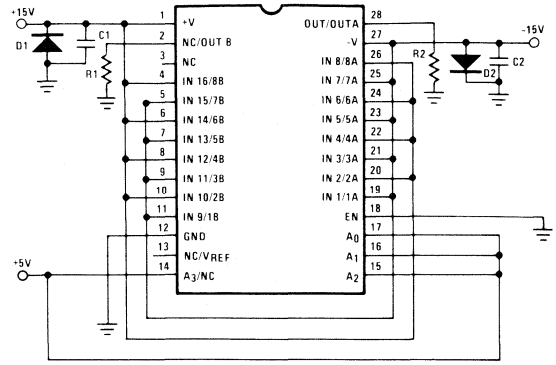
NOTES:
$R_1 = R_2 = 10k\Omega \pm 5\%$ (per socket)
$C_1 = C_2 = 0.01\mu F$ (per socket) or $0.1\mu F$ (per row)
$D_1 = D_2$ = IN4002 or equivalent (per board)
$|(V+) - (V-)| = 30V$

55 HI-390



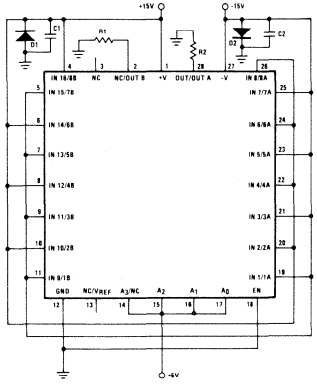
NOTES:
$R_1 = R_2 = R_3 = R_4 = 10k\Omega \pm 5\%$, 1/4 or 1/2W
$C_1 = C_2 = 0.01\mu F$ (per socket) or $0.1\mu F$ (per row)
$D_1 = D_2$ = IN4002 (per board)
$|(V+) - (V-)| = 30V$

56 HI-506/HI-507; HI-506A/HI-507A; HI-546/HI-547



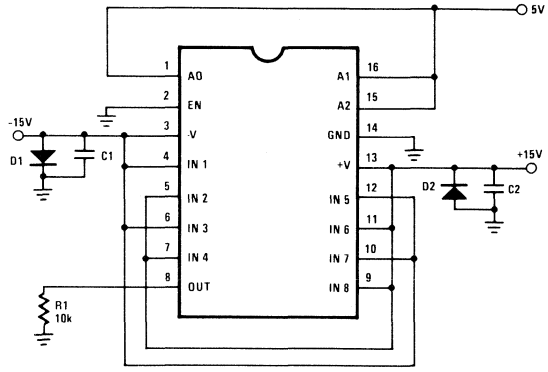
NOTES:
$R_1 = R_2$ 10k$\Omega \pm 5\%$, 1/4 or 1/2W (per socket)
$C_1 = C_2 = 0.01\mu F$ (per socket) or $0.1\mu F$ (per row)
$D_1 = D_2$ = IN4002 or equivalent (per board)

57 HI-506/HI-507; HI-506A/HI-507A; HI-546/HI-547 (LCC)



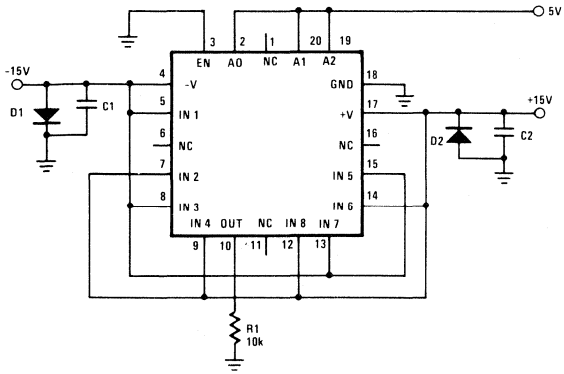
NOTES:
$R_1 = R_2$ 10k$\Omega \pm 5\%$, 1/4 or 1/2W (per socket)
$C_1 = C_2 = 0.01\mu F$ (per socket) or $0.1\mu F$ (per row)
$D_1 = D_2$ = IN4002 equivalent (per board)

58 HI-508; HI-508A; HI-548



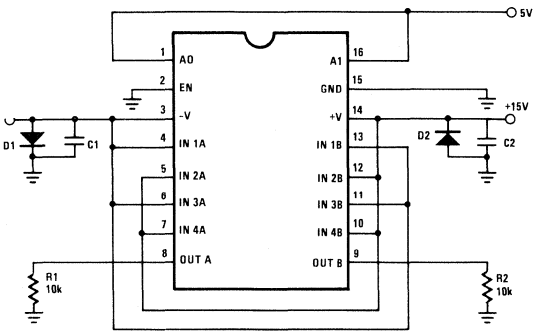
NOTES:
$R_1 = 10k\Omega \pm 5\%$, 1/4 or 1/2W (per socket)
$C_1 = C_2 = 0.01\mu F$ (per socket) or $0.1\mu F$ (per row)
$D_1 = D_2$ = IN4002 or equivalent (per board)

59 HI-508; HI-508A; HI-548 (LCC)



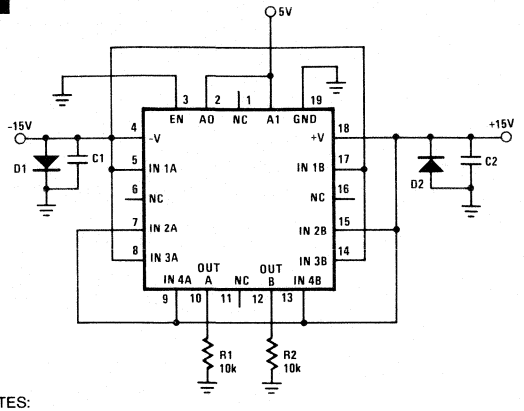
NOTES:
$R_1 = 10k\Omega \pm 5\%$, 1/2 or 1/4W (per socket)
$C_1 = C_2 = 0.01\mu F$ (per socket) or $0.1\mu F$ (per row)
$D_1 = D_2$ = IN4002 or equivalent (per board)

60 HI-509/HI-509A; HI-539; HI-549



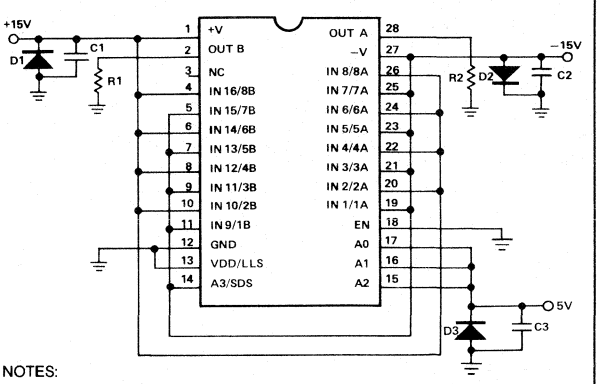
NOTES:
$R_1, R_2 = 10k\Omega \pm 5\%$, 1/4 or 1/2W (per socket)
$C_1 = C_2 = 0.01\mu F$ (per socket) or $0.1\mu F$ (per row)
$D_1 = D_2$ = IN4002 or equivalent (per board)

61 HI-509/HI-509A; HI-539; HI-549 (LCC)



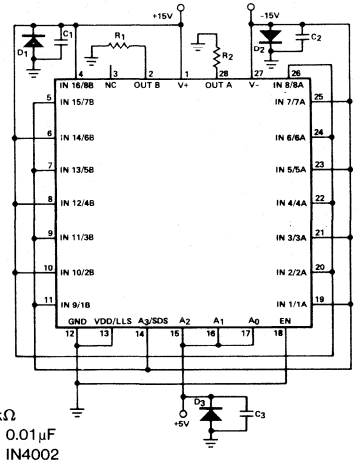
NOTES:
$R_1 = R_2$ 10kΩ ± 5%, 1/4 or 1/2W (per socket)
$C_1 = C_2$ = 0.01µF (per socket) or 0.1µF (per row)
$D_1 = D_2$ = IN4002 or equivalent (per board)

62 HI-516



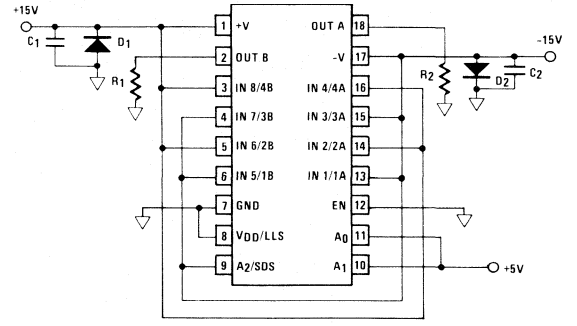
NOTES:
R_1, R_2 = 10kΩ
C_1, C_2, C_3 = 0.01µF
D_1, D_2, D_3 = IN4002

63 HI-516 (LCC)



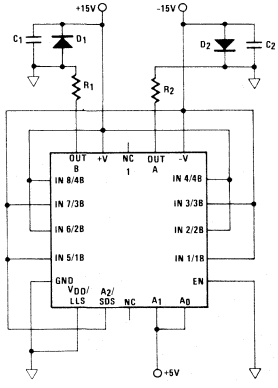
NOTES:
R_1, R_2 = 10kΩ
C_1, C_2, C_3 = 0.01µF
D_1, D_2, D_3 = IN4002

64 HI-518



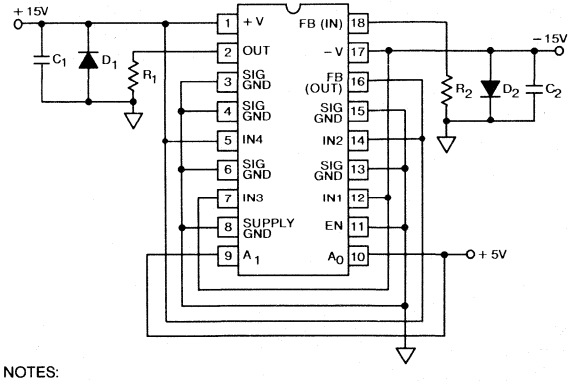
NOTES:
$R_1 = R_2$ = 10kΩ ± 5%, 1/4 or 1/2W
$C_1 = C_2$ = 0.01µF (one per socket) or 0.1µF (one per row)
$D_1 = D_2$ = IN4002 or equivalent (per board)

65 HI-518 (LCC)



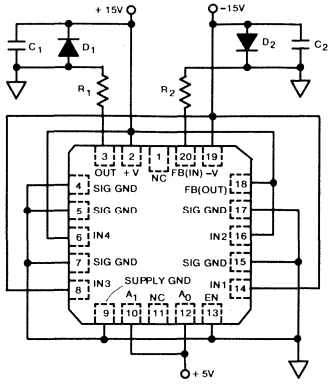
NOTES:
$R_1 = R_2$ = 10kΩ ± 5%, 1/4 or 1/2W (per socket)
$C_1 = C_2$ = 0.01µF (one per socket) or 0.1µF (one per row)
$D_1 = D_2$ = IN4002 or equivalent (per board)

66 HI-524



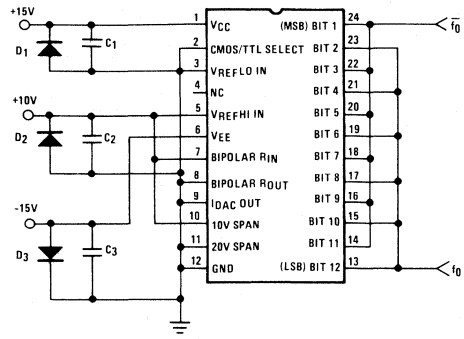
NOTES:
$R_1 = R_2$ =10kΩ ± 5%, 1/4 or 1/2W (per socket)
$C_1 = C_2$ = 0.01µF (one per socket) or 0.1µF (one per row)
$D_1 = D_2$ = IN4002 or equivalent (per board)

67 HI-524 (LCC)



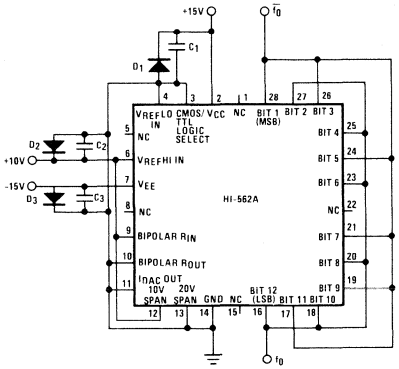
NOTES:
$R_1 = R_2 = 10k\Omega \pm 5\%$, 1/4 or 1/2W (per socket)
$C_1 = C_2 = 0.01\mu F$ (one per socket) or $0.1\mu F$ (one per row)
$D_1 = D_2$ = IN4002 or equivalent (per board)

68 HI-562A



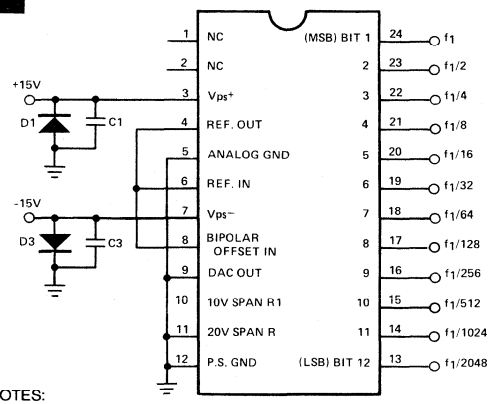
NOTES:
$C_1 = C_2 = C_3 = 0.01\mu F$ (per socket) or $0.1\mu F$ (per row)
$D_1 = D_2 = D_3$ = IN4002 or equivalent (per board)
f_0 = 100kHz; TTL levels 50% duty cycle

69 HI-562A (LCC)



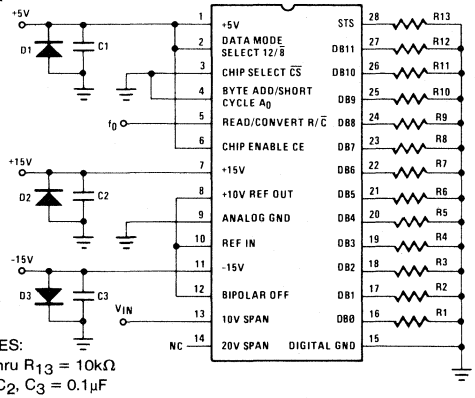
NOTES:
$C_1 = C_2 = C_3 = 0.01\mu F$ (per socket) or $0.1\mu F$ (per row)
$D_1 = D_2 = D_3$ = IN4002 or equivalent (per board)
f_0 = 100kHz; TTL levels 50% duty cycle

70 HI-565A



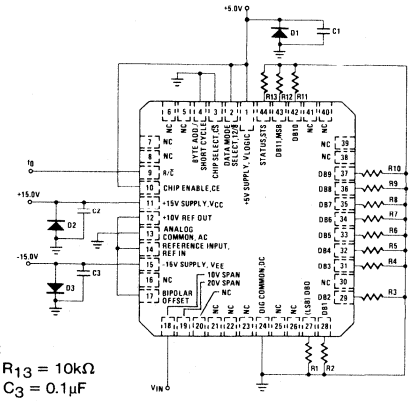
NOTES:
$C_1, C_3 = 0.01\mu F$
D_1, D_3 = IN4002
f_1 = 100kHz

71 HI-574A; HI-674A, HI-774



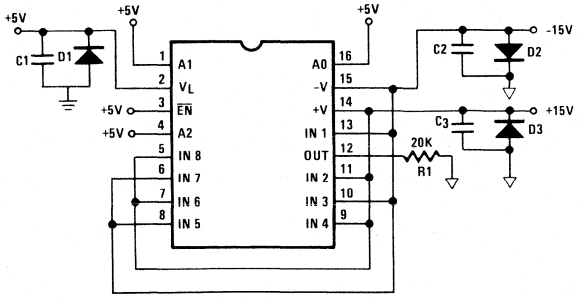
NOTES:
R_1 thru $R_{13} = 10k\Omega$
$C_1, C_2, C_3 = 0.1\mu F$
D_1, D_2, D_3 = IN4002
V_{IN} = triangle wave, +5V to -5V, 1kHz
f_0 = square wave, 10kHz, 90% duty cycle, 0V to 5V

72 HI-574A; HI-674A; HI-774 (LCC)



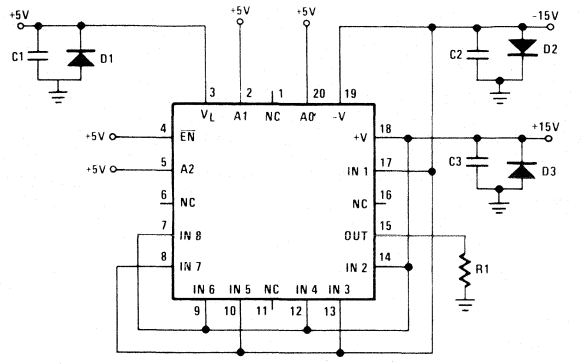
NOTES:
R_1 thru $R_{13} = 10k\Omega$
$C_1, C_2, C_3 = 0.1\mu F$
D_1, D_2, D_3 = IN4002
V_{IN} = triangle wave, +5V to -5V, 1kHz
f_0 = square wave, 10kHz, 90% duty cycle, 0V to 5V

73 HI-1818A



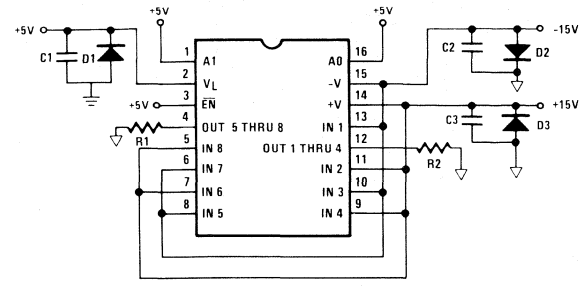
NOTES:
R_1 = 20kΩ ± 5%, 1/4 or 1/2W (per socket)
C_1, C_2, C_3 = 0.01μF (per socket) or 0.1μF (per row)
D_1, D_2, D_3 = IN4002 or equivalent (per board)

74 HI-1818A (LCC)



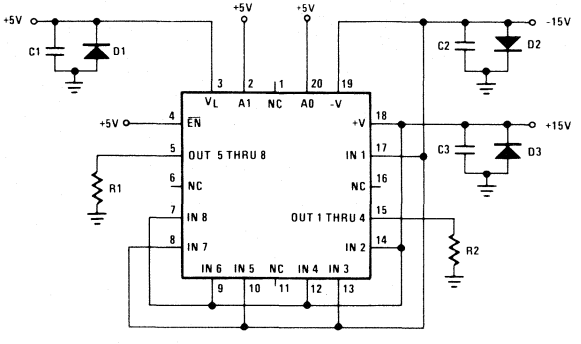
NOTES:
R_1 = 20kΩ ± 5%, 1/4 or 1/2W (per socket)
C_1, C_2, C_3 = 0.01μF (per socket) or 0.1μF (per row)
D_1, D_2, D_3 = IN4002 or equivalent (per board)

75 HI-1828A



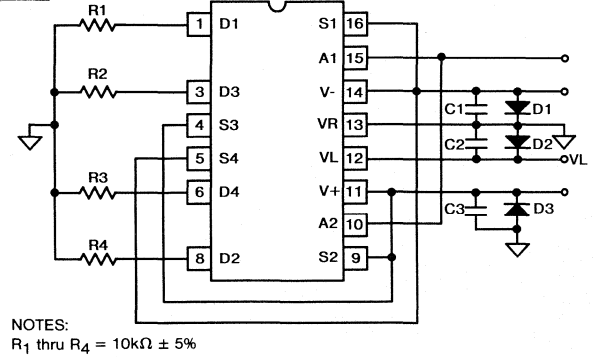
NOTES:
R_1, R_2 = 20kΩ ± 5%, 1/4 or 1/2W (per socket)
C_1, C_2, C_3 = 0.01μF (per socket) or 0.1μF (per row)
D_1, D_2, D_3 = IN4002 or equivalent (per board)

76 HI-1828A (LCC)



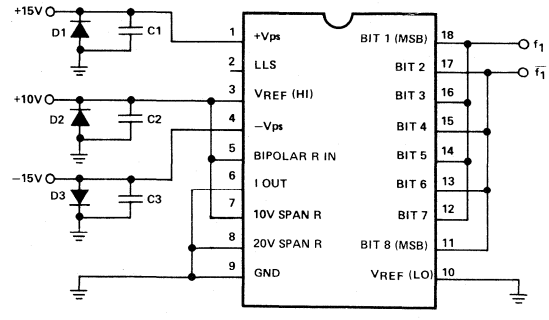
NOTES:
R_1, R_2 = 20kΩ ± 5%, 1/4 or 1/2W (per socket)
C_1, C_2, C_3 = 0.01μF (per socket) or 0.1μF (per row)
D_1, D_2, D_3 = IN4002 or equivalent (per board)

77 HI-5040 Thru HI-5051



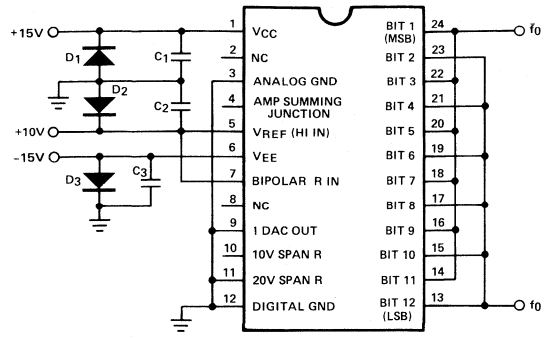
NOTES:
R_1 thru R_4 = 10kΩ ± 5%
C_1, C_2, C_3 = 0.1μF
D_1, D_2, D_3 = IN4002
V_L = +5V
$A_1 = A_2$ = +5V
| (V+) - (V-) | = 30V

78 HI-5618A/HI-5618B



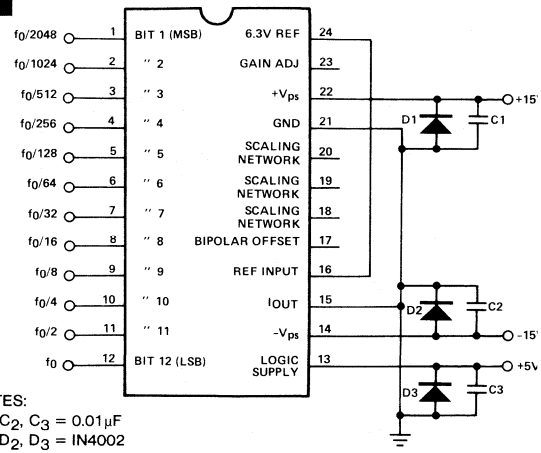
NOTES:
C_1, C_2, C_3 = 0.1μF
D_1, D_2, D_3 = IN4002 or similar
f_1 = 100kHz, TTL level, 50% duty cycle

79 HI-5660/HI-5660A



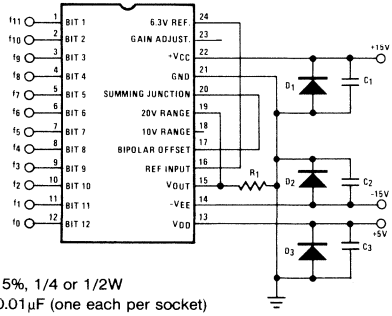
NOTES:
C_1, C_2, C_3 = 0.01µF
D_1, D_2, D_3 = IN4002
f_0 = 100kHz, 50% duty cycle

80 HI-5687(I)



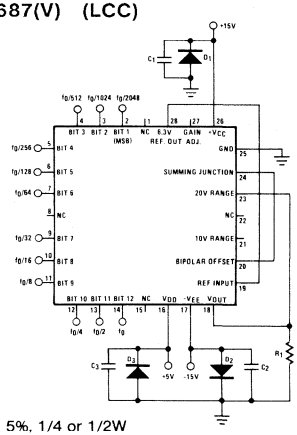
NOTES:
C_1, C_2, C_3 = 0.01µF
D_1, D_2, D_3 = IN4002
f_0 = 100kHz, TTL logic levels

81 HI-5687(V)



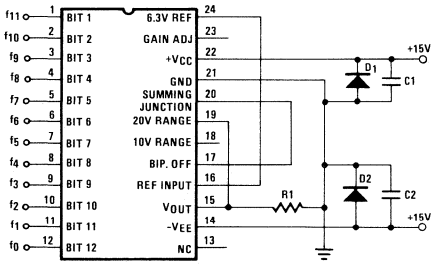
NOTES:
R_1 = 2.0kΩ ± 5%, 1/4 or 1/2W
C_1, C_2, C_3 = 0.01µF (one each per socket)
D_1, D_2, D_3 = IN4002 (one each per board)
f_0 = 100kHz, TTL logic levels
$f_1 = f_0/2$
$f_2 = f_0/4$
$f_3 = f_0/8$
$f_4 = f_0/16$
$f_5 = f_0/32$
$f_6 = f_0/64$, TTL logic levels
$f_7 = f_0/128$
$f_8 = f_0/256$
$f_9 = f_0/512$
$f_{10} = f_0/1024$
$f_{11} = f_0/2048$

82 HI-5687(V) (LCC)



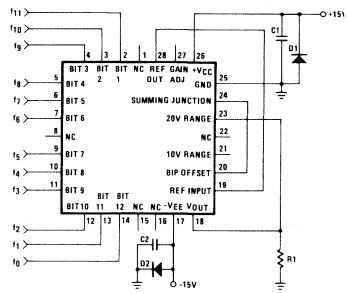
NOTES:
R_1 = 2.0kΩ ± 5%, 1/4 or 1/2W
C_1, C_2, C_3 = 0.01µF (one each per socket)
D_1, D_2, D_3 = IN4002 (one each per board)
f_0 = 100kHz (TTL logic level)

83 HI-5697(V)



NOTES:
R_1 = 2kΩ ± 5%, 1/2W
$C_1 = C_2$ = 0.01µF (per socket) or 0.1µF (per row)
$D_1 = D_2$ = IN4002 or equivalent (per board)
f_0 = 100kHz, TTL levels
$f_1 = f_0/2$ 50% duty cycle
$f_2 = f_0/4$
$f_3 = f_0/8$
$f_4 = f_0/16$
$f_5 = f_0/32$
$f_6 = f_0/64$, TTL levels
$f_7 = f_0/128$ 50% duty cycle
$f_8 = f_0/256$
$f_9 = f_0/512$
$f_{10} = f_0/1024$
$f_{11} = f_0/2048$

84 HI-5697(V) (LCC)



NOTES:
R_1 = 2kΩ ± 5%, 1/2W
$C_1 = C_2$ = 0.01µF (per socket) or 0.1µF (per row)
$D_1 = D_2$ = IN4002 or equivalent (per board)
f_0 = 100kHz, TTL levels
$f_1 = f_0/2$ 50% duty cycle
$f_2 = f_0/4$
$f_3 = f_0/8$
$f_4 = f_0/16$
$f_5 = f_0/32$
$f_6 = f_0/64$, TTL levels
$f_7 = f_0/128$ 50% duty cycle
$f_8 = f_0/256$
$f_9 = f_0/512$
$f_{10} = f_0/1024$
$f_{11} = f_0/2048$

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535	Design Considerations for a Data Acquisition System (DAS)	A collection of guidelines for the design of a Data Acquisition System. Includes signal conditioning, transducers, single-ended vs. differential signal paths, low level signals, filters, Programmable Gain Amplifiers, sampling rate, and computer interfacing.	10-73
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539	A Monolithic 16 Bit D/A Converter	Detailed description of the HI-DAC16 D-A Converter, chip photo and schematic, plus applications and interface considerations.	10-85
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541	Using HA-2539/2540 Very High Slew-Rate Wideband Operational Amplifiers	Prototyping considerations, output short circuit protection, offset voltage adjustment, frequency compensation, composite amplifier scheme, DC error reduction, boosting output current, increasing output signal swing, cascade amplifier, video gain block, high frequency oscillator, wideband signal splitter.	10-94
543	New High Speed Switch Offers Sub-50ns Switching Times	Application enhancement using the HI-201HS, high speed multiplexers, high speed sample and hold, analog switch and op amp circuitry, integrator with start/reset, low pass filter with select break frequency, amplifier with programmable gain, future applications.	10-98
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552	Using the HA-2542	Prototyping guidelines, thermal considerations and heat sinking, performance enhancements, applications (multi-channel security system, unbalanced coaxial driver, flash converter driver, programmable power supply, bridge load driver, high current stage, differential line driver, DC motor speed control).	10-158
553	Using the HA-5147/ 5137/5127	Construction and operation, low noise design applications (instrumentation amplifier bridge sensor, multiplexer, precision threshold detector, audio driver, NAB amplifier, multivibrator, programmable gain stage, log amp, professional mixer).	10-163
554	Low Noise Family HA-5101/5102/5104/ 5111/5112/5114	Low noise design, operation, applications (Electronic scales, programmable attentuator, Baxandal circuit, RIAA amplifier, NAB preamplifier, microphone amplifier, standard and simple biquads, professional mixer.	10-171
555	Ultra Low Bias Amplifier, HA-5180	Construction, layout hints, low noise design, applications (Sample and Hold, precision sample and hold, pH probe, light sensor, photo diode sensor, precision integrator, time, atomic partical counter circuit).	10-178
556	Thermal Safe-Operating-Areas for High Current Op Amps	Thermal management equations and curves indicating areas of V_{OUT} and I_{OUT} safe operation. Also, the effects of packaging and heat sinking are examined.	10-185
557	Recommended Test Procedures for Analog Switches	Description of analog switch test methods employed at Harris Semiconductor.	10-190
571	Using Ring Sync with HC-5502A and HC-5504 SLICs	Describes use of the SLICs Ring Synchronization pin and why you should use it.	10-196
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APP NOTE

FOR YOUR INFORMATION

No. 509

Harris Analog

A SIMPLE COMPARATOR USING THE HA-2620

G. G. Miller

The input current and impedance of a comparator circuit frequently loads the source and reference signals enough to cause significant errors. This problem is frequently eliminated by using a high impedance operational amplifier between the signal and the comparator. Figure 1 shows a simple circuit in which the operational amplifier is used as a comparator which is capable of driving approximately ten logic gates. The input impedance of the HA-2620 is typically 500 MΩ. The input current is typically 1 nA. The minimum output current of 15 mA is obtainable with an output swing of up to ±10 volts.

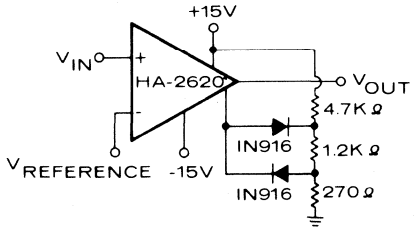


FIGURE 1 - HIGH IMPEDANCE COMPARATOR

The bandwidth control point is a very high impedance point having the same voltage as the amplifier output. The output swing can be conveniently limited by clamping the swing of the bandwidth control point. The maximum current through the clamp diodes is approximately 300 μA. The switching time is dependent on the output voltage swing and the stray capacitance at the bandwidth control point.

Figure 2 shows the waveforms for the comparator. The stray capacitance at the bandwidth control point can be reduced considerably below that of the breadboard circuit; this would improve the switching time. The switching time begins to increase more rapidly as the overdrive is reduced below 10 mV and is approximately 1μs for an overdrive of 5 mV. Dependable switching can be obtained with an overdrive as small as 1 mV. However, the switching time increases to almost 12 μs.

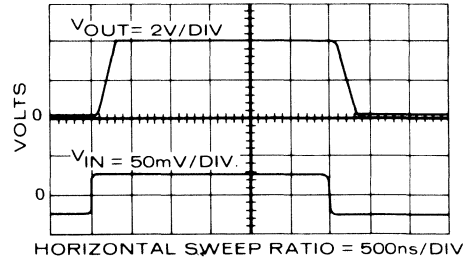


FIGURE 2 - WAVEFORMS FOR HA-2620 COMPARATOR

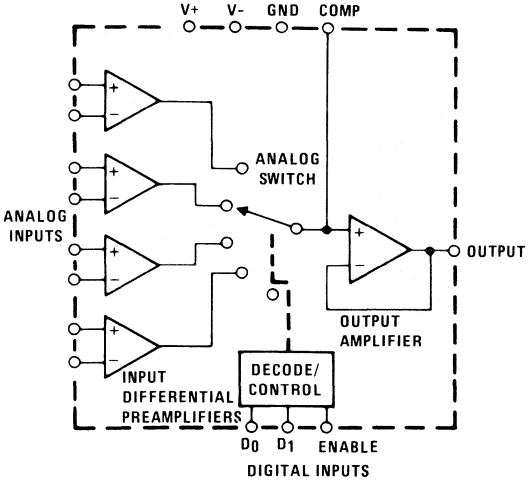
A common mode range of ±11 volts and a differential input range of ±12 volts makes the HA-2620 a very versatile comparator. The HA-2620 can sink or supply a minimum of 15 mA. The ability to externally clamp the output to any desired range makes the HA-2620 a very flexible comparator which is capable of driving unusual loads.

THE HA-2400 PRAM FOUR CHANNEL OPERATIONAL AMPLIFIER

By Don Jones

Introduction

Harris Semiconductor has announced a new linear device, the HA-2400/HA-2405 Four Channel Operational Amplifier. This combines the functions of an analog switch and a high performance operational amplifier, and makes practical a large number of new linear circuit applications.



A functional diagram of the HA-2400 is shown above. There are four preamplifier sections, one of which is selected through the DTL/TTL compatible inputs and connected to the output amplifier. The selected analog input terminals and the output terminal form a high performance operational amplifier.

In actuality, the circuit consists of four conventional op-amp input circuits connected in parallel to a conventional op-amp output circuit. The decode/control circuitry furnishes operating current only to the selected input section.

Circuit Connections

These input control the selection of the amplifier input channels in accordance with the truth table below:

GAIN, VOLTS/VOLT		C_{COMP}	BANDWIDTH (TYPICAL)	SLEW RATE (TYPICAL)
NON-INVERTING	INVERTING	pF	(-3dB), MHz	VOLTS/μs
1	–	15	8.0	15
2	1	7	8.0	20
3	2	4	8.0	22
5	4	3	6.0	25
8	7	2	5.0	30
>10	>9	0	40 ÷ GAIN	50

The digital inputs can be driven with any DTL or TTL circuit which uses a standard +5.0V supply.

Compensation

Frequency compensation for closed loop stability is recommended for closed loop gains less than 10. This is accomplished by connection of a single external capacitor from Pin 12 to A. C. ground (the V+ supply is recommended). The following table shows the minimum suggested compensation for various closed loop gains, with the resultant bandwidth and slew rate. Obviously, when the four channels are connected with different feedback networks, the channel with the lowest closed loop gain will govern the required compensation.

D_1	D_0	ENABLE	CHANNEL 1	CHANNEL 2	CHANNEL 3	CHANNEL 4
L	L	H	ON	OFF	OFF	OFF
L	H	H	OFF	ON	OFF	OFF
H	L	H	OFF	OFF	ON	OFF
H	H	H	OFF	OFF	OFF	ON
L or H	L or H	L	OFF	OFF	OFF	OFF

0V ≤ L ≤ +0.8V +2.0V ≥ H ≥ +5.0V

Compensation capacitors of greater value can be used to obtain lower bandwidth, greater

phase margin, and reduced overshoot, at the expense of proportionately reduced slew rate.

External lead-lag networks could also be used to optimize bandwidth and/or slew rate at a particular gain.

Applications

Any circuit function which can be constructed using a conventional operational amplifier can also be constructed using any channel of the HA-2400. Similar or different networks can be wired from the output to each channel input pair. The device can therefore be used to select and condition different input signals, or to select between different op-amp functions to be performed on a single input signal.

To wire a particular op-amp function to a channel, simply connect the appropriate network between the two inputs for that channel and the common output in the same manner as in wiring a conventional op-amp. It is often possible to design with fewer external components than would be required in wiring four separate op-amps (see Application Numbers 2 and 3 on the following pages). It should be remembered that the networks for unselected channels may still constitute a load at the amplifier output and the signal input, as if the unselected input terminals were disconnected from the network.

If offset adjustment is required, it can generally be accomplished by resistive summation at either of the inputs for each channel (see Application Number 8).

The analog input terminals of the OFF channels draw the same bias current as the ON inputs. The maximum differential input voltage of these terminals must be observed and their voltage levels must never exceed the supply voltages.

When the Enable input is held low, all four input channels are disconnected from the output. When this occurs, the output voltage will generally slowly drift towards the negative supply. If a zero volt output condition is required, one channel should be wired as a voltage follower with its positive input grounded.

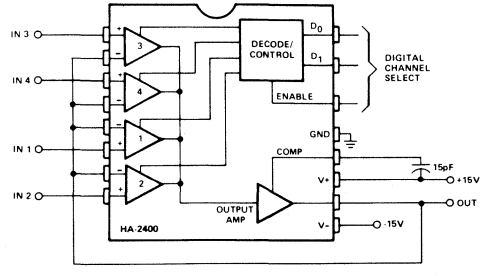
The amplifier output impedance remains low, even when the inputs are disabled; so it is not generally practical to wire the outputs of two or more devices directly together. The compensation pins of two devices, however, could be wired together to produce a switch with one output and more than four input channels.

The voltage at the compensation pin is about 0.7V more positive than the output signal, but has a very high source impedance. Maximum current from this pin is about 300μA, which makes it a convenient point for limiting the output swing through clamping diodes and divider networks (see Application Number 13).

Even if the application only requires a single channel to be switched on and off, it is often more economical to use the HA-2400, rather than a separate analog switch and high performance op-amp. Unused analog channel inputs should be grounded. Unused digital inputs may be wired to ground for a permanent "low" input, or either left open or wired to +5.0V for a permanent "high" input.

Illustrated on the following pages are a few of the thousands of possible applications for the Four Channel Operational Amplifier. These will give the reader a general impression of how the units can be connected; and probably will help generate many other ideas for applications. Also included are some "challenges" for the reader to modify the illustrated designs to perform different functions.

Applications No. 1



ANALOG MULTIPLEXER WITH BUFFERED INPUT AND OUTPUT

This circuit is used for analog signal selection or time division multiplexing. As shown, the feedback signal places the selected amplifier channel in a voltage follower (non-inverting unity gain) configuration, and provides very high input impedance and low output impedance. The single package replaces four input buffer amplifiers, four analog switches with decoding, and one output buffer amplifier.

For low level input signals, gain can be added to one or more channels by connecting the (−) inputs to a voltage divider between output and ground. Bandwidth is approximately 8 MHz, and the output will slew from one level to another at about 15.0V per microsecond.

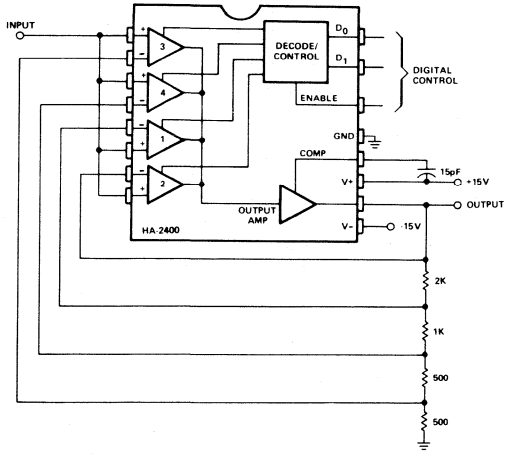
Expansion to multiplex 5 to 12 channels can be accomplished by connecting the compensation pins of two or three devices together, and using the output of only one of the devices. The Enable input on the unselected devices must be low.

Expansion to 16 or more channels is accomplished in a straightforward manner by connecting outputs of 4 four-channel multiplexers to the inputs of another four-channel multiplexer.

Differential signals can be handled by two identical multiplexers addressed in parallel.

Inverting amplifier configurations can also be used, but the feedback resistors may cause crosstalk from the output to unselected inputs.

Applications No.2



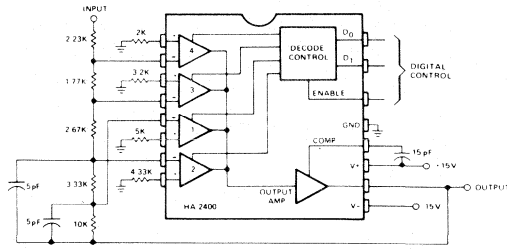
AMPLIFIER, NON-INVERTING PROGRAMMABLE GAIN

This is a non-inverting amplifier configuration with feedback resistors chosen to produce a gain of 0, 1, 2, 4, or 8 depending on the Digital Control inputs.

Comparators at the output could be used for automatic gain selection for auto-ranging meters, etc.

CHALLENGE: Design a circuit using only two HA-2400's which can be programmed to any of 16 different gains.

Applications No.3

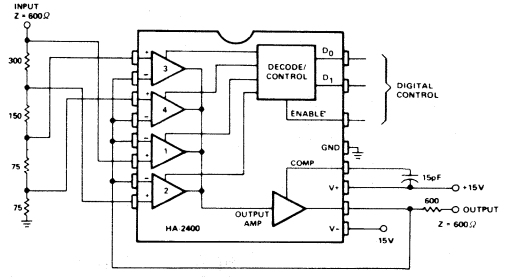


AMPLIFIER, INVERTING PROGRAMMABLE GAIN

The circuit above can be programmed for a gain of 0, −1, −2, −4 or −8.

This could also have been accomplished with one input resistor and one feedback resistor per channel in the conventional manner, but this would require eight resistors rather than five.

Applications No.4

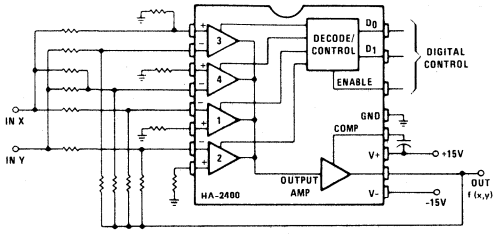


ATTENUATOR PROGRAMMABLE

This circuit performs the function of dividing the input signal by a selected constant (1, 2, 4, 8, or ∞ as illustrated). To multiply by a selected constant, see circuit No. 2. While T, π, or L sections could be used in the input attenuator, this is not necessary since the amplifier loading is negligible and a constant input impedance is maintained. The circuit is thus much simpler and more accurate than the usual method of constructing a constant impedance ladder and switching sections in and out with analog switches.

Two identical circuits may be used to attenuate a balanced line.

Applications No.5

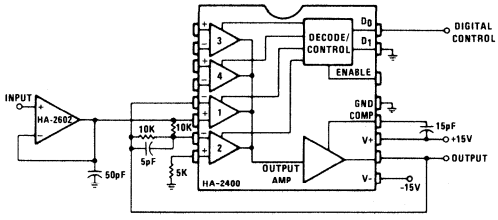


ADDER/SUBTRACTOR PROGRAMMABLE FUNCTION

The circuit shown above can be programmed to give the output functions $-K_1X$, $-K_2Y$, $-(K_3X + K_4Y)$, or $K_5X - K_6Y$. Obviously, many other functions of one or more variables can be constructed, including combinations with analog multiplier or logarithmic modules.

This device opens up many new design approaches in digitally controlled analog computation or signal manipulation.

Applications No.6

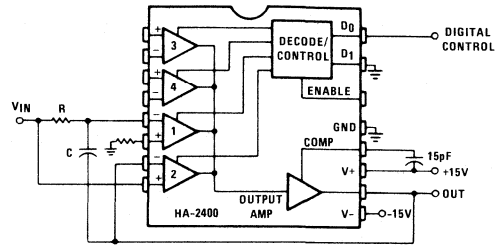


PHASE SELECTOR/PHASE DETECTOR/ SYNCHRONOUS RECTIFIER/BALANCED MODULATOR

This circuit passes the input signal at unity gain, either unchanged, or inverted depending on the Digital Control input. A buffered input is shown, since low source impedance is essential. Gain can be added by modifications to the feedback networks. Signals up to 100 kHz can be handled with 20.0V peak-to-peak output. The circuit becomes a phase detector by driving the Digital Control input with a reference phase at the same frequency as the input signal, the average D. C. output being proportional to the phase difference, with zero volts at $+90^o$. By connecting the output to a comparator, which in turn drives the Digital Control, a synchronous full-wave rectifier is formed.

With a low frequency input signal and a high frequency digital control signal, a balanced (surpressed carrier) modulator is formed.

Applications No.7

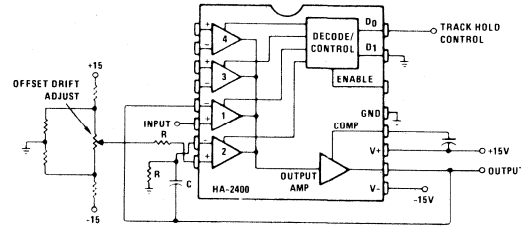


INTEGRATOR/RAMP GENERATOR WITH INITIAL CONDITION RESET

It is difficult in practice to set the initial conditions accurately in an integrator. This usually requires wiring contacts of a mechanical relay across the capacitor - - leakage currents of solid state switches produce integration inaccuracy. The scheme shown above eliminates these reliability and accuracy problems.

Channel 1 is wired as a conventional integrator, Channel 2 as a voltage follower. When Channel 2 is switched on, the output will follow V_{IN}, and C will discharge to maintain zero volts across it. When Channel 1 is then switched on the output will initially be at the instantaneous value of V_{IN}, and then will commence integrating towards the opposite polarity. This circuit is particularly suitable for timing ramp generation using a fixed D. C. input. Many variations are possible, such as programmable time constant integrators.

Applications No.8



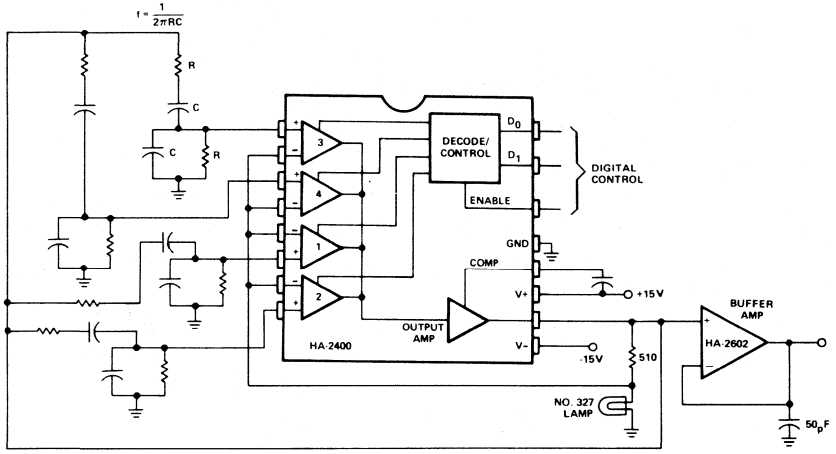
TRACK AND HOLD/SAMPLE AND HOLD

Channel 1 is wired as a voltage follower and

is turned on during the track/sample time. If the product of R x C is sufficiently short compared to the period of maximum output frequency, or sample time, C will charge to the output level. Channel 2 is an integrator with zero input signal. When Channel 2 is then turned on, the output will remain at the voltage across C.

An even simpler circuit can be made by wiring one channel as an amplifier, choosing the compensation capacitor to yield the minimum required bandwidth or slew rate. When the Enable input is pulled low, the output will tend to remain at its last level, because of the charge remaining on the compensating capacitor.

Applications No.9

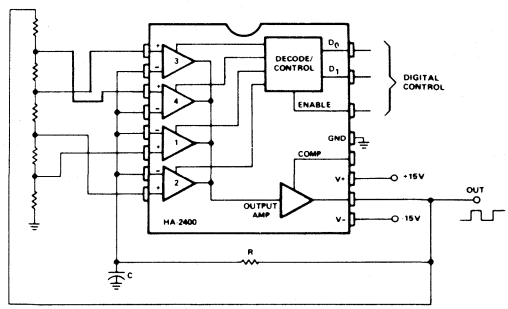


SINE WAVE OSCILLATOR PROGRAMMABLE FREQUENCY

Any oscillator which can be constructed using an op-amp, such as the twin-T, phase shift, crystal controlled types, etc. can be made programmable by using the HA-2400. Illustrated above is a Wien Bridge type, which is very popular for signal generators, since it is easily tunable over a wide frequency range, and has a very low distortion sine wave output. The frequency determining networks can be designed from about 10Hz to greater than 1MHz. Output level is about 6.0V RMS. By substituting a programmable attenuator (Circuit No. 4) for the Buffer Amplifier, a very versatile sine wave source for automatic testing, etc. can be constructed.

CHALLENGE: A high Q, narrow band filter can be made by feeding back greater than 1/3 of the output to the negative input. Design a circuit using the HA-2400 and an RC network which can be programmed either to generate or to detect an audio tone of the same frequency. Such a circuit would be quite useful for data communications.

Applications No.10



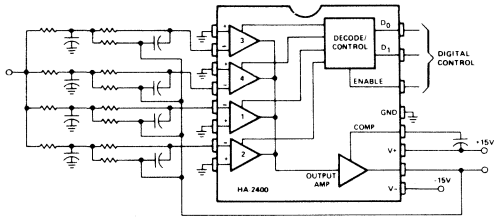
MULTIVIBRATOR, FREE RUNNING, PROGRAMMABLE FREQUENCY

This is the simplest of any programmable oscillator circuit, since only one stable timing capacitor is required. The output square wave is about 25.0V peak-to-peak and has

rise and fall times of about 0.5 μs. If a programmable attenuator circuit (No. 4) is placed between the output and the divider network, 16 frequencies can be produced with two HA-2400's and still only one timing capacitor.

A precision programmable square-triangle generator can also be constructed by adapting circuit described in Harris Application Note 507 to the HA-2400.

Applications No. 11



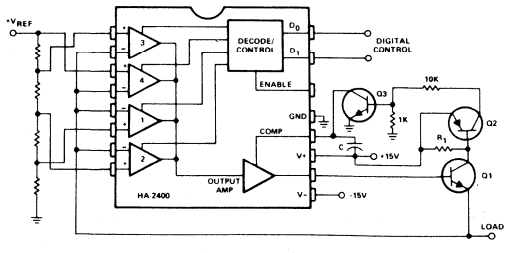
ACTIVE FILTER PROGRAMMABLE

Shown above is a second order low pass filter with programmable cutoff frequency. This circuit should be driven from a low source impedance since there are paths from the output to the input through the unselected networks.

Virtually any filter function which can be constructed with a conventional op-amp can be made programmable with the HA-2400.

A useful variation would be to wire one channel as a unity gain amplifier, so that one could select the unfiltered signal, or the same signal filtered in various manners. These could be cascaded to provide a wide variety of programmable filter functions.

Applications No. 12

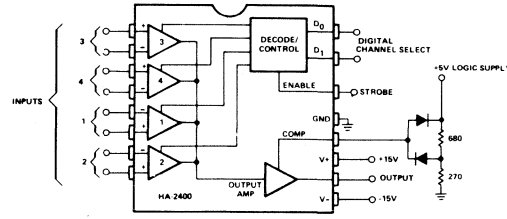


POWER SUPPLY PROGRAMMABLE

Many systems require one or more relatively low current voltage sources which can be programmed to a few predetermined levels. It is no longer necessary to purchase a programmable power supply with far more capability than needed. The circuit shown above produces positive output levels, but could be modified for negative or bipolar outputs. Q1 is the series regulator transistor, selected for the required current and power capability. R1, Q2 and Q3 form an optional short circuit protection circuit, with R1 chosen to drop about 0.7V at the maximum output current. The compensation capacitor, C. should be chosen to keep the overshoot, when switching, to an acceptable level.

CHALLENGE: Design a supply using only two HA-2400's which can be programmed to 16 binary weighted (or 10 BCD weighted) output levels.

Applications No. 13



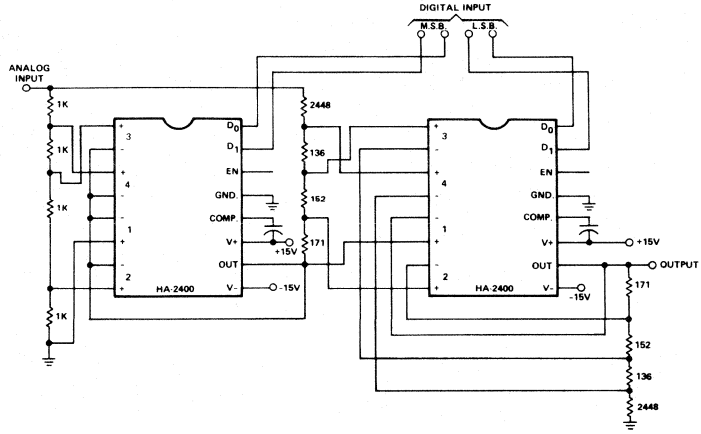
COMPARATOR, FOUR CHANNEL

When operated open loop without compensation, the HA-2400 becomes a comparator with four selectable input channels. The clamping network at the compensation pin limits the output voltage to allow DTL or TTL digital circuits to be driven with a fanout of up to ten loads.

Output rise and fall times will be about 100ns for differential input signals of several hundred millivolts, but will be in the microsecond region for small differential signals.

The circuit can be used to compare several signals against each other or against fixed references; or a single signal can be compared against several references. A "window comparator", which assures that a signal is within a voltage range, can be formed by monitoring the output polarity while rapidly switching between two channels with different reference inputs and the same signal input.

Applications No. 14



MULTIPLYING D TO A CONVERTER

The circuit above performs the function, $V_{OUT} = V_{IN} \cdot \frac{N}{16}$, where N is the binary number from 0 to 15 formed by the digital input. If the analog input is a fixed D.C. reference, the circuit is a conventional 4-bit D to A. The input could also be a variable or A.C. signal, in which case the output is the product of the analog signal and the digital signal.

The circuit on the left is a programmable attenuator with weights of 0, 1/4, 1/2 or 3/4. The circuit on the right is a non-inverting adder which adds weights to the first output of 0, 1/16, 1/8 or 3/16.

If four quadrant multiplication is required, place the Phase Selector circuit (No. 6) in series with either the analog input or output. The D_0 input of that stage becomes the + or − sign bit of the digital input.

More Challenges

One of our favorite college textbooks paused at each climactic point with a statement to the effect that, "Proof of the following theorem is omitted, and is suggested as an exercise for the student."

The following is a list of some additional applications in which we believe the HA-2400 will prove very valuable. The "proofs", at present, remain as exercises for our ingenious readers.

- A to D Converter, Dual Slope Integrating
- Active Filter, State Variable Type with Programmable Frequency and/or Programmable "Q"
- Amplifier with Programmable D.C. Level Shift
- Chopper Amplifiers
- Crossbar Switches
- Current Source, Programmable
- F.M. Stereo Modulator
- F.S.K. Modem
- Function Generators, Programmable
- Gyrator, Programmable
- Monostable Multivibrator, Programmable
- Multiplier, Pulse Averaging
- Peak Detector with Reset
- Resistance Bridge Amplifier/Comparator with Programmable Range
- Sense Amp/Line Receiver with Programmable Threshold
- Spectrum Analyzer, Scanning Type
- Sweep Generator, Programmable
- Switching Regulator
- Touch-Tone™ Generator/Detector (Use Harris HD-0165 Keyboard Encoder I.C.)

Feedback

We believe we have only scratched the surface of possible applications for a multiple channel operational amplifier.

If you have a solution for any of the previous "challenges" or any new application, please let us know. Anything from a one word description to a tested design will be welcome.

APP NOTE

FOR YOUR INFORMATION

No. 515

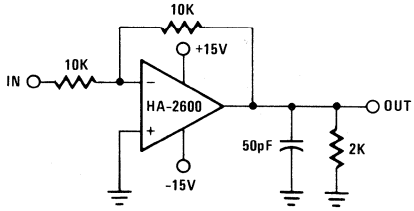
Harris Analog

OPERATIONAL AMPLIFIER STABILITY: INPUT CAPACITANCE CONSIDERATIONS

Author: Don Jones

This note deals with stabilization and optimization of A.C. response in operational amplifiers. One of the more common difficulties in applying operational amplifiers will be discussed.

Let's consider the unity gain inverting amplifier circuit shown below:



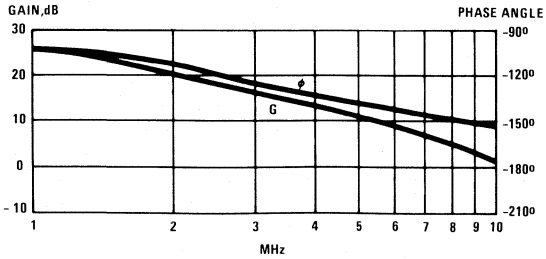
This appears to be a straightforward application with reasonable component values.

But, with the input grounded, the circuit output shows an oscillation at about 5MHz.

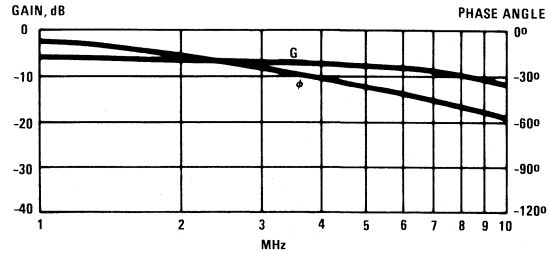
Even more surprising, if the same device is connected as a voltage follower with the same load, it is perfectly stable. Since the inverting amplifier has 6dB less feedback than the voltage follower, shouldn't it be more stable?

The culprit here is capacitance at the amplifier inverting input. The HA-2600 in the TO-99 can has an input capacitance of about 2 or 3pF. When soldered on a P.C. card, or inserted in a socket, wiring capacitance might add another 3 to 6pF. With only 5K effective resistance at this point, 5 to 10pF seems pretty negligible, doesn't it? But let's find out.

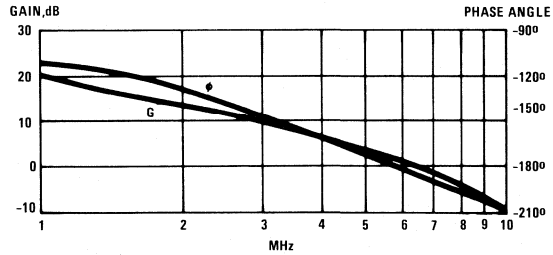
The open loop amplitude and phase response characteristics of the amplifier between 1 and 10MHz looks like this:



The characteristics of the feedback network alone with 5pF capacitance to ground looks like this:

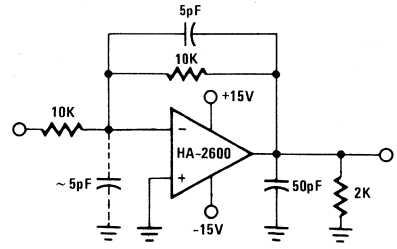


Combining these two graphs by algebraically adding the dB gains together and adding the phase shifts together gives us the open loop response at the summing point:



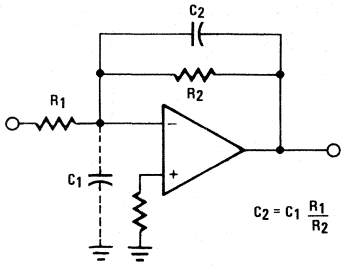
We can see that on the composite response curves, the phase shift crosses 180° at 5.5MHz, and that there is still about +2dB of gain at this frequency. Therefore, closing the loop automatically creates an oscillator.

How can we overcome this effect? If we add a capacitor across the feedback resistor, we can cancel the effects of the input capacitance:



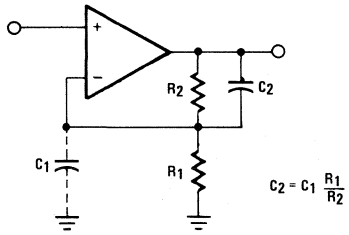
If the feedback capacitance matches the input capacitance, the response curves of the feedback network alone will be a flat -6dB and 0° across the frequency band. The composite curves will then show a bandwidth of 7.5MHz and a positve phase margin of 33°. So the circuit will now be quite stable. It's amazing how much difference that small capacitance can make.

The general scheme for compensation of various circuit types is shown below:

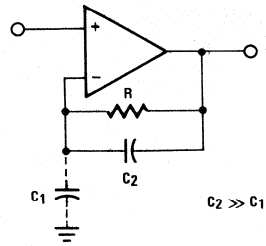


(Include high frequency source impedance in R_1.)

INVERTING AMPLIFIER



NON-INVERTING AMPLIFIER



FOLLOWER WITH FEEDBACK RESISTOR

It's not really necessary to know the exact value of stray capacitance, C_1 for most layouts, about 5 to 10pF is a good guess. Unless you are trying to squeeze out the last Hz of frequency response, it doesn't hurt to guess on the high side. At higher gains, where C_2 calculates out to less than 1 or 2pF, it isn't necessary to use C_2 — but it won't disturb anything if you do use it.

If you are uncertain about whether compensation is necessary, check the pulse response or frequency response of the closed loop stage. Hook a pulse generator to the input, and adjust the amplitude for about a 200 millivolt step at the output — if the output overshoot is less than 40% of the step, the circuit will be stable. Alternately, check the small signal frequency response of the stage if the high frequency peaking is less than +6dB, more than the low frequency gain, the circuit is stable. Of course, you can increase the compensation capacitor if you need even smoother response.

The phenomena we have described are not peculiar to any one amplifier type. Wideband amplifiers require a little more care in the design of feedback networks; but the same type oscillations will show up on 741 type amplifiers with higher feedback resistor values.

APP NOTE

FOR YOUR INFORMATION

No. 517

Harris Analog

APPLICATIONS OF MONOLITHIC SAMPLE-AND-HOLD AMPLIFIERS

DON JONES AND AL LITTLE

Introduction

The sample-and-hold or track-and-hold function is very widely used in linear systems. This function is readily available in modular, hybrid, and monolithic form.

All high quality sample-and-hold circuits must meet certain requirements:

(1) The holding capacitor must charge up and settle to its final value as quickly as possible.

(2) When holding, the leakage current at the capacitor must be as near zero as possible to minimize voltage drift with time.

(3) Other sources of error must be minimized.

Design of a sample-and-hold involves a number of compromises in the above requirements. The amplifier or other device feeding the analog switch must have high current capability and be able to drive capacitive loads with stability. The analog switch must have both low ON resistance and extremely low OFF leakage currents. But, leakage currents of most analog switches (except the dielectrically isolated types) run to several hundred nanoamperes at elevated temperatures. The analog switch must have very low coupling between the digital input and analog output, because any spikes generated at the instant of turn-off will change the charge on the capacitor. The output amplifier must have extremely low bias current over the temperature range, and also must have low offset drift and sufficient slew rate.

Another design consideration is whether to make the input differential or single ended. A single ended sample/hold amplifier has a fixed gain, usually +1, so that it simply provides the sample/hold function. In contrast, a differential input sample-and-hold amplifier is designed to be configured with external feedback, just like an op amp. It may be used to form a filter, integrator, inverting or non-inverting amplifier with gain, etc. This allows the designer to combine any number of op amp signal conditioning circuits with the sample-and-hold function. All Harris sample-and-hold amplifiers are designed with differential inputs to take advantage of this capability.

The HA-2420/2425

The HA-2420/2425 is one of the most versatile monolithic sample-and-hold integrated circuits. A functional diagram is shown in Figure 1.

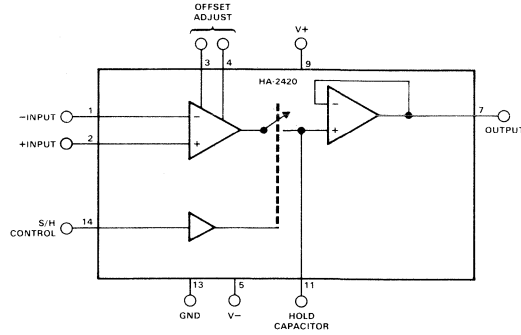


FIGURE 1 - HA-2420/2425 FUNCTIONAL DIAGRAM

The input amplifier stage is a high performance operational amplifier with excellent slew rate, and the ability to drive high capacitance loads without instability. The switching element is a highly efficient bipolar transistor stage with extremely low leakage in the OFF condition. The output amplifier is a MOSFET input unity gain follower to achieve extremely low bias current.

MOSFET inputs are generally not used for D.C. amplifiers because their offset voltage drift is difficult to control. In this configuration, however, negative feedback is generally applied between the output and inputs of the entire device, and the effect of this offset drift at the inputs is divided by the open loop gain of the input amplifier stage.

The HA-3520

The HA-5320 is a high speed monolithic sample/hold circuit which includes its own 100pF hold capacitor. Unlike the HA-2420/2425, this device utilizes an input transconductance amplifier and an integrating output stage as shown in Figure 2. The hold capacitor is charged through a low leakage analog switch at the virtual ground node of the output amplifier. In this configuration, charge injection at the transition from sample to hold is constant over the entire input/output voltage range. Additional hold capacitance may be added to the HA-5320 for improved droop rate, at the expense of increased acquisition time.

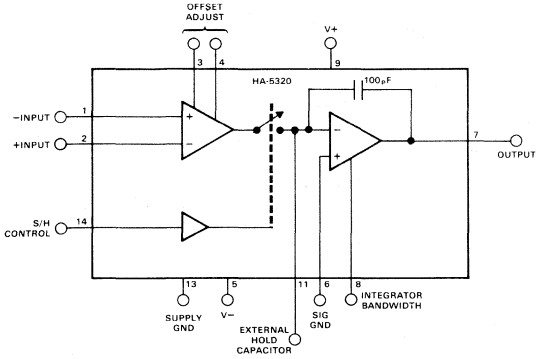


FIGURE 2 - HA-5320 FUNCTIONAL DIAGRAM

The HA-5330

The HA-5330 is a monolithic sample/hold amplifier optimized for very high speed performance, acquiring a 10V step to 0.01% in 500ns. Its circuit topology is similar to the HA-5320 (Figure 3), but there is no provision for external capacitance. The integrated 90pF capacitor provides excellent performance alone; external leakage paths and noise pickup are avoided in this design by not exposing the integrator input node to an external pin.

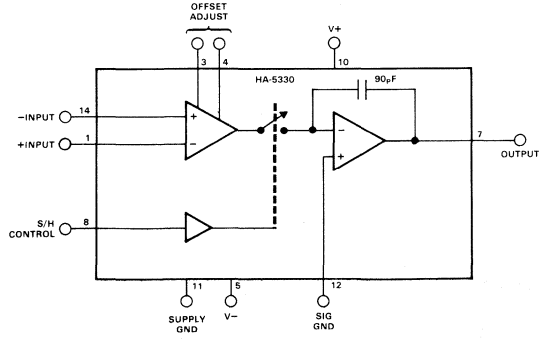


FIGURE 3 - HA-5330 FUNCTIONAL DIAGRAM

Sample-Hold-Hold Applications

A number of basic applications are shown on the following pages. These devices are exceptionally versatile, since they can be wired into any of the hundreds of feedback configurations possible with any operational amplifier. In many applications the device will replace both an operational amplifier and a sample-and-hold module.

The larger the value of the hold capacitor, the longer time it will hold the signal without excessive drift; however, it will also reduce the charging rate/slew rate and the amplifier bandwidth during sampling. So the capacitance value must be optimized for each particular application. Drift during holding tends to double for every 10°C rise in ambient temperature. The holding capacitor should have extremely high insulation resistance and low dielectric absorption-polystyrene (below +85°C), Teflon, or mica types are recommended.

For least drift during holding, leakage paths on the P.C. board and on the device package surface must be minimized. The output voltage is nearly equal to the voltage on C_H for the HA-2420. The output line may be used as a guard ring surrounding the line to C_H. Since the potentials are nearly equal, very low leakage currents will flow. The two package pins surrounding the C_H pin are not internally connected, and may be used as guard pins to reduce leakage on the package surface. A suggested P.C. guard ring layout is shown in Figure 4. The hold capacitor in the HA-5320 operates at virtual ground. For this device, a guard ring must be connected to the SIG GND terminal (pin 6) instead of the output.

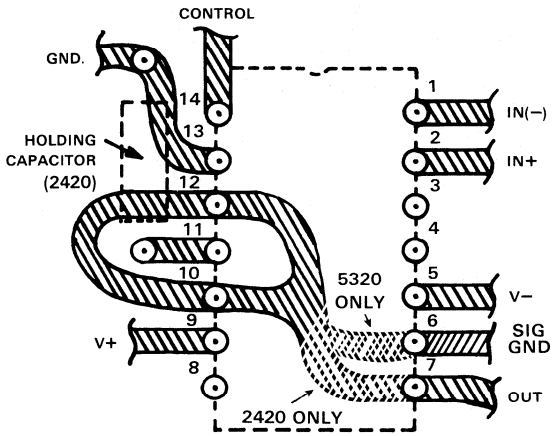


FIGURE 4 - GUARD RING LAYOUT (BOTTOM VIEW)

Since the internal hold capacitor is not accessable in the HA-5330, no P.C. layout consideration to minimize leakage is necessary.

Although the hold capacitor is configured differently for the

three sample/hold devices as shown in Figure 5, most applications are common to all. For simplicity, the hold capacitor has been excluded from circuit diagrams in the following examples and the S/H's are depicted as op amps with a sample/hold control. This symbol is intended to remind the user of the "op amp" capability of these devices.

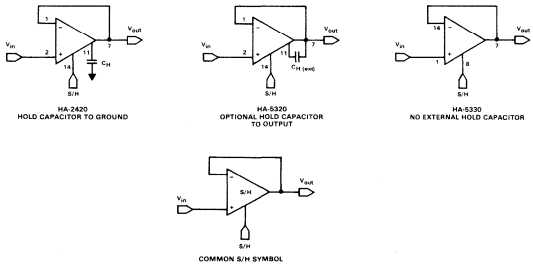


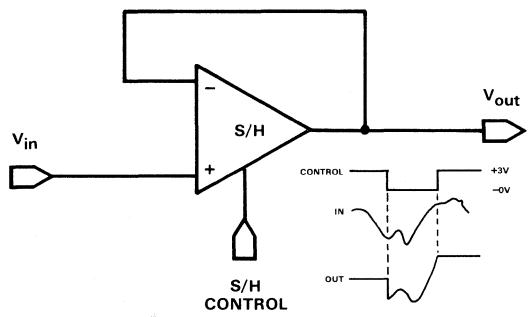
FIGURE 5 - SIMPLIFIED S/H SYMBOL (UNITY GAIN CONFIGURATION)

Application No. 1

Feedback is the same as a conventional op amp voltage follower which yields a unity gain, non-inverting output. This hookup also has a very high input impedance.

The only difference between a track-and-hold and a sample-and-hold is the time period during which the switch is closed. In track-and-hold operation, the switch is closed for a relatively long period during which the output signal may change appreciably; the output will hold the level present at the instant the switch is opened. In sample-and-hold operation, the switch is closed only for the period of time necessary to fully charge the holding capacitor.

BASIC TRACK-AND-HOLD/SAMPLE-AND-HOLD



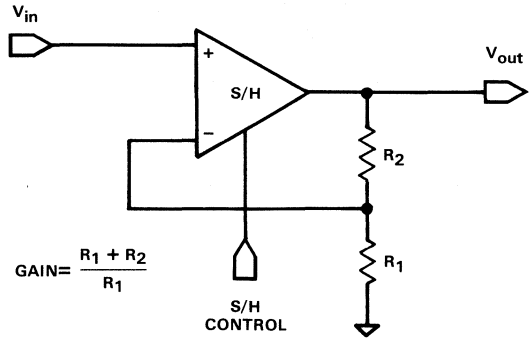
Application No. 2

This is the standard non-inverting amplifier feedback circuit.

It illustrates one of the many ways in which a sample/hold amplifier may be used to perform both op amp and sampling functions, eliminating the need for a separate scaling amplifier and sample-and-hold module.

In general, it is usually best design practice to scale the gain such that the largest expected signal will give an output close to + or − 10 volts. Drift current is essentially independent of output level, and less percentage drift will occur in a given time for a larger output signal.

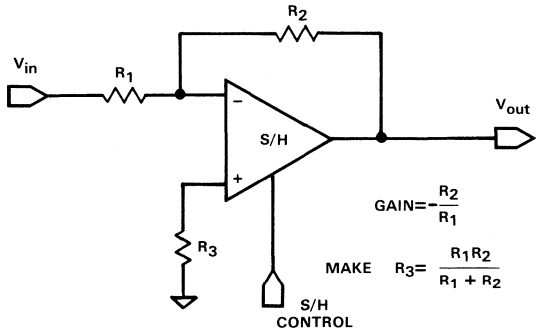
SAMPLE-AND-HOLD WITH GAIN



Application No. 3

This illustrates another application in which the hookup versatility of a sample/hold often eliminates the need for a separate operational amplifier and sample-and-hold module. This hookup will have somewhat higher input to output feedthrough during "hold," than the non-inverting connection, since output impedance is the open-loop value during "hold," and feedthrough will be: $\frac{V_{IN}\,R_O}{R_1 + R_2 + R_O}$

INVERTING SAMPLE-AND-HOLD

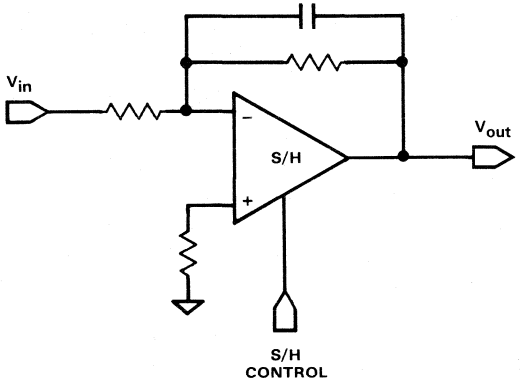


Application No. 4

It is often required that a signal be filtered prior to sampling. This can be accomplished with only one device. Any of the inverting and non-inverting filters which can be built with op

amps can be implemented. However, it is necessary that the sampling switch be closed for sufficient time for the filter to settle when active filter types are connected around the device.

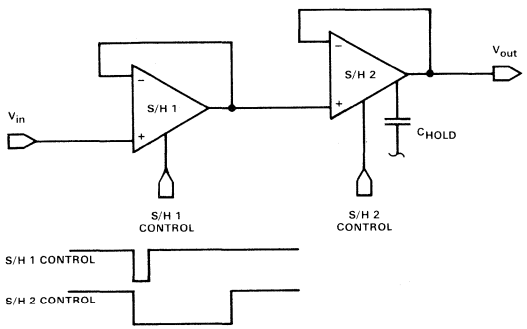
FILTERED SAMPLE-AND-HOLD



Application No. 5

Short sample times require a low value holding capacitor; while long, accurate hold times require a high value holding capacitor. So, achieving a very long hold with a short sample appears to be contradictory. However, it can be accomplished by cascading two S/H circuits, the first with a low value capacitor, the second with a high value. Then the second S/H can sample for as long a time as the first circuit can accurately hold the signal.

CASCADED SAMPLE-AND-HOLD



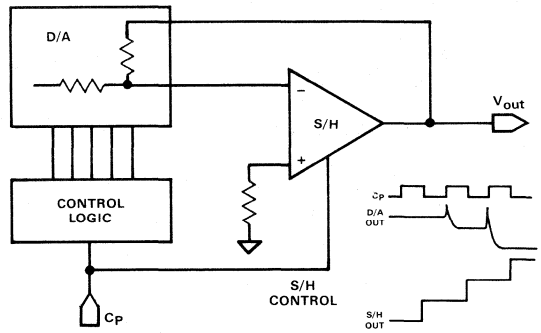
Application No. 6

The word "glitch" has been a universal slang expression among electronics people for an unwanted transient condition. In D to A converters, the word has achieved semi-official status for an output transient which occurs when the digital input address is changed.

In the illustration, the sample/hold amplifier does double duty, serving as a buffer amplifier as well as a glitch remover, delaying the output by ½ clock cycle.

The sample/hold may be used to remove many other types of "glitches" in a system. If a delayed sample pulse is required, this can be generated using a dual monostable multivibrator I.C.

DE-GLITCHER

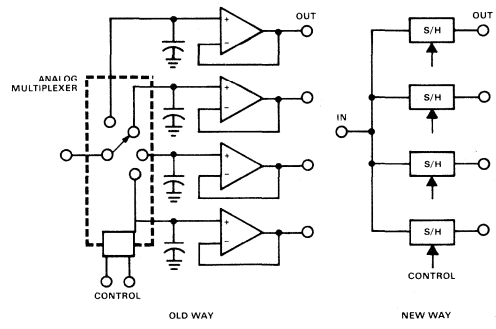


Application No. 7

This circuit reconstructs and separates analog signals which have been time division multiplexed.

The conventional method, shown on the left, has several restrictions, particularly when a short dwell time and a long, accurate hold time is required. The capacitors must charge from a low impedance source through the resistance and current limiting characteristics of the multiplexer. When holding, the high impedance lines are relatively long and subject to noise pickup and leakage. When FET input buffer amplifiers are used for low leakage, severe temperature offset errors are often introduced.

DE-MULTIPLEXER



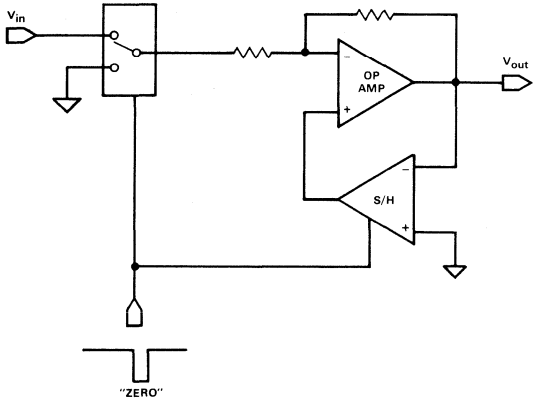
Application No. 8

This basic circuit has widespread applications in instrumentation, A/D conversion, DVM's and DPM's to eliminate offset drift errors by periodically rezeroing the system. Basically, the input is periodically grounded, the output offset is then sampled and fed back to cancel the error.

The system illustrated automatically zeros a high gain amplifier. Care in the actual design is necessary to assure that the zeroing loop is dynamically stable. A second sample-and-hold could be added in series with the output to remove the output discontinuity.

Many variations of this scheme are possible to suit the individual system.

AUTOMATIC OFFSET ZEROING

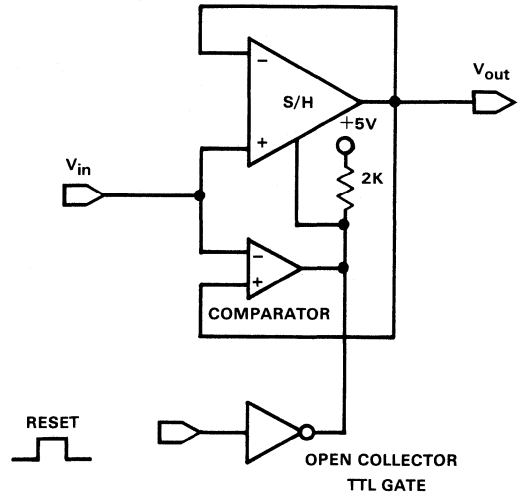


Application No. 9

This accurate, low drift peak detector circuit combines the basic sample-and-hold connection with a comparator. When the input signal level exceeds the voltage being stored in the S/H, the comparator trips, and a new sample of the input is taken. The S/H offset pot should be adjusted for a slight positive offset, so that the comparator will trip back when the new peak is acquired; otherwise the comparator would remain "on" and the S/H would follow the peak back down.

To make a negative peak detector, reverse the comparator inputs and adjust the S/H for a negative offset.

The reset function, which is difficult to achieve in other peak detector circuits, forces a new sample at the instantaneous input level.



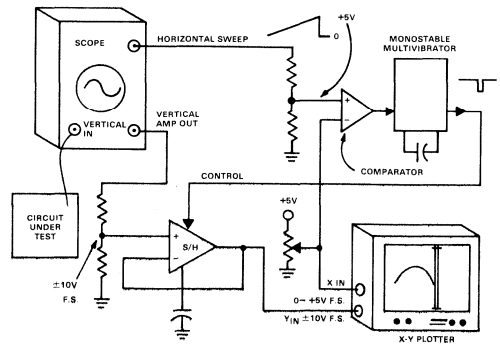
Application No. 10

This useful application illustrates how fast repetitive waveforms can be slowed down using sampling techniques. The input signal is much too fast to be tracked directly by the X-Y recorder, but sampling allows the recorder to be driven as slow as necessary.

To operate, the waveform is first synched in on the scope. Then the potentiometer connected to the recorder X input is slowly advanced, and the waveform will be reproduced. The S/H amplifier samples for a very short interval once each horizontal sweep of the scope. The sampling instant is determined by the potentiometer at the instant when the horizontal sweep waveform corresponds to the X position of the recorder.

This principle can be applied to many systems for waveform analysis, etc.

PLOT HIGH SPEED WAVEFORMS WITH SAMPLING TECHNIQUES



OPERATIONAL AMPLIFIER NOISE PREDICTION

By Richard Whitehead

Introduction

When working with op amp circuits an engineer is frequently required to predict the total RMS output noise in a given bandwidth for a certain feedback configuration. While op amp noise can be expressed in a number of ways, "spot noise" (RMS input voltage noise or current noise which would pass through 1Hz wide bandpass filters centered at various discrete frequencies), affords a universal method of predicting output noise in any op amp configuration.

The Noise Model

Figure 1 is a typical noise model depicting the noise voltage and noise current sources that are added together in the form of root mean square to give the total equivalent input voltage noise (RMS), therefore:

$$E_{ni} = \sqrt{e_{ni}^2 + I_{ni}^2 R_g^2 + 4KTR_g} \quad \text{where,}$$

E_{ni} is the total equivalent input voltage noise of the circuit.

e_{ni} is the equivalent input voltage noise of the amplifier.

$I_{ni}^2 R_g^2$ is the voltage noise generated by the current noise.

$4KTR_g$ expresses the thermal noise generated by the external resistors in the circuit where $K = 1.38 \times 10^{-23}$ joules/^oK; $T = 300^oK$ (27^oC) and $R_g = \left(\frac{R_1 R_3}{R_1 + R_3}\right) + R2$

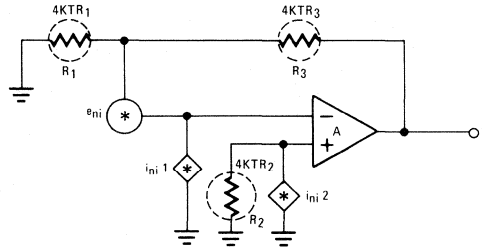


Figure 1

The total RMS output noise (E_{no}) of an amplifier stage with gain = G in the bandwidth between f_1 and f_2 is:

$$E_{no} = G\left(\int_{f1}^{f2} E_{ni}^2 df\right)^{1/2}$$

Note that in the amplifier stage shown, G is the non-inverting gain $\left(G = 1 + \frac{R2}{R1}\right)$ regardless of which input is normally driven.

Procedure for Computing Total Output Noise

1. Refer to the voltage noise curves for the amplifier to be used.
2. Enter values of $e_{ni}2$ line (a) of the table below from the curve labeled "Noise spectral density" (the values must be squared).
3. From the current noise curves for the

amplifier, obtain the values of i_{ni}^2 for each of the frequencies in the table, and multiply each by R_g^2, entering the products in line (b) of the table.

4. Obtain the value of $4KTR_g$ from Figure 14, and enter it on line (c) of the table. This is constant for all frequencies. The $4KTR_g$ value must be adjusted for temperatures other than normal room temperature.

5. Total each column in the table on line (d). This total is E_{ni}^2.

	10Hz	100Hz	1KHz	10KHz	100KHz
(a) e_{ni}^2					
(b) $I_{ni}^2R_g^2$					
(c) $4KTR_g$					
(d) E_{ni}^2					

6. On linear scale graph paper enter each of the values for E_{ni}^2 vs. frequency. In most cases, sufficient accuracy can be obtained simply by joining the points on the graph with straight line segments.

7. For the bandwidth of interest, calculate the area under the curve by adding the areas of trapezoidal segments. This procedure assumes a perfectly square bandpass condition; to allow for the more normal -6db/octave bandpass skirts, multiply the upper (-3db) frequency by 1.57 to obtain the effective bandwidth of the circuit, before computing the area. The total area obtained is equivalent to the square of the total input noise over the given bandwidth.

8. Take the square root of the area found above and multiply by the gain (G) of the circuit to find the total Output RMS noise.

A TYPICAL EXAMPLE

It is necessary to find the output noise of the circuit shown below between 1KHz and 24KHz.

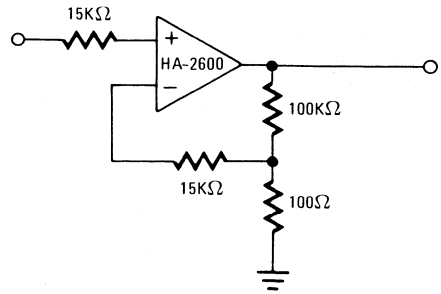
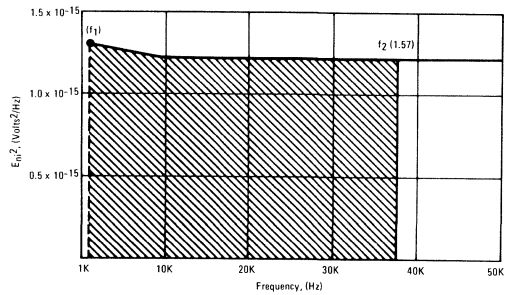


Figure 2
The HA-2600 In a Typical G = 1000 Circuit

Values are selected from Figures 5, 5a and 14 to fill in the table as shown below. An R_g of 30KΩ was selected.

	10Hz	100Hz	1KHz	10KHz	100KHz
(a) e_{ni}^2	3.6×10^{-15}	1.156×10^{-15}	7.84×10^{-16}	7.29×10^{-16}	7.29×10^{-16}
(b) $I_{ni}^2R_g^2$	9.9×10^{-16}	1.89×10^{-16}	3.15×10^{-17}	7.2×10^{-18}	7.2×10^{-18}
(c) $4KTR_g$	4.968×10^{-16}	4.968×10^{-16}	4.968×10^{-16}	4.968×10^{-16}	4.968×10^{-16}
(d) E_{ni}^2	5.09×10^{-15}	1.86×10^{-15}	1.31×10^{-15}	1.23×10^{-15}	1.23×10^{-15}

The totals of the selected values for each frequency is in the form of E_{ni}^2. This should be plotted on linear graph paper as shown below:



HA-2600 Total Equivalent Input Noise Squared

Since a noise figure is needed for the frequency of 1KHz to 24KHz, it is necessary to calculate the effective bandwidth of the circuit. With AV = 60db the upper 3db point is approximately 24KHz. The product of 1.57 (24KHz) is 37.7KHz and is the effective bandwidth of the circuit.

The shaded area under the curve is approximately 45 x 10^{-12} $Volts^2$; the total equivalent input noise is $\sqrt{E_{ni}^2}$ or 6.7 microvolts, and the total output noise for the selected bandwidth is $\sqrt{E_{ni}^2}$ x (closed loop gain) or 6.7 millivolts RMS.

Actual Measurements For Comparison

The circuit shown below was used to actually measure the broadband noise of the HA-2600 for the selected bandwidth:

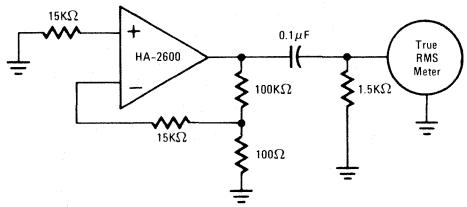


Figure 3
A Typical Test Circuit for Broadband Noise Measurements

The frequencies below the f_1 point of the bandwidth selected are filtered out by the RC network on the output of HA-2600. The measurement of the broadband noise is observed on the true RMS voltmeter. The measured output noise of the circuit is 4.7 microvolts RMS as compared to the calculated value of 6.7 microvolts RMS.

Acquiring the Data For Calculations

Spot noise values must be generated in order to make the output noise prediction. The effects of "Popcorn" noise have been excluded due to the type of measurement system.

The Quan-Tech Control Unit, model no. 2283 and Filter Unit, model no. 2181 were used to acquire spot noise voltage values expressed in ($V\sqrt{Hz}$). The test system performs measurements from 10Hz by orders of magnitude to 100KHz with an effective bandwidth of 1Hz at each tested frequency.

Several source resistance (R_g) values were used in the measuring system to reveal the effects of R_g on each type of Harris' op amps and to obtain proper voltage noise values essential for current noise calculations.

A Discussion On "Popcorn" Noise

"Popcorn" noise was first discovered in early 709 type op amps. Essentially it is an abrupt step-like shift in offset voltage (or current) lasting for several milliseconds and having amplitude from less than one microvolt to several hundred microvolts. Occurance of the "pops" is quite random — an amplifier may exhibit several "pops" per second during one observation period and then remain "popless" for several minutes. Worst case conditions are usually at low temperatures with high values of R_g. Some amplifier designs and some manufacturer's products are notoriously bad in this respect. Although theories of the popcorn mechanism differ, it is known that devices with surface contamination of the semiconductor chip will be particularly bad "poppers". Advertising claims notwithstanding, the authors have never seen any manufacturer's op amp that was completely free of "popcorn". Some peak detector circuits have been developed to screen devices for low amplitude "pops", but 100% assurance is impossible because an infinite test time would be required. Some studies have shown that spot noise measurements at 10Hz and 100Hz, discarding units that are much higher than typical, is an effective screen for potentially high "popcorn" units.

The vast majority of Harris op amps will exhibit less than 3 μV peak-to-peak "popcorn". Screening can be performed, but it should be noted that the confidence level of the screen could be as low as 60%.

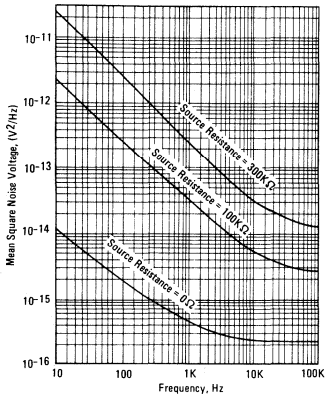
References

Fitchen, F.C. and Motchenbacker, C.D. Low Noise Electronic Design. New York: John Wiley and Sons, 1973.

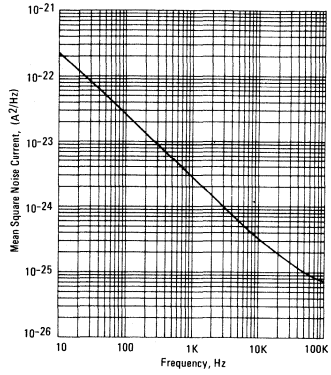
Instruction Manual, Model 2173C Transistor Noise Analyzer Control Unit. Quan-Tech, Division of KMS Industries. Whippany, New Jersey.

Typical Spot Noise Curves Unless Otherwise Noted: $V_S = \pm 15V$, $T_A = +25^oC$

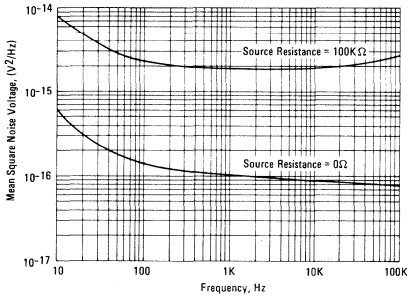
HA-2500/2510/2520 INPUT NOISE VOLTAGE



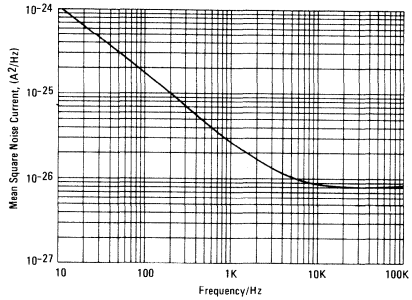
HA-2500/2510/2520 INPUT NOISE CURRENT



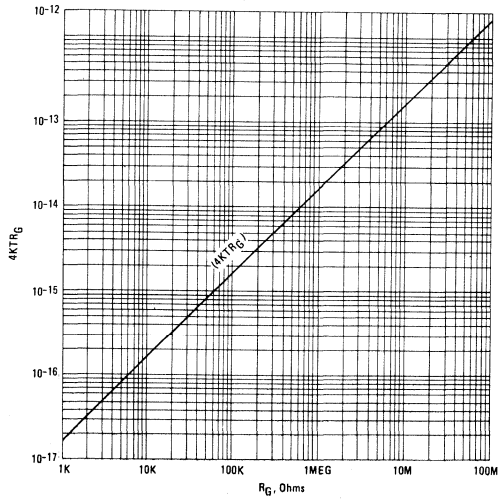
HA-4741 INPUT NOISE VOLTAGE



HA-4741 INPUT NOISE CURRENT



CURVE 12



CMOS ANALOG MULTIPLEXERS AND SWITCHES; APPLICATIONS CONSIDERATIONS

Don Jones and Al Little

Introduction

This article describes several important considerations for the use of CMOS analog multiplexers and switches. It includes selection criteria, parameter definitions, handling and design precautions, interfacing, typical applications, and special topics such as overvoltage protection and R.F. switching. Some other devices which perform analog switching functions are discussed as well.

Application Note 521 is also recommended for the analog multiplexer and switch user. It details the different CMOS processes used by various manufacturers, showing the performance trade-offs and failure modes which may be encountered with each.

Choosing the Right Device

A. Multiplexers: Protected or Unprotected?

Analog input signals which originate externally to a system can be destructive to a multiplexer for several reasons:

1. Analog signals may be present while the MUX power supplies are off.
2. The signal lines may receive induced voltage spikes from nearby sources.
3. Static electricity may be introduced on the signal lines by personnel or equipment.
4. Grounding problems are frequent; A. C. power line voltages at high impedance can appear on the signal lines. Signal lines can be accidentally shorted to other voltage sources.

Each of these situations are common in data acquisition, telemetry, and process control systems. In each case, a voltage at the multiplexer input exceeds the rail voltage. Without current limiting, this voltage will degrade or destroy the device.

Any conventional CMOS multiplexer can be protected against overvoltage destruction by external resistor-diode networks which limit input current to a safe level. Such networks are expensive, however, both in cost and in circuit board space. Another drawback is the output signal corruption that accompanies an overvoltage - regardless of which input is selected. This occurs due to parasitic bipolar transistors within the multiplexer which turn on during overvoltage. (Application Note 521 explains this mechanism in detail).

A few multiplexers feature built-in overvoltage protection, designed to eliminate the external networks. The protection capability varies widely among these devices, however. Some offer very slight advantages over ordinary multiplexers while others withstand wide voltage extremes. Unfortunately, nearly all suffer from the same output signal corruption problem described above.

Harris overvoltage protected multiplexers, HI-506A/507A/508A/509A, are an exception to this rule. During overvoltage, active protection circuitry automatically shuts off the parasitic transistor, thereby preventing output signal contamination. These devices will withstand a continuous voltage on any one input of ±20 Volts greater than either supply (this limitation is due only to temperature rise considerations at maximum ambient) and have withstood simulated static discharge conditions of greater than 4,500 Volts.

It should be emphasized that only the HI-506A through 509A (and exact equivalents from authorized alternate suppliers) will have this kind of protection necessary for inputs from the outside world. Certain CMOS process improvements, such as "floating body" and "buried layer" do help minimize one failure mode (latchup) but will still fail under excess voltage or current conditions prevalent in this type application.

A simplified equivalent circuit of the Harris internal protection network is shown in Figure 1.

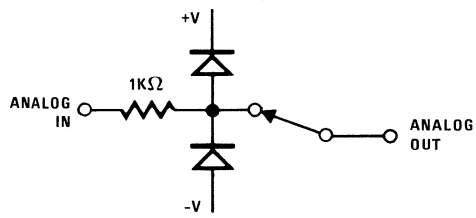


FIGURE 1.

This will help answer the question of what happens when the supplies are turned off, but input signals are present. If the supplies are shorted to ground, then the inputs will have about 1KΩ impedance to ground. If the supplies are open circuit, then the most positive and most negative inputs will act as supplies to the multiplexer.

In normal operating parameters, internally protected multiplexers have one difference from the unprotected versions-ON resistance is necessarily higher because of the added series current limiting resistor. However, to achieve the same degree of protection with conventional devices, the same resistance must be added externally, plus external diodes which would add to the effective leakage currents.

Conventional unprotected multiplexers are suitable for systems where the MUX inputs come from sources within the equipment, such as from op amps powered by the same ±15 volt supplies. The HI-506/507/1818A/1828A are intended for this type system. They are entirely free of any latch-up tendency, which have plagued some other types, even in these more benign applications. They are also free of the performance compromises which have accompanied some attempts to cure the latch-up problem.

B. Which Switch To Switch To?

Harris furnishes a complete line of CMOS analog switches, including replacements for most of the available CMOS and JFET switches. All types feature rugged no-latch-up construction, uniform characteristics over the analog signal range, and excellent high frequency characteristics.

The HI-200 and HI-201 replace the popular, low cost DG200 and DG201 types dual and quad switches.

The HI-1800A is low leakage dual DPST switch with a versatile addressing scheme, allowing use of a single type for many different switching functions.

The HI-5040 through HI-5051 are low resistance types, offering one to four switches in virtually all combinations. These replace the HI-5040 series with significantly better performance, and with both 75 ohm and 30 ohm switches available in all configurations. These are also plug-in replacements for many of the DG180 and DG190 series of FET hybrid switches, offering the advantage of monolithic construction, but with slightly longer switching times.

The analog switches do not contain overvoltage protection on the analog inputs, although they will withstand inputs 2 or 4 volts greater than the supplies. External current limiting should be provided if higher overvoltages are anticipated, such as a resistor in series with the analog input of value: $R(ohms) \geq (V_{IN} - V_{SUPPLY}) \times 50$ where VIN is the maximum expected input voltage. All digital inputs do have overvolgate/static charge protection.

Data Sheet Definitions

A. Absolute Maximum Ratings

As with all semiconductors, these are maximum conditions which may be applied to a device (one at a time) without resulting in permanent damage. The device may, or may not, operate satisfactorily under these conditions - conditions listed under "Electrical Characteristics" are the only ones guaranteed for satisfactory operation.

B. V_S, Analog Signal Range

The input analog signal range over which reasonable accurate switching will take place. For supply voltages lower than nominal, V_S will be equal to the voltage span between the supplies. Note that other parameters such as R_{ON} and leakage currents are guaranteed over a smaller input range, and would tend to degrade towards the V_S limits. All Harris devices can withstand $+V_S$ applied at an input while $-V_S$ is applied to the output (or vice-versa) without switch breakdown - this is not true for some other manufacturers' devices.

C. R_{ON}, On Resistance

The effective series on-switch resistance measured from input to output under specified conditions. Note that R_{ON} changes with temperature (highest at high temperature) and to a lesser degree with signal voltage and current.

D. $I_S(OFF)$, $I_D(OFF)$, $I_D(ON)$: Leakage Currents

Currents measured under conditions illustrated on the data sheet. Harris prefers to guarantee only worstcase high temperature leakages, because room temperature picoampere levels are virtually impossible to measure repeatable on available automated test equipment. Even under laboratory conditions, fixture and test equipment stray leakages may frequently exceed the device leakage. Leakages tend to double every 10°C temperature rise, so it is reasonable to assume that the +25°C figure is about 0.001 times the +125°C measurement; however, in some cases there may be ohmic leakages, such as on the package surface, which would make the +25°C reading higher than calculated.

Each of these leakage figures is the algebraic sum of all currents at the point being measured: to each power supply, to ground, and through the switches; so the current direction cannot be predicted. In making an error analysis it should be assumed that all leakages are in the worst-case direction.

In most systems, $I_D(ON)$ has the most effect, creating a voltage offset across the closed switch equal to $I_D(ON) \times R_{ON}$.

E. V_{AL}, V_{AH}; Input Thresholds

The lower and upper limits for the digital address input voltage at which the switching action takes place. All other parameters will be valid if all "0" addressd inputs are less than V_{AL} and all "1" inputs are greater than V_{AH}. Logic compatibility will be discussed in detail later in this paper.

F. I_A, Input Leakage Current

Current at a digital input, which may be in either direction. Digital inputs on Harris devices are similar to CMOS logic inputs; connection to MOS gates through resistor-diode protection networks. Unlike some other devices there is no DC negative resistance region which could create an oscillating condition.

G. T_A, T_{ON}, T_{OFF}; Access Time

The logic delay time plus output rise time to the 90% point of a full scale analog output swing. After this time the output will continue to rise, approaching the 100% point on an exponential curve determined by $R_{ON} \times C_D(OFF)$.

H. T_{OPEN}, Break-Before-Make Delay

The time delay between one switch turning OFF and another switch turning ON; both switches being commanded simultaneously. This prevents a momentary condition of both switches being ON, generally a very minor problem.

I. $C_S(OFF)$, $C_D(OFF)$, $C_D(ON)$ Input/Output Capacitance

Capacitance with respect to ground measured at the analog input/output terminals. $C_D(ON)$ is generally the sum of $C_S(OFF)$ and $C_D(OFF)$. $C_D(OFF)$ is usually the most important term as rise time/settling characteristics are determined by $R_{ON} \times C_D(OFF)$, as well as the high frequency transmission characteristics.

J. $C_{DS}(OFF)$, Drain to Source Capacitance

The equivalent capacitance shunting an open switch.

K. OFF Isolation

The proportion of a high frequency signal applied to an open switch input appearing at the output:

$$\text{off isolation} = 20 \log \frac{V_{IN}}{V_{OUT}}$$

This feedthrough is transmitted through $C_{DS}(OFF)$ to a load composed of $C_D(OFF)$ in parallel with the external load. The isolation generally decreases by 6dB/octave with increasing frequency.

L. C_A, Digital Input Capacitance

Capacitance to ground measured at digital input. This chiefly affects propagation delays when driven by CMOS logic.

M. P_D, Power Dissipation: I+, I-

Quiescent power dissipation, $P_D = (V+ \times I+) + (V- \times I-)$. This may be specified both operating and standby ("Enable" pin ON/OFF). Note that, as with all CMOS devices, dissipation increases with switching frequency; but that Harris devices exhibit much less of this effect.

Care And Feeding of Multiplexers And Switches

Dielectrically isolated CMOS ICs require no more care in handling and use than any other semiconductor - bipolar or otherwise. However, they are not indestructible, and reasonable common sense care should be taken.

In a laboratory breadboard, power should be shut off before inserting or removing any IC. It is especially important that supply lines have decoupling capacitors to ground permanently installed at the IC socket pins, as intermittent supply connections can create high voltage spikes through the inductance of a few feet of wire.

Because each of the major manufacturers of CMOS multiplexers and switches uses a radically different process, it is urged that units from all prospective suppliers be equally tested in breadboards and prototypes. It will be interesting to note which types survive best the hazards of a few weeks of breadboard testing.

Particular care of semiconductors during incoming inspection and installation is quite important, because the cost of reworking finished assemblies with even a small percentage of preventable failures can seriously erode profits. All equipment should be periodically inspected for proper grounding. With these devices, it is not usually necessary to shackle personnel to the nearest water pipe, if reasonable attention is paid to clothing and floor coverings; but be alert for periods of unusually high static electricity. If special lines are already set up for handling MOS devices, it wouldn't hurt to use them.

There are a few good rules for P.C. card layout:

1. Each card or removable subassembly should contain decoupling capacitors for each supply line to ground. This not only helps keep noise away from the analog lines, but gives good protection from static electricity damage when loose cards are handled.

2. When digital inputs come through a card connector, the pull-up resistor should be at the CMOS input. This forces current through the connector and prevents possible dry circuit conditions (see following discussion on digital interface).

3. All unused digital inputs must be tied to logic "0" (ground) or logic "1" (logic supply or device + supply) depending on truth table and action desired. Open inputs tend to oscillate between "0" and "1". It would also be best to ground any unused analog inputs/outputs and any uncommitted device pins.

Digital Interface

A. Reference Connection

HI-5040 thru HI-5051 and HI-1800A/1818A/1828A require a connection to the digital logic supply (+5V to +15V).

The HI-200/201/506A/507A have V_{REF} pins which are normally left open when driving from +5 volt logic (DTL or TTL), but may be connected to higher logic supplies (to +15V) to raise the threshold levels when driving from CMOS or HNIL. The HI-200/201 will have significantly lower power dissipation when V_{REF} is connected to a high level supply.

The HI-506/507/508A/509A do not have V_{REF} terminals, but will operate reliably with any logic supplied from +5 to +15 volts.

B. DTL/TTL Interface

One major difference found in comparisons of similar devices from different manufactures is the worst-case digital input high threshold (V_{AH} or V_{IH}). These range anywhere from +2V to +5V; and anything greater than +2.4V is obviously not compatible with worst-case TTL output levels. The fact is that no CMOS input is truly TTL compatible unless an external pull-up resistor is added. TTL output stages were not designed with CMOS loads in mind.

The experienced designer will always add a pull-up resistor from CMOS input to the +5 volt supply when driving from TTL/DTL:

1. Interchangeability: allows substitution of similar devices from several manufacturers.
2. Noise immunity: a TTL output in the "high" condition can be quite high impedance. Even when voltage noise immunity seems satisfactory, the line is quite susceptible to induced noise. The pull-up resistor will reduce the impedance while increasing voltage noise immunity.
3. Compatibility: one manufacturer does guarantee +2.0 volt minimum V_{AH}. However, this is accomplished with circuitry that is anything but TTL compatible: input current vs. voltage shows an abrupt positive then negative resistance region which is not the kind of load recommended for an emitter follower stage. A pull-up resistor will swamp out the negative resistance. Other CMOS inputs capacitively couple internal switching spikes to the input which could cause double-triggering without the pull-up resistor.
4. Reliability: it shouldn't happen with carefully processed ICs, but any possible long term degradation of CMOS devices usually involves threshold voltage shifts. The pull-up resistor will help maintain operation if input thresholds drift out of spec. On units without adequate input protection, the resistor will also help protect the device when a loose P.C. card is handled. Where the interface goes through a P.C. connector, the resistor will force current through the connector to break down any insulating film which otherwise might build up and cause erratic dry circuit operation.

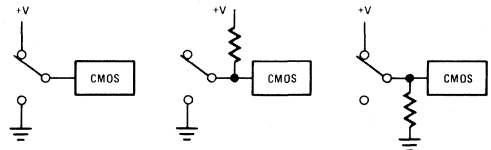
A 2K ohm resistor connected from the CMOS input to the +5 volt supply is adequate for any TTL type output. If power consumption is critical, open collector TTL/DTL should be used, allowing a higher value resistor - the voltage drop across the resistor is computed from the sum of specified "1" level leakage currents at the TTL output and CMOS input.

C. CMOS Interface

The digital input circuitry on all Harris devices is identical to series 4000 and 54C/74C logic inputs, and is compatible with CMOS logic with supplies between +5V and +15V without external pull-up resistors.

D. Electromechanical Interface

When driving inputs from mechanical switches or relays, either a pull-up or pull-down resistor must be connected at the CMOS input to clear the dry circuit and damp out any spikes, as illustrated in Figure 2, (b) and (c).



(a) POOR (b) GOOD (c) GOOD

FIGURE 2.

A Practical Multiplexer Application

Figure 3 illustrates a practical data acquisition system hookup using an analog multiplexer, a monolithic sample-and-hold and an A/D converter. The HA-2420/2425 sample-and-hold is a particularly good choice for this type application because it eliminates the need for a separate high impedance, high slew rate buffer amplifier. Its acquisition time is consistent with CMOS multiplexer settling times and most available A/D conversion times. Errors, after initial adjustment, are consistent with up to 12 bit absolute accuracy over a wide temperature range.

A. Accuracy

D.C. error sources include:

1. Multiplexer:
   a. input offset = R source x I_S(OFF)
   b. output offset = R(ON) x (I_D(ON) + I bias (S/H)
2. Sample-and-Hold
   a. input offset voltage
   b. charge injection; sample-to-hold offset
   c. gain error during "hold"
   d. drift during hold
3. A/D converter:
   a. linearity
   b. gain drift
   c. offset drift

Item 1(a) and (b), and 2(d) become significant only at very high temperatures. 2(a) and (b) are initially adjusted out with the offset adjustment pot on the S/H. 2(c) is usually adjusted out by A/D gain adjustment, but could also be removed by a voltage divider feedback on the S/H to give a slightly greater than unity gain during "sample". After initial adjustments, typical S/H errors are less than 0.5mV over 0°C to +75°C. Note that after adjustment, there may be an appreciable offset at the S/H output when switching from sample to hold. This is not a problem, since accuracy is required only during "hold", and the system is adjusted for this.

The largest system errors are usually 3(b) and (c), drifts with temperature and time. If two multiplexer channels can be dedicated for stable (+) and (-) reference voltage inputs, then the data processor can continuously calibrate the system, effectively removing all errors, except 1(a) and 3(a) which are usually negligible.

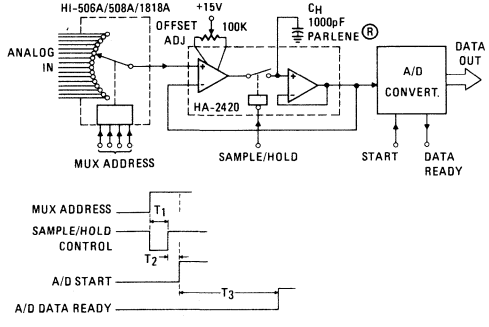


FIGURE 3.

B. Timing

The timing diagram in Figure 3 indicates the necessary system delays for each multiplexer address:

T_1 is the combined acquisition time for the multiplexer and S/H.
T_2 is the short interval required for the sample-to-hold transient to settle.
T_3 is the A/D conversion time.

The following table indicates minimum recommended timing for ±10 volt input range for acquisition/settling times to ½ LSB accuracy:

	T_1	T_2
10 bit:	6μs	1μs
12 bit:	12μs	2μs

The multiplexer, by itself, requires about 2μs and 9μs settling to 10 bit and 12 bit accuracy, respectively; but fortunately this can be concurrent with S/H acquisition time. This is longer than would be predicted by the R_{ON} C_D time constant; probably because of internal distributed capacitance, a rather long period is required to traverse the last few millivolts towards the final value.

It should be noted that impedance conditions at the multiplexer inputs can affect the necessary acquisition time. At the instant the multiplexer switches from one channel to a new one, there is appreciable current pulled through the new channel input in order to charge C_D from its old level to its new level. This can cause ringing on signal lines, or glitches at signal conditioning amplifier outputs which require longer periods to settle. It is best for signal conditioning amplifiers to be wide band types, such as HA-5170, so that their high frequency output impedance is low and recovery from load transients is fast; even though the signal to be measured is very low bandwidth.

The T_1 and T_2 times could be eliminated by alternating two S/H circuits, acquiring a new signal on the second while A/D conversion is taking place. The two S/H circuits would have inputs connected together, and outputs alternately connected to the A/D by an analog switch. Total time, then, would be T_3 plus the analog switch settling time.

If the MUX input channels are sequentially switched, each channel will be sampled at a rate of:

$$FS = \frac{1}{N(T_1 + T_2 + T_3)}$$

samples per second, where N is the number of channels. The frequency spectra of the input signals must then be no higher than $\frac{FS}{2}$.

In many systems, however, each channel carries a different maximum frequency of interest, and it may be desirable to depart from simple sequential scanning. Quickly varying signals, for example, could be addressed several times during a scanning period.

C. Adding Channels

For more than sixteen channels, several multiplexers may be tied together at the outputs, and addressed in parallel, but with only one "enabled" at a time. The MUX output offset will be increased, since I_D (OFF or ON) is additive. Also, output capacitance, C_D, is additive, creating increased access times.

These errors can be minimized in large systems by having several tiered levels of multiplexing; where the outputs of a number of MUXs are individually connected to the inputs of another MUX.

D. Differential Multiplexing

When low level analog signals must be conducted over a distance, it is generally better, from a noise pickup standpoint, to use a balanced transmission line carrying signals which are differential with respect to ground.

A dual multiplexer is used for this purpose, as shown in Figure 4. Two sample-and-hold circuits plus an op amp form a high impedance differential sample-and-hold with gain. At gains greater than 4, the minimum sampling time (T_1 in previous example) must be increased proportionately to gain to allow for overdamped settling characteristics.

When handling low level, or high impedance signals, consideration should be given to adding signal conditioning amplifiers at the signal sources, since this can often produce less troublesome, more accurate, lower cost systems.

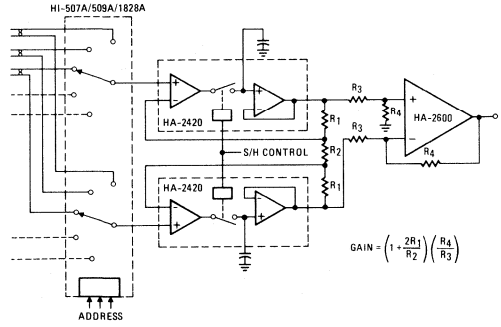


FIGURE 4.

E. Demultiplexing

Since the switches in a CMOS MUX conduct equally well in either direction, it is perfectly feasible to use it as a single input-selected multiple output switch. Figure 5 illustrates its use as a demultiplexer, with capacitors to hold the output signal between samples. When the address lines are synchronous with the address of the original multiplexer, the output lines will create the original inputs, except level changes will be in steps.

Overvoltage protection is not effective with signals injected at the normal MUX output, so an external network should be added, if necessary.

A more accurate demultiplexer could be constructed using the HA-2420/2425 sample-and-hold for each channel, connecting inputs together and sampling each channel sequentially.

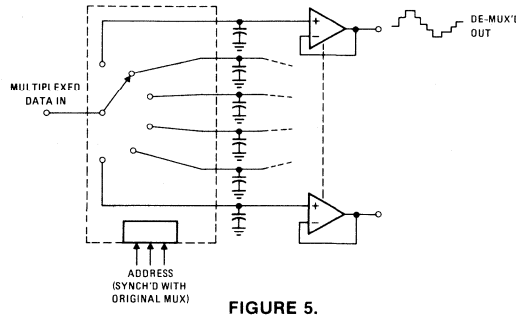


FIGURE 5.

Analog Switch Applications

A. High Current Switching

Analog switches are sometimes required to conduct appreciable amounts of current, either continuous, or instantaneous - such as charging or discharging a capacitor. For best reliability, it is recommended that instantaneous current be limited to less than 80mA peak and that average power over any 100 millisecond period be limited to $I^2R_{ON} \leq$ (absolute maximum derated power-quiescent power). Note that R_{ON} increases at high current levels, which is characteristic of any FET switch. Switching elements may be connected in parallel to reduce R_{ON}.

B. Op Amp Switching Applications

When analog switches are used either to select an op amp input, or to change op amp gain, minor circuit rearrangements can frequently enhance accuracy. In Figure 6(a), R_{ON} of the input selector switch adds to R_1, reducing gain and allowing gain to change with temperature. By switching into a noninverting amplifier (b), gain change becomes negligible. Similarly, in a gain switching circuit, R_{ON} is part of the gain determining network in (c), but has negligible effect in (d).

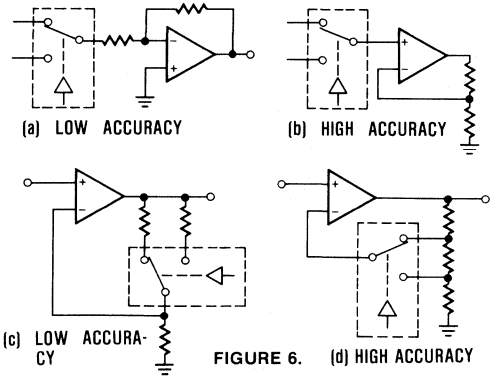


FIGURE 6.

C. Switching Spikes And Charge Injection

Transient effects when turning a switch off or on are of concern in certain applications. Short duration spikes are generated (Figure 7(a)) as a result of capacitive coupling between digital signals and the analog output. These have the effect of creating an acquisition time interval during which the output level is invalid even when little or no steady state level change is involved. The total net energy (charge injection) coupled to the analog circuit is of concern when switching the voltage on a capacitor, since the injected charge will change the capacitor voltage at the instant the switch is opened (Figure 7(b)).

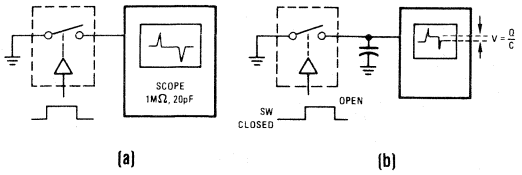


FIGURE 7.

Charge injection is measured in picocoulombs; the voltage transferred to the capacitor computed by

$$V = \frac{\text{Charge (pC)}}{\text{Capacitance (pF)}}$$

Both of these effects are, in general, considerably less for CMOS switches than for equivalent resistance JFET or PMOS devices, since the gate drive signals for the two switching transistors are of opposite polarity. However, complete cancellation is not possible, since the N and P channel switches do not receive gate signals quite simulaneously, and their geometrics are necessarily different to achieve the desired D.C. resistance match.

In applications where transients create a problem, it is frequently possible to minimize the effect by cancellation in a differential circuit, similar to Figure 8.

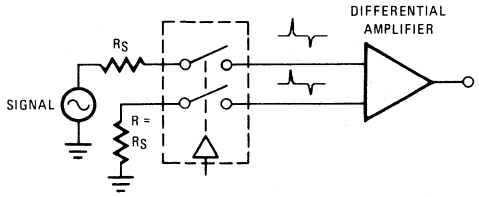


FIGURE 8.

Among the Harris analog switches, the HI-201 is the best from the transient standpoint, having turn-on spikes of about 100mV peak, 50ns width at the 50% point, and charge injection at turn-off of about 20 picocoulombs. Transients of the HI-5040 series are several times higher.

D. High Frequency Switching

When considering a switching element for R.F. or video type information, two factors must be watched: attenuation vs. frequency characteristics of an ON switch, and feedthrough vs. frequency characteristics of the OFF switch. Optimizing the first characteristic requires a low $R_{ON} \times C_D$ product, and the second a low value of C_{DS} (OFF).

One approach is to use the 30 ohm switch types of the HI-5040 series.

Figure 9 illustrates three circuit configurations; (a) is a simple series switch, (b) is a series-shunt configuration to reduce feedthrough, and (c) is a SPDT selector configuration with series-shunt elements. A 1K ohm load is illustrated, which might be the input impedance of a buffer amplifier; a lower load resistance would improve the response characteristics, but would create greater losses in the switch and would tend to distort high level signals.

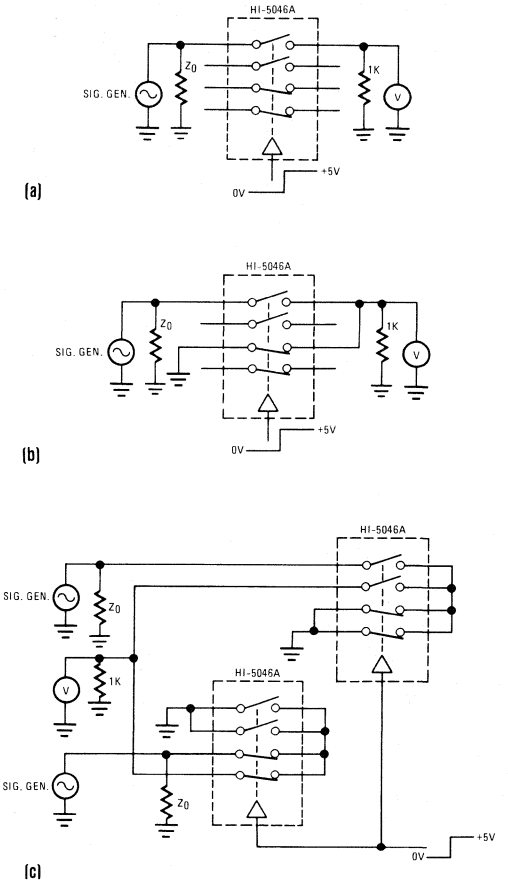


FIGURE 9.

Figure 10 shows ON and OFF frequency response for each of the above configurations. Arbitrarily, we will define useful frequency response as the region where ON losses are less than -3dB and OFF isolation is greater than -40dB.

The simple configuration (a) has excellent ON response, but OFF isolation limits the useful range to about 1MHz (the data sheet indicates -80dB isolation at 100kHz, but this is measured with 100 ohms load, which acounts for the 20dB difference).

The circuit in (b) shows a good improvement in isolation produced by the low impedance of the shunt switch. The useful range is about 10MHz; which could also be achieved in a simple SPDT 2-switch selector if source impedances are very low.

The selector switch in (c) has excellent characteristics, both ON and OFF curves indicating 40MHz useful response. Additional switches connected to the same point would reduce the ON response because of added shunt capacitance; but this could be eliminated by feeding separate summing amplifier inputs.

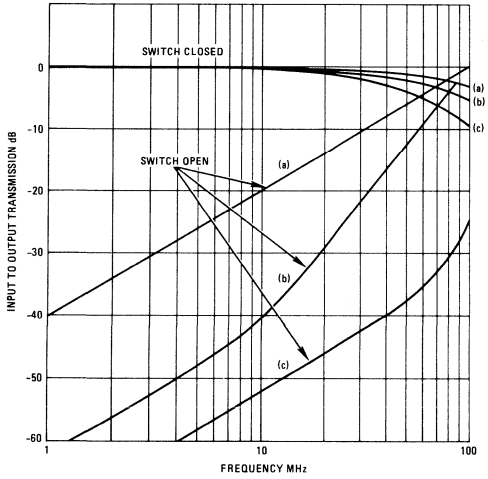


FIGURE 10.

For many applications, a better approach is to use the HI-524 monolithic wideband CMOS multiplexer. This device utilizes a series-shunt multiple switching network to achieve low crosstalk without sacrificing or compromising other operational parameters. As shown in Figure 11, each channel comprises three CMOS FET switch gates, with two in series and the third shunted to ground. The two series switches ensure both a high off isolation and low feed-through capacitance. The shunt grounding switch, closed automatically by the control logic when its corresponding series pair are open, shunts nonselected channels to ground, thus minimizing cross talk. With this circuit topology, crosstalk is typically -60dB at 10MHz.

A buffer amplifier is used with the HI-524 for high frequency applications, due to its higher ON resistance, and should offer sufficient bandwidth and slew rate to avoid degradation of the anticipated signals. For video switching, the HA-5033 and HA-2542 offer good performance plus ±100mA output current for driving coaxial cables. For general wideband applications, the HA-2541 offers

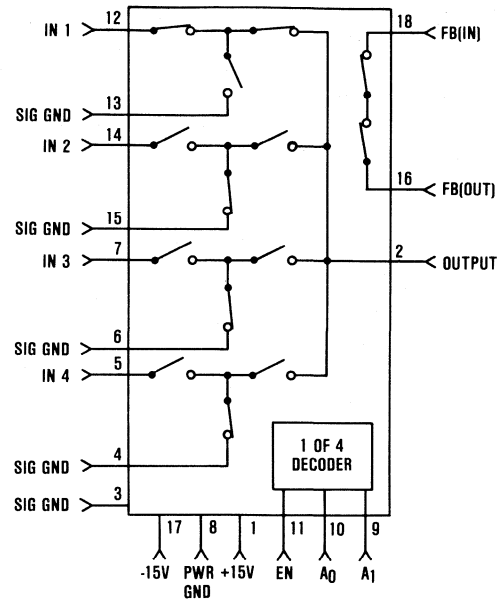


FIGURE 11.

the convenience of unity gain stability plus 90ns settling (to ±0.1%) and ±10V output swing. Also, the HI-524 includes a feedback resistance for use with the HA-2541. This resistance matches and tracks the channel ON resistance, to minimize offset voltage due to the buffer's bias currents.

Careful layout is, of course, important for high frequency switching applications to avoid feedthrough paths or excessive load capacitance.

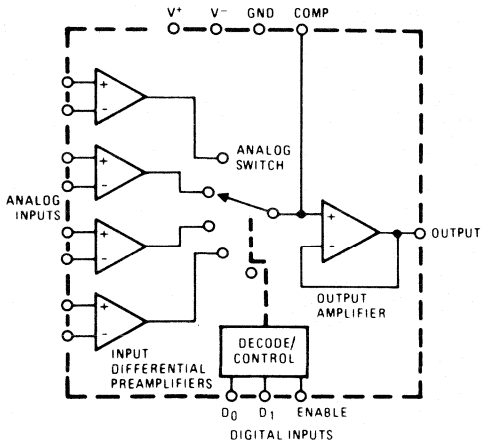
Alternatives to CMOS Switches and Multiplexers

CMOS devices are excellent in many applications. However, there are some other devices which merit consideration in certain analog switching circuits where they may improve performance, reduce parts count, or be more economical.

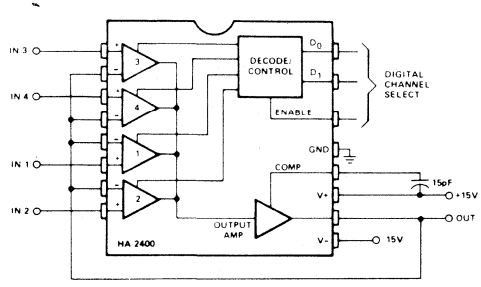
A. The PRAM, Programmable Amplifier

The HA-2400/2405 is a unique monolithic bipolar circuit which combines analog switching with high performance operational amplifiers. It basically consists of four op amp type input stages, any one of which is connected to a single output by bipolar switches controlled through a TTL compatible address decoder. In a single package, it contains the equivalent of 5 op amps plus a 4 channel multiplexer. It has literally hundreds of applications in signal selection and programmable signal conditioning.

Figure 12 illustrates a four channel multiplexer. Connections from the output to each input stage are always the same as a comparable op amp circuit; the +1 gain connection is illustrated.



(a) FUNCTIONAL DIAGRAM



(b) ANALOG MULTIPLEXER WITH BUFFERED INPUT AND OUTPUT

FIGURE 12.

Advantages over a comparable CMOS multiplexer circuit areas follows:

1. High input impedance (10^{12} ohnms), low output impedance (<0.1 ohm) means than ON resistance and leakage currents are no longer of concern. There is negligible transient loading of input lines.
2. Gain filtering, etc. can easily be added with feedback networks.
3. Fast acquistion (1.5μs).
4. Wide bandwidth (8MHz).
5. Superior feedthrough characteristics (-110dB at 10kHz, -60dB at 1MHz).

Disadvantages include:

1. Less accuracy for low level D.C. signals; the offset voltages of each input stage do not necessarily match or track each other.
2. Cannot be used in reverse as a demultiplexer.
3. Disabling the device (enable pin low) does not open the output line, or drive the output to zero. Adding channels may be accomplished by tying compensation pins together.

Figure 13 illustrates the PRAM used as a programmable gain amplifier. Any connection possible with op amps can be wired 4 ways to make programmable active filters, oscillators, etc., etc. Harris Application Note 514 shows many possibilities.

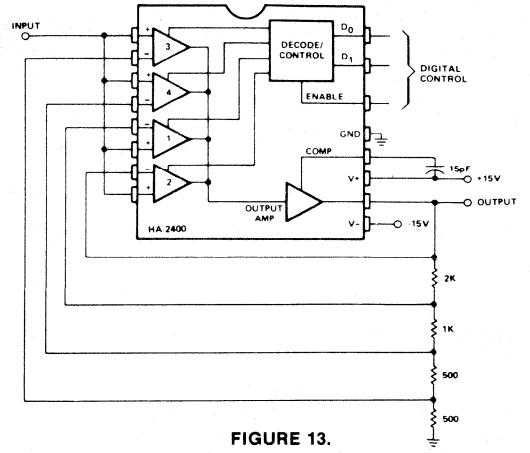


FIGURE 13.
AMPLIFIER, NONINVERTING PROGRAMMABLE GAIN

B. Sample-And-Hold

The sample-and-hold function has often been accomplished with separate analog switches and op amps. These designs always involve performance tradeoffs between acquisition time, charge injection, and droop rate.

The HA-2420/2425 monolithic sample-and-hold, illustrated previously in Figure 3 has many times better tradeoffs, usually at a lower total cost than the other approaches. The switching element is a complementary bipolar circuit with feedback which allows high charging currents (30mA), low charge injection (10pC), and ultra low OFF leakage current (5pA); a combination not approached in any other electronic switch. These factors make it also superior as an integrator reset switch, or as a precision peak detector as shown in Figure 14. Harris Application Note 517 illustrates many other applications.

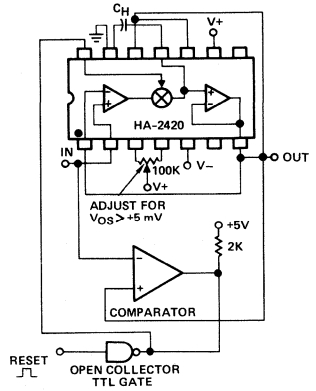


FIGURE 14.

APP NOTE

FOR YOUR INFORMATION

No. 521

Harris Analog

GETTING THE MOST OUT OF CMOS DEVICES FOR ANALOG SWITCHING JOBS

By: Ernie Thibodeaux
and Al Little

Introduction

CMOS analog switches and multiplexers are now widely used for a broad range of applications. They offer low power consumption, low on-resistance, and will conduct a signal in either direction. In addition, CMOS switch structures exhibit no DC offset voltage and can usually handle signals up to the supply rails.

Not all CMOS analog switches are alike, however. Different technologies are employed by different manufacturers. Some types, handicapped by inherent process limitations, can create significant problems for the user. Switches built with older types of junction isolation, for example, can literally self-destruct when a latch-up condition occurs. To prevent destruction, costly external protective circuits are needed, but the devices can still latch up unless the power is turned on and off in a set sequence. Switch circuits can also be destroyed by electrostatic discharge, input overvoltage spikes and power supply transients.

Newer types of technologies include latch-proof junction isolation (JI), floating-body junction isolation, and dielectric isolation (DI). Both JI techniques are conventional processes that have been slightly modified to alleviate the old problem of latch-up. However, both of these JI technologies still require costly external protection circuits to guard against burn-out in such applications as analog-signal multiplexing that interface them with the outside world. That is why JI devices are best suited for internal-switching applications where the electrical environment can be controlled. In contrast, the improved DI technology, by virtue of its construction, offers analog-switching devices suitable for many inside applications, as well as providing on-board analog protection for devices that interface with the other circuits. Happily, the smaller substrate area of the DI device delivers a better speed-power product than the JI technology.

The Basic CMOS Switch

The basic CMOS transistor (Figure 1) has parasitic junctions that are reverse-baised during normal operation. However, certain overvoltage conditions can forward-bias these junctions to cause high currents that could possibly destroy the devices.

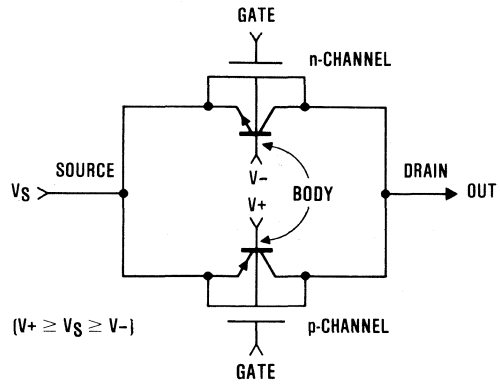


FIGURE 1. BAD

In the basic CMOS analog switch, the parasitic junctions are reversed-biased during normal operation. Large overvoltages, however, make them forward-biased and draw large currents.

The parasitic junctions are actually npn and pnp transistors that are normally reverse-biased by the applied body potentials. However, because many analog switches, and especially multiplexers, are connected to their analog sources through long lines, they are highly susceptible to externally induced voltage spikes. For example, these spikes, which can often exceed the p-channel body potential, V+, can inadvertently turn on a normally off switch through the parasitic pnp transistor (Figure 1).

The n-channel device is similarly affected when the parasitic npn transistor is turned on by a negative overvoltage. This action, commonly known as channel interaction, causes momentary channel-to-channel shorting, which introduces significant errors in the system. This intermittent condition is rarely isolated because it occurs only randomly.

One of the adverse effects of channel interaction is illustrated in Figure 2. Channel 1 of an analog multiplexer is selected when all other channels are off. Channel 16 receives an input-noise spike that momentarily exceeds the positive supply. The sequence causes channel 1 read-out to be +16V because of interaction with channel 16 just before initiating the hold command to the sample-and-hold device. To prevent this annoyance requires additional protective circuits that clamp each channel input to a voltage below the threshold of the parasitics to ensure that the channels remain inactive under any conditions.

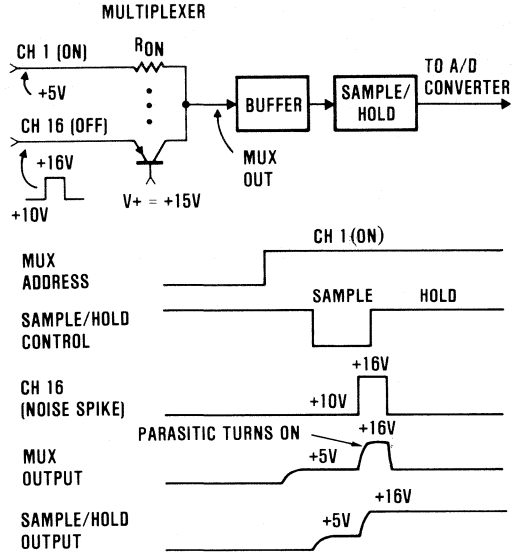


FIGURE 2. WORSE

With CMOS devices, noise spikes can cause channel interaction. In this multiplexer, although channel 1 is only one selected, noise spikes cause cross talk in channel 16, which affects reading.

A more serious condition exists when the substrates (p- or n-) lose their respective potentials to ground (Figure 3) -a condition that occurs when power to the device is turned off while the analog signals are still present. In this situation, the analog switch, which at that point represents a diode connected through the low impedance of the supply, draws high current from the analog source.

This current turns on the switch through its parasitics and shorts all channels to the output. These shorts can easily be catastrophic in multiplexer systems that have different power supplies for the analog source and the multiplexer switch. An error during troubleshooting or an inadvertent supply glitch can trigger this fault mode and destroy the whole system. Therefore, there is obviously much more to system reliability than having latch-proof CMOS devices.

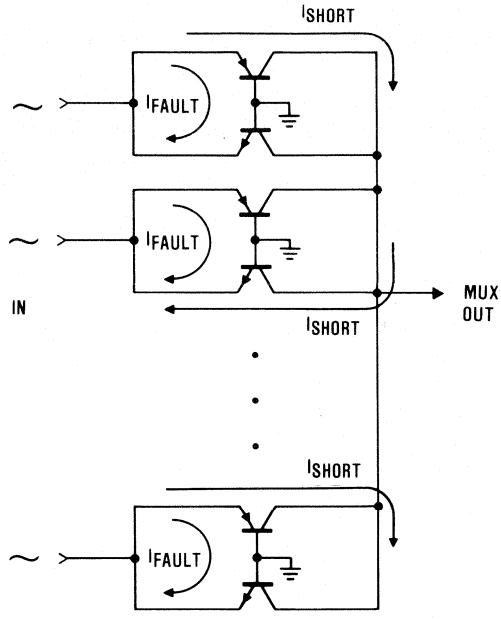


FIGURE 3. STILL WORSE

Most serious in CMOS swithes is losing substrate potential to ground. This condition, which happens when power is lost and the analog signal is present, causes very high currents.

Considering Latch-Proof JI Technology

The standard JI process has been modified by what is claimed to be latch-proof construction through control of the effective betas of the parasitic transistors. A cross section in Figure 4(a) shows the CMOS structure along with its parasitic transistors and the equivalent circuit in Figure 4(b) that gives rise to the silicon-controlled-rectifier latch-up problem.

Under any of the fault conditions previously mentioned, the npn and/or pnp can trigger this quasidual-gate SCR into a state of high conduction. If the transistor β product is 1 or greater, this configuration is sustained until either the device burns up or all sources of power are removed. By using a buried-layer configuration, as shown in the cross section, the β product is reduced to less than 1, eliminating the latch-up conditions.

Again, especially in multiplexer applications, the latch-free devices do not guarantee against destruction, and the JI multiplexer still requires costly discrete circuits around

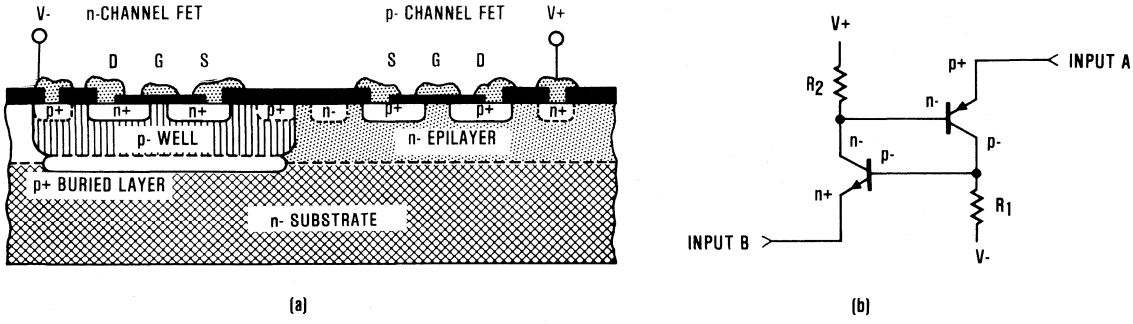


FIGURE 4. LATCH-PROOF.

Junction-Isolated devices are now made latch-proof with a buried-layer configuration (a), which keeps beta of parasitic transistor under unity. That kills chance for latch-up (b), which plagues devices built with older junction-isolation technology.

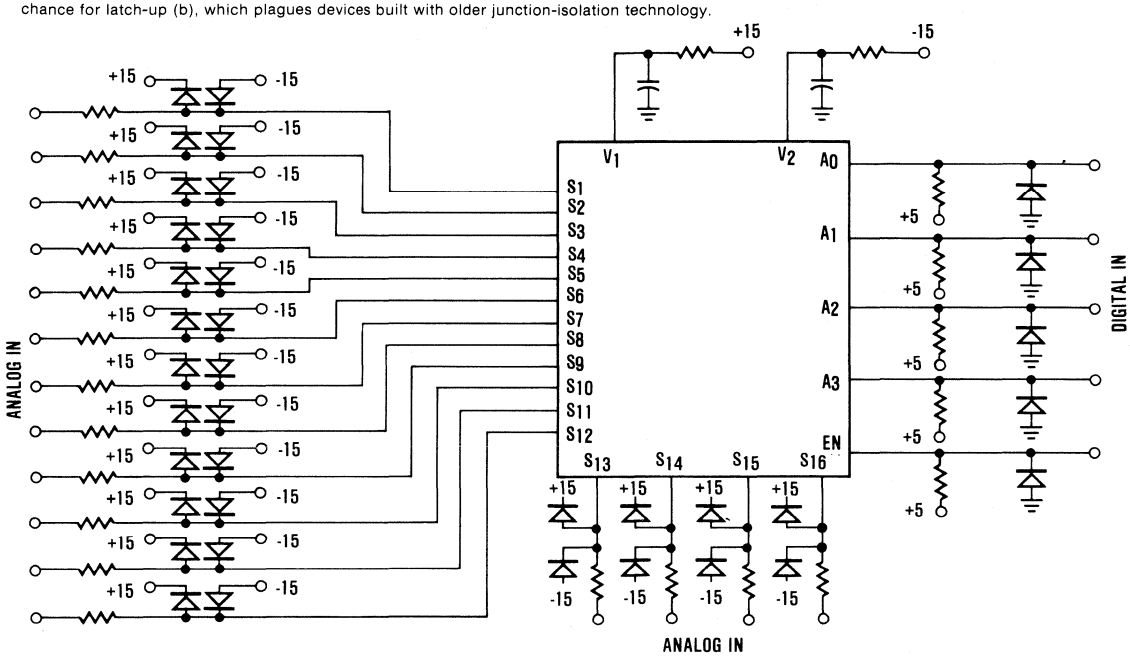


FIGURE 5. PROTECTION STILL NEEDED.

Although new JI devices won't latch up, they still can be destroyed by large currents. That's why typical JI multiplexers, like the one shown here, still need to be surrounded by external protective components, which drive up system costs.

the device, as shown in Figure 5. If an overvoltage exists, the resistor/diode circuit at each analog input limits the input voltage to the supply-voltage range to prevent the parasitic transistor action.

The resistors limit the overvoltage currents through the diodes. The diodes must have a low threshold voltage-much lower than the 0.6V silicon-junction threshold of the internal parasitic diodes-to ensure that the parasitics do not turn on.

A germanium diode offers a low threshold voltage, but its high leakage current makes it impractical, especially in 0.1% systems. Therefore, in most applications, more expensive low-leakage diodes are used.

For example, Schottky diodes meet the requirements but they are expensive. The total cost per multiplexer, including parts and labor, for the discrete protection circuit may well be double the initial purchase price of the device. Even then, its reliability will never approach that of an IC that has this protection already built in.

The Floating-Body JI Technology

Standard JI technology allows another approach to latch-proof device construction: a portion of the SCR continuity is broken by floating the "body" or substrate of the

n-channel switching device. A cross section of this process is similar to that in Figure 4(a), excluding the buried layer and the negative supply connection to the p- substrate, so that the dual-gate SCR is changed to a single-gate device that can only be triggered by the pnp parasitic. This, of course, reduces the latch-up probability by 50%.

To completely eliminate latch-up, as before, the β product of the transistors is reduced to less than 1. This accomplishment, certainly a significant improvement over the conventional process, offers greater reliability, but certain trade-offs must be made when the body of a MOSFET is floated.

Nominal source-to-drain breakdown voltages are reduced which limit the peak-to-peak signal range. Over-all breakdown is limited by the collector-emitter breakdown voltage, BV_{CEO}, of the non-parasitic transistor of the floating n-channel MOSFET. The breakdown voltage increases with the degree of reverse-bias potential applied to the substrate. With a floating body, BV_{CEO} is minimum, so particular care is necessasry when using these devices in configurations such as single-pole double-throw, dpst, and dpdt, where each side of the switch connects to opposite polarities. The peak-to-peak handling capability is specified at a minimum of 22V; therefore, 30V pk-pk cannot be switched with ±15V supplies, as it can with other CMOS devices.

What's more, the leakage currents of floating-body JI devices are higher than other types, simply because the ICEO of the floating base for the npn is much greater than ICBO of other devices having fixed reversed-biased body potentials. The increased leakage currents in spst switches may not be too significant.

However, in multiplexers that have the outputs of as many as 16 switches tied together in one IC, the total summation of currents can significantly affect system accuracy. For example, the specification for a worst-case 16-channel floating-body multiplexer is 10 microamperes, and the channel on resistance is 550 ohms. The DC offset error would be 5.5 millivolts, representing an accuracy to 0.055%.

Other 16-channel types specify worst-case parameters of 500 nanoamperes and channel resistance between 550 ohms and 2 kilohms. Their DC offset error is between 0.28mV and 1mV, respectively, allowing accuracy to 0.01% or better.

Finally, the effective off impedance of the floating-body switch is degraded by the floating-body technique. Off-isolation characteristics of a MOSFET are primarily determined by its source-to-drain capacitance. But with the base floating, the effective capacitance from emitter to collector is increased by the series combination of emitter-base and base-collector-junction capacitances (Figure 6a). This increase degrades the over-all off-isolation characteristics. For example, the off isolation for a typical floating-body channel at 1 megahertz that has R_L = 100 ohms is specified to be -54 decibels, which compares favorably with other types. However, at lower frequencies such as 1kHz, the isolation is only -62dB, compared to more than -110dB for improved devices. Capacitances C_1 and C_2 for them are shunted by the low AC impedance of the supply voltage (Figure 6b).

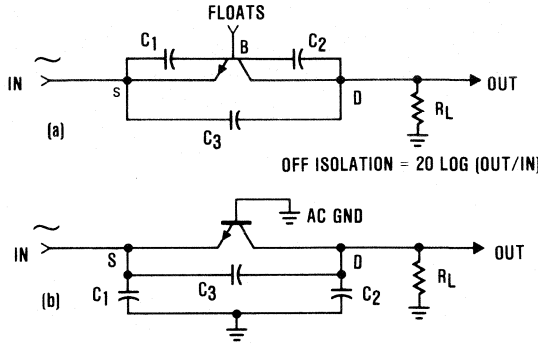


FIGURE 6. FLOATING BODIES.

Floating-body switches have degraded "off" impedance because total capacitance (a) combines two junction capacitances. In DI circuit (b), capacitances are shunted out.

The Linear Dielectric-Isolation Technology

The linear dielectric-isolation process requires no modifications to guard against latch-up. Its basic construciton ensures that the SCR configuration that causes latch-up can not exist. The functional cross section in Figure 7 reveals the silicon-dioxide isolation barrier fabricated between all parasitic transistors. This isolation allows each active element to be self-contained and independent with no interface junctions. At most, only three-layer structures are permitted for each tub, so that four-layer structures, or SCRs, are impossible. Also, since the DI technology requires no guard bands, junction capacitances, leakage currents, and size are minimized. The resulting increase in packing density per wafer, together with increased yields, enables these devices to be cost-competitive with other types.

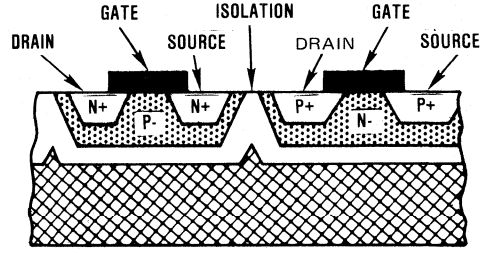


FIGURE 7. HOW DI DOES IT.

Dielectric isolation eliminates latch-up by a silicon-dioxide isolation barrier between devicees. This separates all active elements, eliminating interface junctions that cause parasitic SCRs.

In working with DI devices, the IC designer is not burdened with the fixed substrate potentials found in JI devices. He may let the substrate float, fix it to some

potential, or even modulate it. Figure 8 depicts a typical DI analog switch circuit that minimizes the variation of on resistance with the analog signal. Ordinarily, in conventional circuits, the body or substrate potentials of the n and p-channel devices are fixed and the source-to-body bias potentials vary with the analog input voltage. This change in body bias causes a wide variation of on resistance within the analog signal range. However, in the DI circuit, the bodies of P_1 and N_1 are connected together through N_3 during the on state. This allows the body to follow the input voltage providing a constant source-body bias and therefore a constant on resistance. During the offstate, the bodies of N_1 and P_1 are at their respective supply potentials through P_2 and N_2, thereby preserving high off isolation and low leakage currents.

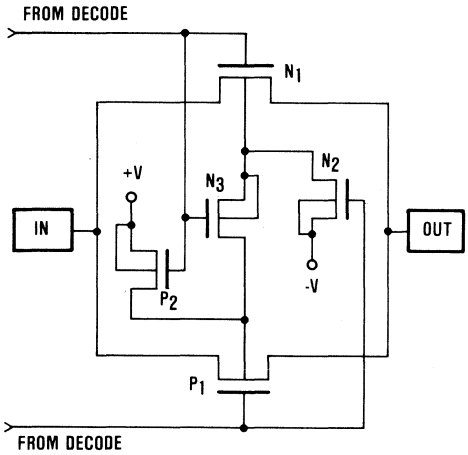


FIGURE 8. DI DOES IT.

In dielectrically isloated switches, on resistance modulation by the analog input is minimized by connecting N_1 and P_1 bodies together through N_3.

Designing a Foolproof CMOS Analog Multiplexer

In dielectrically isolated multiplexer circuits, protection can be provided on the chip primarily to eliminate channel interaction. This protection prevents normally off channels from being turned on by parasitics from other channels. And because this interaction is prevented, even worst-case power-supply faults cannot destroy the device. Moreover, since DI structures have no SCR effect, protection against latch-up and power-sequencing are not necessary. In short, DI multiplexers with built-in protection can withstand virtually any conceivable fault from the outside world.

The typical protected DI multiplexer (Figure 9) benefits from a combined bipolar/CMOS technology. The illustrated bipolar section is used to sense an analog over voltage condition and steer current away from the parasitic MOSFET junctions. Each of the switching devices, N_1 and P_1, has its own proteciton circuits. Devices P_3, D_6, D_7 and Q_6 protect P_1, while N_3, D_4, D_5 and Q_5 protect N_1. When the switch is off, the substrate of the p-channel FET, P_1, is connected to V+ through P_3 and diode D_7 for maximum isolation and low leakage currents in the off state. If the input voltage suddenly exceeds V+, the source-body junction, which would normally conduct, is instead clamped by transistor Q_6.

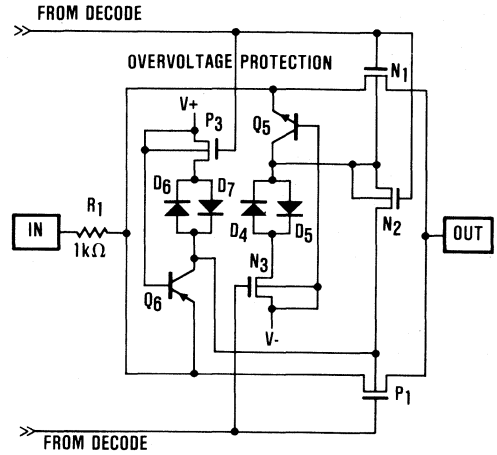


FIGURE 9. WINNING COMBINATION.

Combining bipolar and MOS technologies in the same multiplexer gives built-in protection. This circuit is typical for each channel in multiplexers HI-506A/07A/08A/09A and HI-546/47/48/49.

The base-emitter junction conducts to hold the source-body diode off with a saturation voltage VCE(SAT) of about 0.2V. Thus clamped, the switch is protected from the effects of overvoltage.

Clamp Q_6 always turns on before the forward-voltage drop of the source-body diode is exceeded because diode D6 requires an additional forward-voltage drop for conduction though the parasitic junciton. Moreover, resistor R_1 limits the current flowing through Q_6 when high overvoltages exist. Although R_1 adds to the total on-resistance of the channel, its associated error is insignificant, since most systems provide high-impedance buffering anyway. For negative overvoltages, N_1 is similarly protected. What's more, the protection circuit, rated at a continuous overvoltage of 35V, reveals a cross-talk current of only about 5nA (Figure 10).

When the switch is normally turned on, the substrates of N_1 and P_1 are connected together through N_2, which, as described before, results in a constant on resistance.

This condition represents an absolute error from channel interaction of only 6 microvolts (R_{ON} × 5nA) - certainly negligible in most systems. In contrast, floating-body types have guarantees only that they won't be burned up by ±25V overvoltage. Their manufacturers do not make any claim against channel interaction. In fact, channel interaction occurs readily in these devices when the n- and p-channel thresholds are exceeded by an overvoltage.

For example, the n-channel device, although floating, would be inadvertently turned on if the analog input exceeded the negative supply by its gate-to-source threshold, which is typically 1.5V.

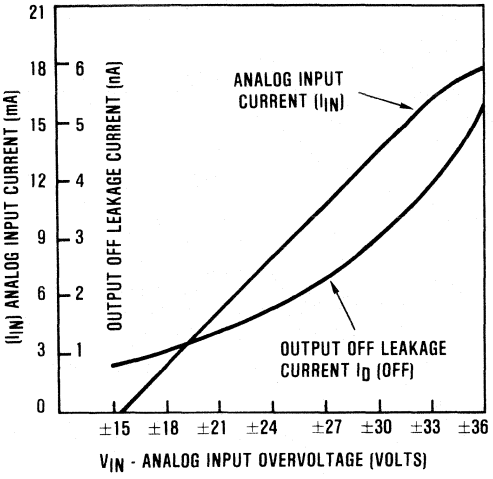


FIGURE 10. BLOCKING CROSS TALK.

DI switches have minimal cross-talk problems. An overvoltage of 33V produces a cross-talk current of only 5nA - an absolute error from channel interaction of only 6μV.

In addition to handling continuous input overvoltages, the HI - 506 A / 546 series multiplexers also survive very large transient conditions. These devices typically withstand repeated static discharges well beyond 4,000 volts at any analog input. In fact, even the unprotected HI-506/507/508/509 units can withstand discharges beyond 3,000 volts, though they do not compare to the steady state and signal protection offered by the "A" series.

Adding Benefits

Additional DI benefits are passed on to the user in the design of the digital input-protection circuit shown in Figure 11. The fabrication of all components as isolated silicon islands eliminates any possibility of latch-up. The diodes switch fast and quickly discharge any static charge that may appear at the digital MOS input gates. Tests have shown that the digital inputs can typically withstand repeated discharges at the 2,000 volt level.

The DI technology enables a wide variety of active elements to be integrated on the same chip to provide maximum versatility. For example, in the transistor-transistor-logic/CMOS reference circuit shown in Figure 12, the bipolar technology enables realization of a simple zener reference circuit, consisting of resistor R_2 and transistors Q_1, Q_2, and Q_3.

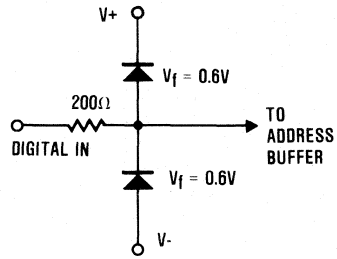


FIGURE 11. DIGITAL PROTECTION.

DI devices also protect digital inputs. For example, the diodes in this circuit quickly discharge any static charge that may appear on an MOS input gate.

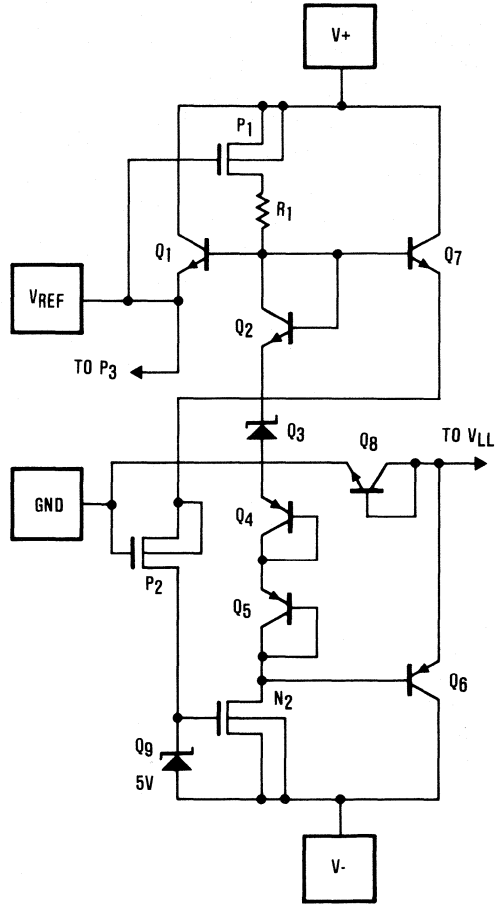


FIGURE 12. PACKING IT IN.

DI technology increases chip density of analog switch, allowing more circuit capability per package. For example, DI designs make possible this internal logic reference circuit in HI-200 and HI-201 switches.

The circuit develops a stable 5V reference for interfacing with TTL and eliminates the need for an additional 5V logic supply. Current for the zener (Q_3) is supplied through the normally on MOSFET, P_1, which can be easily turned off if not needed to minimize power consumption when interfacing with CMOS-logic circuits. P_1 turns off when V+ or supply voltage V_{DD} is applied to the reference terminal V_{REF} to convert the ICs power consumption from bipolar to CMOS level. If power is not critical, V_{REF} can be left open to speed switching.

In high-speed data acquisition systems, the designer is concerned with both quiescent power and dynamic power consumption. If JI devices are used, the capacitance or leakage currents are so high they contribute a major portion of total power consumption. That situation is caused by the large-geometry parasitic junctions formed by the n- junction.

In contrast, the smaller substrate area of the DI device provides much less power drain. Dynamic-power consumption as a function of frequency for several 16-channel analog multiplexers ±15V supplies is shown in Figure 13. The DI device consumes only 100mW at 1MHz to yield the best speed-power product.

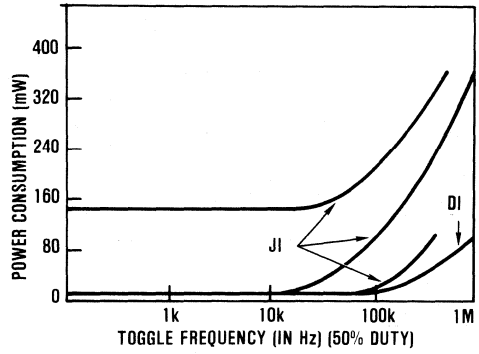


FIGURE 13. DI PERFORMS.

DI devices not only perform well, but do it with less power. Dynamic-power consumption data for commercial multiplexers shows DI device consuming only 100mW at 1MHz.

DIGITAL TO ANALOG CONVERTER TERMINOLOGY

By Dick Ti Tung

Introduction

In recent years the development and rapid reduction in cost of digital integrated circuits have resulted in an explosion in the applications of digital processing systems in the area of data acquisition and automatic process control. The need for a building block, such as the digital-to-analog converter (DAC), which interfaces the digital system with the analog world, is evident.

The purpose of digital-to-analog conversion is to produce a unique but consistent analog quantity, voltage or current, for a given digital input code. The most commonly used input digital code to a DAC is the natural binary number. A natural binary number is represented as

$$N = A_n2^n + A_{n-1}2^{n-1} + \ldots + A_12^1 + A_02^0 + A_{-1}2^{-1} + \ldots + A_{-n}2^{-n}$$

where the coefficients A_i (for $n \geqslant i \geqslant -n$) assume the values of "0" or "1" and is called a "bit". The left half portion of the binary number N

$$A_n2^n + A_{n-1}2^{n-1} + \ldots + A_12^1 + A_02^0$$

constitutes the integer part of the number N, whereas the right portion

$$A_{-1}2^{-1} + A_{-2}2^{-2} + \ldots + A_{-n}2^{-n}$$

constitutes the fractional part of the number N. The bit that carries the greatest weight (left most bit) is called the most significant bit, or MSB. Similarly, the bit with the smallest weight (right most bit) is called the least significant bit, or LSB.

The analog output of a n-bit binary DAC is related to its binary number in the following manner:

$$E_o = FS(A_{-1}2^{-1} + A_{-2}2^{-2} + \ldots + A_{-n}2^{-n})$$

where the term FS is defined as the nominal Full-Scale output of the DAC and it is known as the unreachable Full-Scale. It is easy to see that the actual Full-Scale output of the DAC, E_{FS}, with all the input bits "1" is

$$E_{FS} = FS(2^{-1} + 2^{-2} + \ldots + 2^{-n}) = FS(1-2^{-n}).$$

The term $FS(1/2^n)$ is the smallest output level that the DAC can resolve and it is known as the 1 LSB output level change. It is universal practice that the input code of a DAC is written in the form of binary integer with the fractional nature of the corresponding number understood.

As an example, the transfer function of an ideal 3-bit binary DAC is plotted as shown in Figure 1. Since a 3-bit DAC has only 8 discrete input codes which correspond to 8 different output levels (ranging from zero to 7/8 FS), no other output levels can exist and it is plotted as a bar graph. The line that connects the Zero and FS is called the Gain Curve.

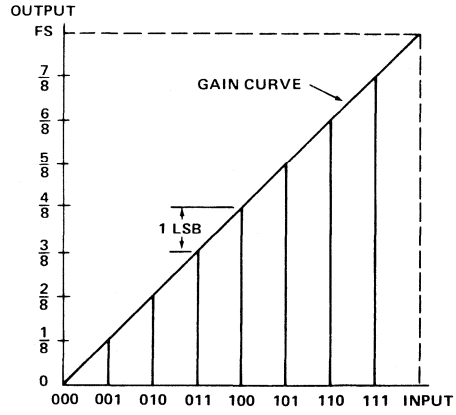


Figure 1 – Ideal Transfer Function Straight Binary (Unipolar)

There are two other input codings associated with binary DACs known as Bipolar codes, which are offset binary and two's complement binary codes. The offset binary code is obtained by offsetting the binary code such that the half-scale code, 10 . . . 0, becomes zero. And the two's complement code is achieved by inverting the MSB of the offset binary

code such that it is mathematically consistent with computer arithmetic. The transfer functions for the 3-bit DAC with offset binary input code and two's complement input code are plotted as shown in Figure 2 and Figure 3, respectively. (The +FS and -FS limits are used for easy interpretation of Bipolar operations. They are not confined by the previous definition of FS.)

In practical DACs, the zero output level may not be exactly zero (offset error), the range from zero to FS may not be exactly as specified (gain error), the differences in output levels may not be changing uniformly (nonlinearity), and so on. In selecting a DAC for a given application, some characteristics may have to be weighted more than the others. An understanding of some of the terms and characteristics involved in D/A conversion is helpful in choosing the correct part.

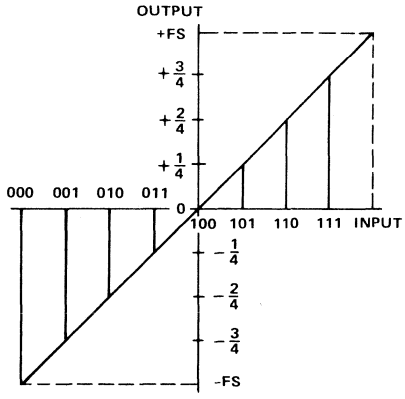


Figure 2 – Ideal Transfer Function Offset Binary (Bipolar)

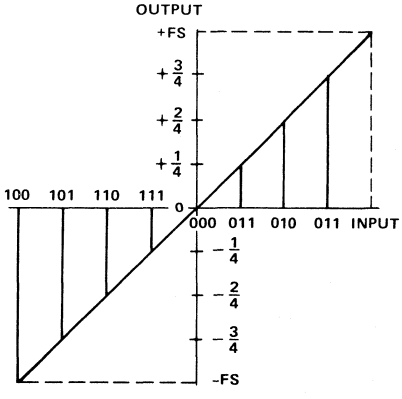


Figure 3 – Ideal Transfer Function Two's Complement (Bipolar)

Least Significant Bit (LSB) – The digital input bit carrying the lowest numerical weight ($1/2^n$); or the analog output level shift associated with this bit ($FSR/2^n$) which is the smallest possible analog output step.

Most Significant Bit (MSB) – The digital input bit carrying the highest numerical weight (1/2); or the analog output level shift associated with this bit. In a binary DAC the MSB creates a 1/2 FSR output level shift.

Resolution – An indication of the number of possible analog output levels a DAC will produce. Usually, it is expressed as the number of input bits. For example, a 12-bit binary DAC will have $2^{12} = 4096$ possible output levels (including zero) and it has a resolution of 12 bits.

Absolute Accuracy – A measure of the deviation of the analog output level from the ideal value under any input combination. Accuracy can be expressed as a percentage of full scale range, a number of bits (n bits accuracy means a magnitude of $1/2^n$ FSR possible error may exist), or a fraction of the LSB (if a DAC with n-bit resolution has 1/2 LSB accuracy the magnitude of the possible error is $1/2(1/2^n FSR)$). Accuracy may be of the same, higher, or lower order of magnitude as the resolution. Possible error in individual bit weight may be cumulative with combination of bits and may change due to temperature variations. Usually, the accuracy of a DAC is expressed in terms of nonlinearity, differential nonlinearity, and zero and gain drift due to temperature variations.

Nonlinearity (linearity error) – A measure of the deviation of the analog output level from an ideal straight line transfer curve drawn between zero and full scale (commonly referred as endpoint linearity).

Differential Nonlinearity – A measure of the deviation between the actual output level change from the ideal (1 LSB) output level change for a one bit change in input code. A differential nonlinearity of ± 1 LSB or less guarantees monotonicity; that is the output always increases for an increasing input.

Gain Drift – A measure of the change in full scale analog output, with all bits 1's, over the specified temperature range expressed in parts per million of full scale range per °C (PPM of FSR/°C). It is measured with respect to +25°C at high (T_H) and low (T_L) temperature, and it is specified the larger of the two representing worst case drift.

Offset Drift (Unipolar or Bipolar) – A measure of the change in analog output, with all bits 0's, over the specified temperature range expressed in parts per million of full scale range per °C (PPM of FSR/°C). It is measured with respect to +25°C at high (T_H) and low (T_L) temperature, and it is specified the larger of the two representing worst case drift.

Settling Time – The total time measured from a digital input change to the time the analog output reaches its new value within a specified error band. Usually, the settling time is specified for a DAC to settle for a Full-Scale code change (00 . . . 0 to 11 . . . 1 or 11 . . . 1 to 00 . . .0) to within $^{+}1/2$ LSB of its final value.

Compliance – Compliance voltage is the maximum output voltage range that can be tolerated and still maintain the specified accuracy.

The effects of gain error, offset error, nonlinearity, and differential nonlinearity on the transfer functions are plotted, respectively, as shown in Figure 4, 5, 6, & 7. A conversion chart which shows the number of bits and its resolution is given in Table 1.

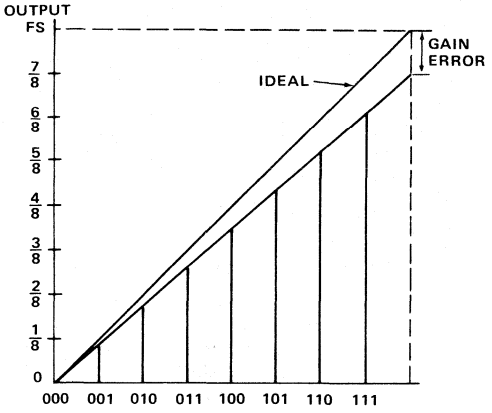


Figure 4 – Gain Error

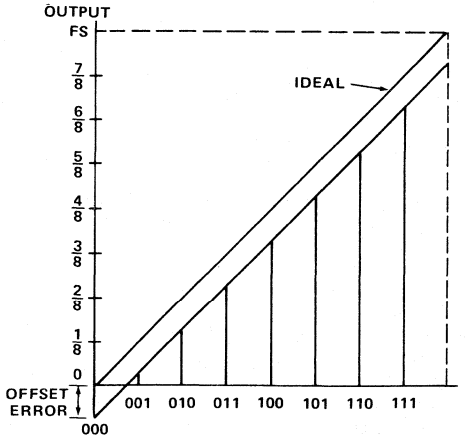


Figure 5 – Offset Error

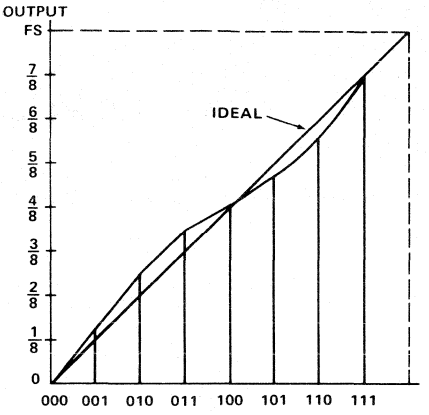


Figure 6 – Linearity Error

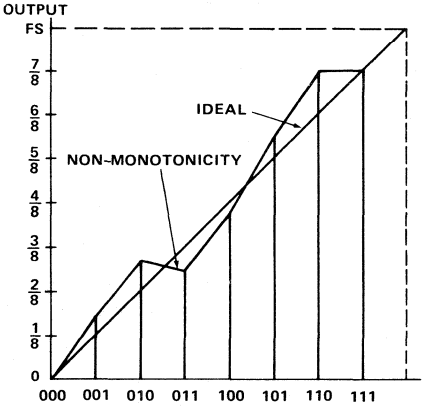


Figure 7 – Differential Linearity Error (Non-Monotonicity)

Table 1 – Conversion Chart

# OF BITS	LSB	RESOLUTION		TEMPCO PPM/°C – 1 LSB DRIFT OVER	
		%	PPM	0°C ≤ TA ≤ 75°C	-55°C ≤ TA ≤ 125°C
6	$FS/64$	1.5620	15,625	208.3	86.8
7	$FS/128$	0.7812	7.812	104.2	43.4
8	$FS/256$	0.3906	3,906	52.1	21.7
9	$FS/512$	0.1953	1,953	26.0	10.9
10	$FS/1024$	0.0977	977	13.0	5.4
11	$FS/2048$	0.0488	488	6.5	2.7
12	$FS/4096$	0.0244	244	3.3	1.4
13	$FS/8192$	0.0122	122	1.6	0.68
14	$FS/16384$	0.00610	61	0.8	0.34
15	$FS/32768$	0.00305	31	0.4	0.17
16	$FS/65536$	0.00153	15	0.2	0.08

APP NOTE

FOR YOUR INFORMATION

No. 524

Harris Analog

DIGITAL TO ANALOG CONVERTER HIGH SPEED ADC APPLICATIONS

By Dick Ti Tung and Tom Westenburg

Analog-To-Digital Converter (ADC)

The uses of high speed DACs in CRT display, industrial process control, signal regeneration, etc., are well established. Perhaps one of the most important applications is to use the DAC in high speed ADC design. There are two types of ADC design where high speed and high resolution DACs are essential.

TRACKING ADC OR SERVO TYPE ADC

The tracking ADC is very efficient in monitoring one analog signal continuously, converting it into a sequence of digital codes representing the analog signal in real time.

Functionally, the analog input is compared with the output of a DAC, with the digital input of the DAC being driven by a counter. After the ADC is turned on, the counter increments until the DAC output crosses the analog input value. The counter will then, running up or down, drive the DAC 1 LSB at a time to track the input signal. The counter state represents the digital equivalent of the input signal.

In Figure 1, the analog input is fed into the span resistor of a DAC. The analog input voltage range is selectable in the same way as the output voltage range of the DAC. The net current flow through the ladder termination resistance, i.e. 2kΩ for HI-562A, produces an error voltage at the DAC output. This error voltage is compared with 1/2 LSB by a comparator. When the error voltage is within ± 1/2 LSB range, the Q output of the comparators are both low, which stops the counter and gives a data ready signal to indicate that the digital output is correct. If the error exceeds the ± 1/2 LSB range, the counter is enabled and driven in an up or down direction depending on the polarity of the error voltage.

Since the digital output changes state only when there is a significant change in the analog input, the data ready signal is then very useful in adaptive systems or computer systems for efficient data transfer. When monitoring a slowly varying input, it is necessary to read the digital output only after a change has taken place. The data ready signal could be used to trigger a flip-flop to indicate the condition and reset it after read-out.

The main disadvantage of the tracking ADC is that the time required to initially acquire a signal, for a 12 bit ADC, could be up to 4096 clock periods. The input signal usually must be filtered so that its rate of change does not exceed the tracking range of the ADC (1 LSB per clock period).

SUCCESSIVE-APPROXIMATION ADC

Perhaps the most widely used technique for a high speed analog-to-digital converter design is the successive approximation method. Ideal for interfacing with computers, this type is capable of both high speed and high resolution, and the conversion time is fixed and independent of the magnitude of the input voltage.

Figure 2 shows a block diagram of a successive-approximation ADC. When a negative going start conversion pulse is applied to the ADC, the internal registers of the successive approximation register (SAR) are set to low except for the MSB, which is set to high. This turns on the MSB of the DAC. The FS output current of the DAC is compared with the current fed through the span resistor by the analog input. The net current flow through the ladder termination resistance produces an error voltage at the DAC output. This error voltage is then compared with a fixed reference by a comparator to determine whether the analog input is greater or less than the present state of the DAC. The result of the comparison is clocked into the SAR at the rising edge of the clock. The MSB of the SAR will be set to high if the analog input is greater; otherwise, it will be set to low. At the same time, the second bit of the SAR is set to high with the remaining bits at their previous states. During the second clock period, the sum of the result of the first choice and the weight of the second bit is compared with the analog input. The second bit is set to high or low in the same manner as the MSB, and so on, until the LSB is updated.

During this conversion time, the output of a status flip-flop is set to high, indicating that a conversion is taking place. It will return to low at the end of conversion to signify that the output state of the SAR represents the digital equivalent of the input analog voltage.

It is easy to see that in any successive-approximation ADC application, the analog input should remain reasonably constant during the conversion to avoid erroneous results. This is usually accomplished by using a sample-and-hold circuit in the analog line.

However with the new digital error correction circuitry incorporated in the HI-774A the input can vary. During the first portion of the conversion the input can move up to +0.78%/-0.76% of FSR and remain 12-bits accurate. This error correction window allows the user to start a conversion before the input has completely settled.

Data Acquisition System

The typical data acquisition system is depicted in Figure 3. The HI-506 multiplexer is used as an analog input selector. Which is controlled by a binary counter to address the appropriate channel. The HA-5330 is a high speed sample and hold. Sample Hold Control is tied to the status (STS) output of the HI-774A, so that whenever a conversion is in process the S/H is in the hold mode. A conversion is initiated by the clock input going low, and when the clock goes high the mux address changes. The mux will be acquiring the next channel while the ADC is converting the present input, held by the S/H. The clock low time should be between 225ns and 6.5μs, with the period greater than 8.5μs. With this timing R/C will be high at the end of a conversion so the output data will be valid $\sim$100ns before STS goes low. This allows STS to clock the data into the storage register. The register address will be offset by one, if this is a problem then a 4-bit latch can be added to the input of the storage register. With a 100KHz clock rate each channel will be read every 160μs.

This 16-channel data acquisition system is applicable to industrial process control, and multi-channel panel display. It can also interface with an intelligent terminal, such as a micro-computer system, to provide multi-channel data conversion function. The offset error and gain error of the data acquisition system over the operating temperature range can be easily compensated by proper programming.

By the same token, a 15-channel data acquisition system with offset correction could be easily incorporated as shown in Figure 4. Consider the case that one of the analog input channels is dedicated to sense the ground level, and its binary equivalent is stored in latch register B in its complementary form to establish a ground reference in real time. All the other analog input channels will then be converted and stored in register A, one at a time. The binary adder will perform the binary subtraction in less than 1μs for the given pair of A and B. This, in fact, eliminates the offset error of the ADC, offset error of the S/H circuit, and excess droop of the S/H due to temperature variation.

This circuit is easy to implement and is especially useful when an intelligent terminal is not available. To expand this concept one step further, the gain error of the system due to temperature variations could also be eliminated if a binary multiplier is used to correct the gain facter in real time.

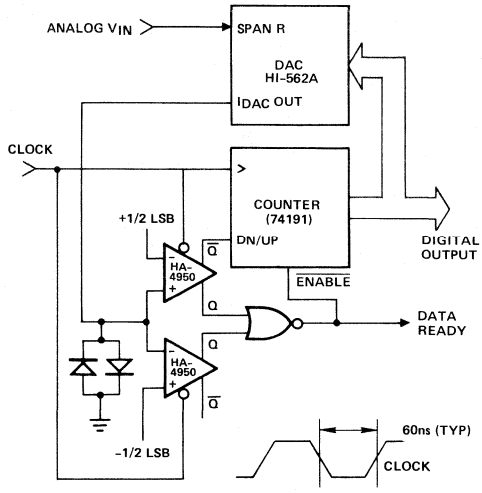


Figure 1. Tracking ADC

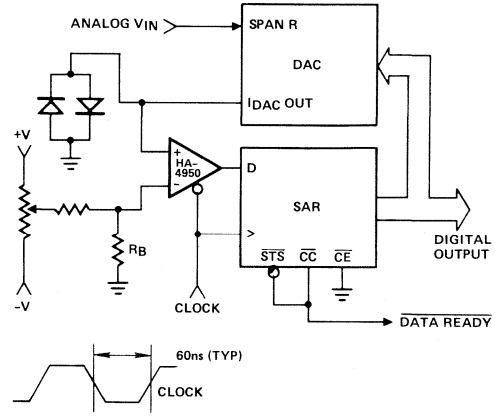


Figure 2. Successive-Approximation ADC

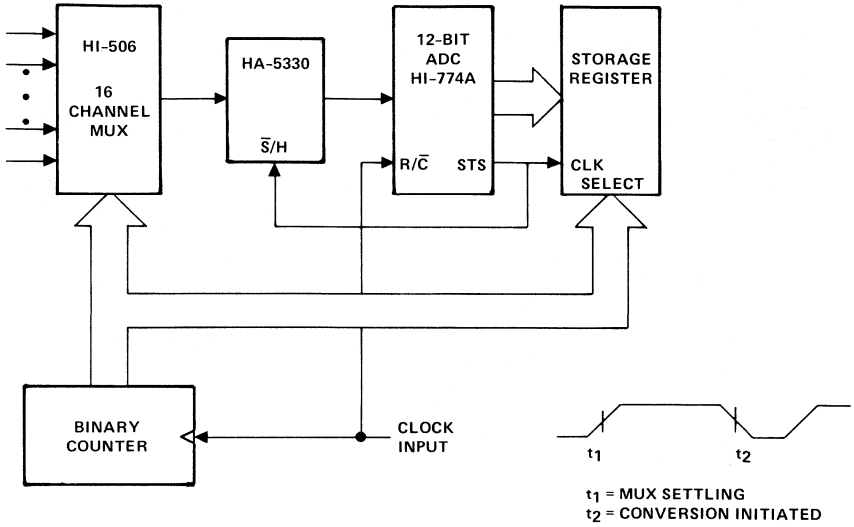


Figure 3. 16 Channel Data Acquisition System

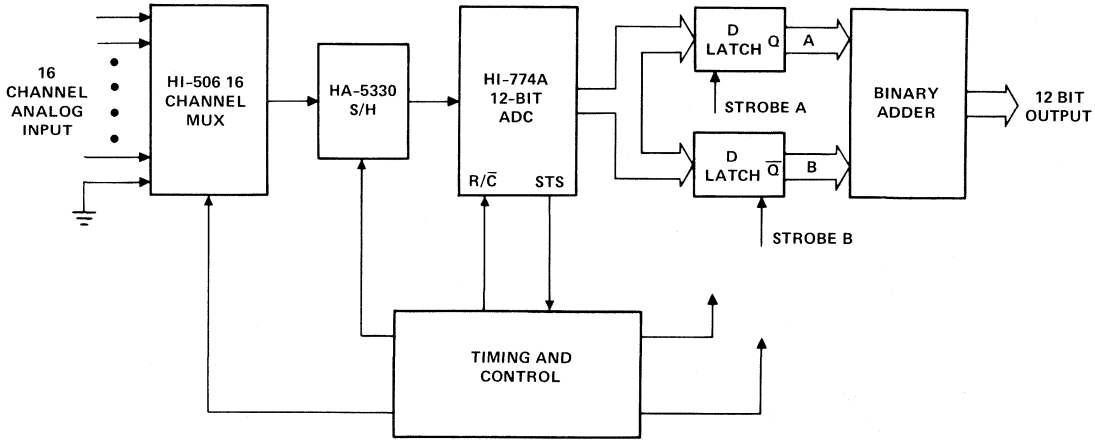


Figure 4. 15 Channel Data Acquisition System with Offset Correction

HA-5190/5195 FAST SETTLING OPERATIONAL AMPLIFIER

By G. Cotreau, D. Jones, R. Whitehead

Introduction

The military temperature range HA-5190 and its commercial temperature equivalent, HA-5195, are monolithic operational amplifiers featuring ±200V/μs slew rate, 150MHz gain-bandwidth-product, and 70ns settling time. Similar performance has previously been available only in more costly modular and hybrid amplifiers, which require much higher bandwidth and slew rate to achieve the same settling time as HA-5190/5195. Since it exhibits a classical -6dB/octave rolloff over most of its frequency range, remarkably smooth output wave forms are generated by HA-5190 when reasonable care is employed.

Applications for this op amp include pulse, RF, and video amplifiers, wave form generators, high speed data acquisition and instrumentation circuits.

Inside the HA-5190/5195

Figure 1 shows the schematic of the HA-5190/5195 design. The schematic can be simplified to show the AC signal path as shown in Figure 2.

The input stage consists of two symmetrical differential transistor pairs. The signal path for positive going signals is Q_1, Q_2, and Q_3, while negative going signals pass through Q_4, Q_5, and Q_6. The signal then goes through the output stage (represented by the voltage follower symbol) consisting of one PNP and two NPN emitter followers.

In Figure 2, the compensation network is C_1, C_2, C_3, and R_{29}. This network makes the amplifier system appear as second-order critically damped. The scheme produces the dominant pole plus two zeros. The zeros are positioned to cancel the effects of undesired poles developed by the F_t of the transistors.

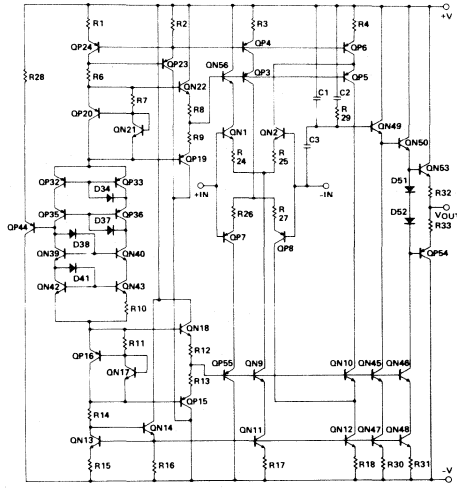


Figure 1. HA-5190/5195 Schematic.

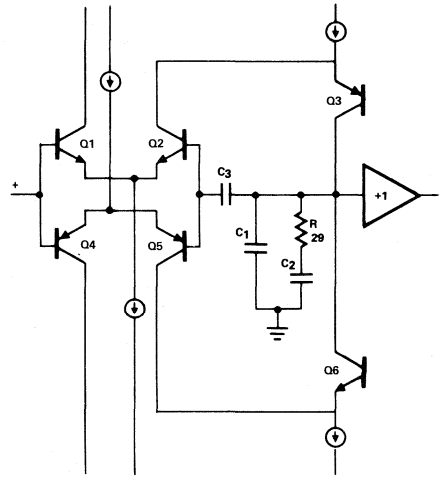


Figure 2. Simplified HA-5190 Schematic.

Considerations For Prototyping

When using the HA-5190, high frequency layout techniques are recommened for bread-boarding. The device should be mounted through a ground plan and all No Connect (NC) Pins should be tied to this plane for pin isolation. If an IC socket is to be used, Teflon types are recommended. Feedback components should be mounted between Teflon insulated standoffs located as close as possible to the device pins.

The input impedance characteristic of the HA-5190 is such that the closed loop performance (DC and AC) will depend on both the feedback component ratio and the actual impedance presented to each amplifier input. For best high frequency performance, resistor values for feedback networks should be limited to a maximum of 5K ohms (preferably less than 1K ohm). Film type resistors are recommended. Power supply decoupling with ceramic capacitors from the device supply pins to ground is essential.

It is recommended that optimum circuit values for a particular application be developed through experimentation using amplifiers from several production runs. The PC artwork in the vicinity of the HA-5190 should be prototyped early to determine any sensitivites to layout.

OPERATION AT ELEVATED TEMPERATURES

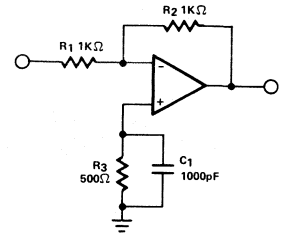
HA-5190/5195 may be used without a heat sink up to +75°C, ambient. Above this temperature, the power derating is 9.6mW/°C for the 14 Lead Ceramic DIP. THERMALLOY Model 6007 or AAVID Model 5602B are recommended. For the 12 Lead To-8 Metal Can, derate at 11.5mW/°C and recommended heat sinks are THERMALLOY Model's 2240A or 2268B.

FREQUENCY COMPENSATION

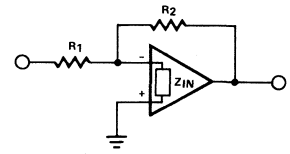
HA-5190/5195 is stable in standard DC amplifier configurations with closed loop gains exceeding +5 or -4. At these or higher gains, optimum AC performance can be achieved by keeping network resistor values as low as is practical.

Quite simple circuitry, as illustrated in Figure 3, gives excellent performance for lower closed loop gains. The compensation schemes use the amplifier's differential input impedance to reduce both the input and feedback signals thereby raising the effective noise gain approximately 14dB to a stable point on the frequency response curve.

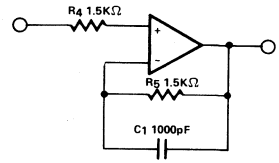
Inverting and non-inverting unity gain connections for HA-5190 are shown in Figure 3 (a) and (c). R_3 and R_5 serve only to balance DC voltage offsets due to input bias current, and may be replaced with a short for AC applications. C_1 is not neccessary for stability, but helps reduce overshoot and smooth the frequency response. Settling time or frequency response can be optimized (about 30MHz small signal bandwidth is practical) by fine tuning component values.



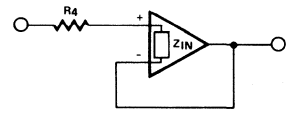
(a) Gain = -1



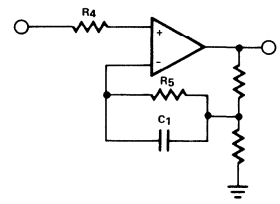
(b) Stabilization using Z_{IN}.



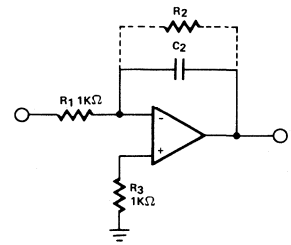
(c) Gain = +1



(d) Stabilization using Z_{IN}.



(e) Non-inverting gain stage.



(f) Integrator

Figure 3. Compensation recommended when $1 + \frac{R_2}{R_1} < 5$.

For closed loop gains between 1 and 5, reducing R_1 in Figure 3 (a) and (e) will raise the gain with minimum effect on bandwidth. However, in the inverting configuration, R_1 determines the input impedance, and it may be more practical to raise R_2 at the expense of bandwidth. In Figure 3 (e), R_4 and R_5 may be reduced as gain is increased and removed entirely at gains greater than +4.

For applications requiring 100% feedback at high frequencies, such as integrators and low pass filters, HA-5190/5195's compensation scheme should be thoroughly evaluated through experimentation. The circuit in Figure 3 (f) is quite stable, using the two 1K ohm resistors.

Suggested Methods For Performance Enhancement

To avoid compromising AC performance, the HA-5190 design does not include provisions for internal offset adjustment.

The circuits in Figure 4 (a) and (b) show two possible schemes for offset voltage adjustment.

Figure 5 (a) and (b) uses the inherent qualities of the FET to reduce input bias currents by several orders of magnitude and raise input impedance to thousands of megohms. Both circuits are shown in the unity gain follower mode. Circuit gain can be implemented using normal feedback techniques. To optimize for speed, care should be taken in layout. Experimental results yielded slew rates of approximately 130V/μs.

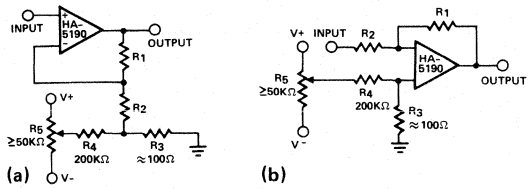
Figure 5 (c) illustrates a composite inverting amplifier which greatly reduces DC errors due to the HA-5190 input bias current and gain, while retaining superior settling time. The 0 dB frequency of the integrator section approximates the open loop low frequency pole (~2.5kHz) of the HA-5190. This circuit might also be connected as a current-to-voltage amplifier for use with a high accuracy, high speed DAC.

Figure 6 shows a composite amplifier scheme for boosting output current drive of the HA-5190/5195. The circuit gain (shown A_V = 5) can be adjusted using normal feedback systems. HA-5190 used in conjunction with HA-5033 can drive 50 ohm coaxial cable, with proper termination to 250MHz.

Applications

INTRODUCTION

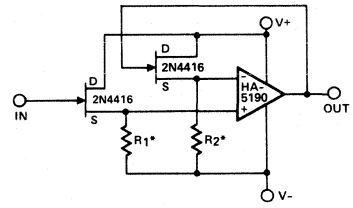
HA-5190/5195 represents an ideal building block for high speed, precision data acquisition systems and for video pulse amplification. Although this amplifier can be used in a wide variety of other applications, the ones to be discussed show where it can be used most advantageously.



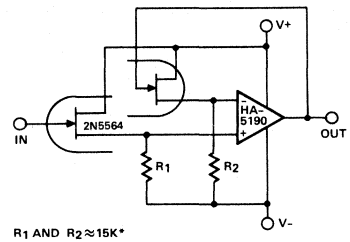
RANGE OF ADJUSTMENT FOR BOTH NON-INVERTING (LEFT) AND INVERTING AMPLIFIERS (RIGHT) DETERMINED BY PRODUCT OF V_{SUPPLY} AND R_3/R_4 RATIO.

$$A_V = 1 + \frac{R_1}{R_2 + R_3}$$

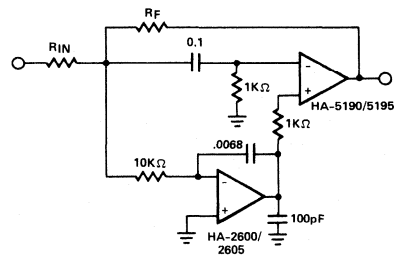
Figure 4. Offset Nulling.



(a) * VALUES SHOULD BE DETERMINED EXPERIMENTALLY FOR OPTIMIZED PERFORMANCE.



(b) R_1 AND $R_2 \approx 15K^*$
INPUT FETS ARE MATCHED PAIR 2N5564



(c)

Figure 5. Reducing Input Bias Currents.

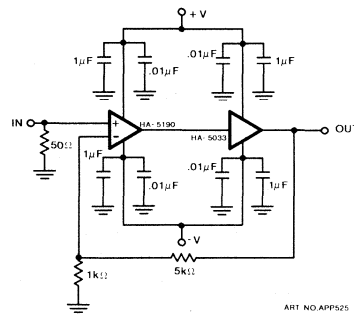


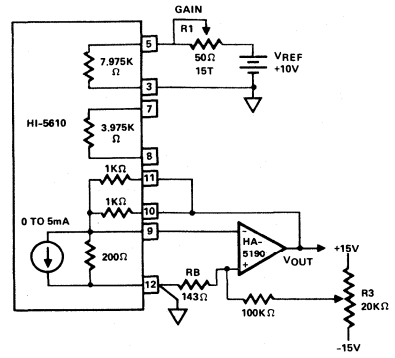
Figure 6. Boosting Output Current.

Application 1 Fast DAC Output Buffer

The circuit at right illustrates the HA-5190's usefulness as a high speed DAC buffer.

The amplifier operates as a current-to-voltage converter/output buffer to the HI-5610 which is a precision 10 bit DAC with output current settling time less than 100ns. The voltage divider on the non-inverting input serves to null any DC errors introduced into the system. The amplifier maximizes speed of the system since its dynamic performance exceeds that of the DAC.

Application 1



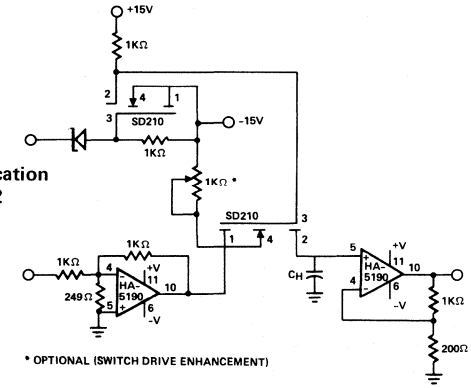
Application 2 High Speed Sample/Hold

Sample/Hold circuits are used in many areas of data acquisition systems such as de-glitchers for D/A converters and input stages for successive approximation A/D converters.

The circuit at right uses the speed and drive capability of the HA-5190 coupled with two high speed DMOS FET switches.

The input amplifier is allowed to operate at a gain of -5 although the overall circuit gain is unity. Acquisition times of less than 100ns to 0.1% of a 1 volt input step are possible. Drift current can be appreciably reduced by using FET input buffers on the output stage of the Sample/Hold.

Application 2

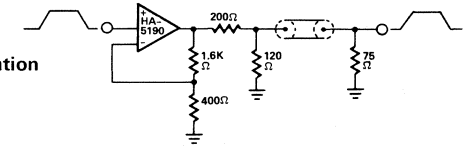


Application 3 Video Pulse Amplifier/75 ohm Coaxial Driver

HA-5190/5195 is also well suited for video pulse applications. The circuit at right could be found in various types of video broadcasting equipment where 75 ohm systems are commonly employed.

HA-5190 can drive the 75 ohm coaxial cable with signals up to 2.5 volts peak-to-peak without the need for current boosting. In this circuit the overall gain of the circuit is approximately unity because of the impedance matching network.

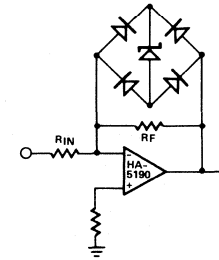
Application 3



Application 4 Output Limiter

HA-5190 is rated for ± 5 volt output swing, and saturates at ± 7 volts. As with most op amps, recovery from output saturation is slow compared to the amplifier's normal response time; so some form of limiting, either of the input signal or in the feedback path, is desirable if saturation might occur. The circuit above illustrates a feedback limiter, where gain is reduced if the output exceeds ± (Vz + 2Vf). A 5 volt zener with a sharp knee characteristic is recommended.

Application 4



VIDEO APPLICATIONS HA-5190/5195

By L. E. Garner

Introduction

Offering superior performance in video and RF circuits, the HA-5190/5195 family can be used effectively in the design of television broadcast studio equipment, test instruments, and monitoring or surveillance TV systems. A very high 200V/μs slew rate, a full power bandwidth of 6.5MHz, and a fast settling time of only 70ns (typ) are but three of the unique characteristics which make these devices ideal for critical wideband video and RF applications. Other features include true differential operation, excellent stability with gains ≥ 5, and complete freedom from latch up, the latter a result of the exclusive HARRIS dielectric isolation process combined with optimized chip design and layout.

The op amp family can be used, typically, as studio tape head, test instrument, and video camera preamplifiers, as buffers, as broadcast relay link repeaters, as coaxial line drivers, and as cable or industrial system video repeater and bridging amplifiers. Extremely versatile, the devices can be operated effectively in AGC and dc gain controlled configurations as well as in fixed gain designs, and are fully capable of driving low impedance loads.

When used in standard video amplifier configurations, the HA-5190/5195 devices easily meet or exceed the performance tolerance specifications of applicable current FCC (NTSC) composite TV signal standards as well as the requirements of EIA Tentative Standard RS-170A.

Video Performance

The overall color video performance of the HA 5190/5195 family was confirmed by checking a number of standard devices. Tests were made to determine both video response and signal/noise ratio under typical operating conditions. The basic video amplifier circuit illustrated in Figure 1 was used for the tests, with the actual procedures abstracted from those described in EIA Standard RS-250-B. The general test setup is shown in Figure 2.

VIDEO RESPONSE TESTS

Referring to Figure 1, the test video amplifier comprised an HA5190/5195 op amp, BNC coaxial input jack J1, input level control R1 shunted by impedance matching resistor R2, input series stabilization resistor R3, gain control network R4-Rgain, series output limiting resistor Rs, and BNC coaxial output jack J2. Operational power was supplied by a well regulated and filtered dual line operated power supply.

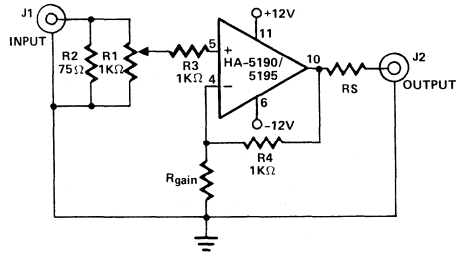


Figure 1–Test Video Amplifier

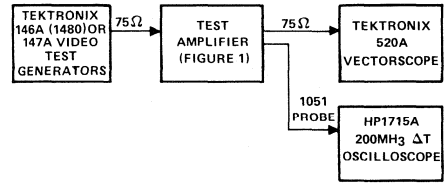


Figure 2–Video Response Test Setup

Initially, standard NTSC and EIA ramp and timing test signals were applied using the Tektronix Models 146A (1480) and 147A video test generators. Amplifier performance was observed and measured at various levels with a Tektronix 520A Vectorscope and HP Model 1715A 200MHz delta time Oscilloscope. Three of the RS-250-B specified test waveforms used are illustrated in Figure 3, including the (a) ramp linearity, (b) 12.5T and 2T sine-squared pulse and bar, and (c) multiburst signals. With the test signal level maintained at 1.0V p-p, level control R1 was adjusted as needed to establish a 1.0V p-p output signal (at J2) for each gain value. The Vectorscope was used to measure color differential phase and gain, with the Oscilloscope used to check for distortion of the 2T, 12.5T, multiburst and color bar signals. The average test results are summarized in Table A. All measured values were well within applicable specifications.

Table A - Summary of Test Results

NOMINAL GAIN	R_{gain}	R_s	DIFF ϕ	DIFF GAIN	2T	12.5T	MULTI	COLOR BARS
1	∞	0	-0.2°	-0.5%	UNM*	UNM*	FLAT	UNM*
2	1k	75Ω	-0.15°	≈0	UNM*	UNM*	FLAT	UNM*
5	251Ω	200Ω	-0.2°	≈0	UNM*	UNM*	FLAT	UNM*
10	110Ω	200Ω	-0.4°	-0.5%	UNM*	UNM*	FLAT	UNM*

*UNM : UNMEASURABLE DISTORTION

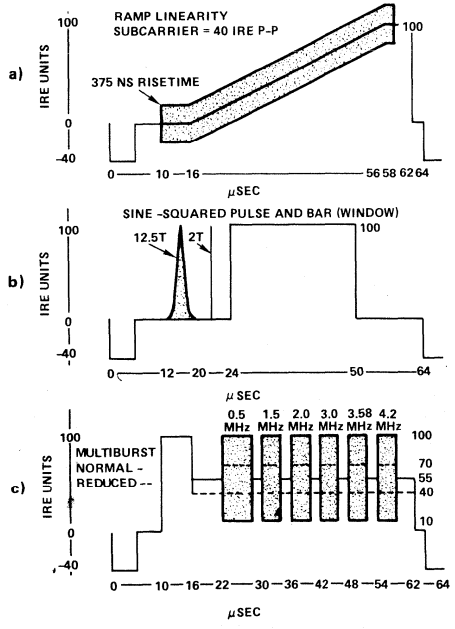


Figure 3—Video Test Signal Waveforms

S/N RATIO

Signal/noise (S/N) ratio measurements were made using the same basic amplifier configuration, but with Rgain fixed at 251Ω, ±1%, and Rs at 200Ω ±5%. The dc power supply terminals were bypassed with a 100 μF tantalum capacitor. A Tektronix 147A NTSC Test Signal Generator was used as a signal source, with output measurements made using a Rhode & Schwartz Video Noise Meter, as diagrammed in Figure 4. The Tektronix 147A was set to deliver a flat field signal at 50 IRE units, with the R&S Video Noise Meter adjusted as follows: (a) 10kHz High pass, (b) Video Bandpass, (c) Subcarrier Trap OFF, (d) Internal Sync, (e) Tilt & Sag Comp OFF.

Under the specified conditions and with level control R1 adjusted to deliver a 1.0V p-p signal at J2, the measured p-p signal/RMS noise ratio averaged 68dB, or well over the minimum value required by applicable standards.

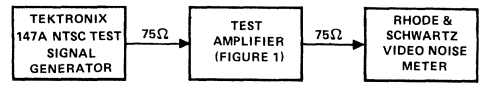


Figure 4—S/N Ratio Test Setup

General Considerations

Since the HA-5190/5195 devices do not require special treatment, optimum video performance can be achieved by observing standard high frequency design and wiring practices. However, the following suggestions, abstracted in part from HARRIS Application Note 525, should prove helpful when developing practical designs.

POWER SUPPLY REQUIREMENTS

A well-regulated, well-filtered dual dc power source is required for best operation, for the op amps draw moderate currents during normal operation. Although not essential in all applications, it is recommended that the power supply lines be decoupled using 0.01 μF ceramic capacitors to circuit ground, with the capacitors located as near to the amplifier terminals as possible to minimize lead inductances. For optimum performance and operation at specified parameters, the dc power supply should furnish not less than ±10V dc, with higher source voltages (±15V, typically) preferred.

TEMPERATURE CONSIDERATIONS

The HA-5190/5195 devices can be used without heat sinks at ambient temperatures up to 75°C. Under these conditions, the internally generated heat stabilizes device operation and ensures relative immunity

to external temperature variations. At ambients above 75°C, however, the 14 Lead Cerdip devices should be derated 9.6mW/°C, with a suitable heat sink, such as a THERMALLOY Model 6007, or AAVID Model 5602B. To provide adequate heat dissipation. For the 12 Lead To-8 Metal Can derate at 11.5mW/°C and recommended heat sinks are THERMALLOY's 2240 or 2268B. Application Note 556 also suggest safe operating area conditions.

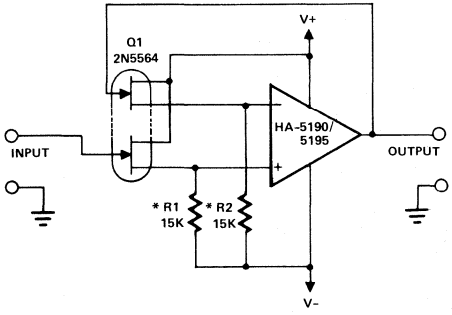
Under some conditions, the internally generated heat can affect other components. Therefore, avoid mounting temperature sensitive devices or components near or directly adjacent to the op amps.

DESIGN HINTS

Except for their exceptional performance specifications, the HA-5190/5195 devices are essentially standard op amps and may be treated as such by the video equipment or system designer. Thus, conventional design techniques may be used when developing specific circuit configurations, as long as maximum ratings are observed and adequate compensation is made for device operational characteristics. For example, the closed loop performance (dc and ac) at gains ≥ 5 depends on both the feedback component ratio and the actual impedance at each amplifier input. Since the devices offer a comparatively low input impedance, feedback network resistor values should be 5kΩ or less (preferably, less than 1kΩ) for optimum high frequency performance.

If the intended video application requires a high input impedance, a FETpreamp stage may be added ahead of the HA-5190/5195 op amp, as shown in Figure 5. Full details and an additional FET input circuit are provided in HARRIS Semiconductor Application Note 525.

Where used, a FET preamp not only raises the effective input impedance from (approximately) 10kΩ to thousands of megohms, but also reduces the input bias current requirement by several orders of magnitude. There is, of course, a trade-off in frequency response, with a FET input stage reducing the effective overall slew rate from 200V/μs to 130V/μs (typically). However, the full power bandwidth with a FET input is more than adequate for all low to mid level video applications.



*Approximate Values

Figure 5– FET Input Circuit

Some video applications may require output currents which exceed the maximum capabilities of the HA-5190/5195 devices. In these cases, the HA-5190/5195 op amps can be teamed with high performance current boosters such as, for example, the HA-5033. A typical cascaded op amp/booster circuit is illustrated in Figure 6. Since the current booster, a unity gain device, has a typical slew rate and bandwidth (Slew Rate = 1300V/μs FPBW = 65MHz) far grater than that of the op amp, the overall frequency performance of the composite amplifier is essentially that of the op amp alone.

To compensate for manufacturing tolerances and ensure optimum performance, the fixed component values used in specific designs should be finalized empirically, using active devices from several production runs.

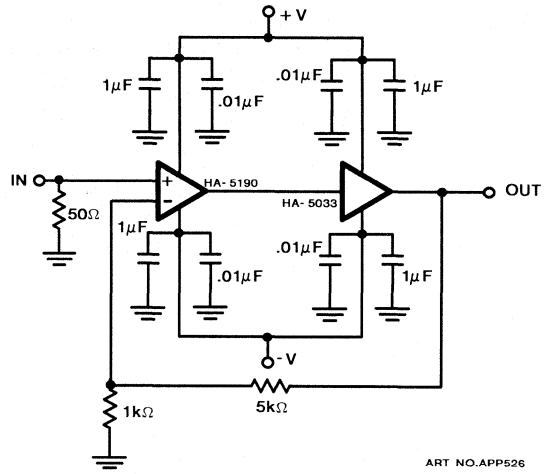


Figure 6–Boosting Output Current

PROTOTYPING TIPS

In accordance with standard engineering practice, new circuit designs should be breadboarded to verify overall operation. Afterwards, a number of preproduction prototypes identical to the planned production design should be assembled and tested using active devices from several production runs. These prototype tests permit optimization of component values and determination of circuit sensitivities to layout and component positioning. Preliminary environmental tests, if required, also may be made using the prototypes.

If IC sockets are used, Teflon types are preferred to minimize distributed capacitances. For the same reason, feedback components should be mounted between Teflon insulated standoffs located as close as practicable to the device pins or socket terminals. For maximum stability, film type resistors are recommended for the feedback networks.

Signal carrying leads should be kept short and direct, of course, to minimize both lead inductances and distributed capacitances. The devices should be mounted through a ground plane. If this is impracticable, single point grounding should be used to avoid ground loops.

Typical Applications

The test circuit given in Figure 1 may be used as a general purpose video amplifier, although minor changes in component values may be needed to optimize operation for specific requirements. Additional practical circuits are illustrated in Figures 7 and 8.

RF AGC AMPLIFIER

Designed and checked as a buffer for the head preamp of a studio video tape recorder, the circuit shown in Figure 7 functions as a wide band adjustable AGC amplifier. With an effective bandwidth of approximately 10 MHz, it is capable of handling RF input signal frequencies from 3.2 to 10MHz at levels ranging from 40mV up to 3V p-p.

AGC action is achieved by using opto coupler/isolator OCI as part of the gain control feedback loop. In operation, the positive peaks of the amplified output signal drive the OCI LED into a conducting state. Since the resistance of the OCI photosensitive element is inversely proportional to light intensity, the higher the signal level, the lower the feedback resistance to the op amp inverting input and hence the greater the negative feedback, thereby lowering stage gain. Any changes in gain occur smoothly because the inherent memory characteristic of the photoresistor acts to integrate the peak signal inputs. In practice, the stage gain is adjusted automatically to a point where the output signal positive peaks are approximately one diode drop above ground.

GAIN SET control R5 applies a fixed dc bias to the op amp non-inverting input, thus establishing the steady-state zero input signal current through the OCI LED and determining the signal level at which AGC action begins. In experimental tests under large signal conditions (i.e., E_{IN} = 3V p-p), a GAIN SET value of -0.26V provided unity gain, while a value of -1.55V yielded on A_V of 2.7 , with a flat response to 5.0MHz at both levels. Under small signal conditions (i.e., E_{IN} = 40mV), gains from 8 to 50 could be achieved as the GAIN SET value was adjusted from 0.65V to -80mV. At A_V = 8, the frequency response was flat to 5MHz, while at A_V = 80, the response was limited to that of the HA-5190/5195.

The effective AGC range depends on a number of factors, including individual device characteristics, the nature of the RF drive signal, the initial setting for R5, et al. Theoretically, however, the AGC range can be as high as 4000:1 for a perfect op amp, for the OCI photoresistor can vary in value from 1 Megohm with the LED dark to 250Ω with the LED full on.

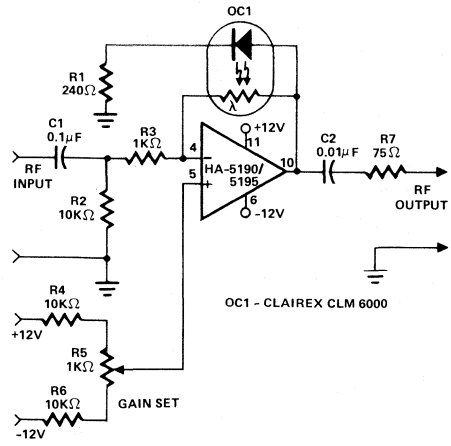


Figure 7–RF AGC Amplifier

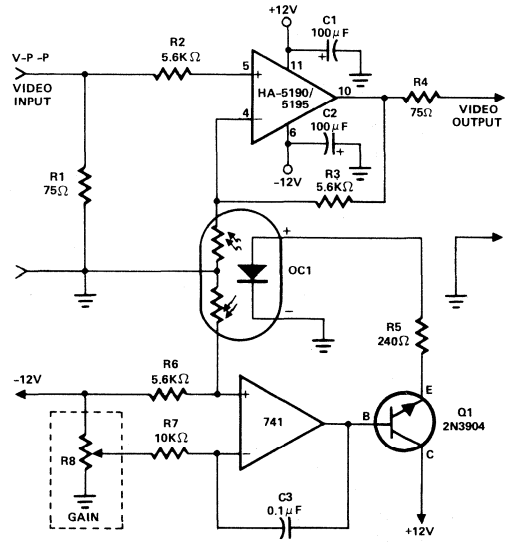


Figure 8–DC Gain Controlled Video Amplifier (Analog Multiplier)

DC GAIN CONTROLLED VIDEO AMPLIFIER

Suitable for use in virtually any application requiring a variable gain wideband or video amplifier, the circuit illustrated in Figure 8 employs a cascaded op amp integrator and transistor buffer (Q1) to drive the amplifier gain control element. Except for a simple modification, the HA-5190/5195 stage is connected as a conventional non-inverting operational amplifier, and includes input and output impedance matching resistors R1 and R4, respectively, series stabilization resistor R2, and power supply bypass capacitors C1 and C2. The circuit differs from standard designs in that the gain control network includes a photoresistor, part of OCI.

Referring to the schematic diagram, opto coupler/ isolator OCI contains two matched photoresistors, both activated by a common LED. The effective resistances offered by these devices is inversely proportional to the light emitted by the LED. The greater the current through the LED, then, the more intense its light emission, and the lower the effective values of the photoresistors. One photoresistor is part (with R3) of the HA-5190/5195 gain network, while the other forms a voltage-divider with R6 to control the bias applied to the integrator non-inverting terminal.

In operation, the dc voltage supplied by GAIN control R8 is applied to the integrator inverting input terminal through input resistor R7. Depending on the relative magnitude of the control voltage, the integrator output will either charge or discharge C3. This change in output, amplified by Q1, controls the current supplied to the OCI LED through series limiting resistor R5. This action continues until the voltage applied to the integrator non-inverting input by the R6-photoresistor voltage divider matches the control voltage applied by R8 to the inverting input. At the same time, of course, the ratio of the R3-photoresistor gain network is changing, adjusting the op amp stage gain. As the control (R8) voltage is readjusted, the OCI photo-resistances track these changes, automatically readjusting the op amp gain in accordances with the new control voltage setting.

In experimental tests with typical devices, the amplifier gain could be varied from 12dB to 2dB as the dc control voltage was changed from 5.0 to 10.5Volts. Typical plots of stage gain (A_V) versus control voltage (V) are shown in Figure 9.

Since all temperature sensitive components are inside the integrator feedback loop, the circuit is quite stable with respect to changes in the ambient temperature.

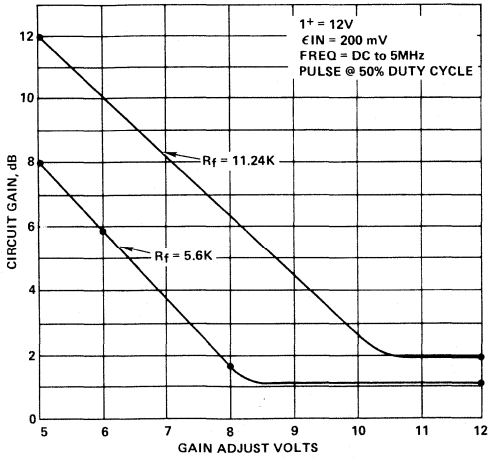


Figure 9 - Plot Of AGC Circuit Gain Versus Control Voltage

ACKNOWLEDGEMENTS

A. J. Carl Cooper of HARRIS CVS (Consolidated Video Systems), 1255 E. Arques Ave., Sunnyvale, CA. 94086, developed the basic circuits described herein and, in addition, devised and executed the initial evaluation and performance tests.

B. Richard Whitehead and Robert Junkins of HARRIS SEMICONDUCTOR, P.O. Box 883, Melbourne, Fla. 32901, carried out additional confirmation tests of circuit performance and made other significant contributions to this publication.

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1. HA-5190/5195 Wideband, Fast Settling Operational Amplifiers (Harris data brochure)

2. Application Note 525 - HA-5190/5195 Fast Settling Operational Amplifier. January 1988.

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APP NOTE

FOR YOUR INFORMATION

No. 531

Harris Analog

ANALOG SWITCH APPLICATIONS IN A/D DATA CONVERSION SYSTEMS

By Richard Whitehead

Introduction

A choice of three approaches is available when implementing a data conversion system: 1). "build-from-scratch", 2) buy sub-systems and configure a system, or 3) purchase a pre-engineered system which meets the requirements. Also, as a matter of economics, the users of sensor-based data acquisition systems make it common practice to ensure a maximum number of elements are shared in the system. An invaluable tool used in this process is the analog switch or multiplexer. The purpose of this article is to focus attention on those parts of the system which require analog switches and to emphasize the importance of relative operating parameters.

Basic System Configurations

A/D data conversion systems can be categorized into two general groups: 1) low level signal conversion (analog signals below 1 volt) and 2) high level signal conversion (analog signals above 1 volt). Within these categories, four basic data conversion configurations are illustrated to point out the advantages of using analog switches.

Conditioning the analog signals prior to multiplexing (Figure 1A) is the most popular system arrangement and is both efficient and capable of high performance This configuration, which shares the level signals. Figure 1B represents a more austere approach resulting in lower cost and decreased performance. This type is useful in less demanding applications such as processing high level signals. To process multichannel, single event information such as wind tunnel or seismographic measurements the arrangement shown in Figure 1C is most likely to be used. This configuration represents a more expensive, less efficient approach due to the decreased number of shared elements. Figure 1D shows the elimination of the analog multiplexer and sample and hold circuits. By moving the multiplexing task to the digital domain, slower and lower cost A/D converters can be used.

Types Of Analog Switches

The most commonly used types of analog switches found in today's data conversion systems are: reed relay, JFET, and CMOS. Reed relays offer low ON and high OFF resistance and are capable of handling very high voltages, but have slow speeds. JFET switches have lower OFF leakage current and are capable of very high speeds. CMOS switches, which are the most popular and widely used in multiplexer applications, have low OFF leakage currents, good speed, and stable ON resistance under varying input signal conditions.

Selecting The Proper CMOS Analog Switch

The data conversion system error budget should be used to narrow the field of CMOS analog switches suitable for the application. Primarily, the speed of the switch must be consistent with the systems's sample rate requirements without introducing unacceptable transfer error. Significant dynamic errors inherent to CMOS analog switches are OFF channel leakage current and a settling time value dictated by the device's ON resistance and its inherent capacitance. Figure 2 shows the equivalent of a CMOS analog switch giving all of the inherent and distributed properties which may become the source of unwanted system errors.

Other system restrictions may further narrow the field of candidates suitable to performing the switching task. These restrictions could include, low power budget, hostile environment, cost, alternate sourcing, and package density. It's possible that all of

these restrictions could occur, and this situation mat influence the user to seek a compromise solution to his problem.

Fortunately, CMOS analog switches consume very little power and only the most demanding power budget would feel the strain of their power requirements. If the poerating environment of the device includes high voltage spikes, excessive noise pickup, and/or power supply interruptions, the selection should be narrowed to the internally protected analog multiplexers such as the HARRIS HI-506A/507A or the HI-546/547. These multiplexers come with guaranteed overvoltage specifications which engance the reliability of the data conversion system. They also insure output signal integrity while an overvoltage condition occurs on an unselected channel. It should also be ensured that the CMOS analog switch selected does not exhibit any inherent latch-up tendencies. The Harris dielectrically isolated CMOS analog switches offer latch free operation.

To some users the proper CMOS analog switch selection may become complicated leading to possible alternate solutions. An example of such a situation could be in high speed data conversion system where the settling time constraint placed on the multiplexer results in an unacceptable time penalty (Figure 3A). Figure 3B shows an alternate and practical solution to this problem. The two tiered multiplexing scheme may reduce the errors caused by leakage currents and settling time by an order of magnitude. Another practical solution would be to select an analog signal processor such as the HARRIS HY-9590/9591 shown in Figures 4A and 4B. These devices facilitate user application and reduce engineering time thereby reducing overall cost.

Other Uses For CMOS Analog Switches

Attention has been focused on the selection of CMOS analog multiplexers used to increase efficiency of data conversion systems through shared elements. But the versatile CMOS switch is not limited to only that function. Obviously they can be used in sample and hold circuits, with important parameters being switching speed, OFF leakage current, and charge transfer. Analog switches such as the HARRIS HI-200/201 and HI-300 series may be used in sample and hold circuits and also in auto-zeroing circuits for integrating type data converters (Figure 5).

Figure 6 shows the CMOS analog switch used to program the gain of an instrumentation amplifier.

Highlights

In A/D data conversion systems analog switches are mainly used as multi-channel multiplexers to increase system efficiency through shared elements.

CMOS analog switches are the most widely used in data conversion systems.

When selecting the proper CMOS analog switch, look for low OFF leakage current, good settling time, latch free operation, and stable ON resistance under varying analog signal input conditions.

If the environment is hostile, select from the internally protected CMOS analog multiplexers.

Where an alternate solution is required, attempt to ensure your solution is the most practical with respect to your error budget.

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Kaufman, Milton and Seidman, Arthur H. Handbook of Electronic Calculations. New York: McGraw-Hill Book Company, 1979.

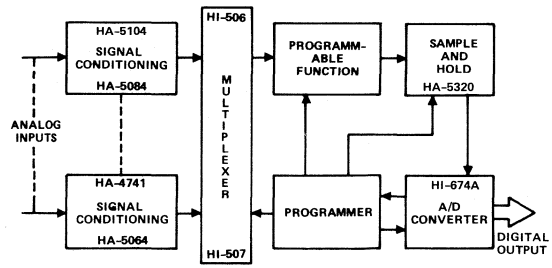


Figure 1A – Multiplexed, Signal Conditioning for Low Level Inputs

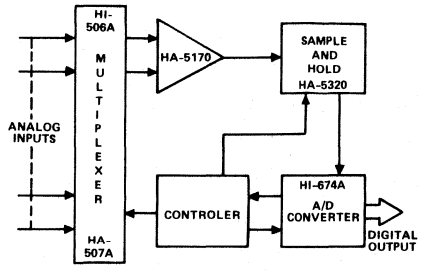


Figure 1B – Multiplexed. High Level Inputs

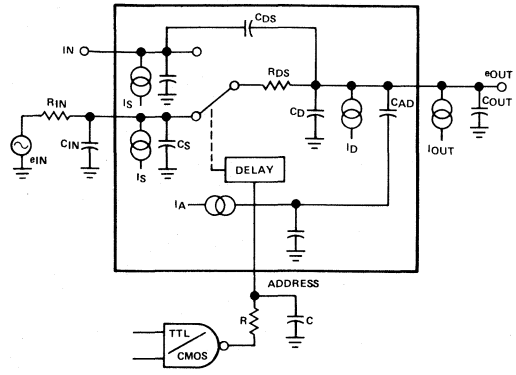


Figure 2 – Equivalent CMOS ANALOG SWITCH
DC Offset Error = $R_{DS} \times I_D$
Settling Time Determined by $R_{DS} \times C_D$

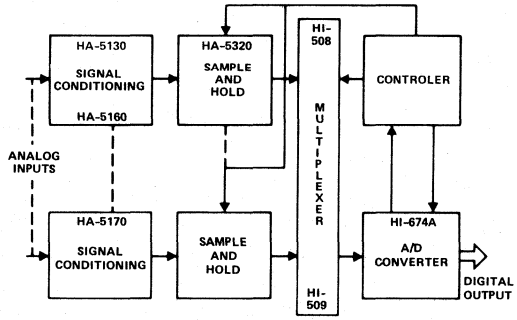


Figure 1C – Multiplexed. Sample / Hold Outputs

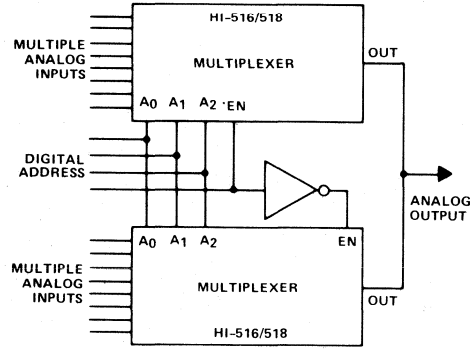


Figure 3A – Cascaded Multiplexers: Output Leakage Currents and Output Capacitance Increase Errors

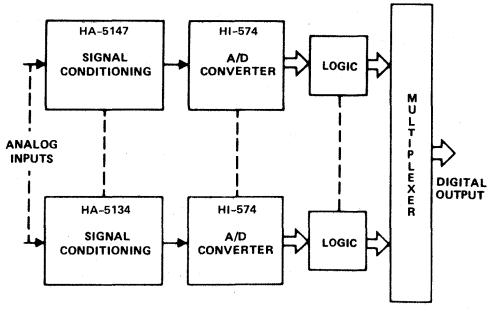


Figure 1D - Drgrtally Multiplexed A/D Outputs

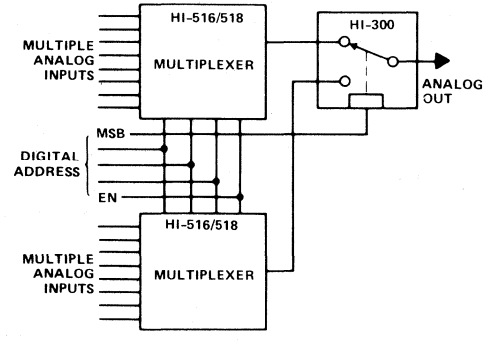


Figure 3B – Cascaded Multiplexers Two - Tiered Method : Errors Reduced Through Shared Switch

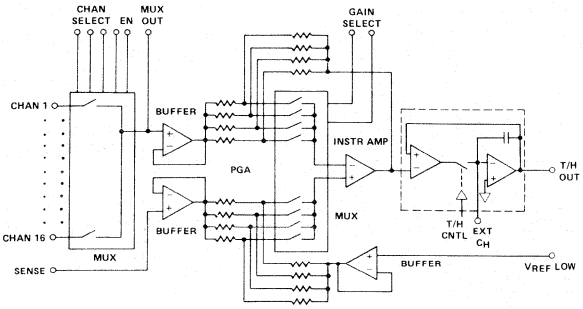


Figure 4B - Programmable DAQ Front-End (Single - Ended)

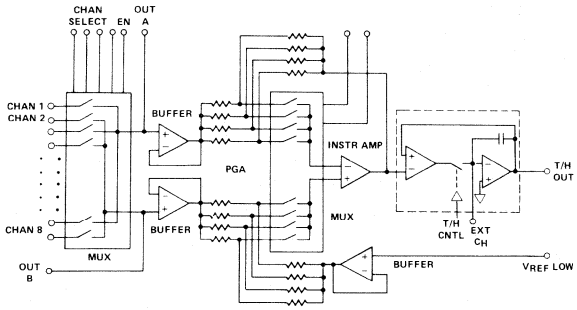


Figure 4A - Programmable DAQ Front-End (Differential)

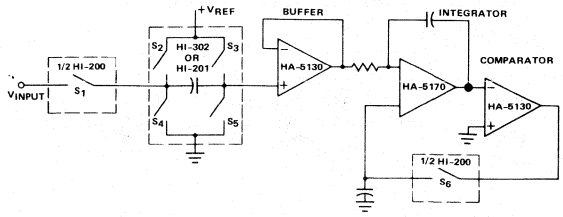


Figure 5. This autozero integrating converter uses six analog switches – S_1 through S_6. Zero correction occurs when S_3, S_4 and S_6 are "on". Integration occurs with S_1 closed. Integrate-reference takes place when S_2 or S_5 is "on".

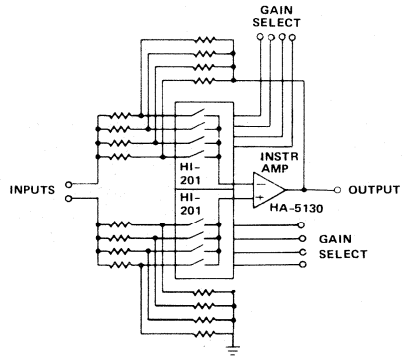


Figure 6 – Programmable Gain Instrumentation Amplifier

APP NOTE

FOR YOUR INFORMATION

No. 532

Harris Analog

COMMON QUESTIONS CONCERNING CMOS ANALOG SWITCHES

By Carl Wolfe

Introduction

The following information is a direct result of a significant amount of time spent in response to questions from users of HARRIS analog switches. Among the variety of questions are a few which seem to be asked more frequently than others. Over the next few pages, these questions are discussed with the hope that the answers will be helpful to the users and potential users of HARRIS analog switches. Some questions are technical in nature while others are simply questions on interpretation of the HARRIS Analog Data Book.

Power Supply Considerations

The first two questions are similar questions and the explanation will apply to both:

QUESTION #1: If the power supplies are off, will the switch be open? (Present a high impedance to the input signal)

QUESTION #2: If the power supplies are off, can an input signal be applied?

Both of these questions refer to an overvoltage condition when the supplies are off and an input signal is applied. A common misunderstanding is that the switch will be open and block the signal when actually the opposite occurs.

What is meant by the power supplies being off? Does it refer to the supplies being shorted to ground or does it imply they are open circuited?

If the power supplies go to ground, the input signal will pass through the switch and appear at the output. The explanation for this can be seen in Figure 1, which is a simplified CMOS switch cell. This switch cell consists of two enhancement type field effect transistors, one N-channel and one P-channel. An enhancement type of device is a FET which is normally off without some potential (gate voltage) to turn it on. A P-channel FET requires a negative potential (gate to source voltage) to turn it on and an N-channel FET requires a positive potential (gate to source). Contained in the physical structure of the FETS are parasitic transitors which are shown in Figure 1 as diodes from the source and drain to the body potentials of the devices. These diodes or parasitic junctions are normally reversed biased. If those junctions are forward biased, a fault condition exists where the signal is passed through the parasitic transitor. This is what occurs if the power supplies go to ground. Depending on the polarity of the input signal, either the N or P channel FET parasitics will be forward biased and the signal passed through the switch.

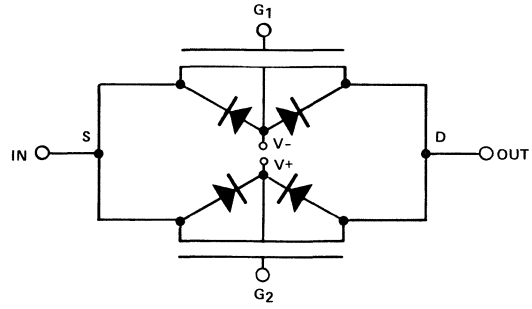


Figure 1. Basic CMOS Transmission Gate

Having the signal pass through the switch may be acceptable in some applications, but most likely it is not. An example would be user who was switching various voltages (transducers) as shown in Figure 2. If the supplies go to ground and these signals pass through the switch, the input voltage sources could easily be shorted.

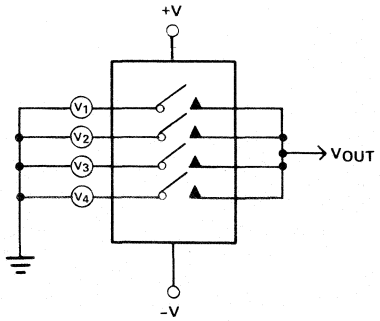


Figure 2. Switching Multiple Inputs

Another situation occurs if the power supplies are open circuited where the most positive and negative input signals will provide power to the switch. In this case, the signals being used for power will be passed to the output, but the remaining switches with inputs less than those used for supply will operate properly.

Input Overvoltage Protection

There is a possibilty the switch will be damaged if exposed to excessive current levels during an overvoltage condition. A second overvoltage condition is the case where the input signals exceed the existing power supply levels. Neither of these situations are recommended and the following questions are similar to those frequently asked.

QUESTION #3: Can an input greater than the supplies be applied?

QUESTION #4: In my application, there is a possibility that the switch will lose power and the input signal will still be applied. Is there a way to protect the switch if this situation occurs?

Referring to Figure 1 once again, if the input signal exceeds the supply by an amount greater than the breakdown voltage of the parasitic junction, the normally reversed biased junction will come forward biased. These forward biased junctions will pass the input signals to the output and possibly short out the input voltage sources.

The most common form of protection circuit for these types of overvoltage conditions is the resistor-diode network at the input of the switch as shown in Figure 3.

This circuit protects the device if the supplies go to ground or if the input exceeds the supply. If either of these situations occur the diodes will be forward biased and current path to ground will exist. This will protect the switch from excessive current levels. The primary purpose of the resistor is to limit the current through the diode.

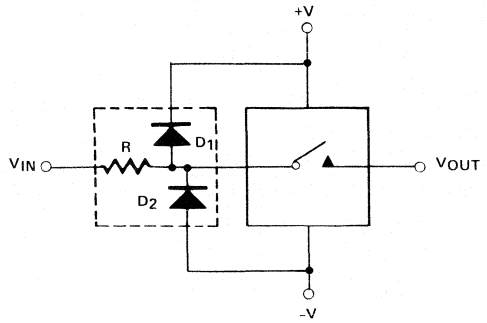


Figure 3. Protection for Each Analog Input

Another advantage of using diode protection is that it prevents the input signal from passing to the output. This is a result of the input being clamped to the breakdown voltage of the protection diodes. If this breakdown voltage is less than the threshold voltage (turn on voltage) of the parasitic diodes, the parasitic transistor will remain reverse biased and the signal will not pass through the switch.

There are some disadvantages to the user with this type of protection. One would be the economics involved with using external protection for each analog input. This could present a cost problem if a large number of channels were involved. Another concern would be the current limiting resistors which adds to the on resistance of the switch contributing to the overall system error. A further possible source of error is current leakage in the diodes. It is recommended that low leakage diodes, such as schottkey diodes be used.

The protection circuit just discussed is not used to protect the switch from latch up. The HARRIS switches are constructed using the dielectric isolation process and the four layer SCR found in JI technology does not exist. This circuit is intended to protect the device from high current levels which result from the forward biasing of the parasitic transistors which are inherent in all FET structures.

If for some reason the resistor-diode protection circuit cannot be used there are other possibilities. The following method may help to avoid the extra cost of protecting each input. In this method, since the supplies are open circuited, the most positive and most negative signal will power-up the chip and any input with signals less than those being used for power will operate properly. However, this method can only be used if the outputs are not common and a user can afford to have at least two signals pass to the output.

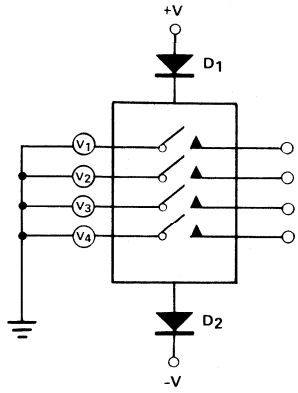


Figure 4. Powering the Switch With the Input Signals

Another alternative does not involve protection circuitry, but instead takes advantage of CMOS technology. An example would be a user who has ±15V supplies and needs to switch a +18V signal as shown in Figure 5. This appears to be an overvoltage condition since the input exceeds the supply. But rather than protect the device, the user can shift the supplies to +20V, -10V. Now the input signal is within the supply level and the switch should work properly. In certain applications the supply voltages can be adjusted in order to pass a larger range of input signals.

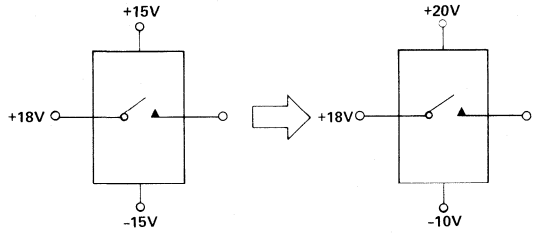


Figure 5. Varying the Supplies to Meet the V_{IN} < V Supply Requirements

Single Supply Operation

Single supply operation is a topic which is discussed frequently and the following are examples of typical questions.

QUESTION #5: Can the switch be operated at a single power supply?

QUESTION #6: What is the minimum power supply possible?

Usually engineers with critical power requirements request single supply operation. An example would be battery operated applications such as portable equipment. In these cases the designer is limited to single supply, low supply or both.

Trade-offs exist with single supply operation that should be pointed out to the user. An example is the HI-300 series of switches which has the capability of operating with a single +5 volt supply. The performance of the switch will vary, however, as the supply voltage varies. So, for the HI-300 series, as supply voltage decreases, the on resistance and the switching times increase. A 300 series switch with a single +5 volt supply will have higher on resistance and slower switching speeds than the same device at ±15 volts or even a single +15 volt supply. This represents a change in both DC and AC performance. Even though the switch may now meet the users power requirements at single supply, the question is whether it will still meet the performance requirements.

The explanation for these variations can be found in the FET devices composing the switch cell itself. The variation in on resistance is due to the fact that the channel impedance of FET is dependent on the gate - source bias. Since the gate voltage is determined by the supply voltage, it can be concluded that the on resistance is a function of the supply voltage.

The fact that the on resistance varies with supply voltage directly relates to the slower switching times, since the higher on resistance will reduce the available current needed to charge the internal capacitance of the switch. Lower changing current relates directly to slower switching times.

Questions About Harris Switches

Many of the questions asked about switches could apply to any CMOS switch manufacturer's products. But some questions are unique to both the Harris product line and data catalog. The following are examples of some of the more common questions concerning the Harris Analog Data Catalog.

QUESTION #7: What is the difference between the VL and VR pins on the HI-5043 and V_{REF} pins on the HI-201 ?

The device pins mentioned above have their own individual functions even though they are all associated wth the logic reference circuits of their respective designs. For the HI-201, the V_{REF} pin is the terminal which establishes the logic threshold levels for which the switch will change state. Although it is normally left open when driving from +5V logic (DTL or TTL), it can be connected to a higher supply in order to raise the switching threshold levels when driving from CMOS Logic greater than 5 volts. The V_{REF} pin enables the user to change from TTL to CMOS Logic.

The reference circuit of the HI-50XX series of switches is different from the HI-201, which accounts for the V_R and V_L pins. Even though the V_R terminal is brought out on the package, it is recommended that this pin be grounded. This terminal establishes the ground for the internal ref-

erence circuit. The V_L pin performs a similar function to the V_{REF} pin on the HI-201. It is normally connected to 5 volts for TTL logic but can be tied to a higher supply for CMOS levels. This effectively raises the switching thresholds to accomodate the higher CMOS level.

The next question is easily the most frequently asked question about HARRIS HI-50XX series of switches.

QUESTION #8: Are the switch functions shown on the data sheet a result of the logic address being HIGH or LOW ?

Actually, the answer to the question is printed at the top of the data sheet page,depicting switch functions "switch states are for a logic 1 input". Therefore, the address is in the HIGH state for the switch functions shown on that page.

Some other areas which are often questioned on the data sheets are the maximum ratings and performance between channels of the switches. The following questions are typical:

QUESTION #9: Will the switch operate at the absolute maximum ratings?

The topic of absolute maximum ratings does create some confusion. Basically, the contents of the Electrical characteristic table are the guaranteed parameters. The switch may operate with conditions other than those recommended, but are not guaranteed parameters. Anything above absolute maximum ratings may permanently damage the device.

Problems sometime arise when a customer tests some parts at conditions other than those which are guaranteed. If the parts work, the user may go ahead and design around these conditions. But there is a good possibility the next batch of switches may not perform in the same manner. The user must be aware that anything outside the guaranteed limits is a user's risk and susceptable to variations in manufacturing.

QUESTION #10: What is the variation in "on" resistance between channels on the switch?

There are two causes for these variation. One cause is process variation which is due to variables in manufacturing. This can create variation between channels on the same unit. The second reason is lot variation which can cause differences in performance from unit to unit. After all variations are taken into account, a good "rule of thumb" is ±10% tolerance on typical parameter values. So if a device has a typical on resistance of 50Ω , a user could expect a ±5Ω variation.

APP NOTE

FOR YOUR INFORMATION

No. 534

Harris Analog

ADDITIONAL INFORMATION ON THE HI-300 SERIES SWITCH

By Carl Wolfe

Introduction

The introduction of the HI-300 series of CMOS analog switches is the latest addition to the HARRIS switch family and gives the designer a viable second source to the Siliconix DG 300 series analog switch.

This family of monolithic, dielectrically isolated, CMOS analog switches consists of twelve products, the HI-300 thru HI-307 and the HI-381 thru HI-390 are designed for TTL level compatibility (logic "0" = .8V, logic "1" = 4.0V). The HI-304 thru HI-307 are CMOS compatible (logic "0" = 3.5V, logic "1" =11V).

The HI-300 series features low and nearly constant on resistance over analog signal range, low leakage and minimal power dissipation.

Improved Performance

An understanding of what a designer would consider important in an analog switch is useful in order to illustrate the advantage of the HI-300 series. Although any parameter could be considered important for a particular application, there are certain parameters considered to be most critical for the majority of applications. These parameters are:

"on" Resistance (Ron)
leakage current (I_{SOFF}, I_{DOFF}, I_{DON})
switching speed (ton, toff)
power supply current (I+, I-)

These parameters are important because the majority of designs require either high accuracy, speed, or low power dissipation.

ON RESISTANCE

In high accuracy systems, such as data acquisition systems, the designer would be concerned with minimizing errors caused by "on" resistance and leakage currents. An inverting programmable gain amplifier shown in Figure 1 will help illustrate the need for low on resistance and leakage current in high accuracy systems.

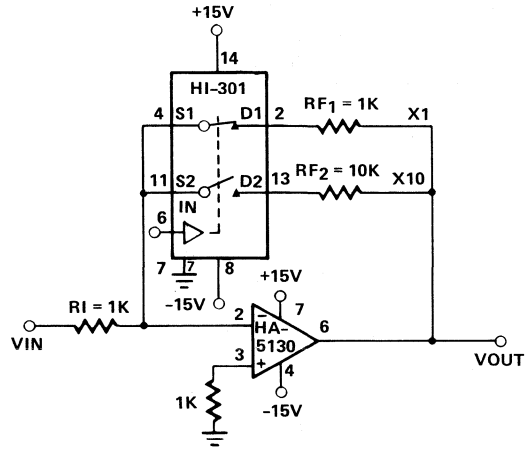


Figure 1 — Inverting Programmable Gain Amplifier

Ideally, the voltage gain of this inverting amplifier would be, $A_V = -(R_F/R_I)$. But when using a switch to program the gain, its characteristics must be taken into account and the amplifier gain equation must be modified to $A_V = -(R_F + R_{ON}/R_I)$. The higher the on resistance of the switch, the greater the gain error. Variations in the on resistance of the switch will also effect the gain error.

LEAKAGE CURRENT

Another source of error occurs in the switch "off" state, where leakage current causes offset voltage errors. In Figure 1, leakage current flowing through the feedback resistor creates an output voltage error equivalent to the expression, $V_O = R_F \times I_{DOFF}$.

SWITCHING SPEED

A designer concerned with switching times would

obviously be sensitive to the ton and toff specifications. A low value of "on" resistance is also important, since this resistance increases the RC time constants and can slow the circuits overall performance.

POWER SUPPLY REQUIREMENTS

The last critical parameter would be power consumption. There are certain applications where power supply currents are the primary concern of the designer. Examples would be portable or battery operated equipment.

The majority of switch applications require critical performance in one or more of the areas just discussed. The HI-300 series offers improved performance in each of these areas. The following tables compare the HI-300 series with existing HARRIS switches. Table 1 contains maximum specifications for T = 125°C and Table 2 consists of typical values at T = 25°C.

+125°C Maximum Specifications

SWITCH TYPE	RON	I LEAKAGE	I SUPPLY	tON	tOFF
HI-200	125Ω	500nA	2mA	500ns	500ns
HI-5040	75Ω	500nA	.3mA	1000ns	500ns
HI-300	75Ω	100nA	.1mA	300ns	250ns

Table 1 – Switch Comparisons at T=125°C

+25°C Typical Specifications

SWITCH TYPE	RON	I LEAKAGE	I SUPPLY	tON	tOFF
HI-200	55Ω	1nA	.5mA	240ns	330ns
HI-5040	25Ω	.8nA	.3mA	370ns	280ns
HI-300	30Ω	.1nA	.23μA	210ns	160ns

Table 2 – Switch Comparisons at T=25°C

From these tables it should be clear that the HI-300 series offers improved performance to the designer.

Inside The HI-300

Figure 2 shows the schematic of the digital input and driver stages of the HI-300. The purpose of this stage is to take the logic level signals and condition them to drive the gates of the FET switch cells.

The HI-300 series has a digital input protection circuit consisting of a 200Ω series resistor and clamping diodes, D1 and D2, to the supplies.

These diodes will quickly discharge any static charge which might appear at the digital inputs.

The F. E. T. Devices N1 thru N5 and P1 thru P5 form the input buffer and level shifter which establishes the proper voltages to drive the switch cell. N6, N7, P6, and P7 form the output buffers which isolate the level shifter from the capacitive load of the switch cell.

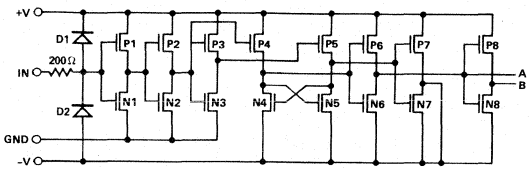


Figure 2 – Partial Schematic

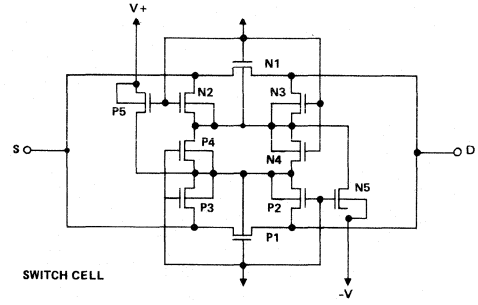


Figure 3 – Schematic

The switch cell shown in Figure 3 is based on the FET devices N1 and P1. The remaining devices, N2 thru P5 serve various functions, such as reducing leakage current, minimizing on resistance variations and minimizing charge injection.

Additional Performance Characteristics

(A) SINGLE SUPPLY OPERATION

The HI-300 series has the capability of single supply operation. These switches can operate to a minimum supply of +5 volts, although designers must be aware of the trade off which exists at these levels. The trade off is the performance of the switch will vary as the supply level varies. Examples of these performance variations are increased on resistance and slower switching times. So, a HI-300 series switch with a single five volt supply will have higher on resistance and slower switching speeds then the same device at ±15 volts or even a single +15 volt supply.

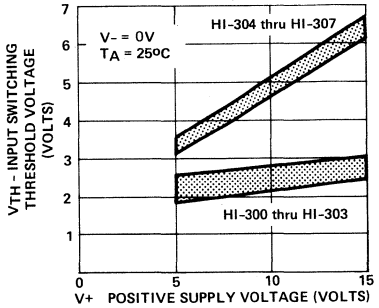
The explanation for these variations can be found in the F.E.T. devices composing the switch cell itself. The variation in on resistance is due to the fact that the channel impedance of the FET is dependent on the gate-source bias. Since the gate voltage is determined by the supply voltage, it can be concluded that the on resistance is a function of the supply voltage.

The fact that the on resistance varies with supply voltage directly relates to the slower switching times. The higher resistance reduces the available current

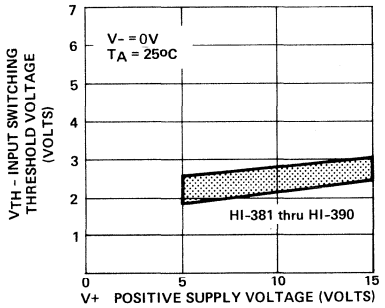
needed to charge the internal capacitances of the switch. Lower charging current directly relates to the slower switching times.

The explanations, just given, along with the following typical curves of the HI-300 single supply operation, should aid the designer in applying the HI-300 series in single supply applications.

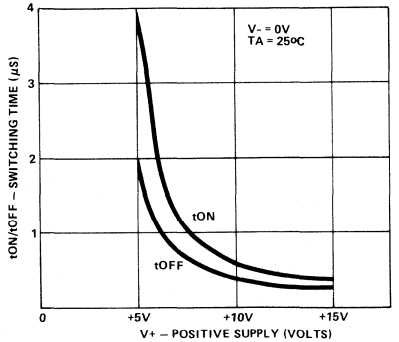
INPUT SWITCHING THRESHOLD VS. POSITIVE SUPPLY VOLTAGE HI-300 THRU HI-307



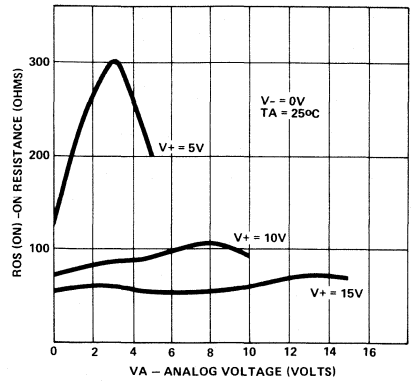
INPUT SWITCHING THRESHOLD VS. POSITIVE SUPPLY VOLTAGE HI-381 THRU HI-390



SWITCHING TIME VS. V+ - POSITIVE SUPPLY VOLTAGE



RDS(ON) VS. ANALOG AND POSITIVE SUPPLY VOLTAGE WITH V- = 0V



B) CHARGE INJECTION

The charge injection of a switch is a critical parameter for certain applications, such as small signal switching or sample and hold circuits.

For the case of small signal switching, unwanted switching spikes result from this transferred charge causing system errors. These spikes are created when the transitions of the gate voltage are capacitively coupled to the output through the gate to source and gate to drain capacitances, as shown in Figure 4. The magnitude of these switching spikes will depend on the values of the load and source impedances, the value of the gate voltage and the size of the internal capacitances of the switch.

For the sample and hold circuit, shown in Figure 5, a common problem is sample to hold offset error. It is caused by the same mechanisms discussed for the small signal application, but in this case the charge is transferred to the hold capacitor and an offset voltage is created. The voltage is determined by the following relationship. V = Q/CH.

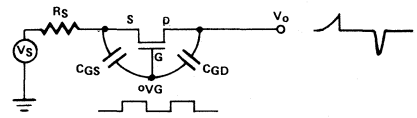


Figure 4 – Charge Transfer

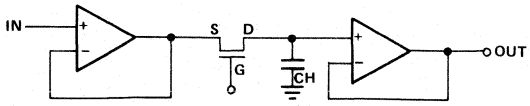


Figure 5 — Sample and Hold

Charge injection can create problems in the type of applications just described. A typical curve of the HI-300 series charge injection performance is shown in Figure 6 as an aid to designing in these type of circuits.

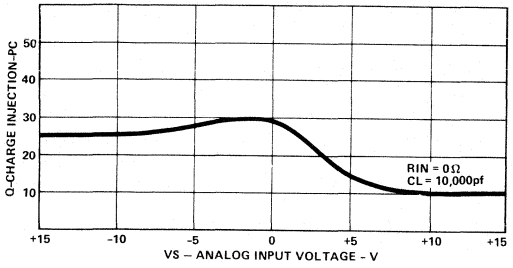


Figure 6 — Charge Injection vs. Input Voltage

Application Hints

A. POWER SUPPLY CONSIDERATIONS

The HI-300 series analog inputs do not feature overvoltage protection. External protection circuitry would be necessary if the switches were subjected to possibly destructive situations.

An example could be an overvoltage condition where the power supplies to the switch go down while an analog input signal is still present. A common misunderstanding is that the switch will be open and block the input signal, when actually the opposite occurs.

If the power supplies go to ground, the input signal will pass through the switch and appear at the output. The explanation for this can be seen in Figure 7, which is a simplified CMOS switch cell. This switch cell consists of two enhancement type field effect transistors, one N-channel and one P-channel. An enhancement type of device is a FET which is normally off without some potential (gate voltage) to turn it on. A P-channel FET requires a negative potential (gate to source voltage) to turn it on an N-channel FET requires a positive potential (gate to source). Contained in the physical structure of the FETS are parasitic transistors which are shown in Figure 7 as diodes from the source and drain to the body potentials of the devices. These diodes or parasitic junctions are normally reversed biased. If those junctions are forward biased, a fault condition exists where the signal is passed through the parasitic transistor. This is what occurs if the power supplies go to ground. Depending on the polarity of the input signal, either the N or P channel FET parasitics will be forward biased and the signal passed through the switch.

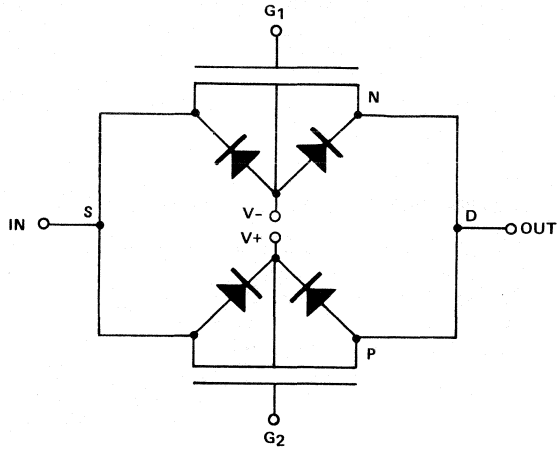


Figure 7 — Basic CMOS Transmission Gate

Another situation occurs if the power supplies are open circuited, the most positive and negative input signals will provide power to the switch. In this case, the signals being used for power will be passed to the output, but the remaining switches with input signals less than those used for supply will operate properly.

A second overvoltage condition is the case where the input signals exceed the existing power supply levels. Referring to Figure 7, if the input signal exceeds the supply by an amount greater than the breakdown voltage of the parasitic junction, the normally reversed biased junction will become forward biased. These forward biased junctions will pass the input signals to the output and possibly short out the input voltage sources.

The most common form of protection circuit for these types of overvoltage conditions is the resistor-diode network at the input of the switch as shown in Figure 8. This circuit protects the device if the supplies go to ground or if the input exceeds the supply. If either of these situations occur, the diodes will be forward biased and a current path to ground will exist. This protects the switch from excessive current levels. The primary purpose of the resistor is to limit the current through the diodes.

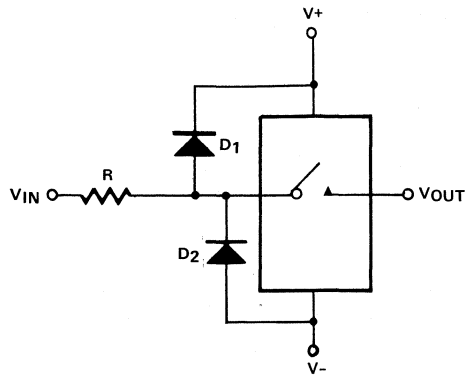


Figure 8 – Protection for Each Analog Input

Another advantage of using diode protection is that it prevents the signal from passing to the output. This is a result of the input being clamped to the breakdown voltage of the protection diodes. If this breakdown voltage is less than the threshold voltage (turn on voltage) of the parasitic diodes, the parasitic transistor will remain reversed biased and the signal will not pass through the switch.

The protection network may introduce unwanted error into the circuit in the form of leakage current and increased on resistance. It is recommended that low leakage diodes be used, such as Schottkey diodes. If the switch is looking into a high impedance, such as the input operational amplifier, the error introduces by the increased on resistance will be negligible.

The protection circuit just discussed is not used to prevent the switch from latch up. The HI-300 series switch is constructed using the HARRIS dielectric isolation process and the four layer SCR found in JI technology does not exist. This circuit is intended to protect the device from high current levels which result from the forward biasing of the parasitic transistors which are inherent in all FETS.

An alternative to protection circuits takes advantage of CMOS technology. Assume an overvoltage condition exists where the input exceeds supply. Rather than use external components to protect the device, it may be possible to shift the supplies in order to accomodate the input signal. An example would be an application with ±15 volt supplies, but attempting to switch a +18 volt input signal. A possible solution would be to shift the supplies to V+ = +20V and V- = -10V and now the input signal is within the existing supplies. In some applications the supply voltage can be adjusted in order to pass larger input signals.

Acknowledgement

A. Engineering staff of Harris Semiconductor, P.O. Box 883, Melbourne, FL 32901, particularly Frank Cooper, whose useful comments contributed to this publication.

References

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(3) Ernie Thibodeax, "Getting the most out of C-MOS devices for analog switching jobs", Harris Application Note 521.

(4) Hunter, Bill, CMOS DATA BOOK: Tab Books, 1978.

DESIGN CONSIDERATIONS FOR A DATA ACQUISITION SYSTEM (DAS)

By Tarlton Fleming

Introduction

This is a collection of guidelines for the design of a data acquisition system. Its purpose is to supplement the more methodical block-by-block discussions available in numerous other papers and application notes. Emphasis in this note is on the less easily quantifiable happenings "between the blocks", rather than a description of the block components and their error contributions. This latter information may be found in the Bibilography under "General".

A data acquisition system is defined to include all the components needed to generate the electrical analogs of various physical variables, transmit these signals to a central location and digitize the information for entry into a digital computer. Among these components are transducers, amplifiers, filters, multiplexers, sample/holds and analog-to-digital converters. The system also includes all signal paths tying these functions together.

Several system architectures will be considered, followed by a general discussion aimed at the designer who must choose hardware for a given application. Topics include:

- Data Acquisition System Architecture
- Signal Conditioning
- Transducers
- Single-Ended vs. Differential Signal Paths
- Low-Level Signals
- Filters
- Programmable Gain Amplifier
- Sampling Rate
- Computer Interface

Data Acquisition System Architecture

At present the most widely used DAS configuration is that shown in Fig. 1. It handles a moderate number of analog channels, feeding into a common multiplexer, programmable gain amplifier (if required), track/hold amplifier and A-D converter.

A more specialized and expensive variation is to place a Track/Hold in each channel as shown in Fig. 2. Switching all channels to HOLD simultaneously produces a "snapshot" view which preserves the phase relation of signals in all channels. This information is important in seismic studies and vibration analyses.

The DAS system of Fig. 3 offers many advantages, but is not yet practical except for slowly changing channel data. Low frequency signals allow dedication of a slow but accurate integrating type A-D converter for each channel. The channel filters often included to reduce aliasing errors and noise are not necessary, since aliasing is not a problem with low bandwidth signals. The integrating converter suppresses wideband noise by averaging it about the instantaneous signal level. Also, the converter's integration period may be chosen to provide almost complete rejection of a specific interference frequency such as 60 Hz. Digital outputs from the converters are then digitally multiplexed.

The system shown in Fig. 3 has an inherent advantage over the other two systems, having eliminated both the track/hold and the analog multiplexer with their many error contributions. The disadvantage, of course, is cost. Fig. 3 would become the system of choice in many more applications, if a significant reduction should occur in the price of successive - approximation A-D converters.

A small RAM may be added at the converter's output in any of these systems, to buffer the computer and offload its involvement with individual conversions. Timing and control may be arranged to scan all channels repeatedly, and continuously update a RAM location for each channel. The computer is then free to look at a recent reading for any channel, at any time.

Further discussion will center on Fig. 1, both in the single-ended version shown, and in the differential version.

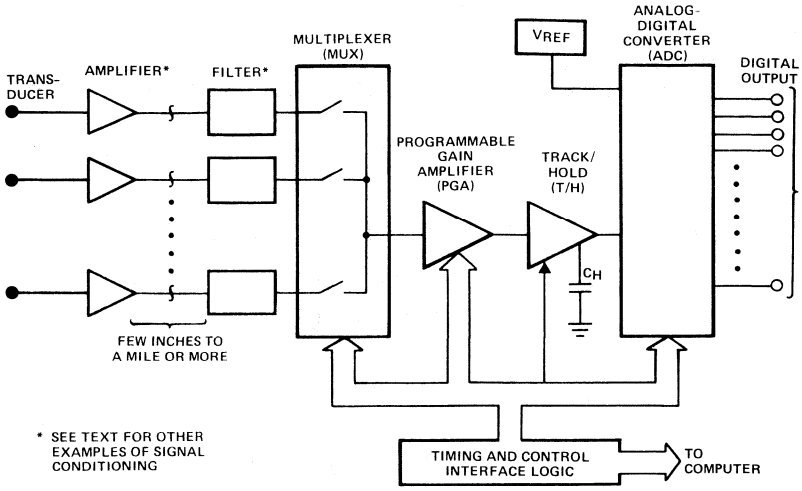


FIGURE 1. Typical Data Acquisition System

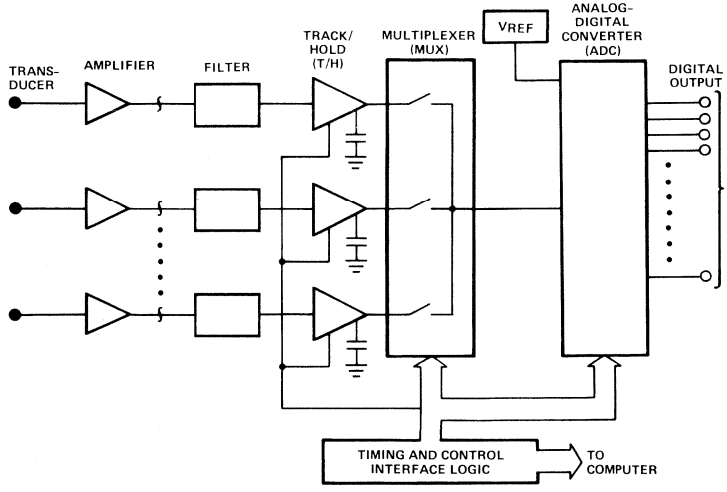


FIGURE 2. DAS System For Simultaneous Sampling Of All Channels

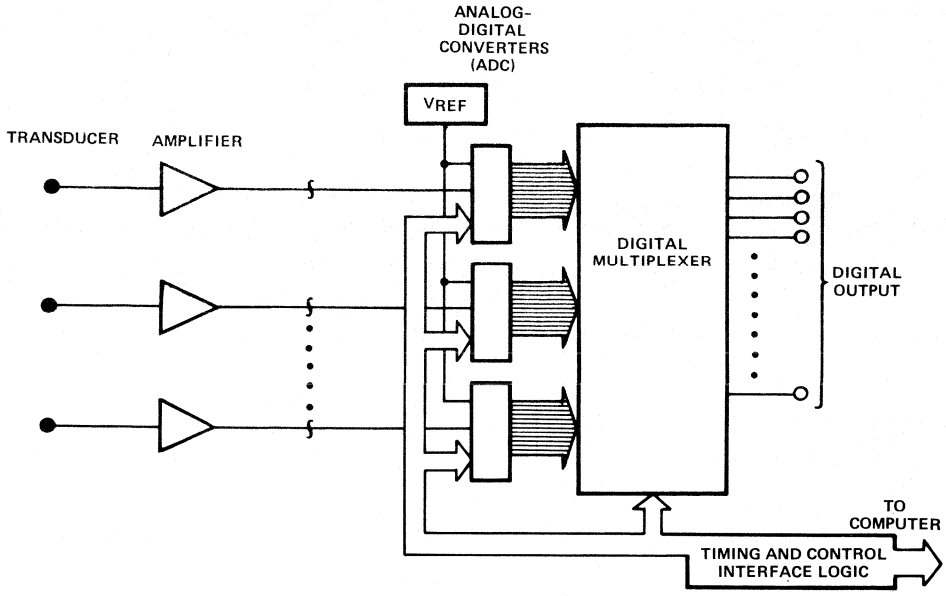


FIGURE 3. High Accuracy, Multi-Converter DAS System

Signal Conditioning

Signal conditioning refers to all the operations performed on a transducer signal up to (and including) digitization by the A-D converter. Standard among these operations are multiplexing, programmable gain, and Track/Hold. Others may be added as required:

- Transducer excitation
- Amplification
- Filtering
- Calibration
- Linearization
- Voltage to current conversion (4 to 20 mA; 10 to 50 mA)
- rms to dc conversion
- Logarithmic signal compression
- Common mode rejection

For highest signal-to-noise ratio all signal conditioning should be performed near the transducer, with the exception of common mode rejection and filtering. Filters should be located near the multiplexer input. Besides minimizing alias errors originating in the high end of the transducer's output spectrum, filters suppress wideband noise picked up on signal lines to the transducer.

Transducers

The first item in the signal path of a DAS is the transducer. This device usually transforms energy from one form to another, producing an electrical analog of the physical variables to be monitored or measured. Transducers are based on a variety of physical principles but most produce a voltage as output. Some yield an intermediate variable such as resistance or capacitance, which is transformed to voltage by an applied electrical excitation (carrier frequency, dc voltage, current source).

Often, several types of transducers are available to sense a given quantity. When selecting a voltage output transducer, remember that a low source resistance is desirable, both to minimize noise and to reduce loading by the next "block" in the signal path. Provision on the transducer for a convenient method of signal calibration will be welcome, once a system is in operation. Also, a center tap on the transducer allows better interface to a balanced line if low level signals are to be transmitted.

Several questions arise at this point:

- Should the signal path be single-ended or differential?
- Should the signal be transmitted at low level (100 mV) or high level?
- What type of conductor should be used for signal transmission?

Answers to these and other questions are covered in the following Sections.

Signal-Ended vs. Differential Signal Paths

Consider the transducer output. A high level signal (100 mV to 10 V) is easier to handle than low level. Is a common mode signal present? If not, is it likely to be acquired as "pickup" during transmission? This is likely if the cable is routed near fluorescent lights, motors or other electrical machinery. If common mode voltage is not expected, then an economical single-ended connection is possible, with a single wire per channel and a common return. (see Fig. 4). High level signals, short distance and controlled conditions will ensure good performance with this arrangement.

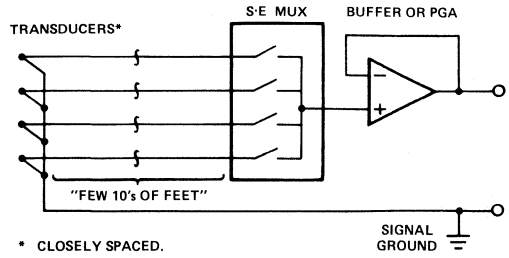


FIGURE 4. Single-ended Data Paths

Low level signals require special treatment. Whether high or low level, the presence of common mode voltage calls for a differential signal path. The most widely used solution is an unshielded, twisted pair of wires, good for 1000 feet or so with a bandwidth of 100 KHz. As a minimum then, two wires per channel feed into a differential amplifier or multiplexer, buffered by a full or pseudo-differential amplifier to reject the unwanted common mode voltage (see Fig. 5).

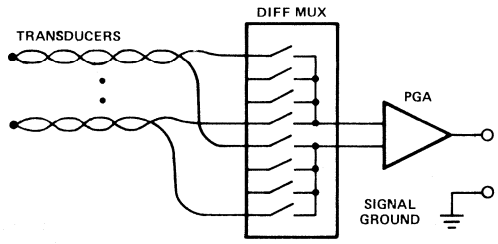


FIGURE 5. Differential Data Paths

For the case in which the transducer output is a low level voltage, the choice is whether to transmit it as is, or to boost the level by adding an amplifier. The amplifier will provide low source impedance as well as gain; two valuable forms of signal conditioning. However, providing power to a remote amplifier can be difficult. Even if a supply is available at the remote site, the voltage between two widely separated commons presents a problem. If the sum of signal plus common mode voltage does not exceed the input range of either the multiplexer or buffer amplifier, Fig. 5 can be used.

A more expensive approach is required for higher common mode voltages. One reliable technique is the "flying capacitor" multiplexer of Fig. 6, using reed relay switches. This works well for thermocouples bonded to machinery and riding on hundreds of volts relative to DAS ground, but in some applications the reed relay's 1 ms response time can be a limitation.

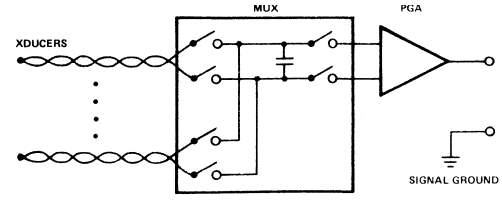


FIGURE 6. "Flying Capacitor" multiplexer using reed relay switches for high CMV signals.

Isolation amplifiers can handle higher voltages and higher bandwidths than the system of Fig. 6. For example, magnetically isolated amplifiers are rated at 2KV and up with a small signal bandwidth of approximately 2 KHz. One of these per channel is expensive, but in addition to common mode rejection it can solve the problem of supplying power at the remote transducer. Isolation amplifier models are available which include ±15V terminals, referenced to the floating front-end of the amplifier. This power can provide transducer excitation and supply an amplifier or other signal conditioning circuitry.

For higher bandwidth data, optically isolated isolation amplifiers are available with $f_{-3dB} = 15KHz$ and 2KV isolation. These amplifiers do not provide the external supply terminals to power transducer circuitry.

Low Level Signals

The main concern with signals below 100mV is that noise, offset voltage, and other aberrations can represent a large percentage error. A shielded, differential signal path is essential for transmitting these signals, especially to maintain a noise level below 50μV rms.

Most transducer outputs are low level and low bandwidth as well. Since shielding precautions to be described are intended to produce an acceptable signal to noise ratio, filters may not be necessary. Otherwise, active filters with their relatively large dc errors should not be used for low level signals. Passive filters on the other hand, are restricted to two or three poles as a practical limit, which in turn restricts the allowable signal bandwidth for a given accuracy (see the Section titled Filters).

The transmission cable carrying the transducer signal is critical in a low level system. It should be as short as practical and rigidly supported. Signal conductors should be tightly twisted for minimum enclosed area, to guard against pickup of electromagnetic interference, and the twisted pair should be shielded against capacitively coupled (electrostatic) interference. A braided wire shield may be satisfactory, but a lapped foil shield is better since it allows only one tenth as much leakage capacitance to ground per foot.

A key requirement for the transmission cable is that it present a balanced line to sources of noise interference. This means an equal series impedance in each conductor plus an equally distributed impedance from each conductor to ground. The result should be signals equal in magnitude but opposite in phase at any transverse plane. Noise will be coupled in-phase to both conductors and rejected as common mode voltage. Again, any such noise will be directly proportional to the source impedance driving the line. An isolation or instrumentation amplifier may be used to terminate the line, providing high input impedance, common-mode rejection, conversion from a differential to single-ended signal path, and a buffer for the ON resistance of the following multiplexer.

Coaxial cable is not suitable for low-level signals because the two conductors (center and shield) are unbalanced. Also, ground loops are produced if the shield is grounded at both ends by standard BNC connectors. If coax must be used, carry the signal on the center conductors of two equal-length cables whose shields are terminated only at the transducer end. As a general rule, terminate (ground) the shield at one end only, preferably at the end with greatest noise interference. This is usually the transducer end for both high and low level signals.

Printed circuit traces and short lengths of wire can add substantial error to a signal even after it has traveled hundreds of feet and arrived on a circuit board. Here, the small voltage drops due to current flow through connections of a few milliohms must be considered, especially to meet an accuracy requirement of 12-bits or more.

The table of Fig. 7 is a useful collection of data for calculating the effect of these short connections. (Proximity to a ground plane will lower the values for inductance.)

WIRE GAGE	EQUIVALENT WIDTH OF P.C. CONDUCTOR (2 OZ. Cu.)	DC RESISTANCE PER FOOT	INDUCTANCE PER FOOT	IMPEDANCE PER FOOT	
				AT 60Hz	AT 10KHz
18	0.47"	0.0064Ω	0.36μH	0.0064Ω	0.0235Ω
20	0.30"	0.0102Ω	0.37μH	0.0102Ω	0.0254Ω
22	0.19"	0.0161Ω	0.38μH	0.0161Ω	0.0288Ω
24	0.12"	0.0257Ω	0.40μH	0.0257Ω	0.0345Ω
26	0.075"	0.041Ω	0.42μH	0.041Ω	0.0488Ω
28	0.047"	0.066Ω	0.45μH	0.066Ω	0.0718Ω
30	0.029"	0.105Ω	0.49μH	0.105Ω	0.110Ω
32	0.018"	0.168Ω	0.53μH	0.168Ω	0.171Ω

FIGURE 7. Impedance of Electrical Connections, +20°C

As an example, suppose the ADC in Fig. 1 has 12-bit resolution, and the system accuracy is to be ± ½ LSB (± 1.2mV). The interface logic might draw 100 mA from the + 5V supply. Flowing through six inches of #24 wire, this current produces a drop of 1.28mV; more than the entire error budget. Obviously, this digital current must not be routed through any portion of the analog ground return network.

Filters

The presampling or anti-aliasing filters shown in Fig. 1 are normally required with high-level signals of significant bandwidth, especially if the signal is to be reconstructed by a digital-to-analog converter after processing. If low level signals require a passive filter, the differential configuration of Fig. 8 preserves some degree of impedance balance on the line.

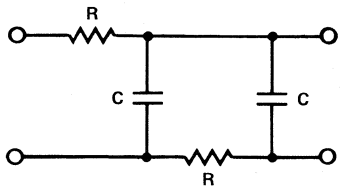
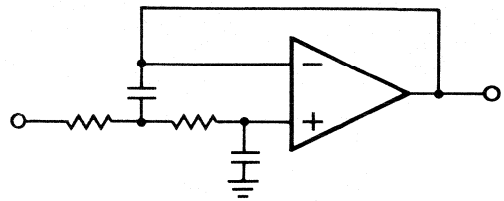


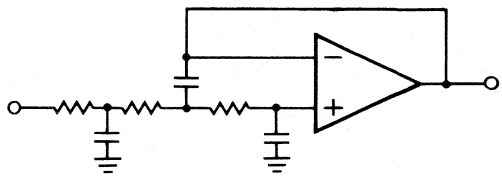
FIGURE 8. A Passive, Two Pole, Low Pass, Differential Input Filter

A low-pass Butterworth response is best for the channel bandlimiting filter in most data acquisition systems. The Butterworth filter output decreases monotonically with frequency, though this attenuation is very slight within the passband. Other filter types produce ripple in the passband, whose amplitude degrades accuracy unless expensive, high tolerance components are used.

Butterworth is not the most linear phase response, and if signal group delay is critical an elliptic (Bessel) filter should be chosen. Again, however, Butterworth fits most applications. A given number of poles may be had by cascading the two and three pole sections shown in Fig. 9. Either reference under "Filters" in the Bibliography gives a systematic procedure for calculating R and C values in terms of a given cutoff frequency. See the Section on "Sampling Rate" for the poles vs. accuracy requirement.



a. TWO POLE SECTION



b. THREE POLE SECTION

FIGURE 9. Butterworth Low-Pass Filters

Programmable Gain Amplifier (PGA)

Unless the ratio of highest to lowest signals anticipated on any channel is ≤ 2, some form of programmable gain amplification is desirable between the multiplexer and A-D converter. Without this variable gain block, the MSB's are idled one after another as input level decreases. Although the resolution of an n-bit converter remains a constant $FS/2^n$ by definition, resolution referred to the input level is decreasing (FS = Full Scale).

Considering resolution as referred to the input level, a 12-bit converter digitizes an input of .06FS to only 8 bits. The full 12-bit resolution applies only for $V_{IN} \geq FS/2$. Therefore to fully utilize the converter, gain should be added as necessary before each conversion, to meet the condition $FS/2 \leq V_{IN} \leq FS$. Then the amount of gain introduced by the PGA is noted by the computer to keep track of the actual input value.

Three other services are performed by the PGA:

1. Buffering: Prevents a loading effect due to the multiplexer's ON resistance.

2. Differential to Single-Ended Conversion: Necessary for the majority of Track (or Sample) /Holds and A-D converters.

3. Common Mode Rejection (CMR). When connected to the output of a differential multiplexer, the PGA's differential input rejects the common mode voltage accumulated by a signal transmission cable. Fig. 10 shows a subtractor or "pseudo-differential" PGA suitable for wideband signals with low common mode content. In this circuit, CMR is limited by precision of the "K" ratio and variations in the channel source impedance.

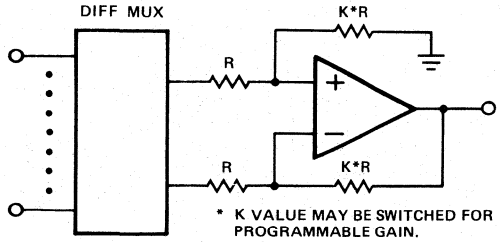


FIGURE 10. Subtractor or Pseudo-Differential PGA

Fig. 11 is the full differential PGA, necessary for low-level, high common mode signals. This version offers the highest gain accuracy and for high gain, the best CMR.

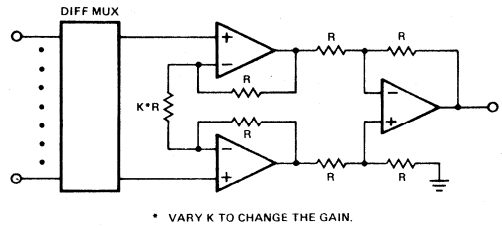


FIGURE 11. Full Differential PGA

The PGA normally precedes the Track/Hold, since the PGA would amplify any error introduced by that device. This order must be reversed to implement an auto-range capability, because the signal voltage must be held at the PGA input for the duration of an auto-range subroutine by the computer. Such an algorithm consists of:

- Set PGA gain
- Trigger a conversion
- Note RESULT
- Iterate until (FS/2 $\leq$ RESULT $\leq$ FS)

Sampling Rate

Throughput rate for a DAS may be defined as the maximum number of digital samples per second that it can produce without exceeding its specified limit for accuracy. The system may run at a lower speed to avoid generating redundant and useless data; but if a waveform of significant bandwidth is to be reconstructed from the digital samples, then "the higher the better" is generally the rule for sampling rate.

The required rate is often higher than one would suppose. For example, using the criteria of data bandwidth alone, a very low sample rate is required for the slowly changing voltage outputs from a solar panel. Once per minute for each channel might be enough. With 60 channels though, the rate required is once per second. In addition, one might require a maximum of one second for notice of failure on any channel, boosting the required sample rate to 60 samples per second. In this manner low bandwidth channels may require a high speed DAS, according to the relationship:

System Sample Rate = (Highest Channel Rate) X (Number of Channels)

Also, a very high sample rate is required to preserve the high frequency content of a transient event on a single channel. The most commonly encountered requirement though, is a multichannel DAS (see Fig. 1) with a modest bandwidth on each channel. For example, each data source might be an accelerometer with an output ranging through several hundred Hertz.

Notice that the low and high bandwidth signals just described cannot be handled efficiently with the same system. A sample rate high enough for the highest bandwidth channel will oversample the lower bandwidth channels, generating unnecessary data. High and low bandwidth data are best handled by separate multiplexer/converter systems.

Presampling filters are essential to ensure accuracy in the sequence of digital samples representing a given channel. Since the multiplexer is a sampler (as is the Sample/Hold and A-D Converter) this means a separate filter dedicated to each channel preceding the multiplexer. A single filter following the multiplexer would do the job, but its modest response time would form a bottleneck restricting the sample rate. Guidelines are needed then, to relate a given level of accuracy to data bandwidth, filter cutoff frequency, and number of filter poles.

As mentioned earler, a filter limits the error due to alias frequencies by restricting the bandwidth of both signal and noise. Either acting alone or in concert may cause error, since alias frequencies arise in several ways:

1. Overlap of the signal spectrum and the lower sideband associated with the sampling frequency f_S.
2. Overlap of the upper and lower sidebands associated with any two consecutive harmonics of f_S.
3. Overlap of any sideband with wideband noise from the data channel.

A band-reject filter would control case 1, but a low-pass type is needed to handle cases 2 and 3 as well. Again, the Butterworth response is preferred in most applications, but it does offer increasing phase shift and gain error for frequencies approaching the cutoff (-3dB) frequency. This cutoff should be set no higher than necessary for acceptable gain error in the highest signal components. A higher cutoff will only include unnecessary noise bandwidth.

Finally, for a given accuracy specification such as ± ½ LSB, a tradeoff may be made between the sample rate and number of poles. These poles usually come from the filter, but the number may include any pole(s) inherent in the transducer, provided they occur at an acceptable location relative to the cutoff frequency.

Fig. 12 shows aliasing error due to the signal spectrum alone vs sampling rate for different numbers of poles. The horizontal axis is normalized to Sampling Frequency/Cutoff Frequency. Notice that a 2-pole filter requires a sampling frequency 30 times the filter cutoff frequency, just to obtain 1% accuracy. For ± ½ LSB error in a 12-bit system (± .01%), a 5-pole filter requires sampling at 11 times the cutoff frequency. Remember, Fig. 12 applies only to the signal spectrum. Noise will cause some additional aliasing error.

Clearly, Nyquist's Sampling Theorem is not a practical guide for sampling rate in real applications. Actual (as opposed to hypothetical) filters cannot bandlimit a signal sufficiently to permit the theoretical minimum of two samples per cycle of highest signal frequency.

MONOLITHIC SAMPLE/HOLD COMBINES SPEED AND PRECISION

By Tarlton Fleming

Introduction

A new Sample-Hold amplifier from Harris Semiconductor offers the best combination of speed and accuracy available in a monolithic device. It was developed for moderate to high speed applications-and particularly as an input for successive-approximation A/D converters which perform a precise conversion in 30 microseconds or less. This second-generation design includes a 100pF MOS hold capacitor, and offers a 1.0 microsecond acquisition time along with high accuracy over the commercial and military temperature ranges.

This new product, the HA-5320, can track a signal indefinitely (like an op amp) while in the sample mode. At the instant a digital HOLD command is applied the corresponding signal level is held and maintained at the output. The ratio of sample (track) to hold time is set by the user, according to the duty cycle of his digital control signal.

Comparision With Earlier Design

The HA-5320 retains the versatility of its predecessor, the popular HA-2420. That is, both have the uncommitted differential inputs of an op amp, allowing their Sample-Hold function to be combined with many conventional op amp circuits. Their circuit designs are different, though, producing significant differences in performance. These are best illustrated by describing the new device in contrast with older HA-2420. Table 1 summarizes the electrical characteristics of each, based on a 100pF hold capacitor.

Both IC's are packaged in a 14 pin DIP and operate on ±15V supplies. The hold capacitor connections differ as shown in Figure 1. Otherwise, the pinouts are compatible to this extent: Either device will operate in an existing HA-2420 socket if pin 6 is grounded, preferably to the system signal ground.

The HA-5320 delivers optimum performance when used as intended — relying on the internal 100pF hold capacitor alone. At +75°C this capacitor allows only 19μV of droop in 15μs. The Droop Rate is proportional to Drift Current, which increases with temperature (Figure 3). Droop may be reduced by adding external cpacitance C_H as shown in Figure 1B. This extra capacitance will reduce the bandwidth (Figure 5) and affect other parameters as shown in Figure 4. Also, a capacitor of value $0.1C_H$ should be added at pin 8 to reduce output noise in the Hold mode. Whether operating with additional hold capacitance or not, an HA-5320 offers a considerable improvement in accuracy over the HA-2420. Particularly welcome is the elimination of variation in "pedestal" error with input voltage. Further, the residual pedestal error may be nulled to zero, yielding great accuracy at a given temperature.

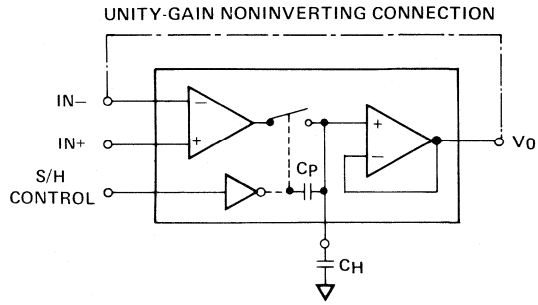


Figure 1A. HA-2420 Diagram

Test Conditions: $V_{PS} = \pm 15V$; $V_{AL} = 0.8V$ (Sample); $V_{AL} = 2.0V$ (Hold); $C_H = 100pF$

(Room Temp R = +25°C; Full Temp. F is -55°C to +125°C)

		HA-5320			HA-2420			
PARAMETERS	**TEMP.**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Characteristics								
Offset Voltage	R		0.2	0.5		2		mV
	F			2.0			6	mV
Bias Current	R		70	200		40		nA
	F			200			400	nA
Offset Current	R		30	100		10		nA
	F			100			100	nA
Common Mode Range	F	±10			±10			V
CMRR	R	-80	-90		-80	-90		dB
Transfer Characteristics								
Large Signal Voltage Gain	R	1×10^6	2×10^6			50K		V/V
Feedthrough Attentuation, 100KHz	F	76	80			76		dB
Gain Bandwidth Product	R		2.0			2.8		MHz
Output Characteristics								
Voltage	F	±10			±10			V
Current	R	±10			±15			mA
Full Power Bandwidth	R		600			100		KHz
Transient Response								
Rise Time	R		100			50	75	nS
Overshoot	R		15			25	40	%
Slew Rate	R		45		5	7		V/S
Digital Input Characteristics								
Voltage High (V_{AH})	F	2.0			2.0			V
Voltage Low (V_{AL})	F			0.8			0.8	V
Current ($V_{AL} = 0V$)	F			-4			-800	μA
Current ($V_{AH} = 5V$)	F			100			20K	nA
Sample/Hold Characteristics								
Acquisition Time,to								
±0.1% FS	R		0.8			2.5		μS
±0.01% FS	R		1.0			3		μS
Aperture Time	R		25			30		ns
Effective Aperture Delay Time	R		-25			30		ns
Aperture Uncertainty	R		0.25			5		ns
Drift Current	R		8			5	50	pA
	F		1.7			1.8	10	nA
Pedestal Error	R		1.0			9		mV
Power Supply Characteristics								
Positive Voltage	F	14.5	15	16		15		V
Negative Voltage	F	-14.5	-15	-16		-15		V
Positive Current	R		11	13		8.5	12.5	mA
Negative Current	R		-11	-13		-8.5	-12.5	mA
PSRR	F	-65	-75		-80	-90		dB

Table 1. Electrical Characteristics HA-5320 vs. HA-2420.

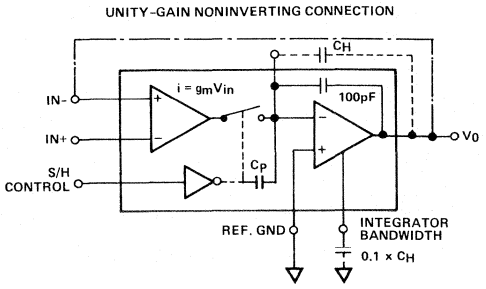


Figure 1B. HA-5320 Diagram

Understanding Pedestal Error

When a S/H amplifier is switched from Sample to Hold, its output voltage rarely matches the ideal value one would expect from a perfect device. Instead, it differs by a small ΔV of a few millivolts, even with a DC input applied. Called "Sample to hold offset" or "pedestal", this error has a predictable polarity and magnitude for given conditions.

In general, this error is affected by magnitude of the input voltage, magnitude of the digital control level V_{AH}, rise time of the logic transition, size of the hold capacitor and temperature. Most troublesome of these is the variation of pedestal with input voltage, and this effect has been completely eliminated in the HA-5320.

Pedestal error is caused by the injection of charge onto the hold capacitor from a digital input, through small values of parasitic capacitance. Injection can come directly from the S/H control input or from the internal switch action. In Figure 1A and 1B, the capacitance of a base-collector junction in the switching circuit is represented as Cp, which varies with base-collector voltage for the transistor. That voltage is constant for the HA-5320, since Cp connects to a virtual ground. Therefore, charge injection and the resulting pedestal error are not affected by changes in V_{IN}. (For the HA-2420 in Figure 1A, Cp varies with V_{IN} and produces a varying pedestal.)

Another source of injected charge is the S/H control signal. This coupling is virtually zero within the HA-5320 chip, but a packaged unit exhibits about one millivolt change in pedestal per volt change in TTL level. However, compensation in the chip has been adjusted for zero pedestal at the nominal TTL level of 3.5V.

Null the Pedestal

This may be accomplished by introducing an equal and opposite voltage at the output, using the Offset Adjust terminals as shown in Figure 2. Since pedestal error does not change with V_{IN}, it may be treated as a simple offset. Use of the Offset Adjust shifts the pedestal error to the Sample Mode though, which may cause problems in a few applications.

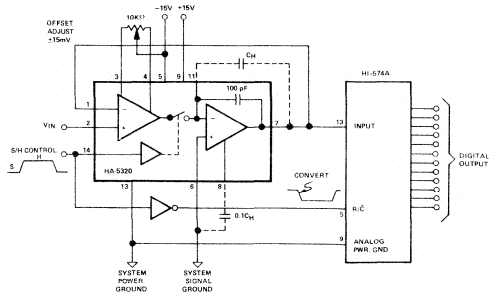
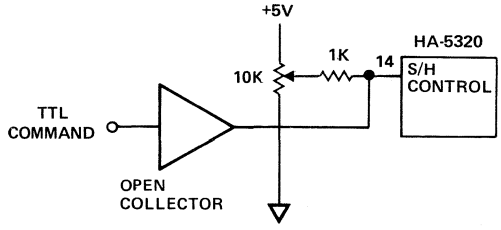


Figure 2. Signal Processing System

For these, one may make use of the relation between pedestal magnitude and the digital input level.

As mentioned earlier, the pedestal changes about one mV per volt of change in the digital "1" level, or V_{AH}. For small systems simply adjust V_{AH} until the pedestal is eliminated. In larger systems, the same adjustment may be made locally:



Understanding Droop Error

"Droop" is a change in output voltage vs. time while in the hold mode, caused by a flow of leakage current from the hold capacitor. For the HA-5320, this change is quite linear with time. The leakage current includes "off" leakage from the bipolar switch and bias current into the inverting input of the output integrator. The switch output consists of the joined collectors of two "off" transistors, NPN and PNP. These are tied to a JFET gate at the integrator input, so the hold capacitor looks at three leakage components, each of which doubles every 10°C. Ideally, these sum to zero and maintain a net zero leakage into the hold capacitor with changes in temperature. Effort has been made to achieve this. The JFET also produces less output noise than does the MOSFET used in the HA-2420.

An externally-supplied hold capacitor may provide other avenues for leakage current, but of course the HA-5320 does not require an external capacitor. Its 100pF internal hold capacitor is a guaranteed and factory-tested component. This eliminates the uncertainty associated with a user supplied com-

ponent, and also eliminates the selection, purchase, stocking, test and assembly of high quality hold capacitors.

The typical leakage (called "drift") current varies with temperature as shown in Figure 3. Then, droop error is directly related to drift current by the relation

$$V_{DROOP} = \frac{I_{DRIFT}\,\Delta t_H}{C_H}$$

where t_H is time in the hold mode. Using C_H=100pF and Δt_H = 25 μs, typical droop error may be calculated for a given temperature:

$$V_{DROOP} = \begin{array}{r} 1.25\,\mu V\ @ +\ 25^oC \\ 23.0\ \ \mu V\ @ +\ 75^oC \\ 425.0\ \ \mu V\ @ +125^oC \end{array}$$

This shows a typical droop error of less than 1/5 LSB in 12 bits at +125°C, for one of the major applications targeted for this device (input to a successive-approximation A/D converter with 25μs conversion time.)

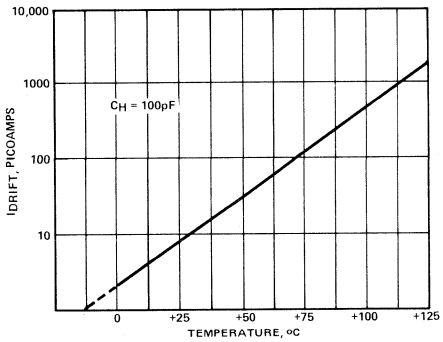


Figure 3. Hold Mode Drift Current v.s. Temperature

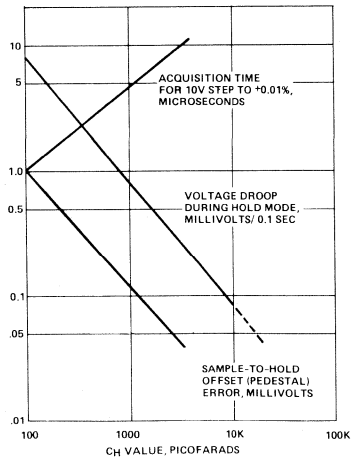


Figure 4. Typical Sample-and-Hold Performance v.s. Hold Capacitance

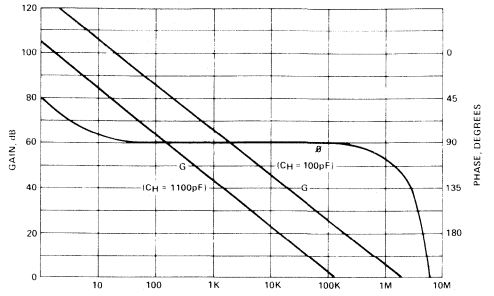


Figure 5. Open Loop Gain and Phase Response

Output Current

Up to ±20mA may flow without damage, but the guaranteed limit for normal operation is ±10mA. The design does not include short circuit protection; consequently output impedance remains low with increasing frequency. This is an advantage in Figure 2, where the S/H output sees step changes in load current as a conversion proceeds. The HA-5320 is able to absorb these current changes with only a small and brief (5mV, 100nS) perturbation in its output voltage. A higher output impedance would extend this transient toward the moment of decision by the converter's comparator, producing a degradation in digital output accuracy.

With power applied, avoid a momentary short of the HA-5320 output to any fixed potential such as ground or either supply.

Signal Processing Considerations

An analog signal may be digitized by a Sample/Hold-AD converter system such as the one shown in Figure 2. If required, the analog signal may then be reconstructed from that sequence of digital samples, using a D/A converter. One might ask, how does the sample/hold alone constrain this sampling process? That is, how high a frequency can be digitized to a given level of accuracy?

The HA-5320 imposes three types of limit on the highest signal frequency applied at its input. First, the analog channel in the Sample mode has a 2MHz small signal BW, and a 600KHz Full Power BW (20 Vpp input). Next, Aperture Uncertainty Time contributes a trade-off between accuracy and frequency. Finally, Acquisition Time places a ceiling on the maximum sample rate obtainable with a given A/D converter, according to:

$$MAX\ SR = \frac{1}{t_{ACQ} + t_{CONV}}$$

where t_{CONV} is the A/D converter's conversion time. (Input frequency must not exceed one half the Sample rate, unless the application is tolerant of "alias" errors).

For example, the typical HA-5320 Acquisition Time for a 10V step is:

Temp	Acquisition Time, t_{ACQ} ±0.1%	±0.01%
+25°C	0.8μs	1.0μs
+125°C	0.9μs	1.1μs

Thus a 25μs converter could generate approximately $(1\mu s + 25\mu s)^{-1} = 38{,}460$ samples per second, allowing input frequencies as high as 19.23 KHz under ideal conditions (a low noise signal source with abrupt bandlimiting).

In most applications though, a low pass "antialiasing" filter is required to bandlimit the HA-5320 input. This filter controls "alias" error by reducing the amplitude of all signals and noise at and above the Nyquist frequency (SR/2). A given accuracy requirement translates to a minimum attenuation at the Nyquist frequency, which is accomplished by increasing the sample rate and/or the filter complexity (# poles). Twelve bit (±1/2 LSB) accuracy for example, calls for a 5 pole filter and sampling at 11X the highest signal frequency of interest. Using 38.46KHz for Sample Rate, this limits the input frequency to 3500Hz (SR/11). If this seems low, bear in mind that 12 bits ±1/2LSB is a tight specification.

The HA-5320's Aperture Uncertainty Time also imposes a limit on input frequency, independent of that due to filter poles and sample rate. The relation is

$$f_{max} = \frac{1}{2^{n+1}\,\pi\,t_{AU}}$$

where t_{AU} is the aperture uncertainty and f_{max} is the highest frequency that can be sampled to ±1/2 LSB accuracy at n-bit resolution. Typical t_{AU} is 270ps for the HA-5320, leading to 143.9 KHz for f_{max} at 12 bits. That makes the HA-5320 compatible with some of the fastest 12 bit converters available today. Also, since f_{max} increases for lower resolution, the frequency limit based on aliasing will be encountered first in nearly all applications.

Another parameter of concern is feedthrough. After sampling a signal and holding it, how much of that signal will couple to the output and appear superimposed on the DC level there? At 100KHz, the answer is 1mVpp at the output, due to 10Vpp at the input. At 10KHz, the feedthrough is still -80dB indicating the coupling path is resistive over this range.

At lower frequencies, the feedthrough is less (better) than this, since the HA-5320 is designed for relatively short hold periods. For example, the 3500Hz limit mentioned above for a 12 bit, 25μs converter requires 285μs to complete one cycle. The HA-5320 will see only a small fraction of this input cycle during each hold period.

Op Amp Properties

Both the HA-5320 and HA-2420 behave like op amps in the sample mode, and may be treated as such-that is, external feedback may be connected to form filters, integrators, inverting and non-inverting amplifiers with gain, etc. This versatility is in contrast to many other designs in which the inverting input is internally connected, committing the device to the noninverting unity gain configuration.

Referring to Figure 1, it may be noted that the HA-5320 is even more like an op amp that the HA-2420. Where the HA-2420 input stage is a voltage amplifier (actually an op amp by itself), the HA-5320 input stage is a transconductance amplifier, producing an output current $g_m V_{IN}$. Also, the HA-5320 output stage is an integrator, analogous to the 2nd stage of a classical op amp. The hold capacitor corresponds to the op amp's compensation capacitor, through here the analogy falters. Like the op amp though, closed loop gain-bandwidth product for the HA-5320 may be predicted from the expression g_m/C_H.

Fabrication of the HA-5320 features the Harris high frequency dielectric isolation (DI) process, with front-diffused collectors and P-channel JFET's. This approach has yielded DC input characteristics which compare well with those of premium monolithic op amps. Typical Offset Voltage is 200μV at +25°C and only 2mV at +125°. Offset Current is guaranteed less than 100nA at +125°C, or half the value of Bias Current at that temperature. Common Mode Rejection is guaranteed 80dB minimum over the ±10V range, with 90dB typical.

The HA-5320 is very stable in the noninverting unity gain connection. Typical phase margin is 60° at an open loop unity gain frequency of about 2MHz.

As mentioned earlier, the addition of external hold capacitance has a direct affect on bandwidth. For example, adding 1000pF increases C_H from 100pF to 1100pF. As a result, the 2MHz unity gain bandwidth shrinks to (100/1100) 2MHz = 182KHz. This means more time must be allowed for acquisition for a new sample, but not in the same ratio: Acquisition Time to .01% increases from 1.0μs to only 8.7μs.

Figure 6 shows the response to a 10 volt step in the sample mode. The asymmetry from rise to fall time for slew rate and overshoot is common to all units.

Figure 7 shows some Sample/Hold characteristics for a small signal (10mVpp) input. The Sample to Hold settling time is less than 200ns-higher gain and sweep speed resolve this to about 160ns. Notice

the final overshoot is less than .01% (one millivolt). This response is the same for any signal level. Also, slew rate is proportional to the magnitude of an input step, yielding a fairly constant value for slewing time, regardless of the distance slewed. This produces about one microsecond of acquisition time for any step change exceeding small signal conditions. For the small signal input of Figure 7, however, acquisition time is about 400ns (no slewing).

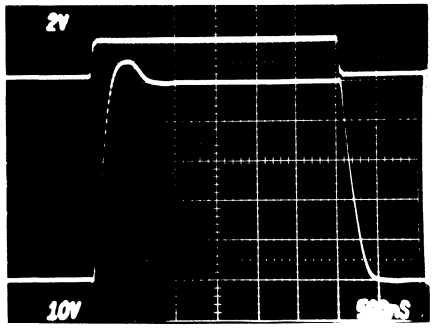


Figure 6. Step Response

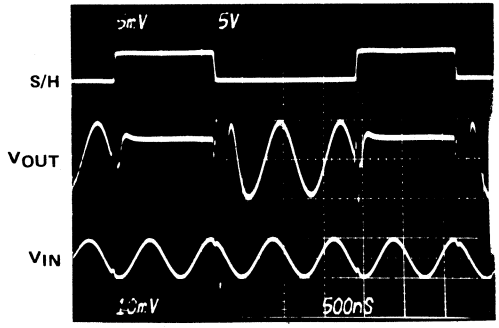


Figure 7. Small Signal Transient Response

Applications

A/D CONVERTER INPUT

An important application has been presented in Figure 2, in which the HA-5320 serves to reduce the aperture time of an A/D converter. More directly, the Sample/Hold "freezes" an instantaneous value of V_{IN} and holds it constant during the analog to digital conversion. In Table 2, f_{max} without a Sample/Hold is relatively low, since aperture time equals the HI-574A conversion time. Adding the HA-5320 substitues a much smaller aperture, which could allow an input frequency over 100KHz, but a lower limit is imposed by alias error effects. This limit depends on various conditions in the application, so the values listed for f_{max} (using the HA-5320) are only representative.

REQUIRED	HI-5712 CONVERSION TIME, MAX.	f_{MAX} (Vin) WITHOUT SAMPLE/HOLD	USING THE HA-5320		
			MAXIMUM SAMPLING RATE	f_{MAX} (Vin)	Min. # POLES, ANTI-ALIASING FILTER
8 BITS ±1/2LSB	7μS	88.8Hz	111KHz	24.8KHz	8
10 BITS ±1/2LSB	8.5μS	18.3Hz	95KHz	6.2KHz	3
12 BITS ±1/2LSB	10μS	3.9Hz	83KHz	1.5KHz	3

Table 2. Accuracy v.s. Maximum Input Frequency f_{max}

PEAK DETECTOR

An analog signal requires about 100ns to propagate through the HA-5320. For time varying signals, this assures a voltage difference between input and output. Also, the voltage changes polarity when the signal slope changes polarity (passes a peak). This behavior makes possible a Sample-Hold peak detector, by adding a comparator to detect the polarity changes.

In Figure 8 the exclusive NOR gate allows a reset function which forces the HA-5320 to the sample

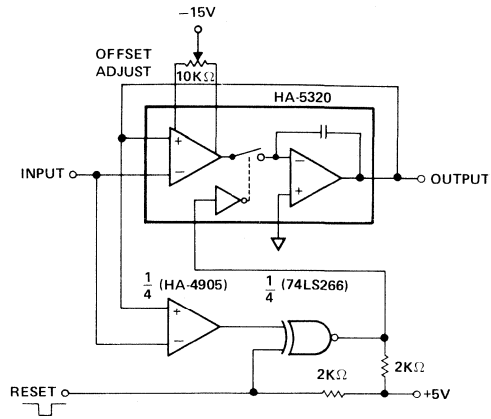


Figure 8. Positive Peak Detector

mode. The connections shown detect positive peaks; the comparator inputs may be reversed to detect negative peaks. Also, offset must be introduced to provide enough step in voltage to trip the comparator after passing a peak.

This circuit works well from below 100Hz up to the frequency at which slew rate limiting occurs. It captures the amplitude of voltage pulses, provided the pulse duration is sufficient for slewing to the top of the pulse.

The author wishes to thank design engineer Paul Hernandez and senior technician Roger O'Brien for their technical support.

A MONOLITHIC 16-BIT D/A CONVERTER

By Tarlton Fleming

Introduction

Close attention to second order error sources has produced a 16 bit monolithic current-output DAC whose performance over temperature surpasses all similar products available at this time. The HI-DAC 16B is a dielectrically-isolated, bipolar device offering typical differential and integral nonlinearities of +1/2LSB, +3/4LSB respectively at room temperature, increasing to double those limits (maximum) at +75°C. Current mode settling time is 1μs to ±.003% FSR. It carries forward a tradition among monolithic electronic components, in performing a function both at lower cost and with smaller size than most of its predecessors.

The prospect of an emerging market for digital audio equipment is driving the development of high-resolution converters within many semiconductor companies. All are anticipating a need for D/A converters in high volume, whose technical requirements are already well established (14 bit resolution and accuracy, monotonic from 0° to 70°, 1-2 μs settling time). Also, the aggressively low selling price of audio playback units dictates a monolithic IC component as the most promising solution.

HARRIS offering in this area was first announced at the 1982 International Solid State Circuits Conference in San Francisco. Called the HI-DAC16, its architecture is an extension of the earlier 12 bit HI-562, but with several significant innovations in circuit design and layout topology. The current result is solid performance at 15 bits. A sixteen bit accurate device is also under development. Since this performance exceeds the present requirements for playback of digital audio, the HI-DAC16 has targeted the markets for high resolution process control and precision instrumentation. It also promises a lower cost alternative for industrial weighing systems, automatic test equipment and high performance vector graphics, as well as digital audio. Performance is specified in Table 1 for the B and C grade units, which were introduced in March.

PARAMETER	MODEL HI-DAC16B	HI-DAC16C
Resolution	16 Bits	*
Unipolar Offset @ 25°C	±.002% FSR	*
0° =75°C	±.5ppm of FSR/°C	*
Integral Nonlinearity @ 25°C	±.0023% FSR	±.0045% FSR
0° -75°C	±.0045% FSR, Max	±.009% FSR, Max
Differential Nonlinearity	±.0015% FSR	±.003% FSR
0° - 75°C	±.003% FSR, Max	±.006% FSR, Max
Reference Input		
Voltage	10V	*
Resistance	10KΩ	*
Output		
Resistance	2.5KΩ	*
Capacitance	10pf	*
Settling Time (Full Scale Transition) Current Settling to ±.003%	1μsec	*
Noise at Output RMS ±1 0.1Hz to 5MHz	1/5 LSB	*
		*
		*
Power Supply Sensitivities		
Gain	85db or .8ppm/%	*
Differential Nonlinearity	95db or .3ppm/%	*
Power Dissipation	465mW	*

Table 1

To appreciate the challenge posed by a 16 bit converter, consider that an LSB is only 153μV, based on a 10V full scale voltage output. Similarly for current outputs, the nominal 2mA full scale sets an LSB at only 30.5 nanoamps. One must be very careful in handling these small increments of signal to avoid losing them among the offsets, noise and bias currents normally present in a system application.

For example, the analog ground connection to a conventional switched current source DAC contains code-dependent currents varying from zero to 2mA or more. Flowing through 6 inches of a typical 40 mil wide printed circuit trace, these currents produce an IR drop of 66 micro volts — nearly 1/2 LSB in a 16 bit system.

The HI-DAC16 eliminates this problem by supplying the ground current from within the chip. This allows its analog ground terminal to sense the system ground at any reasonable distance, without an IR drop.

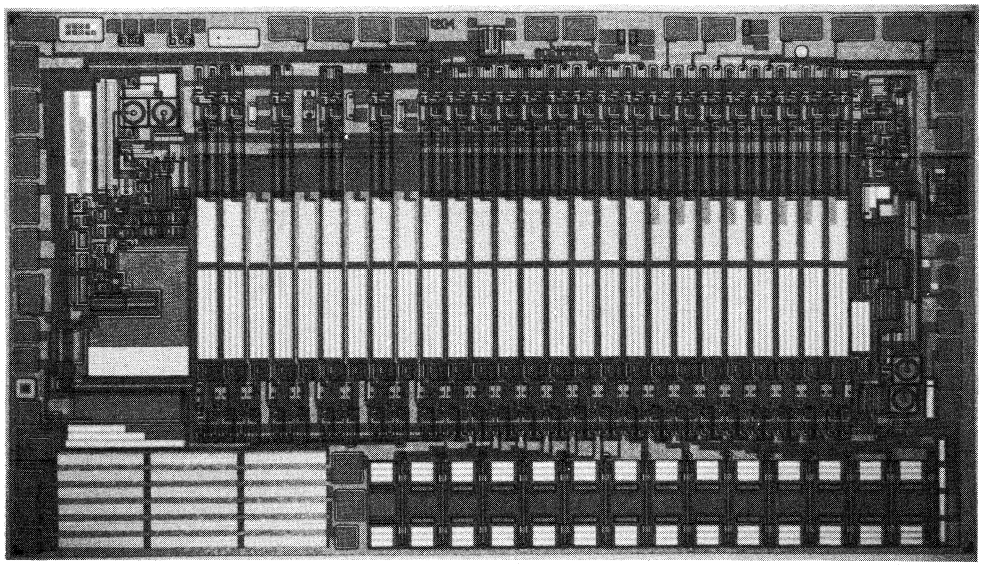


Figure 1.

Photomicrograph of the HI-DAC16. Digital-to-Analog Converter circuit combines dielectrically isolated bipolar technology with nichrome thinfilm resistors.

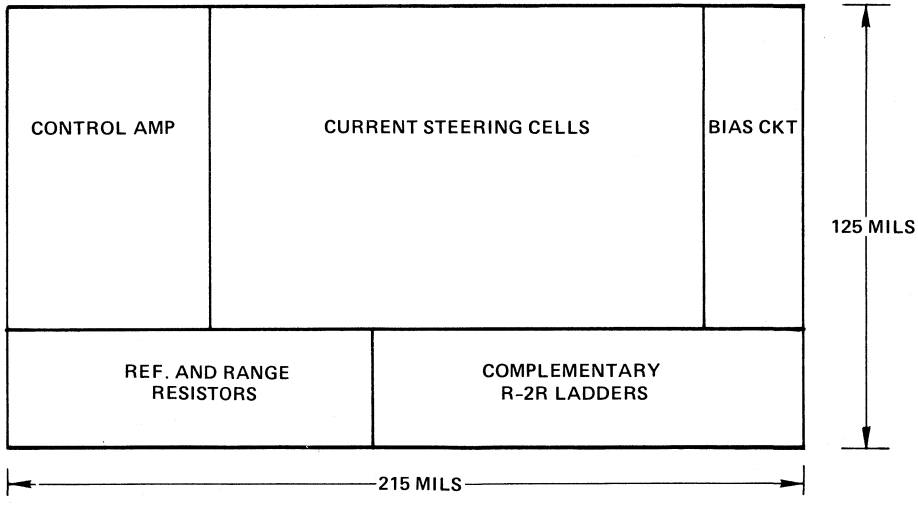


Figure 2.
Chip Diagram

Basic Facts

The HI-DAC16 operates on ±15V , with 456mW typical power dissipation. Package is a 40 pin side braze DIP. The 16 digital inputs accept a TTL compatible Straight Binary code word , and the nominal full scale current output is 2mA. An external +10V reference must be supplied. See Figures 1 and 2 for the chip layout and location of functions.

As shown in Figure 3, an onboard thin-film resistor provides a one-half scale offset for the bipolar ranges. Two more span resistors provide feedback around an external op amp to establish any of the standard ranges of output voltage: +5V, +10V, ±2.5V, ±5V and ±10V.

To minimize offset error due to the op amp's input bias currents, each amplifier input should see the same source resistance. An additional onboard resistor network may be connected to the amplifier's noninverting input to provide this matching for three of the five output ranges.

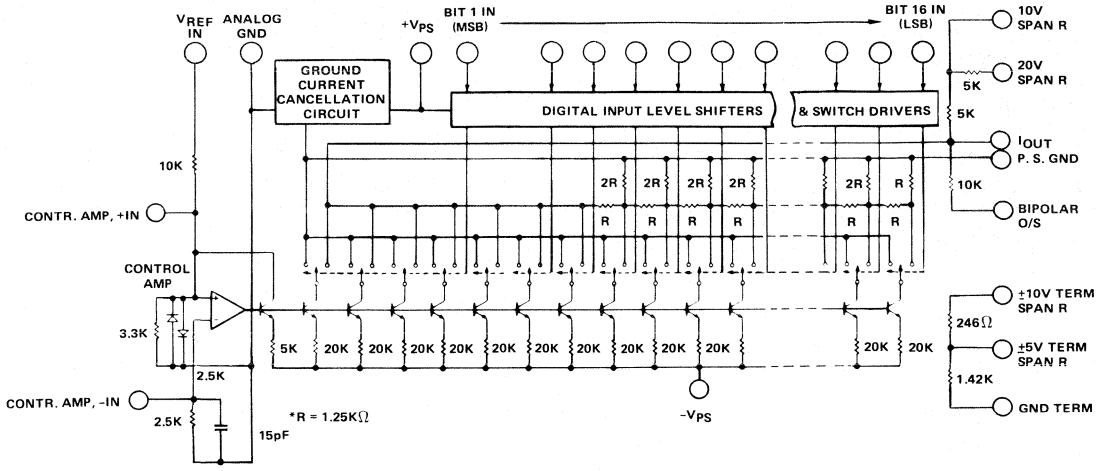


Figure 3.

Simplified Functional Diagram of the HI-DAC16. Details of the ground current cancellation circuit are in Figure 4.

A Look At Design Details

Internal cancellation of ground current is one of the HI-DAC16's most significant improvements. It simplifies application of the device by reducing current in the analog ground terminal nearly to zero. DC offset voltage between the package and system ground is eliminated, and dynamic code-dependent current variations are contained within the chip.

Refer to Figure 4. The chip includes two identical thin film R-2R ladders, deposited with physical symmetry about a common analog ground bus. The main ladder generates output current I_O for the lower 13 bits.

The auxiliary ladder is driven by a complement of the DAC's input code, so the two ladders together draw a constant 3mA from the internal analog ground regardless of input code. (The auxiliary ladder generates a complementary current $\overline{I_O}$ which is dumped into the non-critical power ground.) The nominal three milliamps is supplied internally from the positive power supply, via a current mirror driven by a 0.5mA current source. Net current through the external analog ground is zero. Further, this null condition is maintained with variations in temperature and reference voltage, since the current source is driven by the control amplifier.

To accomplish binary weighting of the sixteen bit currents, identical current cells are employed, each with a 250μA sink and a differential transistor pair used as a two position bipolar switch. For the three MSB's, cell currents are switched either to I_O or power ground. For the remaining 13 bits, binary currents are obtained from an R-2R ladder.

Four cells are switched in tandem for the MSB; two for bit 2 and one for bit 3. In all, 20 cells mirror current from a set of four reference cells, with all 24 driven by an onboard control amplifier and the reference voltage. The resulting transfer function is:

$$I_O = \frac{V_{REF}}{4R_{REF}}\left(4B_1 + 2B_2 + B_3 + \frac{B_4}{2} + \frac{B_5}{4} + \frac{B_6}{8} + \ldots\ldots + \frac{B_{16}}{213}\right)$$

. . . . where B_1 through B_{16} are logical values for the sixteen digital inputs, ie. either "1" or "0".

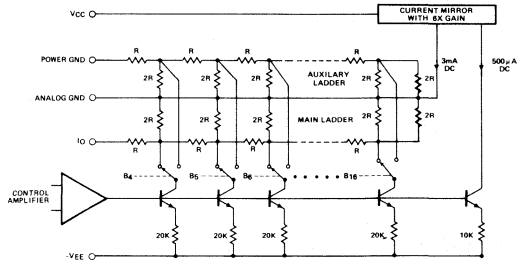


Figure 4.

Ground Current Cancellation. The auxiliary ladder adds complementary current to Analog Ground, to eliminate variations due to input code changes. The resulting DC current is then supplied internally from V_{CC}.

Several measures have been taken to counteract the linearity errors produced by any slight mismatch in cell currents or non-ideal tracking of the composite reference cell. First, the four reference calls are physically positioned among the cells of the first three MSB's in a pattern which minimizes tracking errors. Although close matching is assured by the control of process parameters and the careful matching of resistor and transistor geometries, small errors arise due to thermal gradients and IR drops in the negative supply bus. This bus is configured as a tree rather than a single wide conductor, to minimize the impact of IR drops and their change with temperature. Further, cell matching is enhanced by operation of all cells at the same current, which establishes a uniform power dissipation across the cell array.

"Superposition error" is another aberration in the transfer function of D/A converters, in which the voltage output for a given code does not exactly agree with the sum of those bits if they are turned on one at a time. Small IR drops in the ground line can cause this; as can a slight change in value of the onboard span resistor. Small changes are produced by self heating due to the flow of feedback current from the op amp. This effect is nonlinear with current and may be calibrated to zero at full scale, yielding a maximum error for outputs near 0.6 of full scale.

In the HI-DAC16, however, superposition error is hardly measureable. Ground current has been cancelled, eliminating that error component. To minimize the effect of self heating, the reference resistor is located between the two span resistors to provide a tight thermal coupling among the three. The ratio of reference to span value is only 2:1, using identical geometries, so a temperature change in either span quickly produces a similar effect in the reference resistor. However, a change in the reference produces an opposite effect on the output. The net effect is a first order cancellation of superposition error.

Settling Time-A Challenging Measurement

This measurement is routine at 8 bit resolution and challenging at 12 bits, but at 14 bits it pushes the limit of currently available techniques. As mentioned earlier, typical full scale settling for the HI-DAC16's current output is one microsecond (to ±0.003% of full scale which is ±1/2 LSB at 14 bits). Although the time interval is only moderately fast, it is difficult to measure the ±1/2LSB window at high resolution.

The method in use at Harris Analog Division simulates the conditions seen by a DAC when used in a successive approximation A/D converter. A strobed comparator (The HA-4950) is used to sense the DAC output with respect to a ±1/2LSB window about the final settled value. At 14 bits, the comparator operates reliably (HI-DAC16 provides 203μ V for the LSB in this setup) but at higher resolution the smaller LSB doesn't provide enough overdrive. These measurements will require either a better comparator or a different test method.

For the voltage output case, the LSB is large enough at a given resolution to ease the problem. Also, the settling time is longer. If the amplifier settles in t_a, the DAC in t_d and the measured value for the combination is t_m, then $t_d = \sqrt{t_m^2 - t_a^2}$, provided the amplifier has a single pole response.

Voltage Output-Any Old Op Amp Won't Do

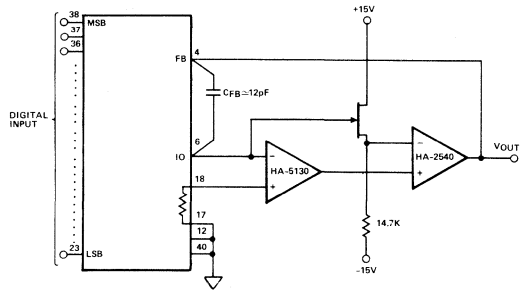


Figure 5.

Composite amplifier provides fast, accurate conversion of output current to voltage.

The HI-DAC16 imposes strenuous demands on its output current-to-voltage amplifier. Amplifier offset voltage adds error to its voltage output; input bias current adds error to the DAC output current; and finite open loop gain introduces gain error. These errors can be compensated by the calibration of offset and gain, but some error will reappear as temperature varies. A precision op amp like the HA-5130 contributes so little DC error that no calibration is required in most cases. It's not fast enough though, for high rates of update at the DAC input. HA-5130 settling time is rated 11μs, just to settle within ±0.1% (for a 10V step, slewing at 0.8V/μS).

Other op amps with different compromises in speed and accuracy may be chosen, but no single monolithic op amp can meet all these requirements:

Input Bias Current	3nA
Input Offset Voltage	15μV
Large Signal Voltage Gain	10^6
Settling Time to $\pm$0.003%	2μs
Unity Gain Stable	

However, a composite based on two monolithic op amps can offer that performance at reasonable cost. The basic connections are shown in Figure 5.

In this arrangement the HA-5130 contributes low input bias current, low offset voltage and high open loop gain, while the HA-2540 contributes high slew rate, wide bandwidth and fast settling. The JFET buffers the HA-2540's input bias current, and C_{FB} may be selected to optimize settling time.

Data Bus Interface

In general, a D/A converter is more readily connected to a digital data bus than its counterpart, the A/D converter. The interface is especially straightforward if the DAC input and data bus have the same width (in number of bits).

Figure 6 for example, shows the HI-DAC16 providing an analog output from the 16 bit data bus of an 8086 system. The DAC is updated with every coincidence of the M/$\overline{IO}$ and $\overline{WR}$ signals and a proper address. Low Power Schottky TTL latches are recommended for minimal time skew in the arrival of individual bit signals. This in turn, minimizes glitch energy in the DAC output during code changes.

Interfacing the HI-DAC16 to an 8 bit data bus simply requires the microprocessor to write two consecutive bytes to the DAC input. Unless some form of double buffering is employed, however, the DAC output will assume an unwanted intermediate state during the interval between application of the first byte and arrival of the second. This problem is eliminated in Figure 7 with a few additional ICs.

In Figure 7, the HI-DAC16 is connected to a generalized 8 bit system. The Address Decode Logic produces exclusive low states on Q_1, then on Q_2, for two consecutive addresses. These two decoded address signals are gated with "Address Valid" and "Write" from the microprocessor to produce clock inputs for the latches. As a result, the first (and least significant) byte is latched into FF1, then both bytes are fed to the DAC input simultaneously via FF2 and FF3.

The programmable interface devices available in most microprocessor component families are not "double-buffered" and so offer little advantage for interface to the HI-DAC16. The circuits of Figures 6 and 7 are more direct and less expensive. Also, digital feedthrough to the DAC's analog output can be a problem when interface circuitry is included on the DAC chip. For the HI-DAC16, external gates and latches provide a barrier to shut out this digital noise from the microprocessor.

The author wishes to thank design engineer, Tom Guy, for technical advice in support of this article.

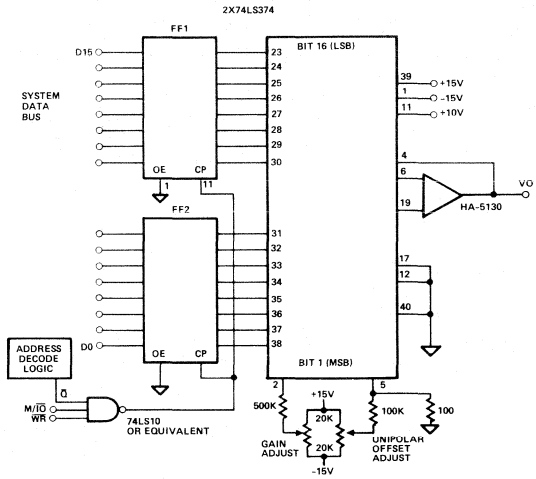


Figure 6.

Interface for a 16 bit DAC and 16 bit data bus (8086 system, minimum mode): New data is latched to the DAC input following a simultaneous low on each input to the NAND gate. The latches are strobed when $\overline{WR}$ returns high.

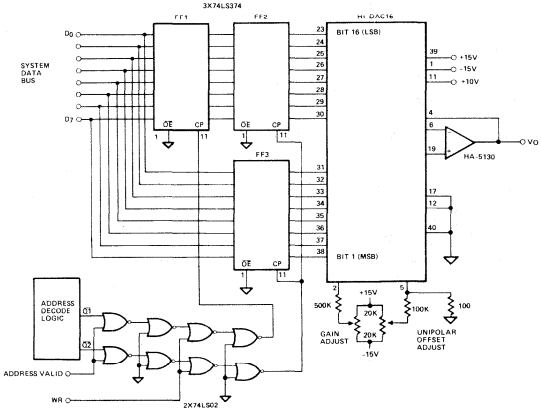


Figure 7.

An 8 bit data bus feeds a 16 bit DAC through this simple interface. The address for the least significant byte produces Q_1. Coincidence of Q_1, ADDRESS VALID and WR Clocks this first byte into FF1. Similarly, the second byte produces Q_2 which results in a strobe to FF2 and FF3, applying both bytes to the DAC input simultaneously.

APP NOTE

FOR YOUR INFORMATION

No. 540

Harris Analog

HA-5170 PRECISION LOW NOISE JFET INPUT OPERATIONAL AMPLIFIER

By J. S. Prentice and R. W. Leath

Introduction

The HA-5170 is a precision, JFET input, operational amplifier which features low noise (12 nV/$\sqrt{Hz}$ at 1kHz), low offset voltage (100 μ V), low offset voltage drift (3 μ V/^{o}C), and low bias currents (20pA). Complementing these excellent input characteristics are dynamic performance characteristics never before available from precision operational amplifiers. An 8V/μs slew rate, 5MHz bandwidth and fast settling times less than 1.5 μs (settling to 0.01%) make the HA-5170 well suited for fast, precision A/D or D/A converter designs, precision sample and holds, precision integrators, or transducer signal amplifier designs.

Inside the HA-5170

The Harris technology has two important advantages. First, a unique ion implant process produces JFET's with excellent matching and low 1/f noise. Second, the JFET's are in their own dielectrically isolated islands which completely eliminates the largest gate current component – the island to substrate leakage.

The HA-5170 has two voltage gain stages. The first consists of a differential JFET pair with resistor loads which develops a gain of 10. The second is a complete bipolar op amp with a gain of 30K. The absence of active loads in the first stage insures that the offset voltage, offset voltage drift and noise voltage result exclusively from the input JFET pair.

When it comes to building low noise JFET componets, bigger is better. The JFET input noise voltage, both the 1/f and white componets, is inversely proportional to the square root of the gate area. Likewise, the input noise voltage due to the drain load resistors is inversely proportional to the square root of the resistance value. The JFET's "weigh in" at a whooping 110 mil^2 gate area with the resistors at 14kΩ. This results in typical noise voltages of 12nV/$\sqrt{Hz}$ at 1kHz, 25nV/$\sqrt{Hz}$ at 10Hz and 1 μ V p-p over the 0.1 to 10Hz frequency band.

Trimming the offset voltage of a JFET op amp usually degrades the offset voltage temperature coefficient, so a trim scheme that simultaneously nulls both the offset voltage and offset voltage temperature drift was developed. The dominant JFET mismatches arise from mismatches in the channel height and doping profiles, not photolithography errors. It is not surprising that the V_P mismatches correlate with the I_{DSS} mismatches.

The amplifier offset voltage is given by

$$V_{OS} = \Delta V_P \left(1 - \sqrt{\frac{I_{DS}}{I_{DSS}}}\right) + \frac{V_P}{2}\sqrt{\frac{I_{DS}}{I_{DSS}}}\left(\frac{\Delta I_{DSS}}{I_{DSS}} - \frac{\Delta I_{DS}}{I_{DS}}\right)$$

In this circuit, the mismatch of the drain load resistor sets the JFET drain current mismatch.

$$\frac{\Delta I_{DS}}{I_{DS}} = -\frac{\Delta R}{R}$$

Thus, the offset voltage can be zeroed by trimming the load resistors. Since V_P has a large positive temperature coefficient, the offset voltage drift is normally degraded. By making the loads from composite resistors, thin film resistors in series with diffused resistors, the temperature coefficient of the Δ R/R ratio can be set to cancel both the trimming induced drift and also the JFET mismatch induce drift. This makes the HA-5170 the first JFET op amp in which trimming the offset voltage simultaneously trims the offset temperature drift. Furthermore, the offset voltage drift is reduced to even lower values when the offset voltage is nulled externally with an offset adjustment pot. The 5170 has a typical offset voltage of 100 μ V, offset drift of 3 μ V/^{o}C (without external offset nulling), and warm-up drift of only 20 μV.

The excellent dc performance of the HA-5170 is complemented with dynamic A.C. performance never before available from precision operational amplifiers. The 8V/μs slew rate and 5MHz bandwidth allow the designer to extend precision instrumentation applications in both speed and bandwidth. The fast settling time of the HA-5170 (typically less than

1.5μs, settling to 0.01%) also makes it well suited for fast precision A/D and D/A converter designs.

Applications

Several applications which utilize the design features and excellent performance of the HA-5170 are described below.

Single Op Amp Instumentation Amplifier

The HA-5170 may be used as a single op amp instrumentation amplifier because of a unique design feature which places the offset adjust terminals at the juncture of two differential gain stages. The instrumentation amplifier, as shown in Fig. 1, is very simple and provides good performance features such as low noise, low offset voltage, low offset voltage drift and high input impedance at low cost.

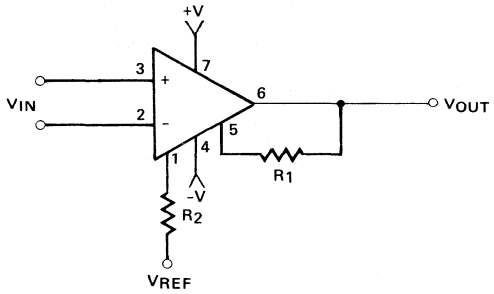


Figure 1. Single Op Amp Instrumentation Amplifier

The gain of the first differential stage is internally fixed at a gain approximately equal to 12. A feedback resistor R_1 connected between the output (Pin 6) and the balance pin (Pin 5) will close the loop around the second differential stage and set its gain. The closed loop gain of the instrumentation amplifier varies directly with the value of R_1 and is approximately

$$A_{VCL} = 12.5\ V/V/k\Omega$$

The minimum gain which can be applied is about 125 ($R_1 = R_2 = 10k\Omega$) because the current into pins 1 or 5 must be limited to 4mA.

The second resistor (R_2, which is connected between Pin 1 and a reference voltage) is used to establish a reference voltage level for the output. This reference voltage may be placed at ground potential or may be variable for use as offset adjustment. The resistor R_2 should also be matched with R_1 in order to maintain high common mode and power supply rejection ratios. Standard 1% tolerance resistors will typically provide 90dB rejection ratios.

The two inputs of the HA-5170, pins 2 and 3, may now be used as high impedance, true differential inputs with a common mode range of $-V_{supply}+3V$ to $+V_{supply}+0.1V$. If resistor values $R_1 = R_2 = 16k\Omega$ are used, for example, this circuit will provide a closed loop gain of 200 with a 3dB bandwidth of 20kHz and a THD $< 0.5\%$ ($V_{out} = 2V_{p-p}$). The gain linearity is typically better than 0.2%. However, the gain also changes about 0.2%/V with both common mode and power supply voltages. The gain T.C. is around 450ppm/°C but this can be reduced to less than 200ppm/°C just by using carbon film resistors which normally have negative T.C.'s (approximately 260ppm/°C for $16k\Omega$ resistors). Of course using resistors which have negative T.C.'s near 450ppm/°C will cancel gain T.C.'s altogether. If a variable gain is desired, a trim pot (in addition to R_1 and R_2) may be placed between the offset adjust pins. Resistors R_1 and R_2 and the maximum value of the trim pot will set the minimum gain. As the resistance of the trim pot is decreased, the gain will increase proportionally to the inverse of the trim pot resistance. This relationship of gain and trim pot resistance is shown in Fig. 2.

This circuit also maintains all the HA-5170's excellent A.C. and D.C. characteristics such as low offset voltage, low offset voltage drift, low noise, and high gain.

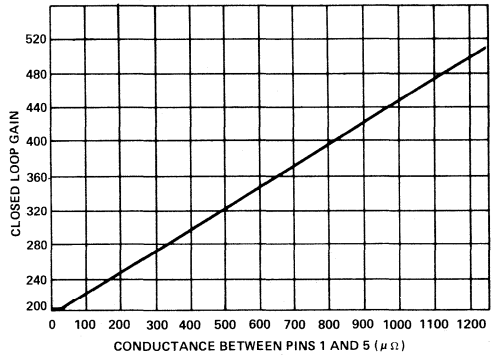


Figure 2. Closed Loop Gain Vs. Conductance Of Trimpot

Sine Wave Oscillator

The instrumentation amplifier circuit described above can be easily modified to produce a low distortion sine wave oscillator with voltage controlled amplitude as shown in Fig. 3. The small changes in gain of the instrumentation amplifier that occur with changes in common mode voltage has been exploited here to provide oscillator amplitude control with a voltage source. Another unique feature of this circuit is that is does not require any of the nonlinear components that most other sine wave oscillators require.

The phase lead network, which consist of R_3, R_4, and C_1, cancel the phase lag through the amplifier and oscillation occurs at the frequency where the product of amplifier gain and voltage feedback ex-

actly equals one. The amplifier gain is expressed as

$$A_V = \frac{A}{(1 + j\omega/\omega_o)}$$

where A is the dc gain (about 125 for $R_1 = R_2 = 10k\Omega$), ω_o is the bandwidth (about 200K rad/s) and ω is the frequency of oscillation. The voltage feedback is expressed as

$$\frac{j\omega C_1 R_4}{[1 + j\omega C_1 (R_3 + R_4)]}$$

For their product to be equal to one, both of the following must be true:

$$\omega = \frac{\omega_o}{[C_1 (R_3 + R_4)]}$$

$$AC_1R_4 = C_1 (R_3 + R_4) + \frac{1}{\omega_o}$$

The oscillation amplitude is stabilized at the point where the loop gain is equal to one by the small gain nonlinearity of the instrumentation amplifier.

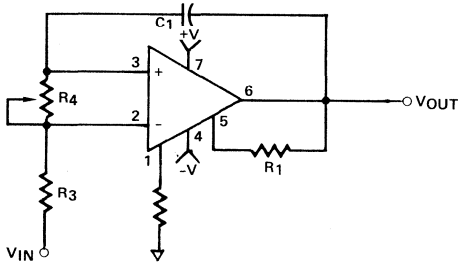


Figure 3. Sine Wave Oscillator With Voltage Controlled Amplititude

This operating point and initial amplitude is set by the resistor divider network of R_3 and trim pot R_4 ($R_4 \ll R_3$). The amplitude can then be varied by applying a common mode voltage (V_{IN}) through R_3. Positive common mode voltages increase amplitude by decreasing gain non-linearity while negative common mode voltages decrease amplitude. A typical curve of amplitude versus common mode voltage is shown in Figure 4. The gain non-linearity of the instrumentation amplifier is small, however, and distortion less than 0.5% can be obtained over a 100Hz to 100kHz range.

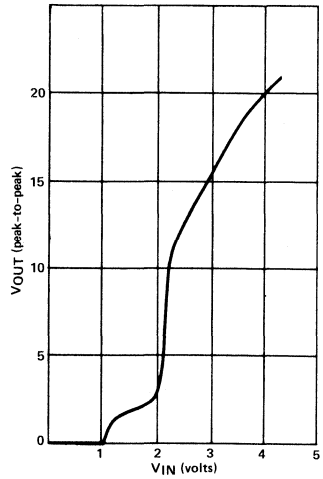


Figure 4. Oscillation Amplitude Vs. V_{IN}

Frequencies down to 10Hz can be achieved by lowering ω_o with a capacitor in parallel with R_1.

High Impedance Transducers

The HA-5170 is well suited as a preamplifier for high impedance transducers, such as photo diodes and hydrophones, because of its high input impedance and low current noise. Fig. 5 shows a photo diode preamplifier circuit whose output voltage is approximately the photo diode current times the value of R_1. When no light is present, the output of the HA-5170 is

$$V_O = I_{ND} R_1 + I_N R_1 + V_{NR} + V_N$$

where I_{ND} = Shot noise of diode
I_N = Noise current of Op Amp
V_{NR} = Noise voltage of resistor
V_N = Noise voltage of Op Amp

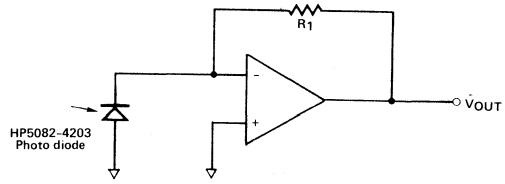


Figure 5. Photodiode Preamplifier

The signal to noise ratio is maximized when the rms sum of op amp and resistor noise current sources is equal to or lower than the noise current of the photo diode. Noise voltage sources are converted to noise current sources by dividing by R_1. The noise current of the photo diode may be approximated by the shot noise formula $2qI_d$, where I_d is the dark current, and is in the range of 10^{-13} to 10^{-14} A/$\sqrt{Hz}$, depending upon the choice of photo diodes. The rms sum of the three sources is approximately 4×10^{-14} A/$\sqrt{Hz}$ at 1kHz, assuming $R_1 = 20M\Omega$. This rms summation is approximately the same magnitude as the noise current of the photo diode with the dominant noise source being the resistor noise (about 2.9×10^{-14} A/$\sqrt{Hz}$). If a bipolar op amp were used instead of the HA-5170, the noise current (typ. 4×10^{-13} A/$\sqrt{Hz}$) would be much higher than the noise current of the photo diode. The response time of the photo diode can be improved by applying 5 to 20 volts of reverse bias but the increased speed is achieved at the expense of higher shot noise.

A resistor equal to the feedback resistor could be inserted between the non-inverting input and ground to reduce offset voltage. This is usually not necessary since the output offset voltage would only be 600μV for a 20MΩ resistor.

Fig. 6 shows a hydrophone preamplifier with a 100Hz to 100kHz bandwith and a gain of 100. Since hydrophone impedance is capacitive, it should be bypassed with a large bleeder resistor to shunt the bias currents to ground.

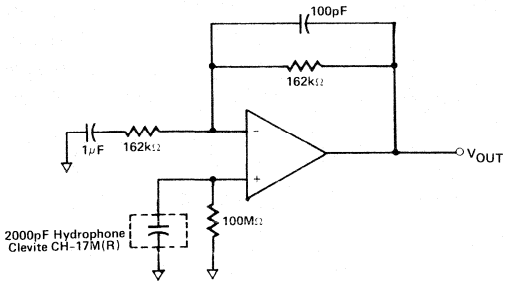


Figure 6. Hydrophone Preamplifier

Current Source/Sink and Current Sense Circuits

The HA-5170 can be used as a well regulated, two terminal, constant current source or sink, as shown in Fig. 7, or as a current sense amplifier, as shown in Fig. 8. These circuits take advantage of FET inputs' capability to accept a common mode voltage up to 0.1V above the positive supply.

The current from the constant current source consists of amplifier supply current and load current through R_2, both of which pass through the sense resistor R_1. The amplifier output will sink just enough current to cause the IR drop across R_1 to equal the amplifier offset voltage. This offset voltage may be adjusted by the trim pot R_3 and typically has a minimum adjustment range of 6mV. Smaller offset voltages give better power supply rejection ratios and usually give better results. The amplifier supply current, typ. 1.8mA, sets the minimum constant current while the amplifier short circuit protection limits the maximum to 15mA. Current regulation better than 0.08%/V and temperature variations better than 0.08%/°C can be achieved with this design.

Two operating constraints should be observed for best results. The resistor R_1 should be selected so that the amplifier output voltage remains at least 1.3V from either supply pin and the total voltage across pins 4 and 7 should be at least 12V but not over 40V.

The HA-5170 may also be used as a simple current sense amplifier in power supply applications. In this circuit, the power supply current develops a small voltage drop across the sense resisitor (R_S in Fig. 8) and the ammeter will display a current which is equal to $I_S \times \frac{R_S}{R_1}$. Of course the HA-5170 could also be placed in an open loop (comparator) configuration in which case the output would "trip" when the IR drop across R_S exceeds the offset voltage. This "trip" point can be controlled by an offset adiust trim pot connected as shown. The low noise, low offset voltage, and low bias current characteristics of the HA-5170 provide accurate measurement of supply current with very few components and can operate over a supply range of 7 to 40V.

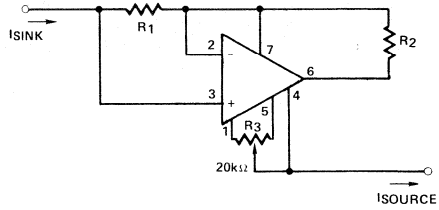


Figure 7. Two Terminal Constant Current Source/Sink

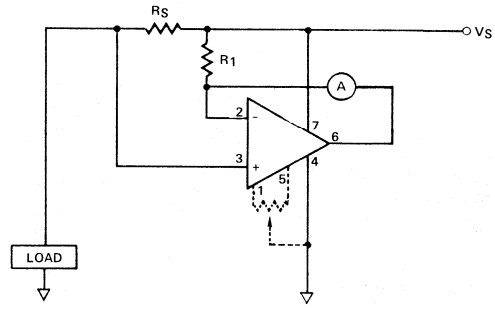


Figure 8. Current Sense Amplifier

APP NOTE

FOR YOUR INFORMATION

No. 541

Harris Analog

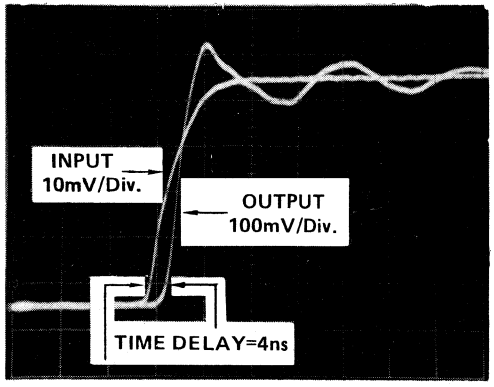
USING HA-2539 OR HA-2540 VERY HIGH SLEW RATE, WIDEBAND OPERATIONAL AMPLIFIERS

By: Richard Whitehead

Introduction

With the superior dynamic performance available from the HA-2539 and HA-2540, a wide variety of applications can be "idealized". From high fidelity audio to television broadcast and receiving equipment these operational amplifiers can be used to provide increased system capabilities. Employing the Harris High Frequency Dielectric Isolation Process, the HA-2539 with true differential input devices offer 600V/μs slew rate coupled with 600MHz gain bandwidth product. These outstanding AC parameters in conjunction with an excellent time delay of 4ns (see photo), standardize HA-2539 in critical wideband video and RF applications.

The HA-2540 is very similiar in design with the HA-2539, except for the addition of some small internal compensation (approximately 7pF). It offers a 400V/μs slew rate and a 400MHz gain-bandwidth product. The pinout of the HA-2540 uses the familiar 14 lead DIP pinout of other Harris wideband amplifiers.



HA-2539 TRANSIENT RESPONSE WAVEFORMS

Prototyping With HA-2539 or HA-2540

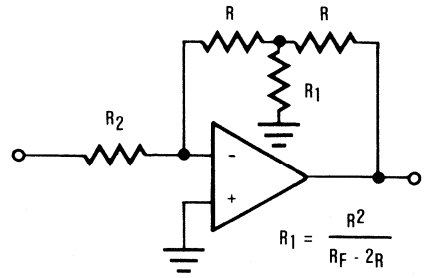
Being a "true" operational amplifier, HA-2539 or HA-2540 may be "designed in" using conventional high frequency amplifier techniques. Quality I.C. sockets may be used, but for maximized dynamic performance it is suggested these devices be mounted through a ground plane. External components should have minimal lead lengths and perferably connected directly to the device pins. Metal film or metal oxide resistors are recommended for feedback components. If direct connection is not possible, Teflon insulated standoffs should be used with locations as close as possible to device pins. Power supply decoupling with .001μF ceramic capacitors from the device supply pins to ground is essential. Alternatively, filter connectors such as Erie 1201-052 are suggested for optimum decoupling.

For best high frequency performance, feedback resistor values should be restricted to minimal values. Values below 5KΩ are recommended to reduce possibilities of introducing unwanted poles into the applications transfer function. Figure 1 indicates how high values for closed loop gain can be implemented, while maintaining feedback element values. This method is called "T network" feedback and values for the resistors can be derived from the following expression.

$$R_1 = \frac{R2}{R_f - 2R}$$

Where:

Rf is the value of feedback resistance to be reduced and R is a value preselected by the designer.



WHERE R IS PRESELECTED AND R_F
IS DESIRED FEEDBACK RESISTOR VALUE

FIGURE 1. KEEPING FEEDBACK VALUES LOW

The HA-2539 and HA-2540 may be used without heat sinks up to +75°C ambient. Power derating above this temperature is 9.6mW/°C and heat sinking is recommended. Thermalloy model 6007, Unitrack CPU 1017, or AAVID 5602B heat sinks are suggested for temperatures up to+125°C ambient. Also refer to Application Note 556 for further Safe-Operating-Area information.

General Operating Considerations

Dynamic performance of the HA-2539 and HA-2540 were maximized through the exclusion of output short circuit protection and internal offset voltage adjustment circuitry.

Although these amplifiers can withstand momentary short circuits to ground, it is recommended that some output current limiting network be used, if the operating environment is hostile. Figure 2 shows a suggested method for output terminal protection.

Offset voltage adjustment may be accomplished by the suggested methods shown in Figure 3 (a) and (b).

As with many wideband, high speed devices, recovery from output saturation can be in the order of microseconds. HA-2539 and HA-2540's saturation recovery from its positive rail is of the classical variety where voltage charges on the "body" capacitance of output devices must discharge before normal operation can be resumed. Recovery from the negative rail is similar to the positive rail recovery except during saturation small signal oscillation may occur. This oscillation is due mainly to a regenerative signal coupled back to the input during saturation.

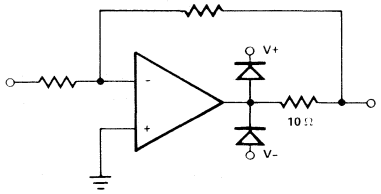
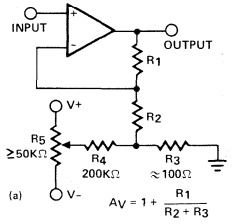
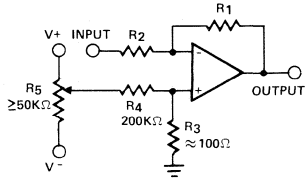


FIGURE 2. OUTPUT PROTECTION FROM FAULT CONDITIONS FOR HA-2539 & HA-2540



3a.



3b. $A_V = -\frac{R_1}{R_2}$

FIGURE 3. OFFSET NULLING FOR HA-2539 AND HA-2540

Range of Adjustment for Both Non-Inverting (Top) and Inverting Amplifiers (Bottom) Determined by Product of V_{SUPPLY} and R_3/R_4 Ratio.

General Applications

FREQUENCY COMPENSATION

HA-2539 and HA-2540 are stable in standard operational amplifier circuits with closed loop gains exceeding +10 or -9. Keeping the network resistor values and source resistance as low as practical in these configurations should optimize the dynamic performance.

Circuit configurations shown in Figure 4 may be used to stabilize the HA-2539 or HA-2540 at closed loop gains less than specified. Figure 4(a) employs capacitance to over damp the amplifiers' response. Stable operation to gains of 5 are practical. Figure 4(b) utilizes the amplifier's differential input impedance to reduce input and feedback signals thereby raising noise gain to a stable point on the response curve. Gains of -3 are practical.

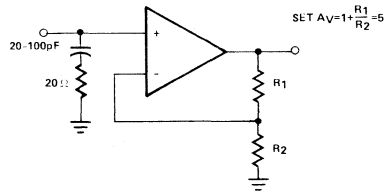


FIGURE 4a. COMPENSATION BY OVERDAMPING

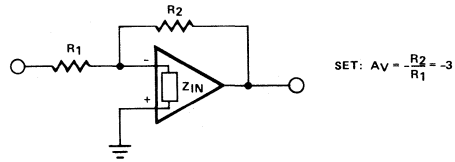


FIGURE 4b. STABILIZATION USING Z_{IN}

Reducing DC Errors

A composite amplifier scheme may be used to reduce errors due to offset voltage and bias current. Figure 5 shows HA-2539 and HA-5170 in a composite configuration which greatly reduces DC errors without compromising the high speed, wideband characteristics of HA-2539. The HA-2540 could also be used, but with slightly lower speeds and bandwidth response.

The HA-2539 amplifies signals above 40KHz which are fed forward via C_2 and R_2. Resistors R_4 and R_5 set the voltage gain at -10. The slew rate of this circuit was measured at 350V/μs. Settling time to a 0.1% level for a 10V output step is under 150ns and the gain bandwidth product is 300MHz.

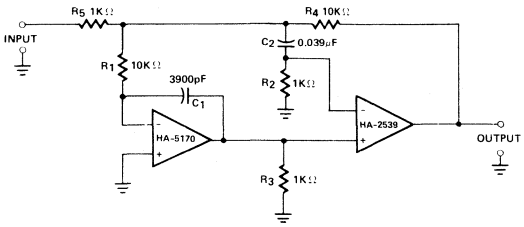


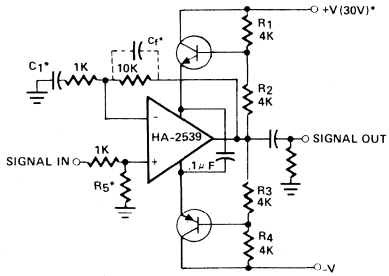
FIGURE 5. COMPOSITE AMPLIFIER

The HA-5170 amplifies signals below 40KHz, as set by C_1 and R_1, and controls the DC input characteristics such as offset voltage, drift, and bias currents of the composite amplifier. Therefore, it has an offset voltage of 100μV, drift of 2μV/°C and bias currents in the 20pA range. The offset voltage may be externally nulled by connecting a 20K pot to pins 1 and 5 with the wiper tied to the negative supply. The DC gains of the HA-5170 and HA-2539 are cascaded, which means that the DC gain of the composite amplifier is well over 160dB.

The excellent AC and DC performance of this composite amplifier is complemented by its low noise performance, 0.5μVrms from 0.1Hz to 100Hz, and makes it very useful in high speed data acquisition systems.

Boosting Output Power and Increasing Output Signal Swing

Figure 6 shows a cost effective method for increasing output voltage swing or boosting power of the HA-2539 or HA-2540 while adapting the device to supply rails which exceed the absolute maximum ratings. The supply rail values are limited only by the breakdown voltages of the transistors used, provided R_1 through R_4, are set to limit the voltage at the device supply pins to nominal supply voltages (±15V). Transistor selection should be limited to high f_T (greater than 60MHz) types such as MPS-A06 and MPS-A56. Physical layout properties may necessitate the use of phase lead compensation, in which case C_F may be added. It has unmeasurable distortion and very low noise within the audio band.



*NOTES:
1. Used for experimental purposes. $C_1 \approx 3pF$.
2. C_1 is optional (.001μF → .01μF ceramic).
3. R_5 is optional as can be utilized to reduce input signal amplitude and/or balance input conditions $R_5 = 500\Omega$ to $1K\Omega$.

FIGURE 6. BOOTSTRAPPING FOR MORE OUTPUT POWER AND VOLTAGE SWING

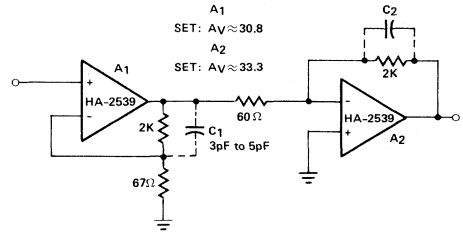
Applications

INTRODUCTION

HA-2539 and HA-2540 may be utilized in a wide variety of applications ranging from active filters to video pulse amplification. However, the applications to follow were selected to show where this can be used most advantageously.

APPLICATION 1: CASCADED AMPLIFIER

Cascaded amplifier sections are used to extend bandwidth and increase gain. Using two HA-2539 devices, this circuit is capable of 60dB gain at 20MHz.



APPLICATION 1. CASCADED AMPLIFIER SECTION

APPLICATION 2: VIDEO GAIN BLOCK

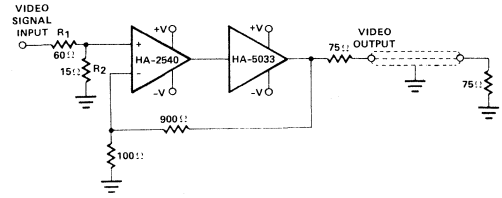
Video drivers and gain blocks used in color video systems are most always required to have outstanding differential phase and differential gain specifications. These requirements historically have eliminated the use of operational amplifiers and favor large discrete amplifiers which can be tailored to minimize systems errors.

This configuration utilizes the wide bandwidth and speed of HA-2540 plus the output capability of HA-5033. Stabilization circuitry is avoided by operating HA-2540 at a closed loop gain of 10 while maintaining an overall block gain of unity. However, gain of the block may be varied using the equation:

$$\frac{V_{OUT}}{V_{IN}} = 5 \quad \frac{R_2}{(R_1 + R_2)}$$

where $R_1 + R_2 = 75\Omega$

A maximum block gain of 3 is recommended to prevent signal distortion.

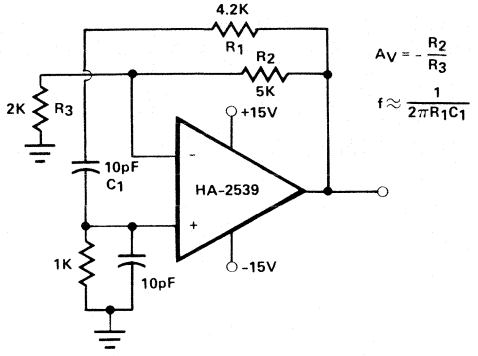


APPLICATION 2. VIDEO GAIN BLOCK HA-2539 & HA-2540

The circuit in Application 2 was tested for differential phase and differential gain using a Tektronix 520A vector scope and a Tektronix 146 video signal generator. Both differential phase and differential gain were too small to be measured.

APPLICATION 3: HIGH FREQUENCY OSCILLATOR

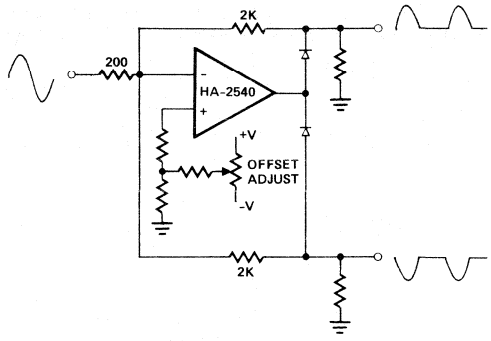
Intended primarily as a building block for a QRP transmitter, this 20MHz oscillator delivered a "clean" $6V_{p-p}$ signal into a 100Ω load.



APPLICATION 3. 20MHz OSCILLATOR

APPLICATION 4: WIDEBAND SIGNAL SPLITTER

With one HA-2539 or HA-2540 and two low capacitance switching diodes, signals exceeding 10MHz can be separated. This circuit is most useful for full wave rectification, AM detectors or sync generation.



APPLICATION 4. WIDEBAND SIGNAL SPLITTER

Acknowledgments

A. Terry D. Hass of Solitron, Inc., Stuart, FL. developed and tested video gain block.

B. Ron Jasinski of Sound Studio Services, 3208 Cahuenga Blvd. West, Los Angeles, CA. 90068 developed and tested bootstrapped output scheme.

C. Russ W. Leath of Harris Semiconductor developed and tested composite amplifier circuit.

References

Application Note 525 — HA-5190/5195 Fast Settling Operational Amplifier May 1979.

Tobey, Braeme, and Huelsman. Operational Amplifiers Design and Applications. New York: McGraw-Hill Company, 1971.

Application Note 552 — HA-2542 "T Network" Schematic

Application Note 556 — Thermal Safe-Operating-Areas For High Current Op Amps

APP NOTE

FOR YOUR INFORMATION

No. 543

Harris Analog

NEW HIGH SPEED SWITCH OFFERS SUB-50ns SWITCHING TIMES

By Carl Wolfe

Introduction

An ideal CMOS analog switch would exhibit such characteristics as zero resistance when turned on, infinite resistance when turned off, zero power consumption, and zero switching time. Unfortunately, such a device is usually found as an example in a college textbook. The real world offers tradeoffs and imperfections which prevent the realization of the ideal. The integrated circuit designer works within these limits and attempts to optimize device performance by utilizing new technologies and improving circuit design. The development of a new high speed analog switch required the use of both of these techniques to achieve its performance. (See Appendix I: "Inside the HI-201HS").

The HARRIS HI-201HS is the industry's first sub-50ns monolithic analog switch and along with fast switching speed, offers improved performance and pin compatibility with industry standard 201's (Fig. 1). This article will discuss the technology, performance, and applications for this product.

Improve Those Existing Designs

The application circuits which follow are examples of typical applications and illustrate how the HI-201HS can improve existing applications where standard 201's are presently being used.

The first example is a high speed multiplexer shown in Fig. 2. The analog multiplexer is a circuit which switches a number of analog inputs to a single output and is used heavily in data conversion and avionic applications. This function can be easily achieved with the HI-201HS by tieing the outputs together and selecting the appropriate analog input. The HI-201HS is an excellent choice for this application since its low on resistance and leakage current will reduce system error, and its high speed is unmatched by any other monolithic analog switch. Since the output capacitance is additive, the RC time constant of the load will increase when the outputs are made common.

The next application is a high speed sample and hold which takes advantage of the improved performance of the HI-201HS and the precision F.E.T. input of the HA-5160 high slew rate amplifier. A sample and hold circuit or track and hold as it is sometimes called, has two operating modes. In one mode the switch is closed and the capacitor charges to the input voltage. The second mode occurs when the switch is opened and the capacitor holds this charge for a specified period of time.

The speed of a sample and hold circuit is directly related to the switching device used and the output amplifier. This characteristic of a sample and hold circuit is called the acquisition time. It is defined as the time required following a "sample" command, for the output to reach its final value. The acquisition time includes the switch delay time, the time constant of the switch on resistance and hold capacitor ($T = R_{ON} C_{HOLD}$), and the slew and settling times of the output amplifier.

The photographs shown in Fig. 3 illustrate the improvement in the acquisition time possible by using the HI-201HS. The first photograph represents the sample/hold circuit using a standard 201 switch and an HA-5100 operational amplifier. The first waveform is the "Sample" voltage (V_A). The second waveform is the voltage on the hold capacitor (V_1). And the third waveform is the output of the amplifier (V_2).

The second photograph is the same circuit with a HI-201HS and on HA-5160 op amp. Comparison of the photographs shows the HI-201HS has significantly reduced the switch delay time and the high slew rate of the 5160 amplifier has also contributed to the reduced acquisition time.

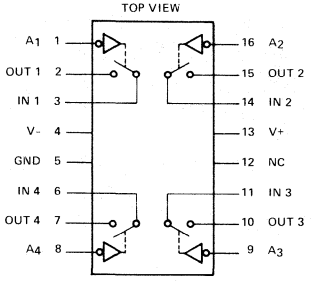
A source of error in this circuit is a d. c. offset which is called sample to hold offset error. This error is

primarily due to the charge injection (Q) of the switch and is related to the hold capacitance by the following expression,

$$\text{offset error } (V_O) = \frac{\text{charge transfer (Q)}}{C_H}$$

The reduced charge injection of the HI-201HS (typically 10 pc) will result in immediate reduction of this error.

Using analog switches with operational amplifiers is common in circuit design. An example is shown in Figure 4 which is an integrator with start/reset capability.

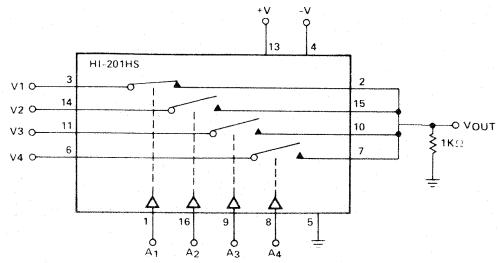


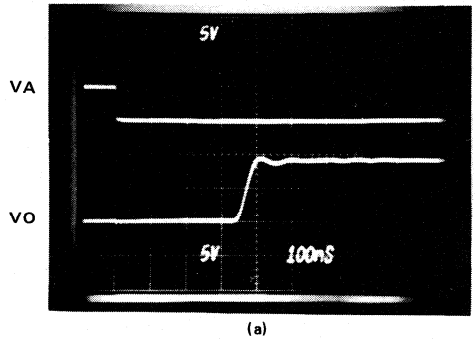
LOGIC	SWITCH
0 - $V_{AL} \leq .8V$	ON
1 - $V_{AH} \geq 2.4V$	OFF

TYPICAL SPECIFICATIONS (±15V Supply)

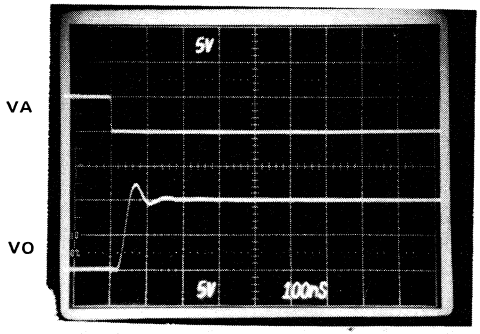
Analog Signal Range	±15V
On Resistance	30Ω
Off Leakage	.3nA
Switch On Time	30ns
Power Dissipation	120mW

Figure 1. Typical Pinout and Specifications – The HI-201HS is pin compatible with standard 201's and offers improved performance. Specifications given are typical values at $T_A = 25^oC$.





(a)



(b)

Figure 2. High Speed Analog Multiplexer: (a) circuit response using the standard 201 (T_{access} = 400ns) (b) circuit response using HI-201HS (t_{access} = 50ns). The access time is defined as total time required to activate an "off" switch to the "on" state. Access time is normally measured from the initiation of the digital input pulse (V_A) to the 90% point of the output transition.

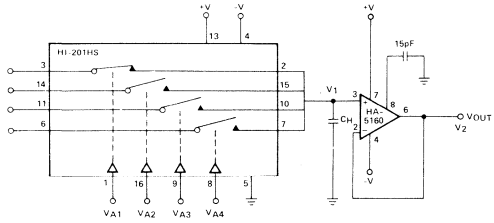


Figure 3A. High Speed Sample and Hold: The basic sample and hold samples the input voltage when the switch is closed and the capacitor holds the voltage when the switch is open. The speed of the switching element affects the speed of the sample and hold.

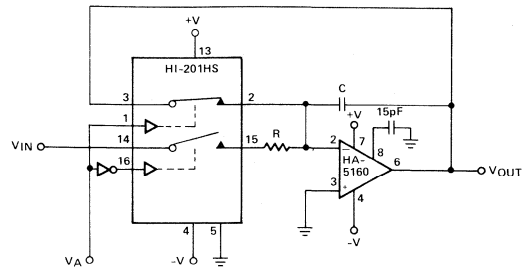


Figure 4A. Integrator with Start/Reset: A low logic input pulse disconnects the integrator from the analog input and discharges the capacitor. When the logic input changes to a high state, integrator is activated.

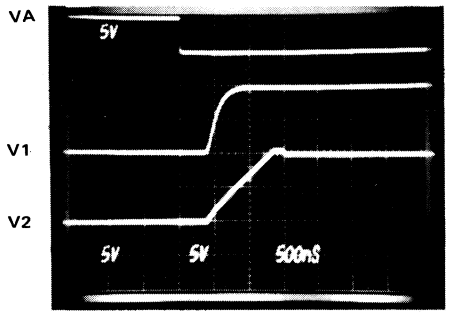


Figure 3B. Circuit response to a "Sample" command using a standard 201 and an HA-5100 operational amplifier (Acquisition time = 1.5μs)

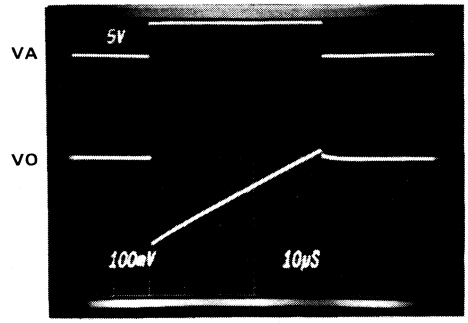


Figure 4B. Low Level Integration— Circuit response using standard 201 switch.

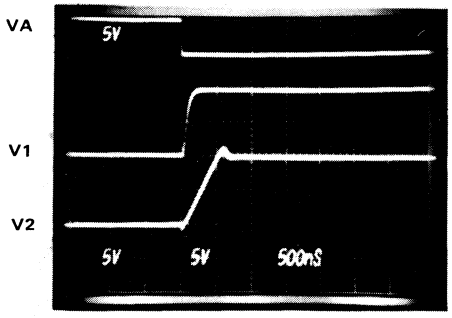


Figure 3C. Circuit response using an HI-201HS and HA-5160: HI-201HS significantly reduces switch delay time. (Acquisition time = 500ns)

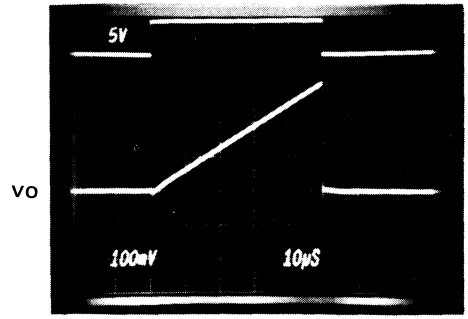


Figure 4C. Low level integration—Circuit response illustrates improved charge injection of the HI-201HS.

The switch is used to apply the input signal and to reset the integrator. Applying a low logic level removes the input signal and the capacitor is discharged. When a logic level high is present, the input signal is integrated with a rate of change equal to

$$dvo/dt = if = \frac{-V_i}{C_f\ R_1C_f}$$

The reduced on resistance, leakage current, and charge injection of the HI-201HS will improve the performance of this circuit and an example of this improved peformance can be seen in the photographs in Figure 4. These photographs illustrate the reduced charge injection which the 201HS offers. The component values are R_1 = 1MΩ , C = 150pF and V_{IN} = -1V. With these values, the amplifier will integrate the input signal with a slope of 6.6mv/μs. For a 50μs time period, the amplifier will integrate to a magnitude of ≈ 300mV. The photographs of the test results indicate this to be true, but it should be apparent that the two photographs are quite different. The first photograph represents the amplifier output using a standard 201 as the reset switch. The second photograph is the same circuit with a 201HS.

The offset error in the first photograph is due to the charge injection of the switch. Using the expression Q = V x C and knowing the standard 201 has a typical charge transfer of 30pc, this offset can be calculated. V = Q/C = 30pc/150pf=200mV.

Other examples of combining switches and amplifiers are shown in figures 5 and 6. In both these applications the switch is used to tailor the amplifiers performance. Figure 5 is a low pass filter with a selectable break frequency.

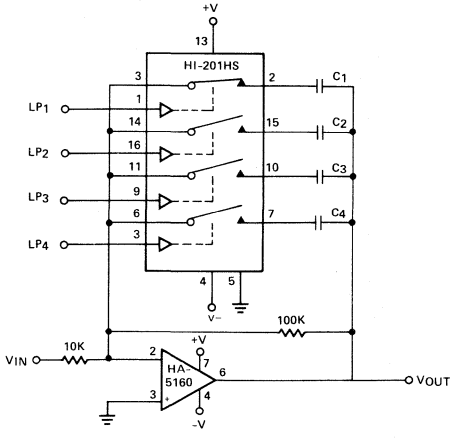


Figure 5. Low Pass Filter with Selectable Break Frequency— Switch selection places various values of capacitance in parallel with the feedback resistor. The value of the capacitor determines the break frequency. The break frequency is that frequency at which the signal begins attenuation.

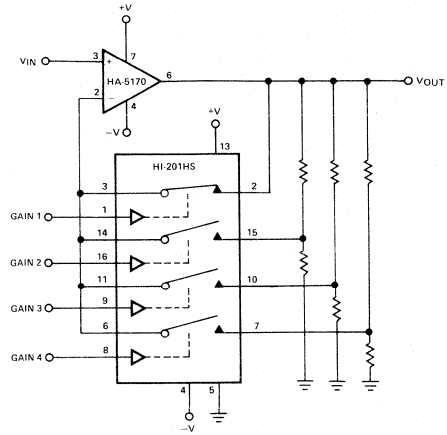


Figure 6. Amplifier with Programmable Gain— Switch selection activates a new voltage gain which is determined by the resistive feedback.

Depending on which switch is selected, a particular cutoff frequency is introduced by the expression,

$$F_C = \frac{1}{2\pi R\ C_x}$$

A programmable gain amplifier is shown in Figure 6. Similar in function to the filter application, the gain of the amplifier is determined by selection of a switch.

When using switches with other components it is important that a switch be selected which introduces a minimal amount of error to the circuit. Operational amplifier gain error due to high on resistance or offset voltages due to excessive leakage current and charge injection are examples of potential error created by the switch. The previous applications have demonstrated that the 201HS offers improved performance by minimizing circuit error and increasing system speed.

On The Drawing Board

Since the introduction of the HI-201HS switch, many engineers have expressed an interest in using this new product. Although much of their work is in a preliminary stage and they do not want to divulge exact details on their designs, the following information is intended to give you an idea of how other engineers are considering using the HI-201HS.

The majority of the engineers are interested in taking advantage of the products fast switching speed. One particular engineering group is investigating replacement of DMOS (double-diffused MOS) transistors with the HI-201HS.

The DMOS transistor is capable of extremely fast switching speeds (1ns) and until now, switches

fabricated using CMOS technology have not been fast enough to be considered. But the HI-201HS is attractive since it offers unprecedented switching speed along with the established benefits of CMOS technology. Such benefits include a wider analog signal range capability and lower operating power requirements.

A common application for analog switches is time division multiplexing, where many signals are processed on a single channel. High speed switching allows higher information capacity on the channel, since the switching speeds of an analog switch are directly related to the maximum switch activation frequency. The faster a switch can turn on and off, the higher the possible switching frequency. An example of this relationship is shown in Figure 7. If a switch is activated at a frequency of 1MHz, it must turn on and off within a 500ns time period. Since the HI-201HS has a maximum on and off times of 50ns, and can turn on and off within a 100ns time period, it theoretically possible that it can be activated at a 5MHz frequency rate. This improved capability is making the HI-201HS an attractive component to design engineers requiring high frequency data processing. Conversations with engineers indicates that possible applications are computer graphics and visual display circuit designs.

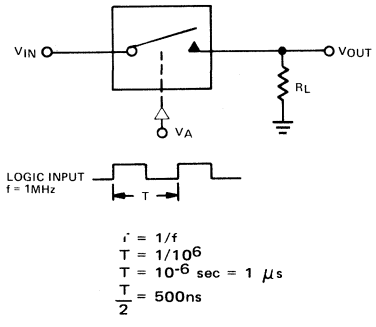


Figure 7. High Frequency Switching — HI-201HS fast switching times allow it to transfer data at a higher rate of frequency.

Another area where the HI-201HS is generating interest is in the area of medical electronics. This is a growing field and improvements are continously being made as products become available much of the medical equipment being designed requires both high speed and accuracy.

Medical test equipment is primarily used to transmit or receive information from the patient. An example where both these functions are used is in the area of ultrasound. Ultrasound testing requires that a signal be transmitted to the patient and the return signal is then amplified and displayed or recorded. The 201HS is being considered for the use in such an application and would be used to control the transmission and reception of these signals.

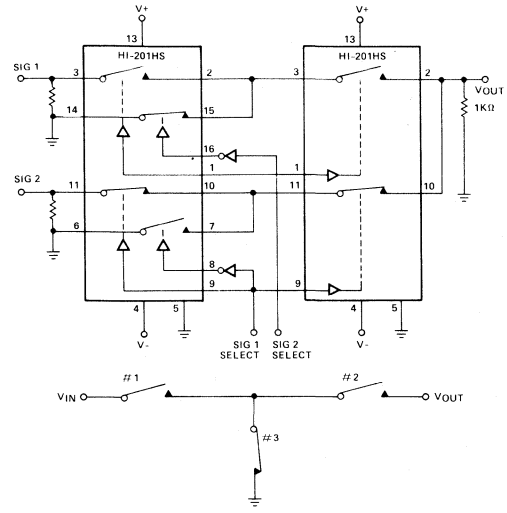


Figure 8. Video Switching with Improved Isolation— Improved high frequency off state performance is obtained by using a T-Switch configuration. When two series switches are off, the third switch is shorted to ground.

The designers are not only interested in fast switching speed, but also in low on resistance. This is an important aspect of the switch since many of the electrical signals in medical electronics are of a small magnitude. An example is patient monitoring equipment which converts physiological parameters into electrical signals. If these low level electrical signals require switching before amplification, a low on resistance switch is essential to minimize the voltage drop across the switch itself. The low on resistance of the HI-201HS enables it to be used in applications using signals of smaller magnitude.

Video circuit design involves the control of high frequency signals. Applications which require the switching of these high frequency signals are usually limited by the off isolation and crosstalk performance of the switch. Off isolation is defined as the amount of feedthrough of an applied signal through an off switch. Crosstalk is the amount of cross coupling of an "off" channel to the output of an "on" channel. Both of these switch characteristics will degrade as the frequency of the input signal increases.

The HI-201HS has some improvement over the standard 201 in these areas but the configuration shown in Figure 8 is being used by designers to improve the isolation capabilities of CMOS analog switches. This configuration is known as "T" switching since the three switches used for passing the signal could be thought of in the shape of the letter T. The simplified figure shows that when switches # 1 and # 2 are off, switch # 3 is tied to ground. When switches # 1 and # 2 are on, # 3 is off. This improves isolation by having two channels in series off and any feedthrough is fed to ground.

Conclusion

The HARRIS HI-201HS is the fastest monolithic CMOS analog switch available. It offers improved performance for existing designs and should be considered for use in any application where switching speed is an important criteria.

ACKNOWLEDGEMENTS

The author would like to thank Gary Maulding, Frank Cooper, and Bob Junkins for their technical assistance, Ken Timko and Dick Whitehead for their editorial comments, and the dynamic duo of Lilly Andrews and Kathy Glines for their secretarial skills and patience in the preparation of this paper.

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2. J. G. Graeme, G.E. Tobey, and L. P. Huelsman, "Operational Amplifiers: Design and Applications". New York: McGraw Hill, 1971.

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4. HA-2420/2425 Fast Sample and Hold data sheet, Harris Semiconductor.

Appendix I-INSIDE THE HI-201HS

The HI-201 is a TTL compatible quad CMOS analog switch which features switching times under 50ns and a typical "on" resistance of 35Ω. The fast switching times are achieved through a combination of process and circuit design techniques. The HI-201HS is fabricated using a dielectric isolation process with complementary PNP and NPN bipolar transistors and polysilicon-gate CMOS. The use of bi-technology process enabled a unique circuit called a D. C. Static Level Shifter to be designed.

The typical CMOS analog switch consists of a switch cell which is driven by a level shifter. The level shifter converts a single logic input into two complementary outputs which drive the gates of the CMOS switch cell (Fig. A). The switch cell represents a capacitive load to the level shifter, so fast switching times require large drive currents to charge these capacitances quickly. The D. C. Static level shifter circuit (Fig. B) provides large drive currents only when switching and dissipates little power in a quiescent condition.

The D. C. static level shifter achieves high switching speeds through the use of a unique bipolar input stage and a network of switching and holding MOS transistors. Devices MN5, MP5, MN9 MP9 are the switching transistors and MN6, MP6, MN10, MP10 are the holding transistors. The major advantage of the bipolar input transistors is that its transconductance (g_m) is much higher than that possible with F. E. T. transistors.

To understand the level shifter operation, consider a change of logic input from low state to high. Initially V_A is low, $Q = Q_1 = Q' = -15V$ and $\overline{Q} = \overline{Q_1} = \overline{Q'} = 15V$. VB is at ground and QN2, QP2 are off. When V_A goes high, QN2, QP2 turn on, which slew the gates of switching devices MN5, MP5 with a current $I = (V_A - 2V_{BE})/R$. The switching devices overcome the holding devices, MN10, MP10 and switch the internal nodes Q_1, and $\overline{Q_1}$. CMOS buffers I_{11}, I_{13} provide large drive currents to the switch cell, while inverters I_{12}, I_{14} provide delayed feedback signals. The feedback signals turn off holding devices MN10, MP10 while turning on holding devices MN6, MP6. The feedback also turns on QN2, QP2 by means of MN1, MP1. These feedback signals have returned the level shifter to a static condition by turning the bipolar input stage and MOS switching transistors off.

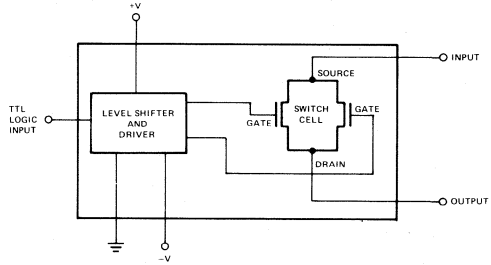


Figure A. Simplified I. C. Analog Switch Operation—Level Shifter converts logic input into drive signal for CMOS switch cell.

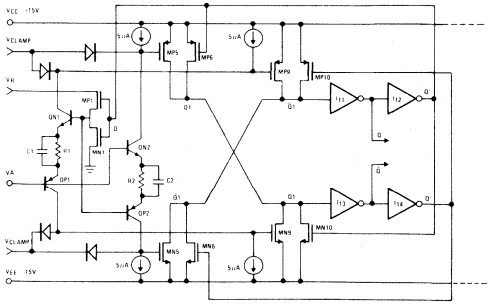


Figure B. Simplified D. C. Static Level Shifter — The level shifter consists of a unique bipolar input stage and a network of switching and holding devices.

Similar operation occurs when V_A goes from high to low, bipolar transistors QN1, QP1 turn on MN9, MP9. The feedback resets the holding devices and turns off the bipolar input stage.

Appendix II-HI-201HS vs. STANDARD 201

The use of a dual technology process and a creative design improves the performance of this analog switch. The following table illustrates the results of this combination by comparing the specification of the HI-201HS with the standard 201.

It should be apparent from Table 1 the substantial improvement in switching speeds offered by the HI-201HS. But since the switch "off" time of the high speed switch is measured differently from the standard 201, a brief discussion of test methods will avoid any confusion.

Figure A is a typical switching time test circuit for an analog switch. The "on" time is measured from the logic input to the 90% point of the output.

The "off" time can be measured from the logic input to either the 90% or 10% point of the output. This variation in the "off" time test point is due to the dependence of the measurement on the load. The dominant component of the switch "off" time is an exponential RC time constant determined by the values of the load resistance and capacitance. The "off" time of the HI-201HS is measured to the 90% point. The RC time constant due to load is excluded from this measurement. The photograph included in Figure A is a typical HI-201HS switching time response.

The remainder of table one compares other critical specifications of CMOS analog switches. The HI-201HS is not only a high speed switch but also offers improved performance in other areas. The parameters of "on" resistance, leakage current, and charge injection can all contribute unwanted errors to system level applications. With the improvements shown in these areas, the HI-201HS offers potential improvement in system accuracy for a wide variety of applications. and since the HI-201HS is pin compatible with existing 201's, the high speed version can be plugged into existing designs for immediate improvement in performance.

The HI-201HS is an improvement over the standard 201 in many areas, but some trade-offs still exist. One such trade-off was the power dissipation of the product. In order to meet the high speed criteria, larger internal currents are needed which in turn demand increased supply current. But this apparent shortcoming is more than offset by the products performance.

Parameter	Temperature	HARRIS HI-201HS	HARRIS HI-201
Switching Speed			
t_{ON}	25°	50ns	500ns
t_{OFF}	25°	50ns	500ns
ON Resistance	125°	75Ω	125Ω
Leakage Current			
I_{SOFF}	125°	100nA	500nA
I_{DOFF}	125°	100nA	500nA
Charge Injection Q	25°	10pc (typ)	30pc (typ)
Power Dissipation Pd	125°	240mw	60mw

Table 1. Specification Comparison: Improved performance of HI-201HS over standard 201's (all values are maximums unless stated otherwise).

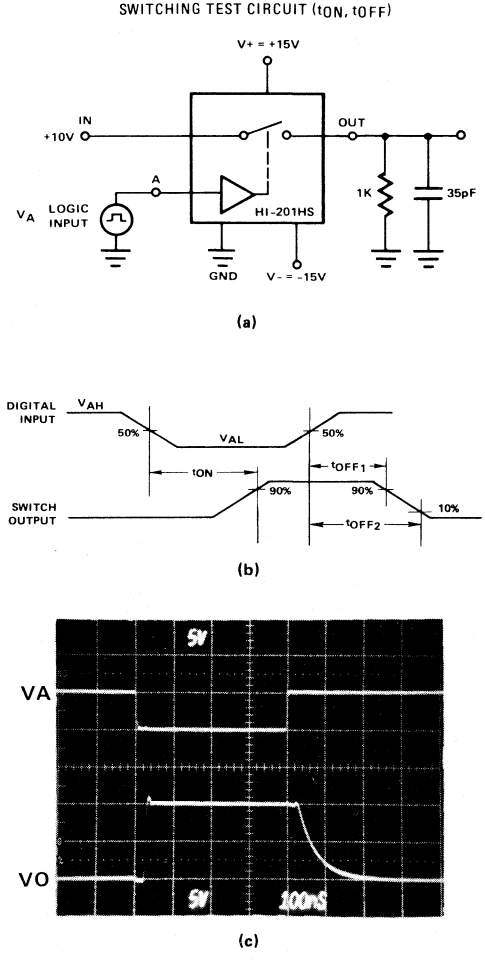


Figure A. Switching Time Test Circuit: (a) Switching test circuit, (b) Switching waveforms, (c) Typical HI-201HS response.

APP NOTE

FOR YOUR INFORMATION

No. 544 February 1988

Harris Analog

APP. NOTE 544

MICROPOWER OP AMP FAMILY HA-5141/42/44 AND HA-5151/52/54

Russell Leath and Richard Whitehead

Introduction

Offering the best speed power product of any low power operational amplifier available, the HA-514X/515X can be effectively utilized in a wide variety of portable system applications. The features available from this family of devices can be easily incorporated into dictation equipment, medical monitoring systems, remote electronic sensors and other system designs.

Low or Micropower?

Actually, the HA-5141/42/44 operational amplifiers are micropower devices. That is, they consume microwatts of power (250μW typ.) as opposed to low power devices which consume 1 to 10mW. This exceptionally low power consumption however does not compromise the speed and flexibility of this family of amplifiers. Table 1 lists the speed/power relationships of some amplifiers in this class. The industry standard 741 was listed to show that HA-5141 has more speed for a fraction of the power consumed. A brief discussion concerning how the HA-514X/515X achieves this unique relationship can be found in the inset below.

For highest speed for power consumed, HA-5141 is a factor of 10 better than the nearest device, and the HA-5151 is six times better than the HA-5141.

Part Number	Power Dissipation	Slew Rate	Full Power Bandwidth	Gain Bandwidth
HA-5141	250μW	1.5V/μs	60KHz	400KHz
RC4132	250μW	0.13V/μs	5.5KHz	150KHz
OP-20	275μW	0.02V/μs	0.9KHz	100KHz
HA-5151	1000μW	4.5V/μs	95KHz	1300KHz
LM1OC	2000μW	0.11V/μs	5.5KHz	80KHz
LM741	8000μW	0.7V/μs	20KHz	1500KHz

TABLE 1. SPEED/POWER RELATIONSHIPS

Dual or Single Supply

Enhancing the micropower consumption and speed capabilities of the HA-514X/515X is its ability to operate over a wide range of supplies. It can be operated in double supply mode from ±15V down to ±1.5V or in single mode from +30V down to +3V. The quiescent supply current remains nearly constant over the entire supply range making it most suitable for operation in battery powered systems. The HA-514X family requires only 60μA/amp, and the HA-515X family requires only 200μA/amp for typical quiescent operation.

Making the Most of Micro Amps

To achieve high slew rate while requiring only microamps to operate, the HA-514X/515X designs utilizes a current amplifying front end. As can be seen in the simplified schematic under zero signal conditions, current source I_1 flows through D_1 and P_1 while I_2 flows through D_2 and P_2. This flow sets up a DC bias current of I_1 and I_2 through N_1 and N_2. This bias current is slightly higher with the HA-515X family and therefore allow a faster response time.

Under small signal conditions, the cross coupling of N_1 to P_2 and N_2 to P_1 establishes small signal currents i_1 and i_2 through collectors of N_1 to P_2 and N_2 and P_1 respectively. This differential current (i_1-i_2) is similar to a standard differential pair and is given by;

$$i_1 - i_2 = gm \text{ where } gm = f(hib)$$

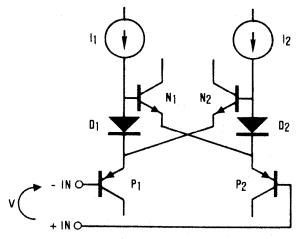
However, under large signal inputs and unlike the standard differential pair, the maximum differential current is not limited by the DC biasing current sources. The maximum slewing current is limited only by the β of N_1 and is orders of magnitude larger than the DC biasing current.

For a standard differential pair under large signal conditions the differential current is given by;

$$i_1 - i_2 = I_1 \tanh V \text{ and } i_1 - i_{2max} = 2I_1$$

But for the HA-514X/515X the large signal differential current is; $i_1 - i_2 = I_1(e^{v/vt} - e^{-v/vt})$

and i_1-i_2 increases exponentially until limited by βN_1. The HA-514X/515X design utilizes two gain stages which allows for high DC gain at lower collector impedance levels. These lower impedance levels permit unstacked device design which allows for lower operating voltage levels.

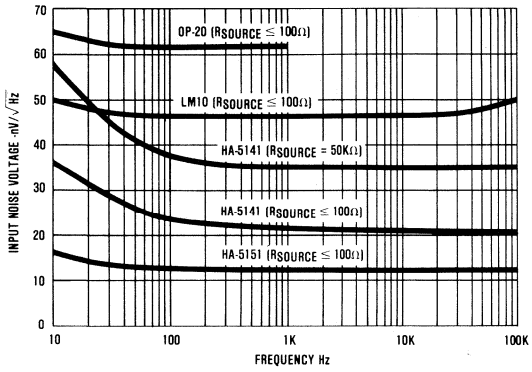


HA-514X/515X CURRENT AMPLIFYING FRONT END

10 APPLICATION NOTES

Noise Parameters Also Attractive

With rugged bipolar construction combined with the dielectric isolation technology, the HA-514X/515X design maintains noise characteristics comparable to amplifiers requiring much higher supply currents. The noise curves compare the HA-514X/515X with other amplifiers in its class. It is readily observed that the HA-5141 has lower noise components even with higher source impedances. With typical noise values of $23nV/\sqrt{Hz}$ and $0.03pA/\sqrt{Hz}$ at 1KHz this device family is very "user friendly" to the portable system designer. As shown, the HA-5151 has even lower noise.



NOISE CURVES COMPARING HA-5151 WITH OTHER AMPLIFIERS

Other Useful Qualities

When operated in single supply mode this family of amplifiers is capable of output voltage swings from 0V to V(+) -1 Volt while sourcing 3mA output current. Their common range under single supply conditions is 0V to V(+) -1V. These qualities coupled with 60KHz full power bandwidth and 0.4MHz small signal bandwidth further widens the application range of the HA-5141/42/44. The HA-5151/52/54 is even more versatile with 1.3MHz small signal bandwidth and 95KHz full power bandwidth.

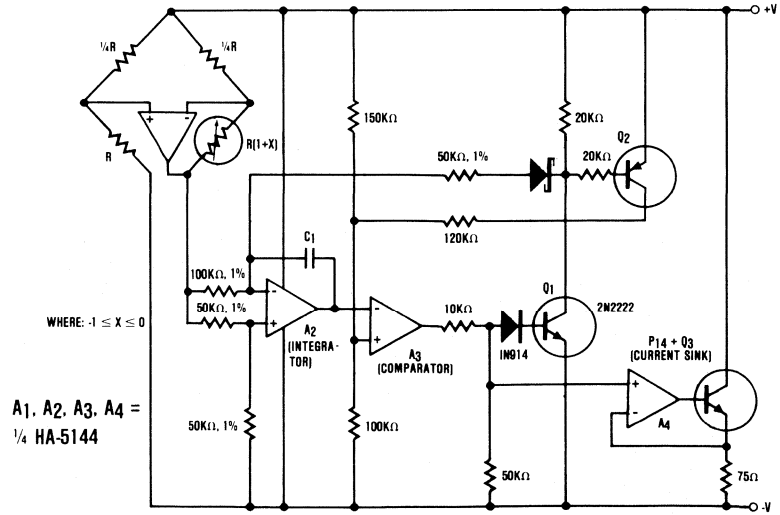
Applications

The flexibility and inherent qualities of the HA-514X/515X are most suitable for battery operated and/or low voltage systems such as remote electronic sensors or solar operated designs. The following applications are just a few of the many possibilities which can best utilize this amplifier's capabilities.

APPLICATION 1—REMOTE SENSOR LOOP TRANSMITTER

This circuit shows amplifier A_1 as a sensor amplifier in abridge configuration. Amplifiers A_2 and A_3 are configured as a voltage to frequency converter and A_4 is used as the transmitter. This entire sensor/transmitter can be powered directly from a 4 to 20mA current loop.

The bridge configuration produces a linear output with respect to the changes in resistance of the sensor. The voltage at the output of A_1 causes the integrator output A_2 to ramp down until it crosses the comparator threshold voltage of A_3. A_3 turns on Q_1 and Q_2. Q_1 causes the output of A_2 to ramp up at a rate nearly equal to its negative slope while Q_2 provides hysteresis for the comparator. In addition, Q_1 and Q_2 help eliminate changes in power supply (loop) voltage. Amplifier A_4 and Q_3 are configured as a constant current sink which turns on when the comparator goes "high". The resulting increase in loop current transmits the frequency of the V to F converter back to the control circuitry.



REMOTE SENSOR — CURRENT LOOP TRANSMITTER

APPLICATION 2—CHARGE POOL POWER SUPPLY

It is usually desirable to have the remote transmitter of a 4 to 20mA current loop system powered directly from the transmission line. In some cases this is not possible due to high power requirements set by the remote sensor/-transmitter system. In these cases an alternative to the separate power supply is still possible. If the remote transmitter can be operated in a pulsed mode where it is active only long enough to perform its function, then a charge pool power supply can still allow the transmitter to be powered directly by the current loop. In this circuit a constant current I_1 is supplied to the charge pool capacitor (CP) by the HA-5141 (where I_1 = 3mA). The voltage V_1 continues to rise until the output of the HA-5141 approaches +Vs or the optional voltage limiting provides by Z_2. The LM2931 voltage regulator supplies the transmitter with a stable +5V supply from the charge collected by CP. Available power supply current is determined by the duration, allowable voltage droop on Cp, and required repetition rate. Example: If V_1 is allowed to droop 4.4V and the duration of operation is 1msec, the available power supply current is approximately

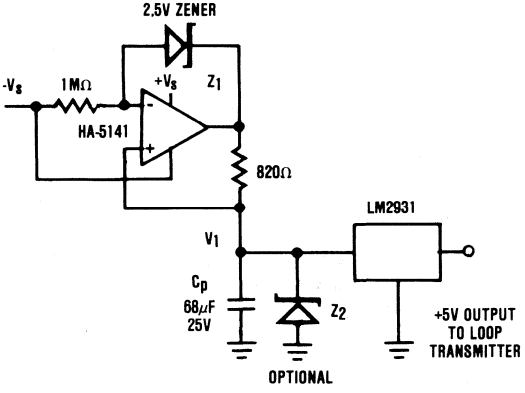
$$I_{ps} = Cp \frac{dV1}{dt} = 68\mu F \cdot \frac{4.4V}{1msec} = 30mA.$$

The repetition rate of operation is determined by the time required for the 3mA constant current source to restore V_1 to its previous value. In this example:

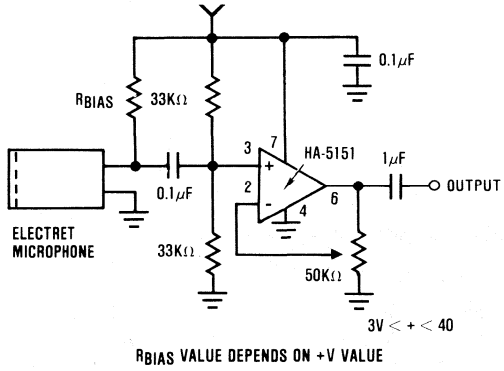
$$t = 68\mu F \cdot \frac{4.4V}{3mA} = 100msec \text{ is required.}$$

APPLICATION 3—LOW POWER MICROPHONE AMPLIFIER

The HA-515X op amp is very well suited for use in audio applications which require high gain, bandwidth and speed at low voltages and with low power consumption. Requirements such as these are usually found in battery, telephone line or solar powered circuits. The circuit below shows how the HA-5151 may be used to amplify the audio signal from an Electret microphone. This circuit may be operated with a single power supply voltage as low as 3V or as high as 40V and can provide over 25dB of gain over the audio frequency range. The 4.5V/μsec slew rate and low noise of the HA-5151 provides low distortion operation while only consuming about 200μA of supply current.



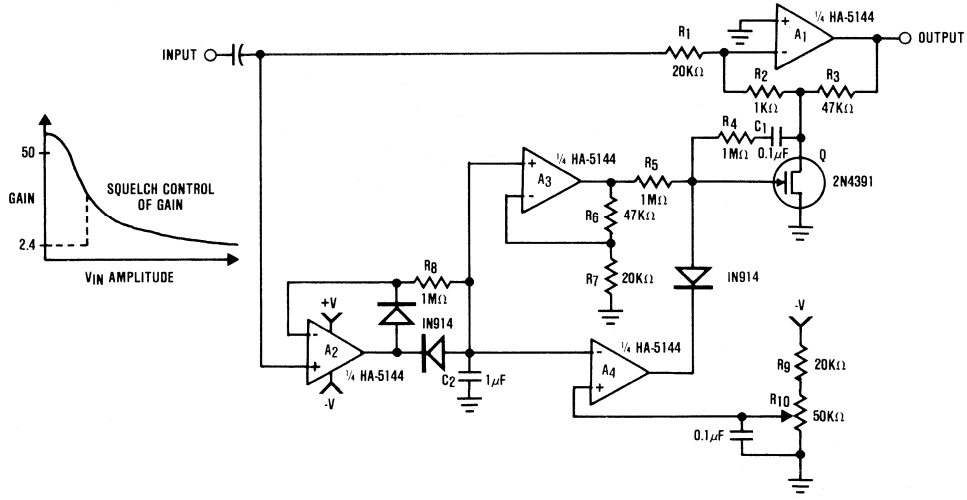
CHARGE POOL POWER SUPPLY FOR PULSED LOAD 4-20mA LOOP TRANSMITTER



LOW POWER MICROPHONE AMPLIFIER

APPLICATION 4—AGC WITH SQUELCH CONTROL

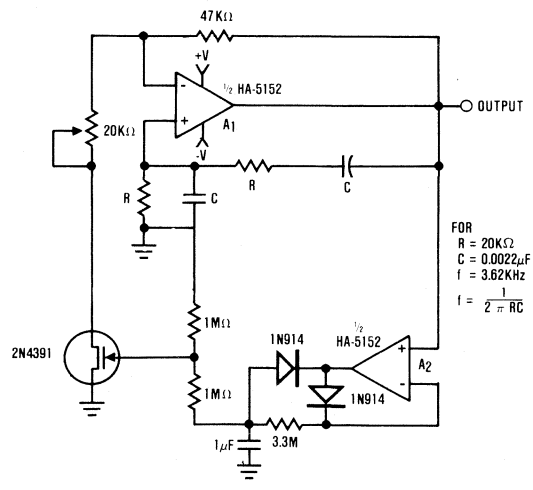
Automatic gain control is a very useful feature in a number of audio amplifier circuits such as tape recorders, telephone speaker phones, communication systems and P.A. systems. The circuits shown below consists of a HA-5144 quad op amp and a FET transistor used as a voltage controlled resistor to implement an A.G.C. circuit with squelch control. The squelch function helps eliminate noise in communications systems when no signal is present and allows remote hands free operation of tape recorder systems. Amplifier A_1 is placed in an inverting gain T configuration in order to provide a fairly wide gain range and to keep the signal level across the FET small. The small signal level across the FET and the addition of resistors R_5 and R_6 help reduce nonlinearities and distortion. Amplifier A_2 acts as a negative peak detector to keep track of signal amplitude. Amplifier A_3 may be used to amplify this peak signal if the cutoff voltage of the FET is higher than desired. Amplifier A_4 acts as a comparator in the squelch control section of the circuit. When the signal level falls below the voltage set by R10 the gate of the FET is pulled low turning it off completely and reducing the gain to 2.4. The output A_4 may also be used as a control signal in applications such as a hands free tape recorder system.



AGC WITH SQUELCH CONTROL

APPLICATION 5—LOW VOLTAGE WEIN BRIDGE OSCILLATOR

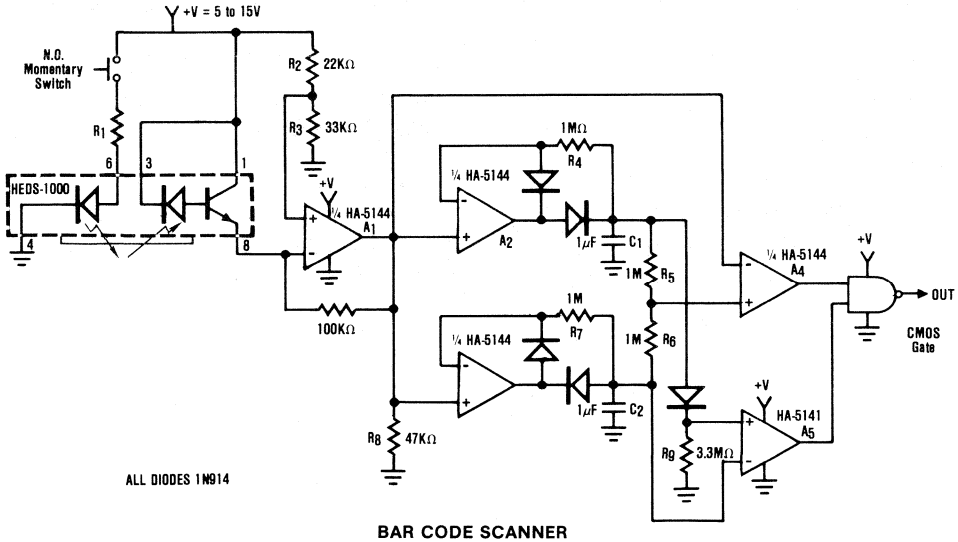
The circuit shown to the right utilizes a HA-5152 dual op amp and FET to produce a low voltage, low power Wein Bridge sine wave oscillator. Resistors R and capacitors C control the frequency of oscillation while the FET, used as a voltage controlled resistor, maintains the gain of A_1 at exactly 3 to sustain oscillation. The 20K pot may be used to vary the signal amplitude. The HA-5152 has the capability to operate down to ±1.5V supplies and this circuit will produce a low distortion sine wave output while drawing only 400μA of supply current.



LOW VOLTAGE WEIN BRIDGE OSCILLATOR

APPLICATION 6—BAR CODE SCANNER

The circuit shown below illustrates a method of interfacing a HEDS-1000 emitter-detector pair with a HA-5144 for use as a bar code scanner circuit. The HA-5144 is used as an amplifier system which converts the bar and space widths of the printed bar code into a pulse width modulated digital signal. Amplifier A_1 is used to amplify the current output of the detector. The output of A_1 is passed to two precision peak detector circuits which detect the positive and negative peaks of the received signal. Amplifier A_4 is used as a comparator whose reference is maintained at the midpoint of the peak to peak signal by resistors R_5 and R_6. This provides a more accurate edge detection and less ambiguity in bar width. Amplifier A_5 is used as an optional noise gate which only allows data to pass through the gate when the peak to peak modulation signal is larger than 1 diode drop. This circuit is operated by a single supply voltage with low power consumption which makes it ideal for battery operated data entry systems.



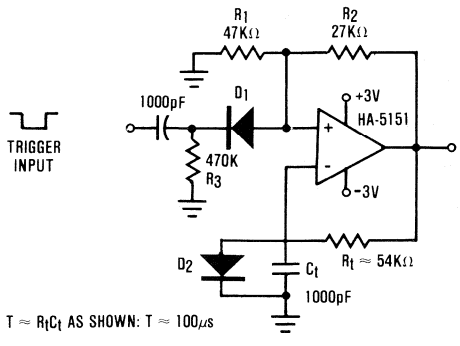
BAR CODE SCANNER

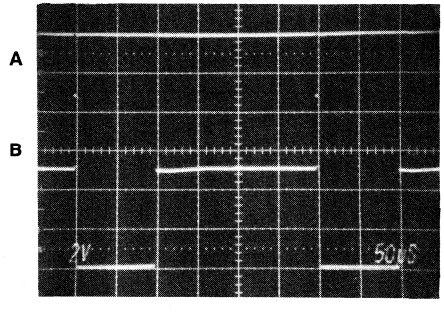
APPLICATION 7—MONOSTABLE MULTIVIBRATOR

The circuit below illustrates the usefulness of the HA-5151 as a battery powered monostable. In this circuit the ratio is set to .632, which allows the time constant equation to be reduced to:

$$T = R_tC_t$$

D_2 is used to force the output to a defined state by clampinng the negative input at +0.6V. Triggering is set by C_1, R_3, and D_2. An applied trigger pulls the positive input below the clamp voltage (+0.6V) which causes the output to change state. This state is held because the negative input cannot "follow" the change due to $R_t \bullet C_t$. As can be seen in the photograph, this particular circuit has a output pulse width set at approximately 100μs. Use of potentiometers for R_t and varible capacitors for C_t will allow for a wide variation in T.





SCALE: VERTICAL, A = 1V/DIV B = 2V/DIV
HORIZONTAL = 50μs/DIV

MONOSTABLE MULTIVIBRATOR

APPLICATION 8—AC COUPLED DYNAMIC AMPLIFIER

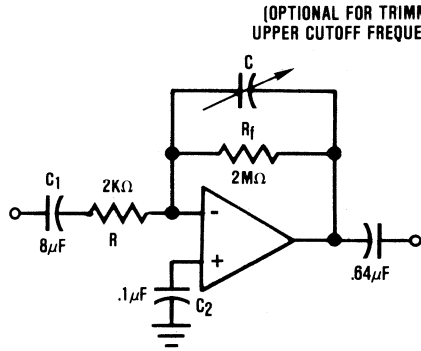
The circuit shown below is yet another of the many ways to utilize the advantages of HA-5141/42/44. This circuit would be most useful for biomedical instrumentation and acts as a bandpass filter with gain. Low frequency cutoff is set at 10Hz while the high frequency break point is given by the open loop roll off characteristic of the HA-5141/42/44. In this case, the A_{VCL} = -60dB where the rolloff occurs at approximately 300Hz. This corner frequency may be trimmed by inserting a capacitor in parallel with R_f.

Acknowledgements

A. Russell Leath of Georgia Institute of Technology — Engineering Experiment Station, Atlanta, GA., developed an evaluated the circuits in this Application Note.

B. Don Jones, Jon Dutra, and David Graen, Harris Semiconductor, Analog Division, Field Application Engineers provided inputs leading to the development of the circuits in this Application Note.

C. Gerry Cotreau, Harris Semiconductor, Analog Division, provided inputs involving operation of HA-514X/HA-5151X devices.



A.C. COUPLED DYNAMIC AMPLIFIER (A_{VCL} = -1000)

A METHOD OF CALCULATING HA-2625 GAIN BANDWIDTH PRODUCT vs. TEMPERATURE

By: Carl Wolfe and John Prentice

Introduction

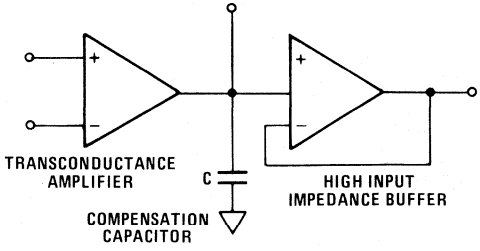
The job of the analog circuit designer would be simplified if all designs were intended to operate at a constant temperature. But since this is usually not the case, the majority of designs require that I.C. performance with respect to temperature be considered.

A common request for analog designers using the HA-2625 operational amplifier is information on the Gain Bandwidth Product (GBP) vs. Temperature. The GBP is defined as the product of the amplifier gain and bandwidth at a specified frequency. Knowledge of this operational amplifier characteristic with temperature provides insight into the amplifier's open loop frequency response variation with temperature.

The following information describes a method of calculating HA-2625 GBP vs. Temperature.

Procedure for Computing Gain Bandwidth Product

A simplified configuration of the HA-2625 op amp is shown in Figure 1. The gain of this operational amplifier over its intermediate frequency range can be expressed by Equation 1.



BENEFITS

- MORE TEMPERATURE-STABLE THAN MILLER INTEGRATOR TYPES
- AVAILABILITY OF HIGH IMPEDANCE INPUT FOR OUTPUT LIMITING

FIGURE 1. TYPICAL HARRIS OP AMP CONFIGURATION

$$A_V = \frac{g_m}{2\pi f C_C} \quad (1)$$

$$\theta_V = \theta_{gm} - 90^o$$

where,

A_V = magnitude of voltage gain

θ_V = phase of voltage gain (-90° due to C_C phase shift)

g_m = transconductance magnitude of op amp input stage

θ_{gm} = transconductance phase

f = bandwidth

C_C = compensation capacitance (includes internal and external capacitance)

Rewriting Equation 1, the GBP can be expressed as a function of transconductance.

$$GBP = A_V f = \frac{g_m}{2\pi C_C} \quad (2)$$

Transconductance magnitude/phase characteristics vs. frequency and temperature are shown in curves 1 through 8. The GBP vs. temperature can be calculated by using Equation 2 and the given transconductance data.

As an example, let's calculate the variation of GBP over the temperature range of +25°C to +75°C. The operating frequency is given to be 100KHz and the external compensation capacitor is 50pF.

Before applying equation 2, both the transconductance magnitude and compensation capacitance values must be determined. Referring to curve 2, the transconductance magnitude for an ambient temperature of +25°C and an operating frequency of 100KHz is 3.2×10^{-3} mmho.

The compensation capacitance value represents total capacitance. Therefore, in addition to the external capacitor component value, C_C should include an internal device capacitance of 3pF plus 5pF to account for fixture capacitance.

So by using values of $g_m = 3.2 \times 10^{-3}$ mmho and $C_C = 50 + 2 + 5 = 57$pF, the GBP is computed as follows:

$$GBP = \frac{3.2 \times 10^{-3}}{2\pi (57 \times 10^{-12})} = 8.94\text{MHz}$$

Next, the transconductance gain at +75°C (Curve 4) is determined to be 2.85 x 10^{-3} and, by applying Equation 2 once again, the calculation is:

$$GBP = \frac{2.85 \times 10^{-3}}{2\pi\ (57 \times 10^{-12})} = 7.96MHz$$

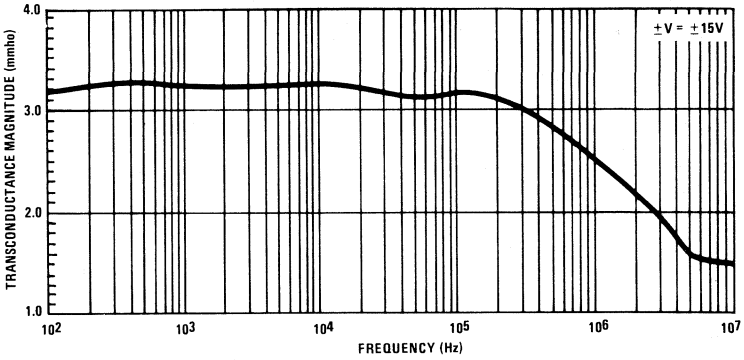
The variation of GBP vs. temperature for this example is:

$$\frac{8.94 - 7.96}{8.94} = 10.9\%$$

The above method applies only for the intermediate frequencies of the op amp since the gain becomes load dependent at both frequency extremes. This is due to the impedance of the op amp output stage being less than that of C_C at very high or very low frequencies.

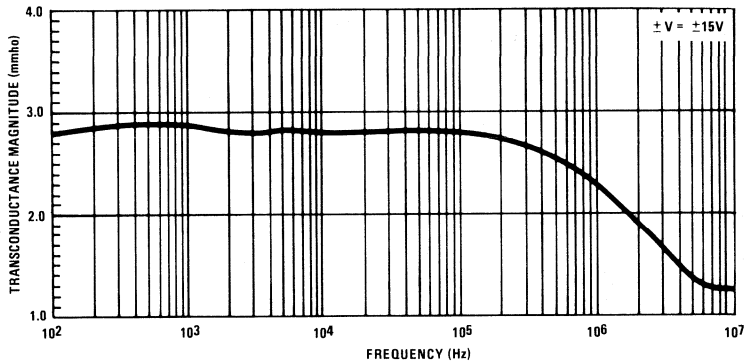
Finally, the transconductance curves provided are based on experimental data and should be considered as typical.

Curve 1



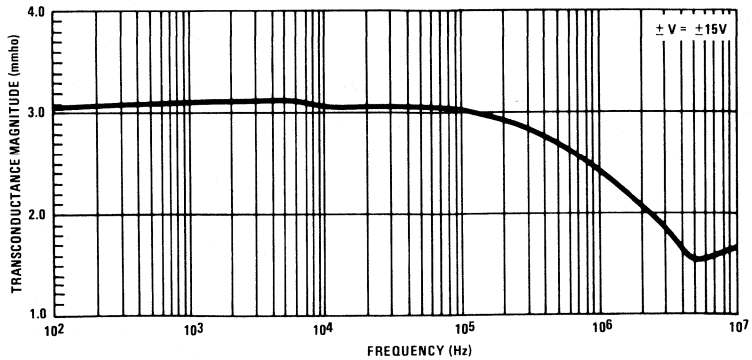
TRANSCONDUCTANCE MAGNITUDE vs. FREQUENCY T_A = 0°C

Curve 2



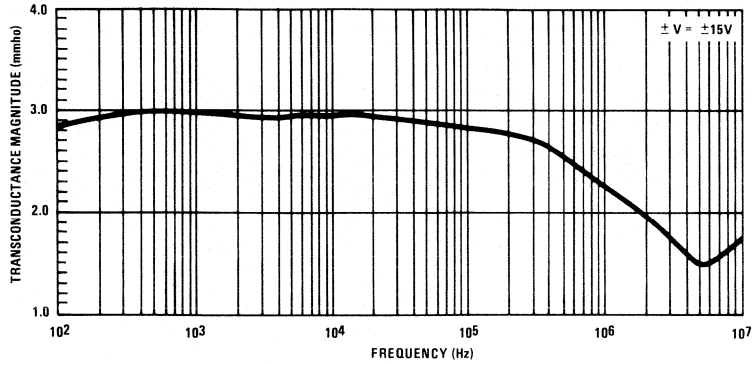
TRANSCONDUCTANCE MAGNITUDE vs. FREQUENCY T_A = +25°C

Curve 3



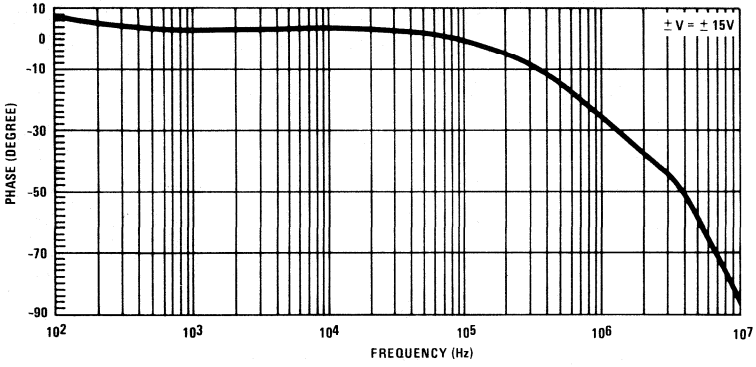
TRANSCONDUCTANCE MAGNITUDE vs. FREQUENCY T_A = +50°C

Curve 4



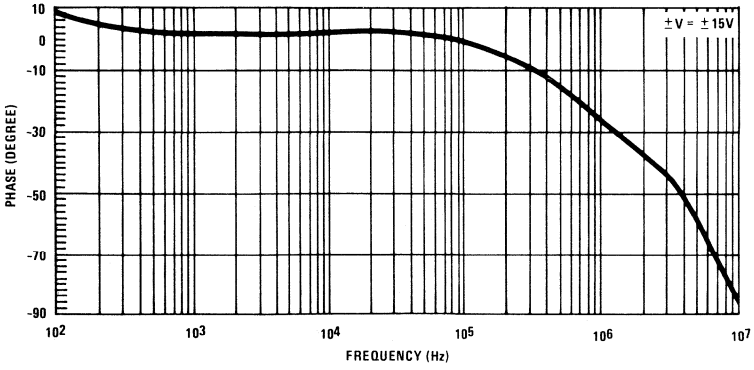
TRANSCONDUCTANCE MAGNITUDE vs. FREQUENCY T_A = +75°C

Curve 5



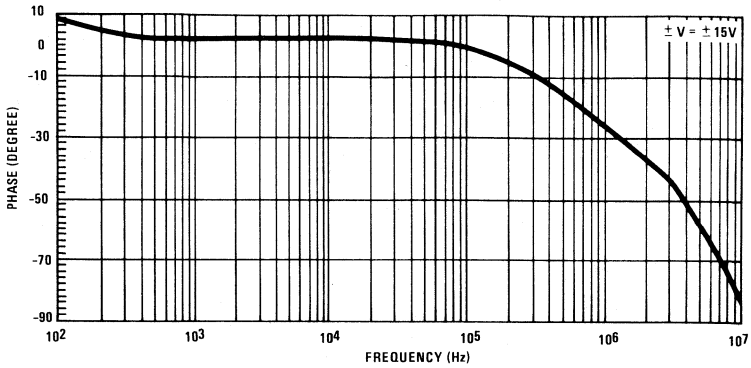
TRANSCONDUCTANCE PHASE vs. FREQUENCY T_A = 0°C

Curve 6



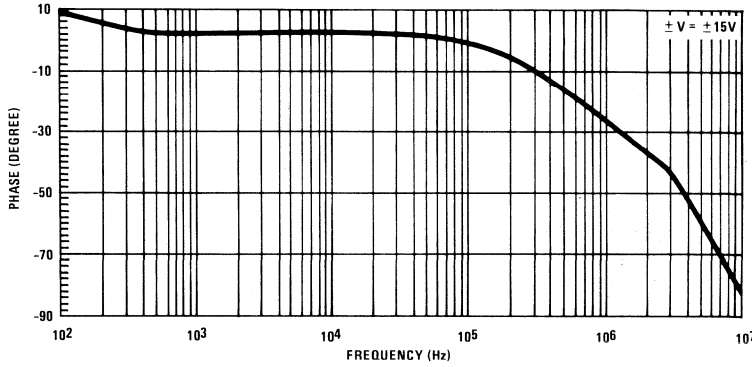
TRANSCONDUCTANCE PHASE vs. FREQUENCY T_A = +25°C

Curve 7



TRANSCONDUCTANCE PHASE vs. FREQUENCY T_A = +50°C

Curve 8



TRANSCONDUCTANCE PHASE vs. FREQUENCY T_A = +75°C

A DESIGNERS GUIDE FOR THE HA-5033 VIDEO BUFFER

Carl Wolfe

Introduction

Harris Semiconductor is an industry leader in the high speed, wideband, monolithic operational amplifier market. Due to the high performance of Harris products, designers in the more specialized areas of electronics have shown interest in utilizing these products in their applications. One such area is video design. In an effort to address this market, Harris has introduced the HA-5033 video buffer.

This paper will discuss the HA-5033 design and provide additional performance characteristics not shown in the data sheet.

HA-5033 Description

The HA-5033 is a unity gain monolithic I.C. designed for any application requiring a fast wideband buffer. A voltage follower by design, this product is optimized for high speed 50Ω and 75Ω coaxial cable driver applications common in color video systems.

Critical performance characteristics are summarized in Table 1. Outstanding differential phase/gain characteristics combined with an output current capability of ±100mA makes the HA-5033 an excellent choice for the line driver applications required in video circuit design.

PARAMETER	MIN	TYP	MAX	UNITS
Input Offset Voltage			15	mV
Input Bias Current			35	μA
Differential Phase		.1		degree
Differential Gain		.1		%
Slew Rate (±15V)	1000			V/μS
Output Current		±100		mA
Bandwidth (small signal)		250		MHz
Bandwidth (V_{IN} = 1 V_{RMS})		65		MHz
Supply Current			20	mA

TABLE 1. HA-5033 SPECIFICATIONS: T_A = +25°C; $\pm V_{SUPPLY}$ = ±12V (UNLESS OTHERWISE SHOWN)

Other features, which include a minimum slew rate of 1000V/μs, make the HA-5033 useful in high speed A/D data conversion and sample/hold circuits.

The HA-5033 is offered in two package configurations, the TO-8 metal can and the 8 pin epoxy Mini-Dip. The pinouts for each package are illustrated in Figure 1.

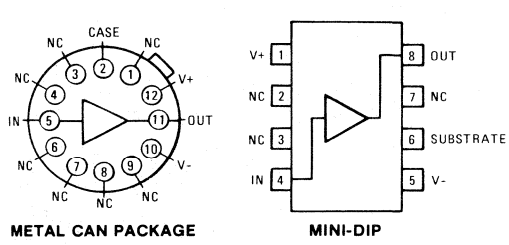


FIGURE 1. HA-5033 PINOUTS: TO-8 METAL CAN-PIN COMPATIBLE WITH THE LH0033 HYBRID. 8 PIN MINI-DIP - FABRICATED USING A COPPER LEAD FRAME. ADVANTAGES INCLUDE EXCELLENT THERMAL CHARACTERISTICS AND BOARD SPACE SAVINGS.

The high performance of this product (summarized in Table 1) is the result of the Harris High Frequency Dielectric Isolation Process. A major feature of this process is that it provides both PNP and NPN high frequency transistors which make wide bandwidth designs, such as the HA-5033, practical.

A Closer Look

Most manufacturer's data sheets provide a schematic diagram and depending upon the complexity of the product, this schematic may be comprehensive or possibly a simplified version. Schematics are a visual means of presenting information, ranging from reliability data, such as transistor counts, to circuit information for circuit analysis or computer simulation. But the most important reason for the schematic is to communicate to the customer the internal structure of the product and therefore, some insight into its operation.

At first glance, a schematic may appear as nothing more than a collection of resistors and transistors. But upon closer examination, particular areas of operation should become evident. Using the HA-5033 as an example (Figure 2), it will be shown that the HA-5033 consists of a signal path, bias network, and performance optimization circuitry.

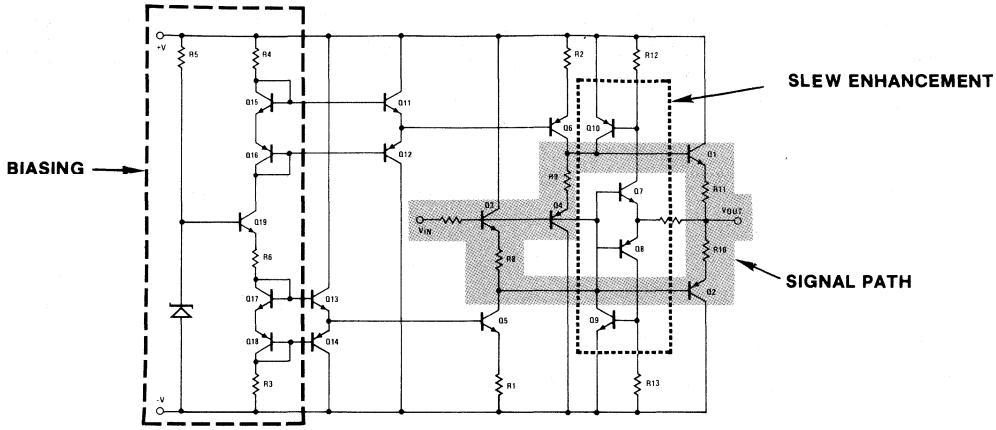


FIGURE 2. HA-5033 SCHEMATIC: VIDEO BUFFER DESIGN CONSISTS OF THREE OPERATING AREAS; SIGNAL PATH, BIAS NETWORK AND PERFORMANCE OPTIMIZATION CIRCUITRY.

Signal buffering is accomplished by cascading two emitter followers. In order to achieve symmetrical positive and negative output drive capability, two pairs are paralleled. The first pair consists of Q1 and Q4 for positive drive while the second pair Q2, Q3, provide negative drive. The emitter resistors of Q1, Q2 ensure stability with respect to load resistance, enhance differential phase/gain performance, and stabilize the quiescent operating point. This signal path has been high-lighted on the schematic.

The bias circuitry consists primarily of the diode-biasing located on the left portion of the schematic along with transistors Q5, Q6. This circuitry ensures the designed performance of the other active elements.

The performance optimization circuits are a slew enhancement circuit and a bias network buffer circuit. The transistors Q7, Q8, Q9 and Q10 are for slew enhancement. If the input voltage exceeds the output by one V_{BE}, Q7 will turn on Q10, which in turn provides extra base drive to Q1. Similary, Q9 will supply extra base drive to Q2.

Transistors Q11, Q12, Q13 and Q14 prevent high frequency or transient signals from affecting the bias circuitry. This prevents C_{CB} multiplication of current sources Q5 and Q6, which also improves differential gain/phase performance.

Note that output current limiting was not designed into the HA-5033. If there is a possiblity of the output being shorted to ground or the supplies, external current limiting will be necessary.

Any designer interested in using the HA-5033 should be aware of a characteristic related to output transistor operation. As the data sheet performance curves (reproduced in Figure 3) show, the output swing is a function of frequency. These curves show the point at

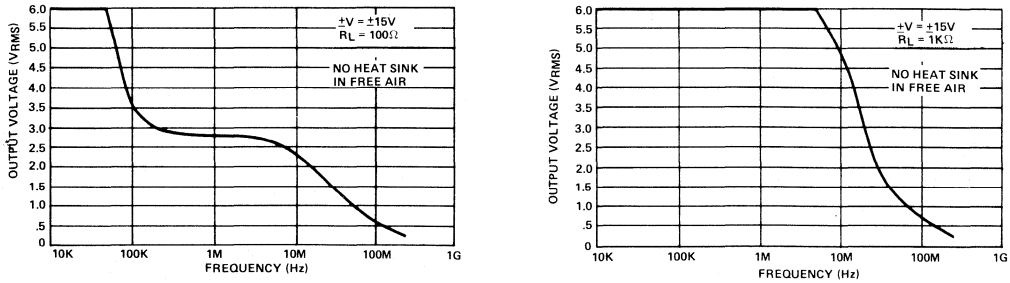


FIGURE 3. OUTPUT SWING VS. FREQUENCY PERFORMANCE CURVES: CURVES SHOW POINT OF OBSERVABLE DISTORTION FOR GIVEN FREQUENCY. OPERATION BEYOND THE CURVES SHOWN WILL APPROACH CONDITIONS WHERE OUTPUT TRANSISTORS ARE SIMULTANEOUSLY ON. THE RESULTING INCREASE IN CHIP TEMPERATURE WILL LEAD TO THERMAL RUNAWAY.

which observable distortion occurs for a given frequency. However, if the signal amplitude, signal frequency or both are increased beyond the curves shown, thermal "runaway" will occur. This is due to both the NPN and PNP output transistors approaching a condition of being simultaneously on. This condition has been computer simulated and the results are shown in Figure 4.

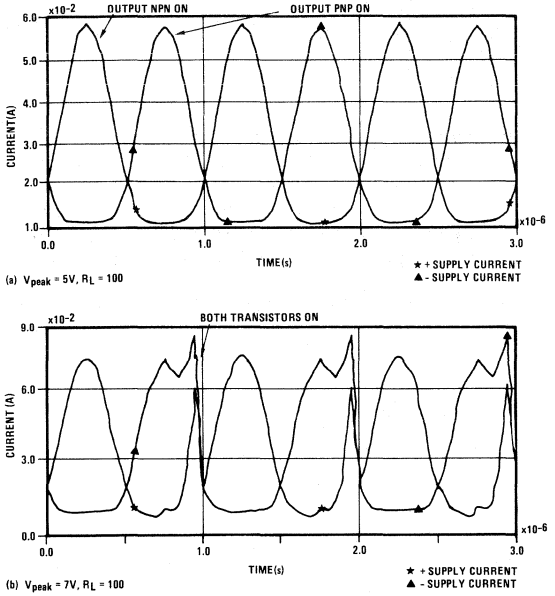


FIGURE 4. OUTPUT TRANSISTOR COMPUTER SIMULATION RESULTS

This condition occurs if the frequency of the analog signed does not allow sufficient time for the output PNP transistor to turn off. The frequency which causes this "push-push" output stage can be determined by using the following relationship,

$$\text{Full Power Bandwidth (FPB)} = \frac{SR}{2\pi V_p}$$

Where:
SR = Slew Rate
V_p = Analog Signal Peak Voltage

Therefore, the designer can determine the approximate frequency of thermal runaway by supplying the peak analog voltage and measuring the buffer slew rate for a particular application.

For example, the slew rate for the HA-5033 with a load of R_L = 1K ohm and C_L = 1000pFwas measured to be 83 V/μS. The FPB for a 5V peak analog signal was calculated,

$$FPB = \frac{83V/\mu S}{2\pi(5V)} = 2.6MHz$$

So the estimated frequency of thermal runaway for the given conditions is 2.6MHz. Measurements in the lab resulted in a thermal runaway frequency equal to 2.5MHz.

Although the FPB relationship gives the designer a method of estimating the frequency of thermal runaway, it is recommended that the HA-5033 be operated to the left of the curves shown in Figure 3. Heat sinking the buffer will not prevent this condition from occuring.

The purpose of heat sinking a semiconductor is to maintain the device junction temperature below a specified maximum limit. This is a thermal problem and can be evaluated using the thermal analog of Ohms Law illustrated in Figure 5.

Where:
P_{dmax} = Power Dissipated ($P_{DC} + P_{AC}$), Watts
T_j = Maximum Junction Temperature, °C
T_a = Ambient Temperature, °C
$\theta_{j\text{-}c}$ = Junction to Case Thermal Resistance, °C/W
$\theta_{c\text{-}s}$ = Case to Heat Sink Thermal Resistance, °C/W
$\theta_{s\text{-}a}$ = Heat Sink to Ambient Thermal Resistance, °C/W

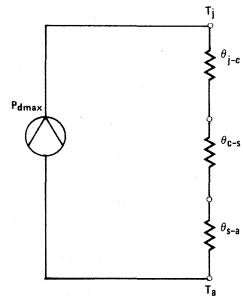


FIGURE 5. THERMAL ANALOG OF OHMS LAW: SEMICONDUCTOR /HEAT SINK SYSTEM

In this thermal system, current is replaced by power, voltage by temperature, and electrical resistance by thermal resistance. By using Figure 5, the following expression is derived,

$$P_{dmax} = \frac{T_{jmax} - T_A}{\theta_{j\text{-}c} + \theta_{c\text{-}s} + \theta_{s\text{-}a}}$$

This expression allows the designer to determine the maximum power dissipation of a semiconductor/heat sink system.

The expression for the semiconductor in free air is,

$$P_{dmax} = \frac{T_{jmax} - T_A}{\theta_{j-a}}$$

In order to make use of these expressions, the following information is required. θ_{j-c} and T_{jmax}, from the semiconductor manufacturer and θ_{c-s} and θ_{s-a}, from the heat sink manufacturer.

For the Harris HA-5033, the maximum junction temperature is $T_{jmax} = 200^oC$. The thermal impedances for the HA-5033 in the T0-8 metal can package are $\theta_{j-c} = 31^oC/W$ and $\theta_{j-a} = 99^oC/W$. The epoxy mini-dip thermal impedances are $\theta_{j-c} = 27^oC/W$ and $\theta_{j-a} = 90^oC/W$.

Recommended heat sinks for the HA-5033 in the T0-8 metal can package are the Thermalloy 2240A[1] and IERC-UP-T08-51CB[2] (base), IERC-UP-C7 (top). Thermal impedances are $\theta_{s-a} = 27^oC/W$ and $\theta_{s-a} = 10^oC/W$, respectively. θ_{c-s} is dependent upon the type of insulator or thermal joint compound used. Both products are two piece heat sinks, but differ in design.

By using the given product information and supplying an operating ambient temperature, the designer can determine the maximum power the system will dissipate and not exceed the maximum junction temperature.

For example, Figure 6 shows the maximum power dissipation for the HA-5033 in a T0-8 metal can package to be 1.75W at 25°C.

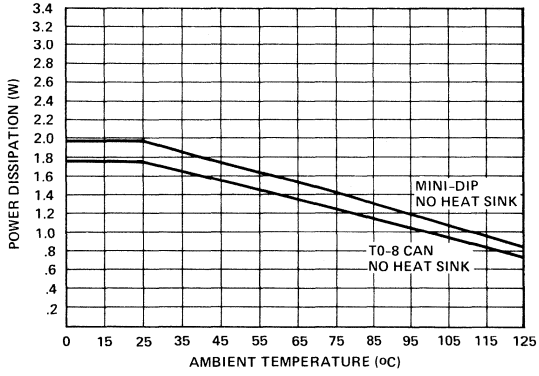


FIGURE 6. HA-5033 MAXIMUM POWER DISSIPATION VS AMBIENT TEMPERATURE: FREE AIR

The maximum power dissipation of the HA-5033/2240A heat sink system is calculated to be,

$$P_{dmax} = \frac{200-25}{31+27} = 3.01W$$

Therefore, the HA-5033 used with the Thermalloy 2240A can dissipate 3.0W at 25°C and not exceed the maximum junction temperature of 200°C.

The power dissipation limits shown in Figure 6 and those determined with the heat sink apply for both quiescent and load related power. Therefore,

$$P_{dmax} > P_{DC} + P_{AC}$$
$$P_{DC} = (+V)(+I) + (-V)(-I)$$
$$P_{AC} = (1/T)_O\int^T v(t)\, i(t)\, dt$$

Video Performance

The images which appear on your television picture tube are created by a process called scanning[3]. Scanning is a method of recreating the optical image of a scene one line at a time. Referring to Figure 7a, an electron beam moves or "scans" from left to right and quickly returns to a position below its starting spot. This process continues until the bottom of the picture is reached and the beam returns to the original top left hand position. This method is called sequential scanning.

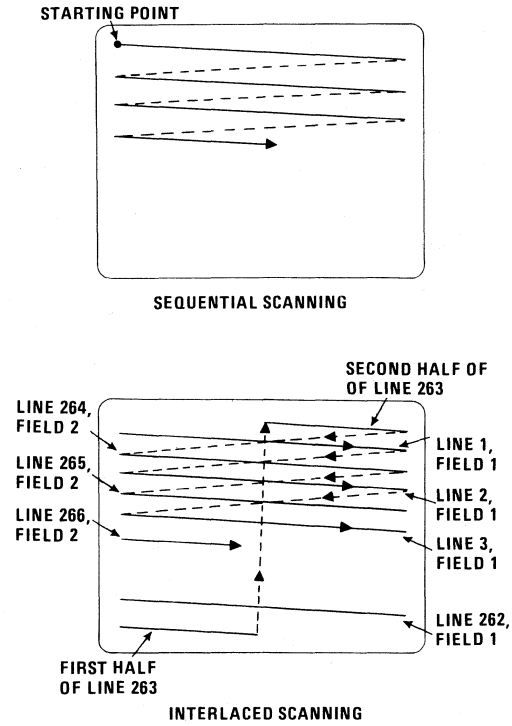


FIGURE 7. SCANNING SEQUENCE

Incorporated into present television broadcast standards is a technique called interlaced scanning. Interlaced scanning recreates the scene by providing two half scans. As shown in Figure 7b, the first scan traces out the odd numbered lines, the second scan fills in the even numbered lines. This technique avoids the flicker problem and excessive bandwidths required for similar picture definition using sequential scanning.

The United States NTSC (National Television Systems Committee) broadcast standard is a 525 line standard. Each scan consists of 262½ lines. The first scan is known as field one, the second, field two. Therefore, the complete picture consists of two fields.

The first 21 lines of each field are blank. Those lines are left open and are not used to broadcast video information. Instead, these lines contain other important information, such as sync pulses, data transmission, and test signals. The test signals contained in these lines are called the Vertical Interval Test Signals (VITS)[4,5], which allows real-time monitoring of the television broadcast signal quality. These test signals were used to evaluate the video performance of the HA-5033.

Four test signals are commonly used in the vertical interval. They are the multiburst, color bar, composite and vertical interval reference. These test signals are shown in Figures 8 through 11.

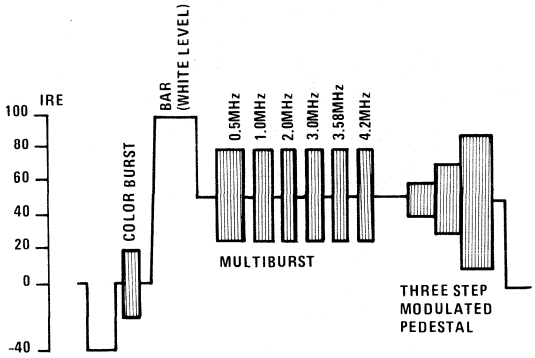


FIGURE 8. MULTIBURST SIGNAL (FIELD 1, LINE 17) ALLOWS FREQUENCY RESPONSE CHECKS

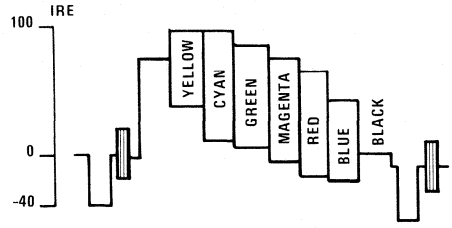


FIGURE 9. COLOR BAR (FIELD 2, LINE 17) ENABLES MONITORING OF COLOR TRANSMISSION QUALITY

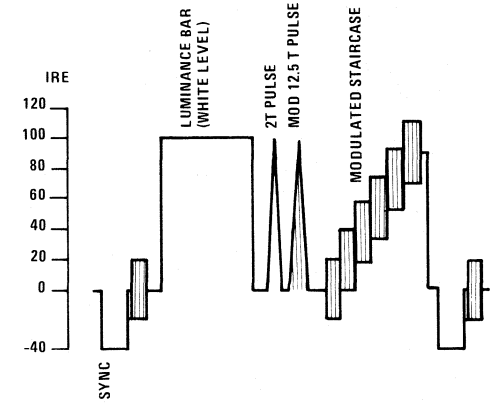


FIGURE 10. COMPOSITE SIGNAL (FIELD 1, AND 2, LINE 18) DESIGNED FOR GAIN AND TIME DELAY TESTS

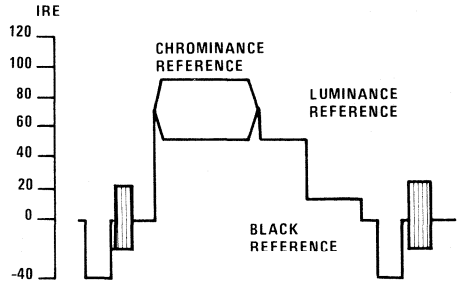
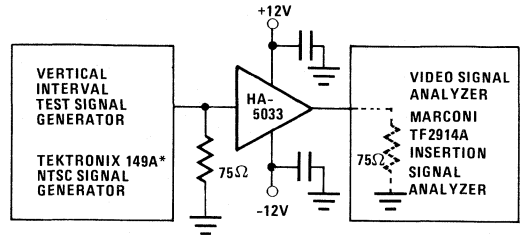


FIGURE 11. VERTICAL INTERVAL REFERENCE SIGNAL (FIELD 1 AND 2, LINE 19) PROVIDES COLOR AND GAIN REFERENCES

Each test signal was created to allow various distortions to be measured without interfering with the normal video transmission. These signal distortions which exist in television systems are defined as linear or non-linear. Non-linear distortion, such as differential phase and gain, vary with the amplitude of the picture signal. Linear distortions, usually dependent upon frequency response, are independent of signal level. For example, the multiburst test signal is very useful for frequency response checks, where as the composite signal contains signals for checking gain error.

Determining the HA-5033's performance level with respect to the NTSC standard required the definition of a measurement method. Test equipment was needed that would produce the necessary NTSC test signals and also monitor the device under test performance. The test configuration, shown in Figure 12 consisted of a Tektronix 149A NTSC[6] generator and Marconi TF 2914A video analyzer[7].



*TEKTRONIX 1910 NTSC DIGITAL GENERATOR RECOMMENDED

FIGURE 12. HA-5033 NTSC PERFORMANCE TEST CONFIGURATION

The TF 2914A has the capability of measuring 24 separate video parameters. Other advantages include direct readout and much more accuracy than possible using scope methods. Table 2 lists the video parameters tested on the HA-5033 along with the particular VITS utilized by the TF 2914A.

VIDEO PARAMETER	VERTICAL INTERVAL TEST SIGNAL USED
Luminance Bar Amplitude	Luminance Bar, Composite Signal (Fig. 10)
Sync Amplitude	Sync Pulse, Composite Signal (Fig. 10)
2T Pulse to Bar Ratio	2T Pulse/Luminance Bar, Composite Signal (Fig. 10)
Chrominance to Luminance Gain Inequality	Chrominance Component Amplitude of the 12.5T Pulse and Luminance Bar Amplitude, Composite Signal (Fig. 10)
Chrominance to Luminance Delay	Time Difference of Chrominance and Luminance Components of the 12.5T Pulse, Composite Signal (Fig. 10)
Luminance Non-Linearity	Largest and Smallest Step Amplitude of the Modulated Step Staircase, Composite Signal (Fig. 10)
Signal to Noise Ratio	Luminance Bar Level to Noise Voltage, Composite Signal (Fig. 10)
Chrominance to Luminance Crosstalk	Chrominance Component of 3 Step Modulated Pedestal and Luminance Bar, Multiburst Signal (Fig. 8)
Low Frequency Error	Amplitude of Low Frequency Signals
Bar Tilt	Difference of Luminance Bar Amplitude, Composite Signal (Fig. 10)
2T K Factor	2T Pulse, Composite Signal (Fig. 10)
Differential Gain	Amplitude Deviation of Modulated Step Staircase, Composite Signal (Fig. 10)
Differential Phase	Phase Deviation of Modulated Step Staircase, Composite Signal (Fig. 10)
Flag	Luminance Amplitude, Multiburst Signal (Fig. 8)
Multiburst 1-6	Amplitude of Each Frequency Burst, Multiburst Signal (Fig. 8)
Color Reference Burst Amplitude	Color Burst Amplitude, Multiburst Signal (Fig. 8)

TABLE 2. TF 2914A VIDEO MEASUREMENT PARAMETERS REFERRED TO VERTICAL INTERVAL TEST SIGNALS

Since the TF 2914A measurement includes any inaccuracies of the NTSC signal generator, a "delta" measurement was neccesary. The NTSC generator was connected directly to the analyzer and the results recorded. Next, the HA-5033 was inserted and the results recorded. The difference between the two readings was considered the actual HA-5033 performance. Table 3 lists the video performance results of the HA-5033.

VIDEO PARAMETER	HA-5033	UNITS
Luminance Bar Amplitude	93.6	IRE*
Sync Amplitude	37.5	IRE
2T Pulse to Bar Ratio	99.9	IRE
Chrominance to Luminance Gain Inequality	99.9	IRE
Chrominance to Luminance Delay	1.5	nS
Luminance Non-Linearity	0.1	%
Signal-to-Noise Ratio	66	db
Chrominance to Luminance Crosstalk	51.6	IRE
Low Frequency Error	0.3	mv
Bar Tilt	0.3	IRE
2T K Factor	0.1	K
Differential Gain	0.1	%
Differential Phase	0.1	degree
Flag	99.5	IRE
Multiburst 1 Amplitude	49.2	IRE
Multiburst 2 Amplitude	49.3	IRE
Multiburst 3 Amplitude	51.0	IRE
Multiburst 4 Amplitude	50.4	IRE
Multiburst 5 Amplitude	49.7	IRE
Multiburst 6 Amplitude	50.0	IRE
Color Reference Burst Amplitude	40.4	IRE

TABLE 3. HA-5033 NTSC VIDEO PERFORMANCE

* IEEE Standard 205-1958 defines the levels of television video signal in terms of IRE units. 100 IRE units = 0.714V, P-P

Applying The HA-5033

The most important consideration when designing with the HA-5033 is layout. The wide bandwidth of the buffer necessitates that high frequency layout procedures be followed. Recommended procedures include the use of a ground plane, minimization of all lead lengths, avoiding sockets, and proper power supply decoupling.

Standard practice in RF/Video layout is the use of a ground plane. A ground plane minimizes distributed circuit capacitance and inductance which degrade high frequency performance. The ground plane can also incorporate the metal case of the HA-5033, since pin #2 is internally tied to package. This feature allows the user to make contact between the ground plane and the package which extends shielding, provides additional heat sinking and eliminates the use of a socket. IC sockets contribute bandwidth limiting interlead capacitance and should be avoided.

For the epoxy mini-dip, additional heatsinking can be derived from soldering the no connection pins #2, 3, and 7 to the ground plane. Also, pin #6 can be tied to either supply, grounded or left open. But to optimize device performance and improve isolation, it is recommended that this pin be grounded.

Another method of enhancing device performance is power supply decoupling. For the HA-5033, it is recommended that the positive and negative power supplies be bypassed with capacitors to ground. Ceramic capacitors ranging in value from .01 to .1 μF will minimize high frequency variations in supply voltage. Solid tantalum capacitors 1μF or larger will optimize low frequency performance. It is also recommended that the bypass capacitors be connected as close to the HA-5033 as possible, preferably directly to the supply pins.

Finally, keeping all lead lengths as short as possible will minimize distributed capacitance and reduce board space. It is essential that the guidelines dis-

cussed above be followed to avoid marginal performance.

Another consideration when applying the HA-5033 is load capacitance. Although the HA-5033 is designed to handle load capacitance values up to .01μF, it has a worst case stability region in the area of 50pF. The computer simulation of the HA-5033 frequency response in Figure 13 illustrates the gain peaking which occurs in the 150MHz region.

There are three suggested methods of dealing with this particular characteristic of the HA-5033. Isolating the load capacitance from the buffer output is the object of the first method. This is accomplished by placing a series resistor between the output and the load.

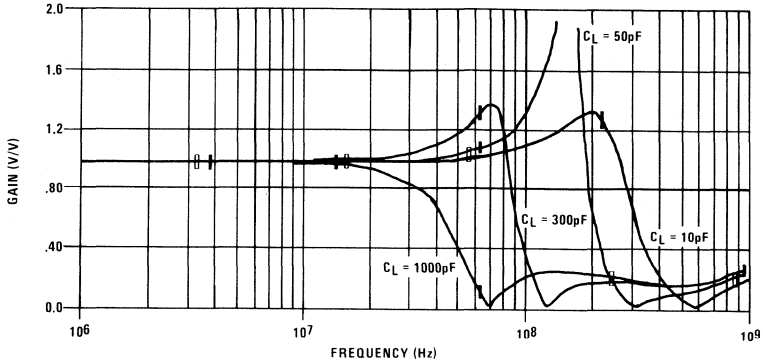


FIGURE 13. COMPUTER SIMULATION OF HA- 5033 GAIN CHARACTERISTICS VS FREQUENCY AND LOAD CAPACITANCE

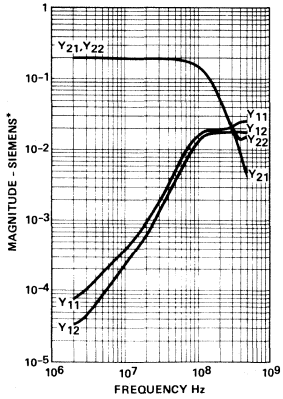
A second technique utilizes the HA-5033 frequency response with respect to load capacitance. Referring once again to Figure 13, notice that the gain peaking is removed with additional load capacitance. This is the basis of method two, adding additional load capacitance to approach a region of stability.

A drawback to adding more load capacitance is that the buffer's dynamic characteristic will degrade and bandwidth performance will be less than data sheet specifications. The third method solves this trade-off by using a "bootstrap" technique of adding capacitance from input to output. This method achieves stability without sacrificing performance.

An explanation of why adding capacitance will stabilize the HA-5033 can be found in the Y parameter data shown in Figure 14. The expression for the buffer gain in terms of Y parameter is:

$$A_V = \frac{V_{OUT}}{V_{IN}} = \frac{-Y_{21}}{Y_{22} + Y_L}$$

Y_{21} = Forward Transmittance
Y_{22} = Output Admittance
Y_L = Load Admittance



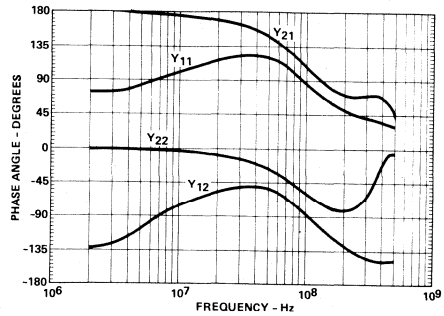


FIGURE 14. HA-5033 Y PARAMETER DATA

Notice that the load admittance, Y_{22}, phase becomes inductive ($-jY_L = -90^o$) at high frequency. So if the load, Y_L, is capacitive ($+jY_C = +90^o$) and the sum of $Y_{22} + Y_L$ become small, peaking occurs. Adding additional capacitance changes the effective phase angle and peaking can be reduced.

Using the HA-5033 as the analog input buffer of a flash converter is an example of application where the suggested stabilization methods are useful. Although its been stressed to keep all distributed capacitance to a minimum to optimize device operation, the load which a flash converter presents to the buffer represents a greater concern.

Flash or parallel converters are a special case, since the analog input circuit must drive a non-linear input impedance[8]. This non-linearity is due to the potential input impedance changes of the 255 parallel comparators which comprise the converter analog input. In addition to the non-linearity, the input capacitance of these converters tends to be relatively large, 100-300pF.

Example of the various stabilization methods tested with the TWR 1007 8 bit video flash converter are shown in Figure 15. Figure 15a illustrates the series resistor method. 15b is the load capacitance method and 15c is the bootstrap method. Photographs of the experimental results show the analog input sampling convert signal (pin 30), the MSB digital output (D1 pin 40), and the buffer output (converter input).

It is recommended that a complete evaluation for each method be conducted to determine the optimum component values. The value of the series resistor will depend upon the input capacitance of the particular converter used. A suggested starting value is 50ohms. With the capacitance methods, the distributed capacitance of the layout will affect component values. These experimental results were obtained using C = 240pf.

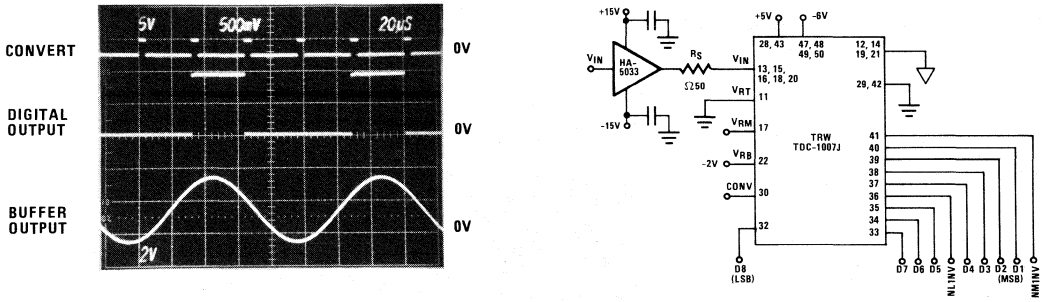


FIGURE 15a. ENHANCING 5033 PERFORMANCE IN FLASH CONVERTER APPLICATIONS: SERIES RESISTOR METHOD

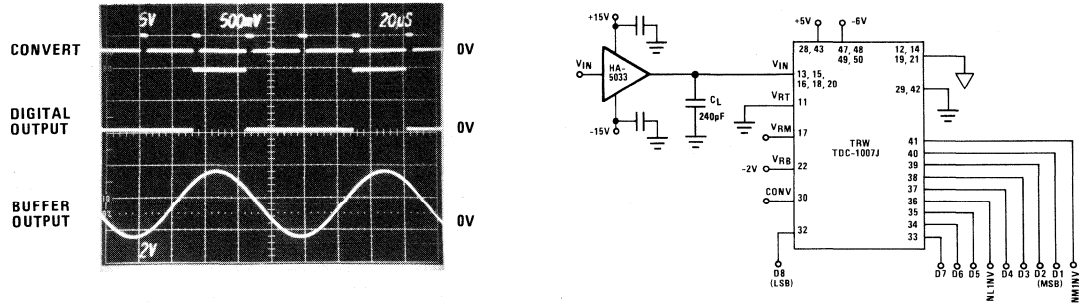


FIGURE 15b. LOAD CAPACITANCE METHOD

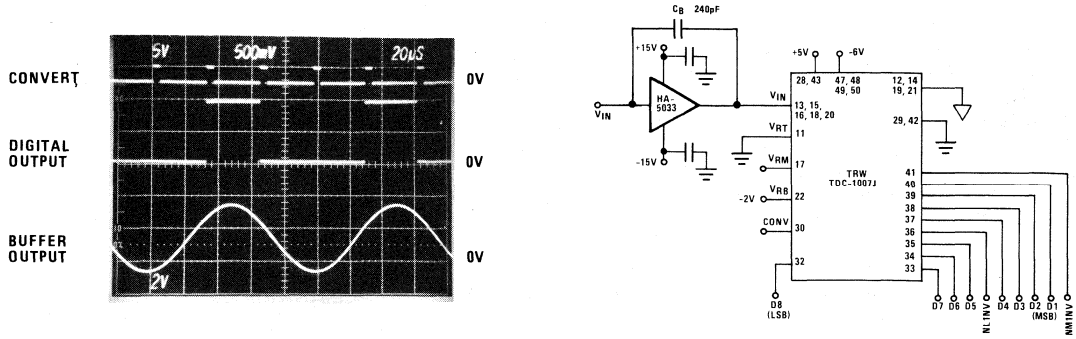
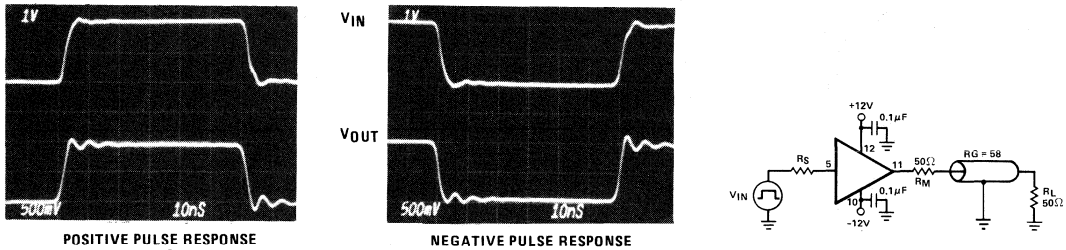


FIGURE 15c. BOOTSTRAP CAPACITANCE METHOD

The signal levels in most video applications are 1V p-p or less. Although the HA-5033 was shown with ±15V power supplies in the converter applications, lower power supplies will accommodate these video signal levels. For example, at ±5V power supplies, the HA-5033 can swing ±2V into a 75 ohm load.

The HA-5033 is an excellent high speed line device capable of driving 50 ohm and 75 ohm coaxial cable.

These type of drive requirements are common in video circuit design. Figures 15 and 16 illustrate two typical application examples. Figure 15 is an example of a 50 ohm system using the HA-5033 alone. R_m matches the buffer output impedance to the cables characteristic impedance. Depending upon the response required, this resistor may not be necessary. If used, the output voltage will be one half the input voltage.



POSITIVE PULSE RESPONSE
$T_A = 25^oC$
$R_S = 50\Omega$
$R_M = R_L = 50\Omega$
$V_O = V_{IN}\left(\frac{R_L}{R_L + R_M}\right) = ½\ V_{IN}$

NEGATIVE PULSE RESPONSE
$T_A = 25^oC$
$R_S = 50\Omega$
$R_M = R_L = 50\Omega$
$V_O = V_{IN}\left(\frac{R_L}{R_L + R_M}\right) = ½\ V_{IN}$

FIGURE 15. VIDEO COAXIAL LINE DRIVER - 50 OHM SYSTEM

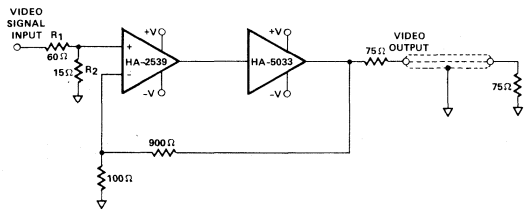


FIGURE 16. VIDEO GAIN BLOCK

Figure 16 illustrates the use of the buffer within the feedback loop of an operational amplifier. This configuration provides additional output current capability for the HA-2539 op amp and gives the designer voltage gain control.

Another application which utilizes the HA-5033's output drive capability is the high speed sample and hold circuit shown in Figure 17. The input buffer provides drive current to the hold capacitor while the output buffer functions as a data line driver. The switching element in this application is the HI-201HS high speed CMOS switch which contributes it's own benefits to the application[9]. Depending upon the application requirements, using the HA-5033 as the output buffer in Figure

17a may not be acceptable. Lab tests have shown that the input bias current of the HA-5033 becomes a factor for low values of hold capacitance ($< .01\mu F$) during the hold mode.

A solution is to add a low bias current F.E.T. input stage, as shown in Figure 17b. Q1 acts as a voltage follower and Q2 is a current source. Matching Q1, Q2 and R1, R2 are important considerations in order to minimize offset voltages.

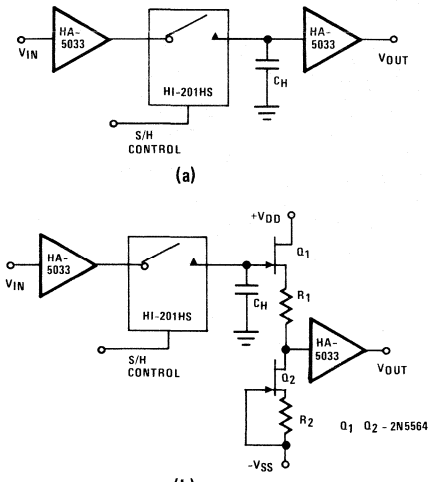
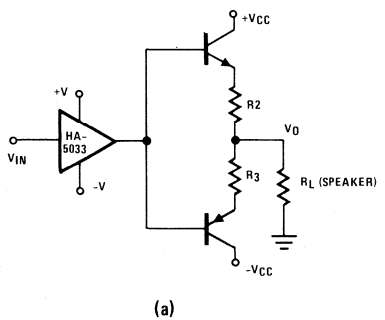


FIGURE 17a. HIGH SPEED SAMPLE/HOLD (b) MODIFIED OUTPUT BUFFER

When the drive capability of the HA-5033 is insufficient, consider adding an external output stage. Figure 18a illustrates an example where a push-pull complementary output stage has been added to the HA-5033. Although unable to drive the low impedances of speakers, typically 4-8 ohm, the buffer can be used to drive audio output transistors. A variation of this configuration is shown in Figure 18b, where separate buffers individually drive each transistor base. A low noise input stage is provided by the HA-5102.



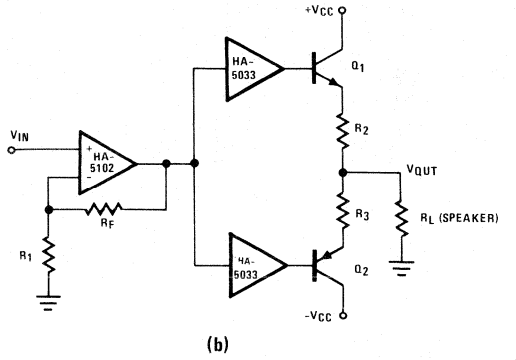


FIGURE 18. AUDIO DRIVERS

A common method of achieving an audio oscillator circuit is to use a transistor or IC amplifier with LC or RC feedback. An alternative technique of generating sinusoidal waveforms, using the HA-5033, is shown in Figure 19. Crystal oscillators offer improved frequency stability over time and temperature. This particular oscillator configuration[10] produces an 18.18 MHz, $2.8V_{p-p}$ sinusoidal waveform into a 1K ohm load.

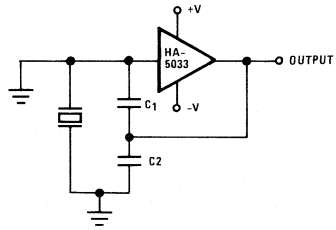


FIGURE 19. CRYSTAL OSCILLATOR: ±V = ±15V, C1 = 12pF, C2 = 39pF, 18MHz QUARTZ CRYSTAL

Conclusion

The HA-5033 is a high performance integrated circuit presently being utilized in a wide variety of applications. This paper has provided additional information to aid designers in applying the HA-5033 video buffer in future applications.

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Acknowledgements

1. Technical contributions of John Prentice and Robert Junkins.

2. Sales and Technical Staff of Marconi Instruments.

THE HC-550X TELEPHONE SUBSCRIBER LINE INTERFACE CIRCUITS (SLIC)

Geoff Phillips, C. Eng., M.I.E.E.

1.0 Introduction

The HC-550X family of telephone subscriber line interface circuits (SLIC) integrate most of the BORSCHT functions of the traditional hybrid and transformer interface circuits onto one chip. The circuits are manufactured in a 200V dielectric isolation (DI) process and together with a secondary protection diode bridge give 1kV of isolation from lightning induced faults between the subscriber loop and the telephone office.

The BORSCHT functions provided are:

- BATTERY FEED WITH LOOP CURRENT LIMITING
- OVERVOLTAGE PROTECTION
- RINGING
- SUPERVISION/SIGNALING
- HYBRID

The HC-5502A is intended for use in systems utilizing single ended tip (positive side) injected ringing and limits the short loop current to 30mA; the HC-5504 is intended for use in ring side (negative side) injected ringing systems and will limit the short loop current to 40mA. It should be noted that the HC-5504 can also be configured to operate in switches employing either of the two single ended ringing methods and in balanced ringing systems.

This note will describe each subfunction of the SLIC and will discuss several system design features, including balance networks and complex impedance matching.

2.0 An Overview of the Basic Phone Loop And Its Environment

Figure 1 illustrates a simplified telephone network. Each subscriber is connected via a 2 wire (2W) loop to a switch office which provides intersubsciber loop switching and signal processing (analog and/or digital).

The SLIC is the primary interface between the 4 wire (4W) (ground referenced) low voltage switch environment and the 2W ("floating") high voltage loop environment.

The loop consists of a wire A (the Tip wire), the telephone set or its equivalent, and wire B (the ring wire). A DC voltage is applied across the Tip and Ring wires at the line card which is housed in the telephone office: The battery is usually a nominal -48V, and is often called the quiet or talking battery. When the telephone is off-hook, a DC path is established around the loop. DC loop current will flow around the loop from tip feed to ring feed. This is called Battery Feed.

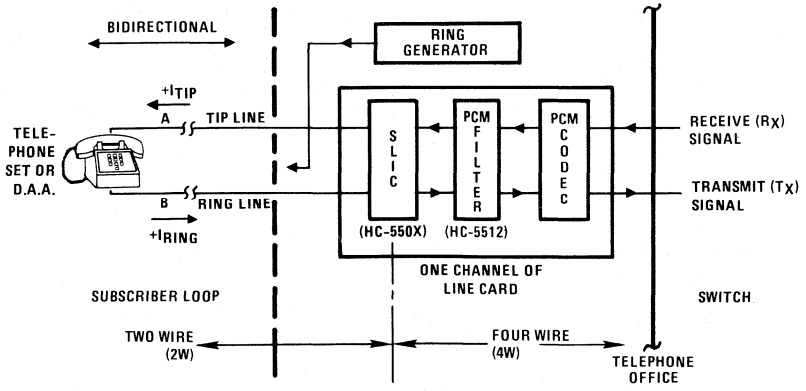


FIGURE 1. SIMPLIFIED TELEPHONE NETWORK.

The SLIC must be able to sense this DC current and flag the switch controller: This is referred to as Switch Hook Detection (SHD). It tells the switch controller that the line is busy, and is a supervisory function.

The subscriber set is often located very close to the switch office. Thus, the loop resistance will be very low and the SLIC should incorporate a feedback network that will limit the loop current to a specified maximum to prevent battery power drain and minimize power dissipation at the board level. The HC-550X SLICs sense the loop current and adjust the voltage on the ring side of the line to cause line current saturation.

The telephone can be rung by switching a ring relay to connect a ring generator to the loop. The on-off switching of the relay (cadencing) is controlled by the Ring Command (RC) input which gates the relay driver output. When the user answers the telephone, the ring relay is automatically tripped, the ring command signal is inhibited and the 2W loop is made ready for voice transmission. Voice signals are transmitted onto the loop by directly modulating the DC feed. This AC voice signal is coupled to the users earpiece via a transformer in the telephone set. Voice transmission for the 2W to the 4W system is called the hybrid function. For 2W to 4W transmission, the subscriber talking into his set modulates the resistance of the telephone microphone. This causes AC current in the loop which is sensed by the SLIC and transmitted as a ground referenced voltage signal to the signal processing electronics within the switch.

Subscriber loops are usually measured in terms of loop resistance. The nominal loop length is 1200 ohms. Owing to the length of the lines and their location near power lines, common mode or longitudinal currents are often induced. The SLIC has to distinguish between these noise signals (longitudinal) and the transversal signals, and reject the unwanted longitudinal components: this is a measure of the SLIC's longitudinal balance. The primary noise sources are 60/50Hz power lines, cable cross talk, and R.F. transmissions. The Harris SLICs will accomodate $15mA_{RMS}$ of noise currents on each side of the loop.

The line is also subjected to lightning strikes. Together with primary and secondary protection networks, the SLIC must withstand 1kV peak of lightning induced energy. In fact, the plastic encapsulated Harris SLIC can withstand a 1kV peak strike with a small signal diode bridge providing voltage clamping, and current steering.

3.0 The Harris HC-550X

The HC-550X family of SLICs are primarily intended for use within Private Branch Exchanges (PBX) although they can be used in the larger switch networks found in Central Offices (C.O.).

Figure 2 shows the functional schematic of the SLIC. The subfunctions to be described are:

A. Line Feed Amplifiers
B. Transversal Amplifiers
C. Loop Current Limiting: Metallic, Fault and Thermal Limiting
D. Ring Trip and Ground Key Detection
E. Spare or Uncommitted Operational Amplifier
F. Logic Network

3.1 Line Feed Amplifiers

The line feed amplifiers are high power op amps, and are connected to the subscriber loop through 300 ohms of feed resistance; the configuration is shown in Figure 3. The feed resistors provide a 600 ohm balanced load for the 2W to 4W transmission, and limit longitudinal currents; the two resistors immediately adjacent to the feed amplifiers function as sense resistors for 2W to 4W transmission and signalling purposes.

The tip feed amplifier is configured as a unity gain non-inverting buffer. A -4V bias (derived from the negative battery (V_{B-}) in the bias network) is applied to the input of the amplifier. Hence, the tip feed DC level is at -4V. The principal reason for this offset is to accomodate sourcing and sinking of longitudinal noise currents up to $15mA_{RMS}$ without saturating the amplifier output. The tip feed amplifier also feeds the ring feed amplifier, which is configured as a unity gain inverting amplifier as seen from the TF amplifier. The noninverting input to the RF amp is biased at a VB-/2. Looking into this terminal the amplifier has a noninverting gain of 2. Thus, the DC output at ring feed is:

$$V_{RF}(DC) = (4 + VB-) \text{ Volts}$$

For a -48 volt battery, V_{RF} = -44 volts. Hence, the nominal battery feed across the loop provided by the SLIC is 40 volts. When the subscriber goes off-hook this DC feed causes current (metallic current) to flow around the loop.

The received audio signal V_{RX} from the switch is fed into the tip feed amplifier and appears at the TF terminal. It is also fed through the ring feed amplifier and is inverted. Thus, a differential signal of $2V_{RX}$ appears across the line: for a 600 ohm line this compensates the 6dB loss due to the 600 ohms of line feed resistance. The V_{RX} signal causes AC audio currents to flow around the loop which are then AC coupled to the earpiece of the telephone set. Figure 4 shows the single ended AC equivalent circuit of the subscriber loop for voice transmission. In the general case the signal design equation for 4W to 2W transmission is given by:

$$V_{LINE} = \left(\frac{Z_{LINE}}{600 + Z_{LINE}} \right) \times 2V_{RX}$$

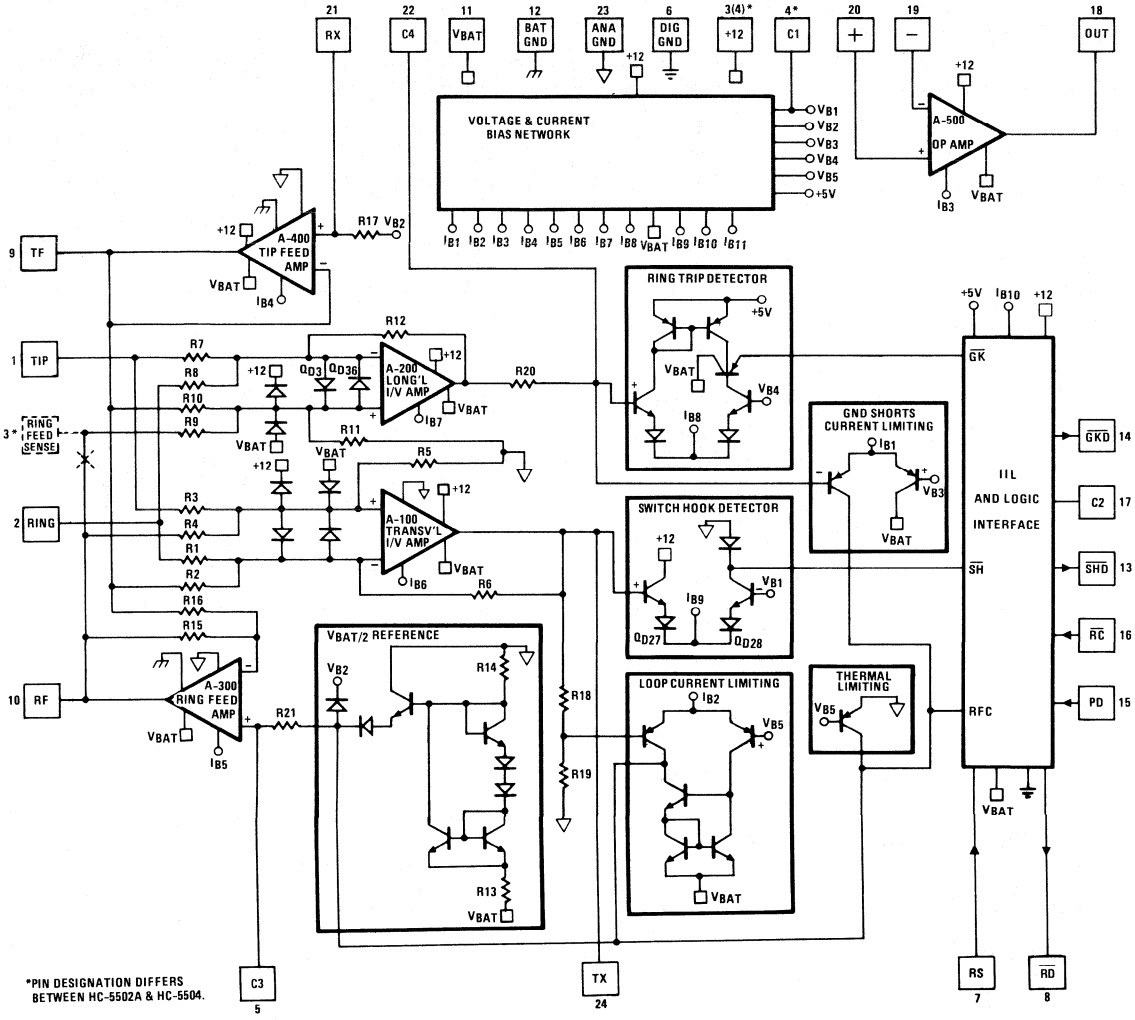


FIGURE 2. SLIC FUNCTIONAL SCHEMATIC.

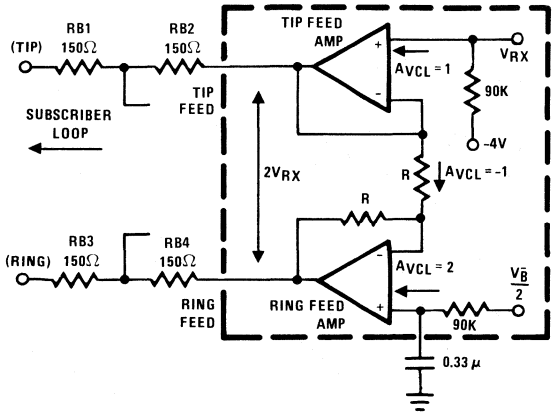


FIGURE 3. LINE FEED AMPLIFIERS.

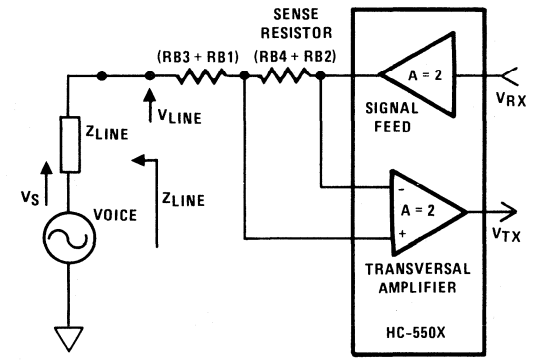


FIGURE 4. SINGLE ENDED AC SIGNAL EQUIVALENT CIRCUIT.

3.2 The Transversal Amplifier (TA)

Whereas the feed amplifiers perform the 4W to 2W transmission function, the transversal amplifier acts as the 2W to 4W hybrid. The TA is a summing amplifier configured to reject common mode signals. It will thus reject 2W common mode signals. Figure 4 shows the single ended signal transmission path. Given below is the design equation of the 2W to 4W signal transmission. It can be seen that RB2 and RB4 act as loop current sense resistors, and that the voice signal output of the amplifier is a function of the differential voltages appearing across RB2 and RB4.

Thus, the transversal amplifier also has a DC output proportional to the metallic current in the loop. The output voltage is given by:

$$V_{TX} = 2(I_{TIP} + I_{RING})\ (R_{B2} + R_{B4})$$

where I_{TIP} and I_{RING} are assumed positive as indicated in Figure 1. This DC level is used as an input to a comparator whose output feeds into the logic circuitry as SH. This signal is used to gate SHD.

Voice signals on the loop are transformed by the TA into ground referenced signals as shown by the above equations. Since the TA output has a DC offset it is necessary to AC couple the output to any external circuitry. Note, that during 4W to 2W transmission, the transversal amplifier will have an audio signal at its output proportional to the 4W audio receive signal and the loop's equivalent AC impedance. This is called the transhybrid return, and must be cancelled (or balanced) out to prevent an echo effect. This is discussed more fully in Section 4 under Transhybrid Balancing.

3.3 Loop Current Limiting

The nominal loop length is equivalent to an 1800 ohm load across the feed amplifiers However, on a short loop the line resistance often approaches zero. Thus, a need exists to control the maximum DC loop current that can flow around the loop to prevent an excessive current drain from the system battery. This limit is typically specified between 30mA and 40mA for general PBX applications. Figure 5 depicts the feedback network that modifies the RF voltage as a function of metallic current. Figure 6 illustrates the loop current characteristics as a function of line resistance.

As indicated above, the TA has a DC voltage output directly proportional to the loop current. This voltage level is scaled by R19 and R18. The scaled level forms the 'Metallic' input to one side of a Transconductance Amplifier. The reference input to this amplifier is

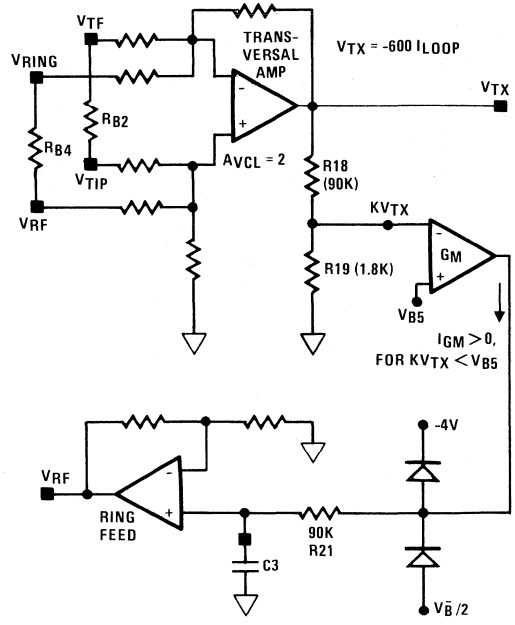


FIGURE 5. LOOP CURRENT LIMIT CONTROL.

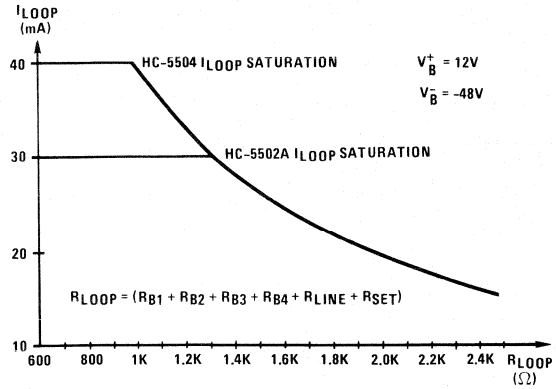


FIGURE 6. DC LOOP CURRENT CHARACTERISTICS.

generated in the bias network, and is equivalent to 30mA or 40mA loop current, typically, for the HC-5502A and HC-5504, respectively. When the metallic input exceeds the set reference level, the transconductance amplifier sources current. This current will charge C3 in positive direction causing the RF (Ring Feed) voltage to approach the TF (Tip Feed), effectively reducing the battery feed across the loop which will limit the DC loop current. C3 will continue to charge until an equilibrium level is attained at $I_{LOOP} = I_{LOOP}$ MAXmA. The time constant of this feedback loop is set by R21 (90K ohm) and C3 which is nominally 0.33μF.

The RF voltage level is also modified to reduce or control loop current during ring line faults (e.g. ground or power line crosses), and thermal overload. Figure 2 illustrates this. It can be seen that the thermal and fault current circuitry works in parallel with the transconductance amplifier.

3.4 Longitudinal Amplifier

The longitudinal amplifier is an op amp configured as a closed loop differential amplifier with a nominal gain of 0.1 (HC-5504) or 0.581 (HC-5502A). The output is a measure of any imbalance between I_{TIP} and I_{RING} as described in Figure 1. The transfer function of this amplifier is given by:

$$V_{LONG} = K(I_{TIP} - I_{RING})150$$

Where K is the gain factor of the amplifier. The gain factor is much less than one since ring voltage (up to $150V_{peak}$) can appear at the Ring or Ring Feed Sense terminals and are attenuated to protect the amplifier.

The longitudinal amplifier's principal functions are Ring Tip Detection (RTD) and Ground Key Detection (GKD). GKD provides a means for the subscriber to flag a PBX attendant and is used extensively in Europe: The ring line is grounded at the telephone set via a push switch incorporated within the telephone. This causes a DC current imbalance between the tip and ring sides of the loop which gives rise to a negative voltage at the output of the longitudinal amplifier. The output of the amplifier after being filtered by R20 and C4 to attenuate AC signals is fed into a detector whose output GK gates the necessary logic to drive GKD or inhibit the ring relay driver to remove ringing signals from the line in an off-hook condition. In order to prevent false ground key owing to line noise or during ring trip, the internal GKD logic is delayed via C2. An internal current source of 5μA has to charge C2 up to a 5V level before allowing the ground key signal to propagate. Thus, for C2 = 0.15μF, a delay of 150ms is established.

Ringing the line and Ring Trip Detection are discussed more fully in Section 4.

3.5 Uncommitted Op Amp

An uncommitted op amp is provided on the chip. This is a standard op amp with an output swing of ±5V. It is primarily intended to be used to balance the transhybrid return signal discussed in Section 3.2 above. The amplifier has an offset voltage of 10mV; an open loop gain of 66dB; a GBW product of 2MHz; slews at 1V/μs typically, and has a ±2mA output current drive capability.

3.6 The Logic Network

The logic network utilizes I^2L logic. All external inputs and outputs are LS TTL compatible: the relay driver is an open collector output that can sink 60mA with a V_{CE} of 1V.

Figure 7 is a schematic of the combination logic within the network. The external inputs RC (Relay Control) and PD (Power Denial) allow the switch controller to ring the line or deny power to the loop, respectively. The Ring Synchronization input (RS) facilitates switching of the ring relay near a ring current zero crossing in order to minimize inductive kick-back from the telephone ringer.

The internal inputs SH and GK control ring trip and provide supervisory flags to the system controller via the Switch Hook Detect (SHD) and Ground Key Detect (GKD) outputs.

4.0 Designing with the Harris SLIC

General application circuits for the HC-5502A and HC-5504 SLICs are given in Figures 8 and 9. In this section, several specific design and application areas will be discussed:

A. Ringing the Line
B. Power Denial
C. Transhybrid and Longitudinal Balance
D. Complex Impedance Matching
E. Surge Protection

4.1 Ringing The Line

The HC-5502A is used for tip injected ringing (also called single ended ground referenced ringing), and the HC-5504 is used for ring injected or single ended

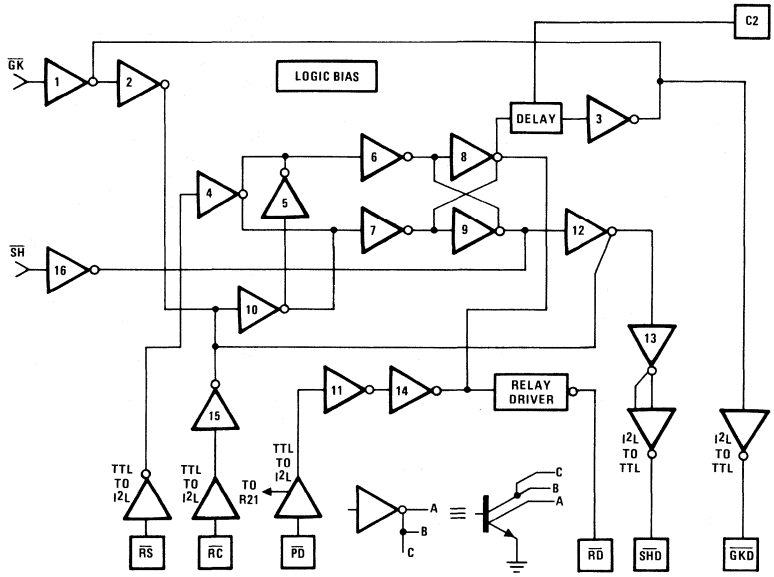
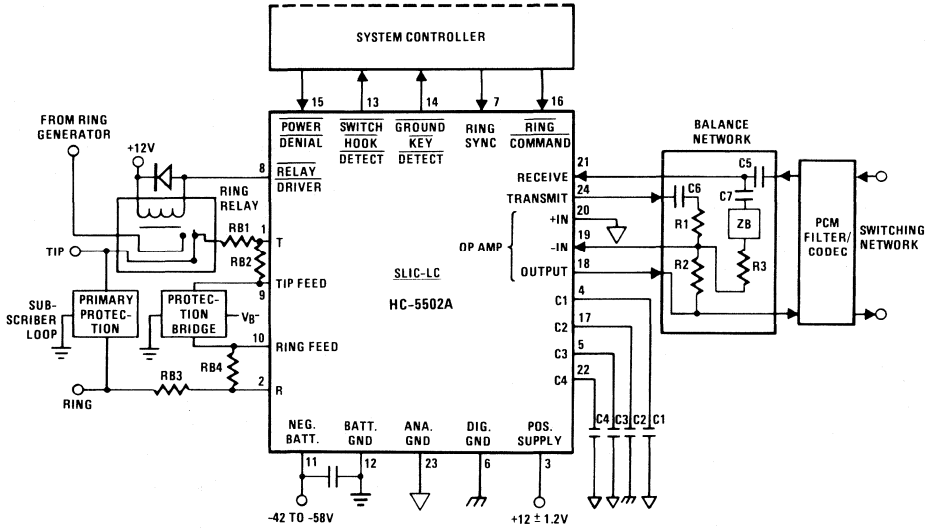


FIGURE 7. HC-5502A/04 LOGIC GATE SCHEMATIC.



TYPICAL COMPONENT VALUES

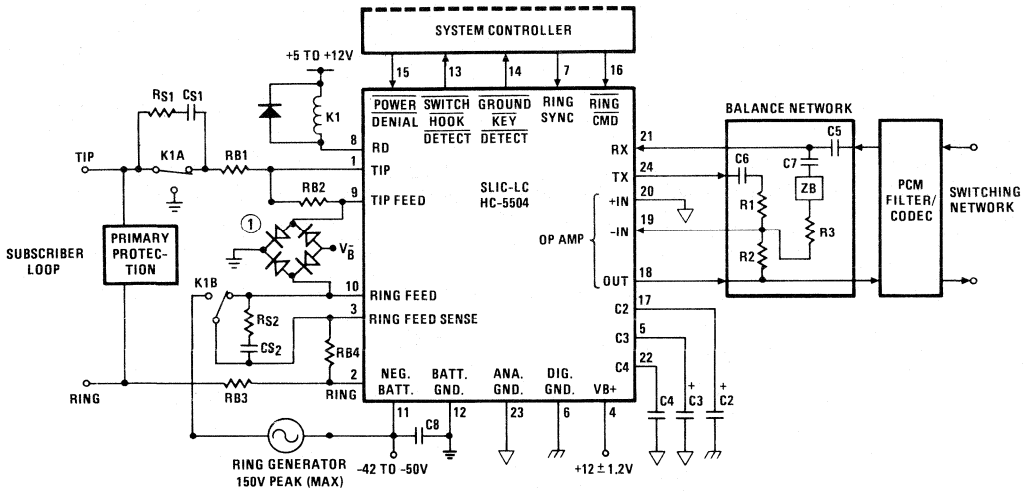
C1 = 0.5μF①
C2 = 0.15μF, 10V
C3 = 0.3μF, 30V
C4 = 0.5μF to 1.0μF, ± 10%, 20V (Must be nonpolarized)
C5 = 0.5μF, 20V
C6 = C7 = 0.5μF (10% Match Required)②, 20V
C8 = 0.01μF, 100V

R1 → R3 = 100kΩ (0.1% Match Required, 1% Absolute Value), ZB = 0 for 600Ω Terminations②
RB1 = RB2 = RB3 = RB4 = 150Ω (0.1% Match Required, 1% Absolute Value)
R_S = 1KΩ , C_S = 0.1μF, 200V Typically, Depending on V_{RING} and Line Length.

NOTES:
① C1 is an optional capacitor used to improve +12V supply rejection. This pin must be left open if unused.

② To obtain the specified transhybrid loss it is necessary for the three legs of the balance network, C6 - R1 and R2 and C7 - ZB - R3, to match in impedance to within 0.3%. Thus, if C6 and C7 are 1μF each, a 20% match is adequate. It should be noted that the transmit output to C6 sees a -22V step when the loop is closed and that too large a value for C6 may produce an excessively long transient at the op amp output to the PCM filter/CODEC. A 0.5μF and 100KΩ gives a time constant of 50msec.

FIGURE 8. HC-5502A LINE APPLICATION CIRCUIT.



TYPICAL COMPONENT VALUES

C2 = 0.15μF, 10V
C3 = 0.3μF, 30V
C4 = 0.5μF, 20V
C5 = 0.5μF, 20V
C6 = C7 = 0.5μF (10% Match Required) ②
C8 = 0.01μF, 100V
R1 = R2 = R3 = 100k (0.1% Match Required, ZB = 0 for 600Ω Terminations ②
RB1 = RB2 = RB3 = RB4 = 150Ω (0.1% Match Required)
$R_{S1} = R_{S2}$ = 1KΩ Typically
$C_{S1} = C_{S2}$ = 0.1μF, 200V typically, depending on V_{RING} and Line Length.

NOTES:

① Secondary protection diode bridge recommended is an MDA 220 or similar.

② To obtain the specified transhybrid loss of 40dB it is necessary for the 3 legs of the balance network, C6 - R1 and R2 and C7 - ZB - R3, to match in impedance to within 0.3%. If C6 and C7 are 1μF each, a 20% match is adequate. It should be noted that the transmit output to C6 sees a -22V step when the loop is closed. Too large a value for C6 may produce an excessively long transient at the op amp output to the PCM Filter/CODEC. A 0.5μF and 100kΩ gives a time constant of 50msec. The uncommited op amp output is internally clamped to stay within ±5.5V and also has current limiting protection.

FIGURE 9. HC-5504 LINE APPLICATION CIRCUIT.

battery referenced ringing. Figures 10 and 11 show the two different ringing schemes. Note, that the HC-5504 can be used for either of the single ended ringing schemes: to use the 5504 for tip injected ringing the Ring Feed Sense (RFS) and RF pins are permanently connected externally, and the scheme shown in Figure 10 adopted.

The Ring Command (RC) input is taken low during ringing. This activates the ring relay driver (RR) output providing the telephone is not off-hook or the line is not in a power denial state. The ring relay connects the ring generator to the subscriber loop. The ring generator output is usually an $80V_{RMS}$, 20Hz signal. For use with the Harris SLIC, the ring signal should not exceed 150V

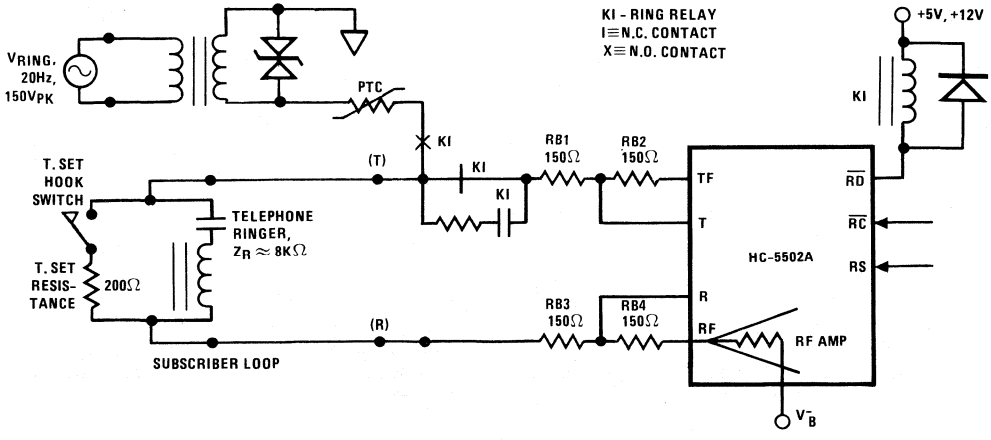


FIGURE 10. HC-5502A TIP INJECTED SINGLE ENDED RINGING.

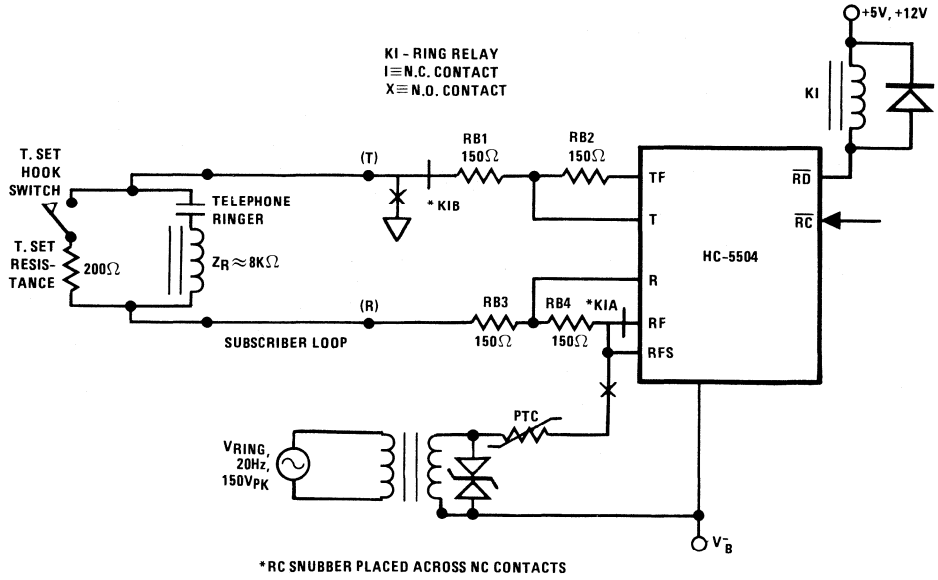


FIGURE 11. HC-5504 RING INJECTED SINGLE ENDED RINGING.

peak. Since the telephone ringer is AC coupled, only ring current will flow. For the HC-5502A SLIC, the ring current is sunk by the ring feed amplifier output stage whereas for the HC-5504 the ring path flows directly into V_{B-} via a set of relay contacts. The high impedance terminal RFS exists on the HC-5504 so that the low impedance RF node can be isolated from the hot end of the ring path in the battery referenced ring scheme.

The AC ring current flowing in the subscriber circuit will be sensed across RB4, and will give rise to an AC voltage at the output of the longitudinal amplifier. R20 and C4 attenuate this signal before it reaches the ring trip detector to prevent false ring trip. C4 is nominally set at 0.47μF but can be increased towards 1μF for short lines or if several telephones are connected in parallel across the line in order to prevent false or intermittent ring trip.

When the subscriber goes off-hook, a DC path is established between the output winding of the ring generator and the battery ground or V_{B-} terminal. A DC longitudinal imbalance is established since no tip feed current is flowing through the tip feed resistors. The longitudinal amplifier output is driven negative. Once it exceeds the ring trip threshold of the ring trip detector, the logic circuitry is driven by GK to trip the ring relay establishing an off-hook condition such that SHD will become active as loop metallic current starts to flow.

In addition to its ability to be used for tip or ring injected systems, the 5504 can also be configured for systems utilizing balanced ringing. Figure 12 shows such an application. The main advantage of balanced ringing is that it tends to minimize cross coupling effects owing to the differential nature of the ring tone across the line.

Figure 13 illustrates the sequence of events during ring trip with ring synchronization for a tip injected ring system. Note, that owing to the 90^{o} phase shift introduced by the low pass filter (R20, C4) the RS pulse will occur at the most negative point of the attenuated ring signal that is fed into the ring trip detector. Hence, when DC conditions are established for RTD, the AC component actually assists ring trip taking place. For a ring side injected ring system, the RS pulse should occur at the positive zero crossing of the ring signal as it appears at RFS.If ring synchronization is not used, then the RS pin should be held permanently to a logic high of 5V nominally: ring trip will occur asynchronously with respect to the ring voltage. Ring trip is guaranteed to take place within three ring cycles after the telephone going off-hook.

It is recommended that an RC snubber network is placed across the ring relay contacts to minimize inductive kick-back effects from the telephone ringer. Typical values for such a network are shown in Figure 9.

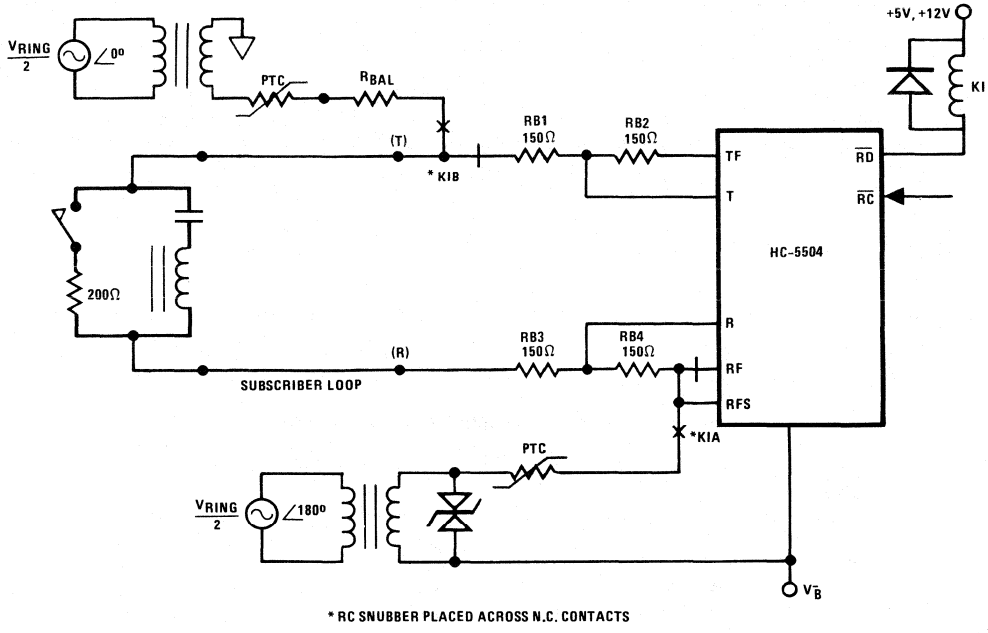


FIGURE 12. HC-5504 BALANCED RINGING CONFIGURATION.

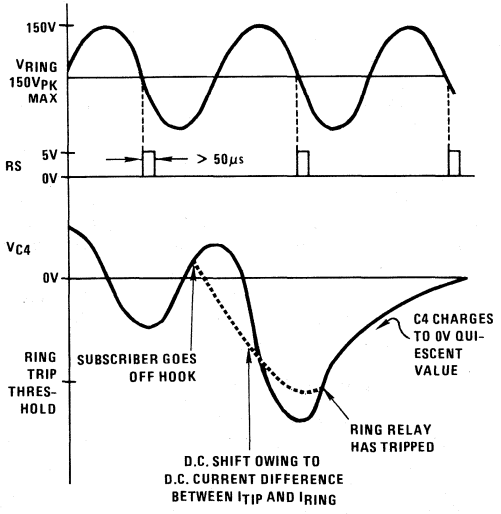


FIGURE 13. RING TRIP SEQUENCE.

4.2 Power Denial (PD)

Power denial limits power to the subscriber loop: it does not power down the SLIC, i.e. the SLIC will still consume its normal on-hook quiescent power during a power denial period. This function is intended to "isolate" from the battery, under processor control, selected subscriber loops during an overload or similar fault status.

If PD is selected, the logic circuitry inhibits RC and switches in a current source to C3. The capacitor charges up to a nominal -3.5V at which point it is clamped. Since TF is always biased at -4V, the battery feed across the loop is essentially zero, and minimum loop power will be dissipated if the circuit goes off-hook. No signalling functions are available during this mode.

After power denial is released (PD = 1), it will be several hundred milliseconds (300ms) before the RF output reaches its nominal battery setting. This is due to the RC time constant of R21 and C3.

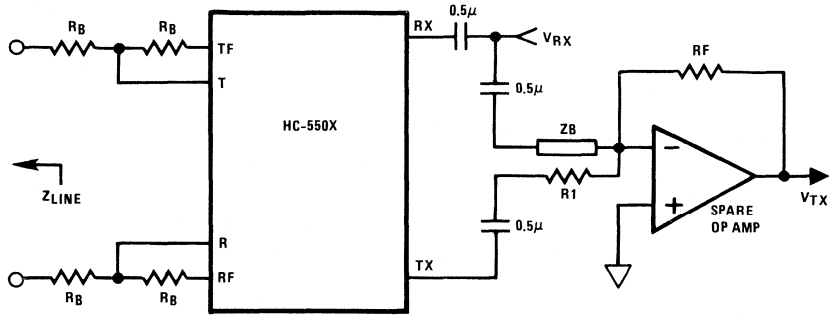


FIGURE 14. SLIC TRANSHYBRID BALANCE EQUATIONS.

4.3 Transhybrid Loss And Longitudinal Balance

During 4W to 2W transmission, the 4W signal is returned to the transmit output: this is called transhybrid return: it is not a reflection from the line as it will only occur if the loop is closed. In order to prevent echo and instability in the switch, this returned signal must be balanced out before it reaches the filter/CODEC. The level of the returned signal is given below, and a balancing network utilizing the on-chip spare op amp is indicated in Figure 14. Since the returned received signal's amplitude and phase are a function of the line's A.C. impedance, the balance network is a function of the same.

For a resistive line, the two arms of the balance network (Figure 14) are also resistive. In the simplest case, for a 600 ohm system, the two parts of the summing network have equi-resistance values. For a transhybrid balance greater than 36dB, component tolerances of ±0.5% are recommended. Both arms of the summing network are capacitively coupled since the TA and TF amplifiers have output and input D.C. biases, respectively. The values of the capacitors are chosen to prevent degradation of the audio frequency response. For capacitive values of 0.5μF, components with tolerances of 10% can be used since at voice band frequencies the reactance of the capacitor has minimal effect on the impedance of the balance network.

The transhybrid returned signal is given by:

$$V_{TX} = -V_{RX} \left(\frac{4R}{(2R + Z_L)} \right)$$

where $R = (R_{B1} + R_{B2}) = (R_{B3} + R_{B4})$, and

Z_L = Line Impedance

For the balance network, the general equation is given by:

$$Z_B = 2R + Z_L \text{ with } R1 = 4R \text{ in Figure 14.}$$

A full derivation of the balance equation is given in Appendix A. A measure off this balance is known as transhybrid loss. For a 600 ohm resistive line, a balance of 40dB at 1kHz is attainable. In practice owing to variations in lines and telephone sets the balance is usually lower than in the ideal case: A balance in the order of 25dB will often be measured and accepted.

By switching out the balance network, it is possible for the controller to conduct loop back tests providing the loop can be closed via a test relay in the line card.

Longitudinal balance is equivalent to common mode rejection ratio. Looking into the line card tip and ring terminals towards the SLIC, the 2W balance is a function of the impedance match between tip and ring to ground. The 4W balance is a funciton of the 2W balance, and the matching of the feedback resistor ratios around the transversal amplifier. (The TA itself must also exhibit a CMRR in excess of the required longitudinal balance.) The SLIC user can only control the matching of the feed resistors. For a nominal 60dB of rejection, these must match within 0.1%. The on-chip resistors are thin film SiCr resistors and are matched within 0.1%. The amplifier has a CMRR of 70dB giving a typical 4W balance of 60dB.

4.4 Complex Impedance Matching

The SLIC is usually used in systems that have a line characteristic impedance of 600 ohms resistive. Thus, the 4 × 150 ohms feed resistors present a balanced 600 ohms load to the line. If the characteristic impedance of the line varies from 600 ohms but remains resistive, then this can be compensated for by increasing or decreasing the value of R_{B1} and R_{B3}. For example, if the line is defined as 900 ohms resistive, then R_{B1} and R_{B3} could be increased to 300 ohms each and the line will be matched. The increase in feed resistance could impact the DC performance on long lines.

In case of lines having a complex characteristic impedance the SLIC circuit can be configured to adequately match the line. Figure 15 shows a typical equivalent line impedance as defined in many European countries. Figure 16 illustrates the circuitry required to match and balance such a line. The component design equations are given below. A qualitative description is given of the circuit to explain its operation; a full mathematical derivation is given in Appendix A.

For the equivalent impedance shown in Figure 15, it can be seen that at low frequencies, the impedance will increase and become more resistive. As the voice frequency increases, the reactance of C_L decreases, thus the line impedance will also decrease. In order to match the line impedance, a feedback network is required that provides low frequency positive feedback and high frequency negative feedback. The scheme of Figure 16 does this. An additional op amp is required to realize the circuit.

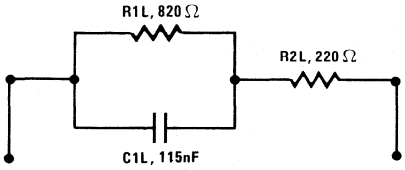


FIGURE 15. TYPICAL EQUIVALENT COMPLEX LINE IMPEDANCE.

The degree of match over the voice band is a function of the R and C component tolerances and the degree of approximation to their theoretical values. The curves in Figure 17 show typical matching characteristics. The objective is to maximize the 2W return loss. Some values are indicated in Figure 17.

Resistor RS in Figure 16 is added to ensure circuit stability. A nominal value of 300 ohms is advised which will not affect the A.C. performance of the circuit. Capacitor CF can be used to optimize the transmit signal's frequency response. This is caused by non-realization of ideal component values. CF adds a pole to the circuit which compensates this non-flat response. (See Figure 18). For complex impedance applications a certain amount of circuit optimization will be required by the user in order to obtain an adequate 2W return loss performance and a satisfactory transmit frequency response.

As indicated, the above method for matching complex lines requires an additional op amp to the SLICs on board op amp. It also requires several capacitors whose values are often non-standard. Also, tightly toleranced capacitors are expensive. A second method exists to match the line; it minimizes the number of capacitors to the number of capactive elements within the line's equivalent impedance model. (There is usually one capacitive element.) Assuming just one capacitor in the line impedance network, the capacitor's value can be scaled to a standard value which will improve the performance of the circuit. A

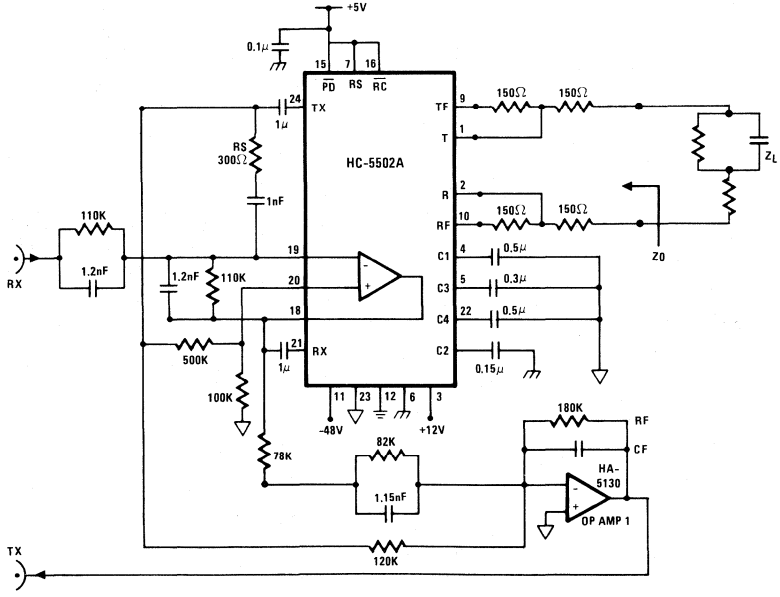


FIGURE 16. COMPLEX LINE IMPEDANCE TRANSFORM CIRCUIT HC-5502A.

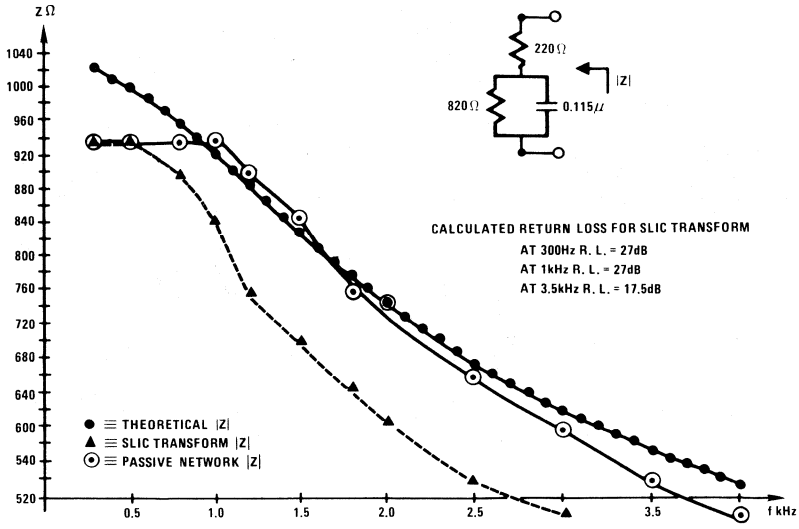


FIGURE 17. | Z | vs. FREQUENCY

second additional external op amp is necessary; however, the ease of implementation and the performance attained could warrant this overhead. The mathematical derivation of this method is given in Appendix B together with an application circuit .

4.5 Line Fault Protection

The subscriber loop can exist in a very hostile electrical environment. It is often in close proximity to very high voltage power lines, and can be subjected to lightning induced voltage surges. The SLIC has to provide isolation between the subscriber loop and the telephone office. Methods for dealing with longitudinally induced power frequency currents and excessive DC line current have been discussed.

The most stringent line fault condition that the SLIC has to withstand is that of the lightning surge.

The Harris monolithic SLIC in conjunction with a simple low cost diode bridge can achieve up to 1KV of isolation between the loop and switch office. The level of isolation is a function of the packaging technology and geometry together with the chip layout geometries. One of the principal reasons for using DI technology for fabricating the SLIC is that it lends itself most readily to manufacturing monolithic circuits for high voltage applications.

Figures 8 and 9 show general application circuits for the HC-5502A and HC-5504 SLICs. A secondary protection diode bridge is indicated which protects the feed amplifiers during a fault. Figure 19 illustrates more clearly the fault current paths during a lightning or transient high voltage strike. Most line systems will have primary protection networks. They often take the form of a carbon block or arc discharge device. These limit the fault voltage to 500V - 1000V peak before it reaches the switch line cards. Thus when a transient high voltage fault has occurred, it will be transmitted as a wave front down the line. The primary protection network limits the voltage to 500V to 1000V. The attenuated wave front will continue down the line towards the SLIC. The feed amplifier outputs appear to the surge as very low impedance paths to the system battery. Once the surge reaches the feed resistors, fault current will flow into or out of the feed amplifier output stages until the relevant protection diodes switch on. Bench measurements have indicated peak fault currents of up to 150mA into and out of the SLIC during the finite turn on time of the diode bridge. Once the necessary diodes have started to conduct all the fault current will be handled by them. The geometry of the SLIC and its package has been designed to withstand the full rated peak fault voltage at its tip (T) and ring (R) terminals: for ceramic packages this is 500V peak, and for plastic (or epoxy) packaged SLICs this is 1000V peak. The circuits are rated against standard lightning characteristics defined by Figure 20. The ceramic package contains an air gap whereas the plastic packages contain no void. The dielectric constant of air is lower than that of the epoxy and it is this which breaks down at lower voltages than the plastic compound.

If the user wishes to characterize SLIC devices under simulated high voltage fault conditions on the bench, he should ensure that the negative battery power supply has sufficient current capability to source the negative peak fault current and low series inductance. If this is not the case, then the battery supply could be pulled more negative and destroy the SLIC if the total (V_{B^+} + V_{B^-}) voltage across it exceeds 75V.

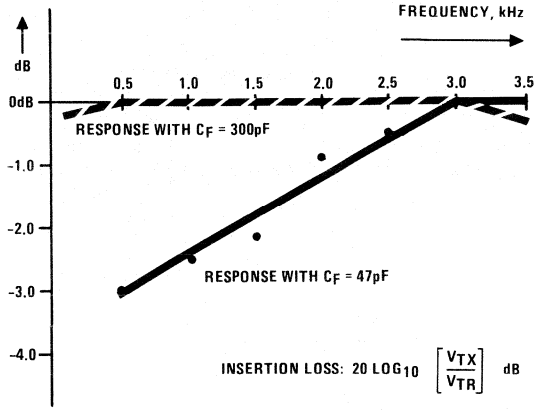


FIGURE 18. TWO WIRE - FOUR WIRE TRANSMISSION:

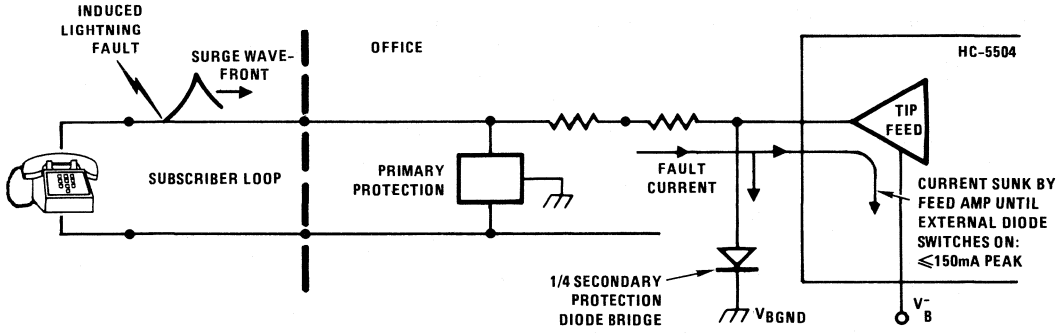


FIGURE 19. FAULT PROTECTION

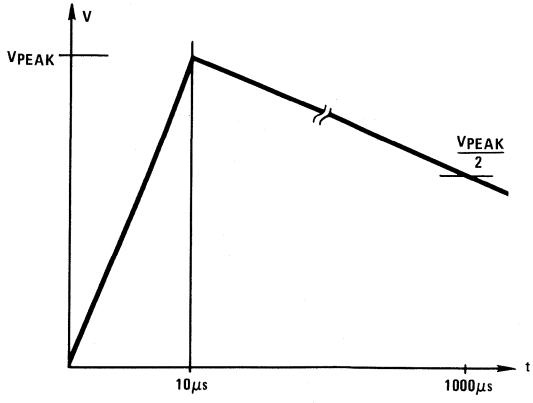


FIGURE 20. SIMULATED LIGHTNING STRIKE WAVEFORM.

APPENDIX A

BALANCING AND IMPEDANCE MATCHING THE HC-550X SLIC

1. Evaluating balance network for HC-5502A/HC-5504 SLIC.

   The Figure A1 schematic illustrates the general 4W to 2W signal implementation of a SLIC IC.

   In order to achieve transhybrid rejection of the Rx signal, the op amp configuration needs to be implemented in order to subtract out any portion of the Rx signal that might appear at the TX terminal of the SLIC. The value of Z_B is a function of Z_L; a general derivation of Z_B is given in Figure A2. Consider the single ended signal path equivalent circuit of the HC-550X.

   For V_{RX} only we require $V_T = 0$.

$$V'_{TX} = \left(\frac{R}{2R + Z_L}\right) \times 2V_{RX} \quad ; \quad V_{TX} = \left(\frac{-4R}{2R + Z_L}\right) \times V_{RX}$$

For $V_T = 0$ we must have the condition:

$$\frac{V_{RX}}{Z_B} = \frac{V_{TX}}{R1} \qquad \text{where } V_{TX} = f(V_{RX})$$

$$\frac{V_{RX}}{Z_B} = \left[V_{RX} \times \left(\frac{4R}{2R + Z_L}\right)\right] / R1$$

$$Z_B = R_1 \times \left(\frac{2R + Z_L}{4R}\right)$$

Thus if $Z_L = 2R$ ...(i.e. 600 ohm)
then $Z_B = R1$

For general case let $R1 = 4R$

$Z_B = 2R + Z_L$

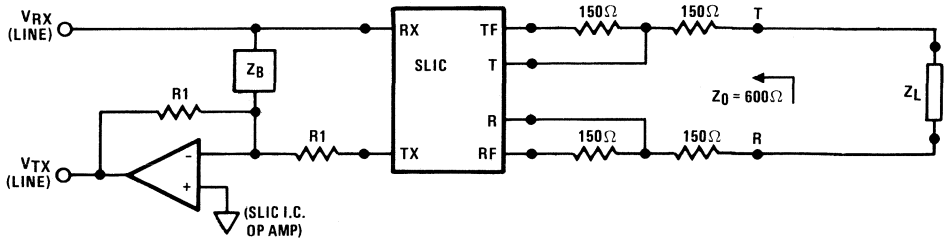


FIGURE A1.

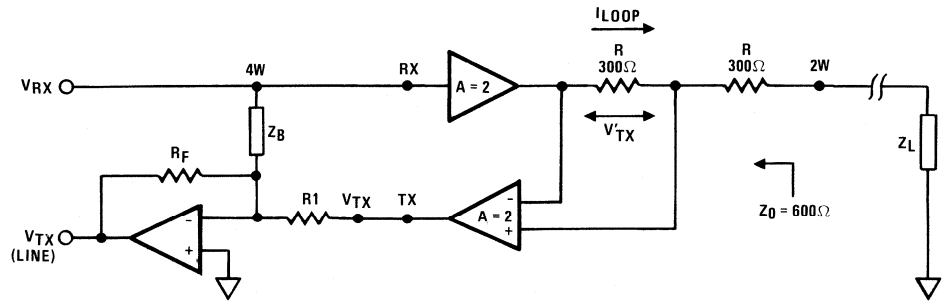
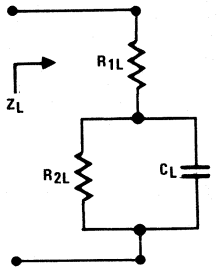


FIGURE A2.

2. Matching complex line/load configurations...
For some users it is necessary for the SLIC to appear as a complex impedance looking into SLIC from the 2W line in order to match complex line impedances.

Consider a typical complex line configuration, see Figure A3.

By implementing positive and negative feedback around the V_{RX} to V_{TX} loop, the output impedance of the SLIC can be transformed to match Z_L. Again, consider the single ended signal path equivalent circuit of the SLIC together with a feedback network H(s), as shown in Figure A4.



$$Z_L(s) = \frac{R_{1L}(1+sT)+R_{2L}}{(1+sT)}$$

where $T = R_{2L}C_L$

as $F \rightarrow 0$, $Z_L \rightarrow R_{1L}+R_{2L}$

as $F \rightarrow \infty$, $Z_L \rightarrow R_{1L}$

FIGURE A3.

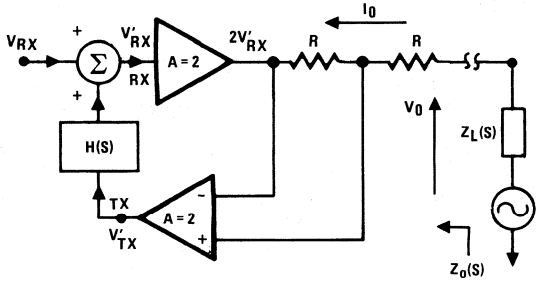


FIGURE A4.

Assume transmission only; $V_{RX} = 0$.

H(s) network will provide positive and negative feedback to give $Z_O(s)$

$$V_O = 2RI_O + 2V'_{RX}$$
$$V'_{RX} = HV'_{TX} = 2HI_OR$$
$$V_O = 2RI_O + 4HI_OR$$
$$Z_O = V_O/I_O$$
$$Z_O = 2R(1+2H)$$
$$H = (Z_O - 2R)/4R \qquad (A)$$

Figure A5 indicates that network H can be configured as follows to provide required positive and negative feedback.

$$i_1 + i_2 = -i_3$$

$$\left(\frac{V'_{TX} - KV'_{TX}}{Z_1}\right) + \left(\frac{V_{RX} - KV'_{TX}}{Z_2}\right) = \frac{KV'_{TX} - V'_{RX}}{Z_2}$$

For $V_{RX} = 0$ and defining $H = V'_{RX}/V'_{TX}$ the above equation reduces to:

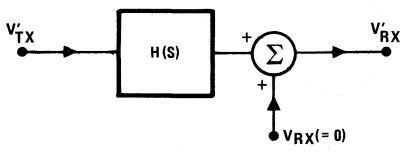
$$H = K\left[\frac{2Z_1 + Z_2\left(1 - \frac{1}{K}\right)}{Z_1}\right] \qquad (B)$$

Equations (A) and (B) are equivalent. Equation (A) can be expanded for a particular Z_O requirement. Equation (B) can then be manipulated so that terms and coefficients of the two final equations can be compared to solve for Z_1, Z_2 and K.

EXAMPLE

This example is given for the complex impedance considered above.

Require Z_O to appear as in Figure A6.



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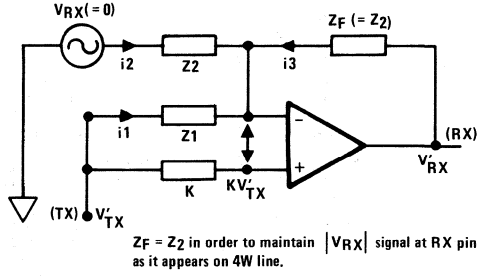


$Z_F = Z_2$ in order to maintain $|V_{RX}|$ signal at RX pin as it appears on 4W line.

FIGURE A5.

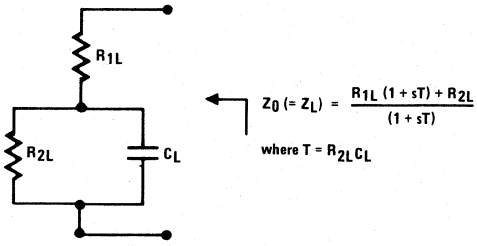


FIGURE A6.

From Equation A, it can be shown that for Z_O above

$$H = \left(\frac{R_{1L} + R_{2L} - 2R}{4R}\right) \times \frac{\left(1 - sT\left[\frac{2R - R_{1L}}{R_{1L} + R_{2L} - 2R)}\right]\right)}{(1 + sT)} \qquad (C)$$

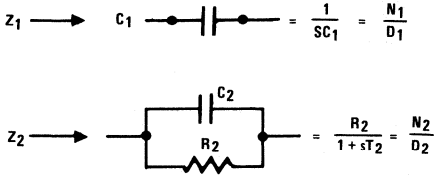
Consider Equation (B). Assume Z_1 and Z_2 have the form N_X/D_X. Thus Equation (B) reduces to:

$$H = K\left[\frac{2N_1D_2 + N_2D_1(1 - 1/k)}{N_1D_2}\right] \qquad (D)$$

Comparing terms in Equations C and D:

$N_1D_2 = (1 + sT)$

Let $N_1 = 1$, Z_1 and Z_2 can be configured thus:



Substituting for Z_1 and Z_2, equation D reduces to:

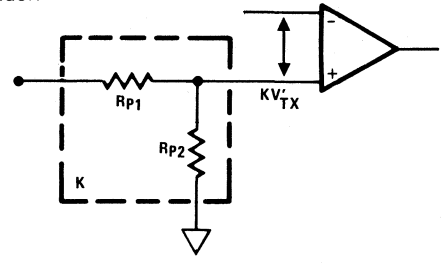
$$H = 2K \times \left[\frac{i - sR_2(C_1\left[\frac{1 - K}{2K}\right] - C_2)}{(1 + sT_2)}\right] \qquad (E)$$

Comparing terms in equations (C) and (E), the following working formula for Z_1 and Z_2 and K are derived:

Z_2: $R2 = R_{2L}$ (1)

$C_2 = C_{2L}$ (2)

K: K is a constant and is configured as a potential divider.



if $R_{P1} = \frac{R_{P2}}{n}$ where n is an integer

then $\frac{2n}{1+n} = \frac{(R_{1L} + R_{2L}) - 2R}{4R}$ (3)

Z_1: $C_1 = C_{2L}\left[\frac{2R_{2L}}{10R - (R_{1L} + R_{2L})}\right]$ (4)

The final circuit configuration will take account of the complex impedance transform network, and the balance network derived in Equation 1. The circuit is illustrated in Figure A7.

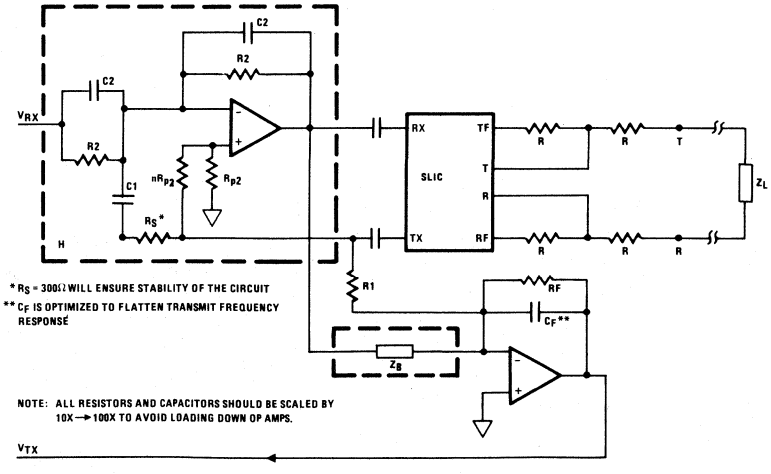


FIGURE A7. BALANCING AND MATCHING THE HC-550X SLIC

APPENDIX B
COMPLEX LINE IMPEDANCE MATCHING WITH SLIC

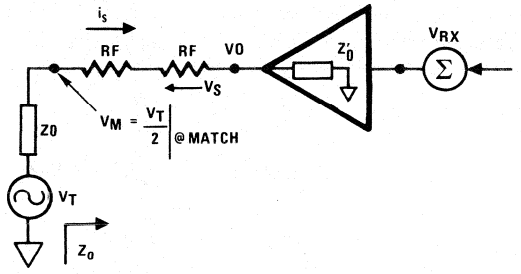


FIGURE B1. TWO TO FOUR WIRE TRANSMISSION. SINGLE ENDED AC EQUIVALENT CIRCUIT OF SUBSCRIBER LOOP.

Consider Figure B1. Assume V_{RX} = 0. (2W to 4W transmission)

At match:

$$i_S = \frac{V_T}{2Zo} = \frac{Vm}{Zo}$$

$$Zo = 2R_F + Zo'$$

$$Zo' = \frac{Vo}{i_S}$$

$$Vo = Zo'.\ i_S = i_S Zo - 2i_S R_F$$

but $Vm = i_S Zo$; $\therefore Vo = Vm - 2i_S R_F$ Equation (1)

$$Vs = i_S RF,\ \therefore Vs = \frac{R_F}{(2R_F + Zo')} \times Vm$$

$$\therefore Vm = (isR_F)\frac{(2R_F + Zo')}{RF}$$ Equation (2)

(2) in (1) for Vm, and Zo = 2RF + Zo'

$$Vo = 2Vs\left(\left(\frac{Zo}{2RF}\right) - 1\right)$$

This matching equation can be realized as shown in Figure B2.

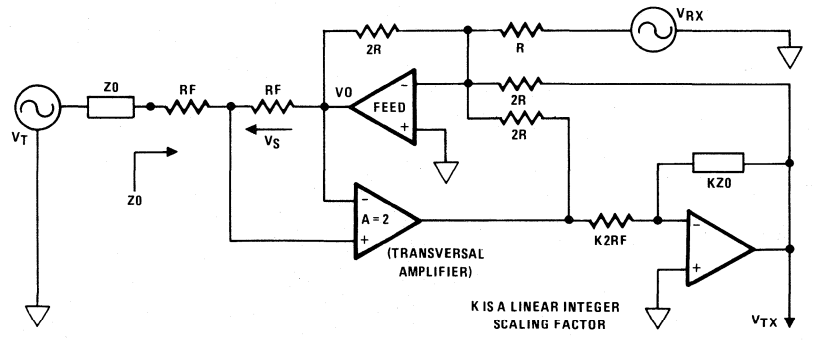


FIGURE B2. FOUR WIRE TO TWO WIRE TRANSMISSION

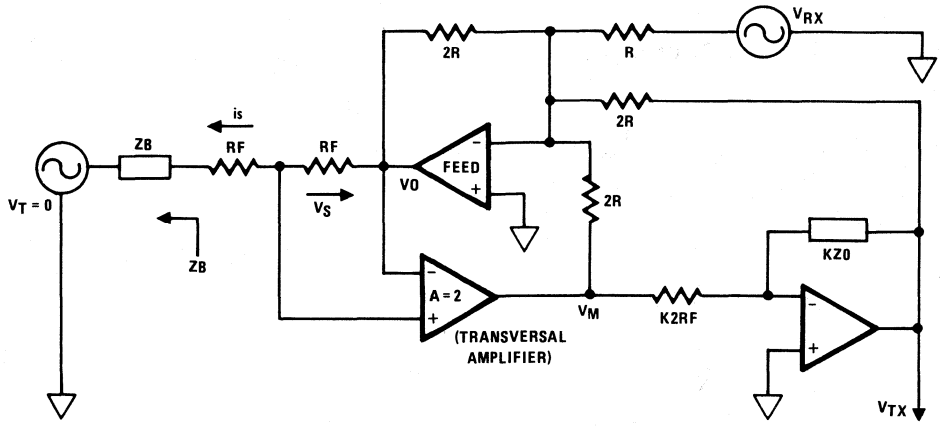


FIGURE B3.

Transhybrid Balance

Consider Figure B3. Evaluate V_{TX} in terms of V_{RX}, in order to establish transhybrid balance equation.

For general case, let line transhybrid impedance be Z_B.

$$Vo = -2\left[V_{RX} + \frac{Vm}{2} + \frac{V_{TX}}{2}\right] \qquad \text{Equation (1)}$$

$$Vm = -2Vs = \frac{-2R_F}{2R_F + Z_B} \times Vo$$

$$V_{TX} = \frac{(Zo)}{(2R_F + Z_B)} \times Vo \qquad \text{Equation (2)}$$

From Equation (1):

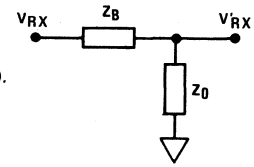
$$V_{RX} = -\left[\frac{Vo}{2} + \frac{Vm}{2} + \frac{V_{TX}}{2}\right]$$

$$2V_{RX} = -\left[\frac{Z_B + Zo}{2R_F + Z_B}\right] \times Vo$$

$$V_{RX} = \frac{-(Z_B + Zo)}{2(2R_F + Z_B)} \times Vo \qquad \text{Equation (3)}$$

Compare Equations (2) and (3): we need to scale Equation (3) by:

$$Zo\left(\frac{2}{Z_B + Zo}\right)$$ in order to equate to Equation (2).



V_{RX} = EQUATION (3).

$$V'_{RX} = \frac{Zo}{2(2R_F + Z_B)} \times Vo$$

$$\therefore V'_{RX} = \frac{-V_{TX}}{2} :$$

Transhybrid balance can be achieved using simple summing amplifier network.

If $Z_B = Zo$ then Equation (3) becomes:

$$V_{RX} = \frac{-(Zo)}{(2R_F + Zo)} \times Vo \qquad \text{Equation (4)}$$

and Equation (2) becomes:

$$V_{TX} = \frac{Zo}{2R_F + Zo} \times Vo \qquad \text{Equation (5)}$$

$\therefore V_{TX} = -V_{RX}$ and TH balance is achieved using a resistive summing amp network. The complete application circuit is shown in Figure B4.

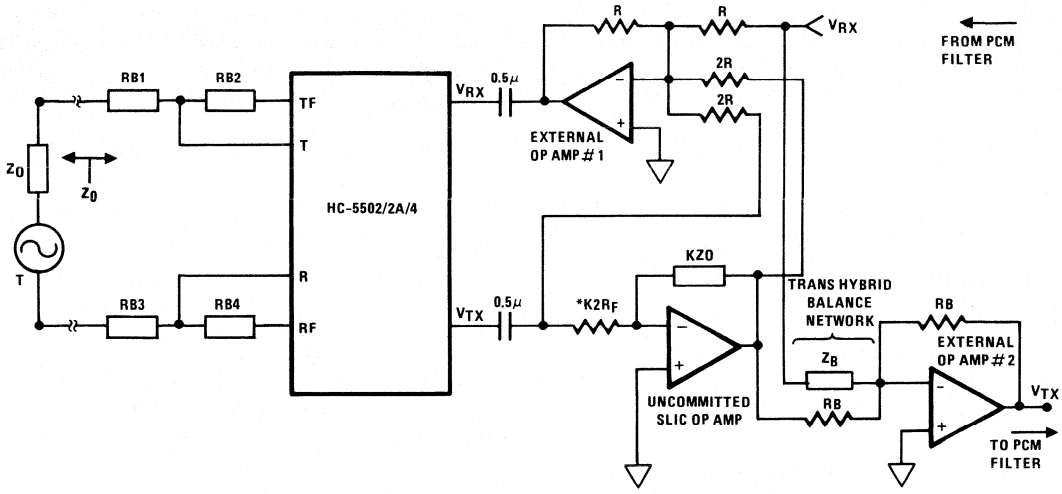


FIGURE B4. APPLICATION OF SECOND LINE IMPEDANCE MATCHING ALGORITHIM.

*$R_F = R_{B2} + R_{B4}$

NOTICE: Information contained in application notes is intended solely for general guidance; use of the information for user's specific application is at user's risk.

USING THE HA-2541

Alan W. Hansford

Introduction

In response to an industry wide need for a faster, unity gain stable, monolithic operational amplifier, Harris Semiconductor has designed and manufactured the HA-2541 device.

This fully differential op amp has an unprecedented set of dynamic parameters which should be most useful for demanding designs in video, data acquisition, robotics, and RF systems. These devices' capabilities may also be utilized when existing systems must be upgraded or modified for additional performance.

The HA-2541's outstanding features include 90ns settling time, 250V/μs slew rate, and 40MHz unity gain bandwidth, which until recently, could only be achieved through hybrid configurations.

The applications information which follows, points in the direction where a vast number of application circuits await the HA-2541.

Prototyping

As with any high performance device, care should be taken in prototyping so as not to undermine the performance characteristics of the HA-2541. Several simple do's and don'ts should avoid most design problems. Standard high frequency layout techniques are strongly recommended in order to gain the full benefit of the HA-2541's capabilities. The first is proper mounting of the HA-2541 through a ground plane. Since sockets tend to extend the lead length and increase parasitic capacitance, they are not recommended. If sockets must be used, Teflon types are preferred. The mounting of the feedback components should be as close as practical to the HA-2541 and on Teflon standoffs.

The wide bandwidth of the HA-2541 makes it prone to unwanted high frequency poles if large value feedback resistors are used (10K ohms). This calls for low value film type resistors. Actual component values may depend heavily on layout implementation. It is therefore suggested that early prototyping be done to verify the quality of operation and to optimize component values. Additionally, power supply decoupling as close to the power pins as possible, is recommended.

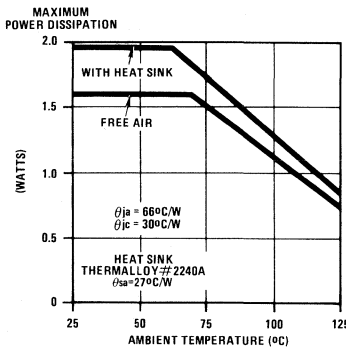
Thermal Considerations

(Also Refer to Application Note 556)

In order to achieve the 250V/μsec slew rate that the HA-2541 is capable of, a high quiescent power level was needed. This, along with the high output capacity of the HA-2541, means that the package must dissipate a large amount of heat.

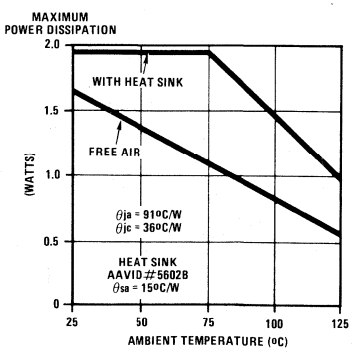
The device's junction temperature upper limit is 175°C. This places a restriction on the power output at elavated ambient temperatures. The charts below mark the acceptable region of operation with and without a heat sink (Thermalloy 2240A or 5602B are acceptable units and the ones used in the construction of the charts). The curves assume proper installation including the use of heat conductive compounds to facilitate the energy transfer.

CHART 1. TO-8 METAL CAN (HA2-2541-X)



NOTE: For maintaining maximum junction temperatures below +175°C, derate at 15.2mW/°C beyond +68°C ambient.

CHART 2. 14 PIN DIP PACKAGE (HA1-2541-X)



NOTE: For maintaining maximum junction temperatures below +175°C, derate at 11.0mW/°C beyond +25°C ambient.

Performance Enhancements

The HA-2541, like any other high performance device, has certain design features, which give the HA-2541 its excellent wideband performance. Although the HA-2541 has been laser trimmed to minimize offset voltage, an external potentiometer connection has been provided to reduce this even more. Figure 1 illustrates the suggested offset adjustment.

The input DC performance is improved by the use of balanced input impedances on the two input terminals of the device. Figure 2 illustrates this technique which greatly reduces any effects caused by the input offset currents.

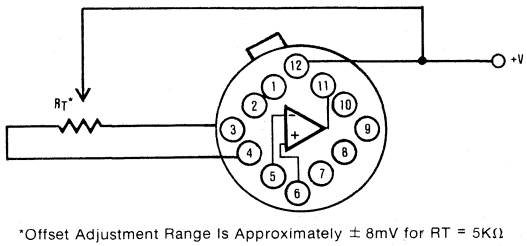
The input signal can be given even more isolation from the effects of input bias currents with the use of FET buffered inputs as shown in Figure 3. The reduction of the input bias currents is quite large, which makes the FET HA-2541 combination an excellent choice for low current applications such as atomic particle detectors (radiation counter circuitry).

Applications

The HA-2541 is a very versatile device with applications in nearly every area of its bandwidth. Perhaps one of the best ways to gain some familiarity with the part is by examining its use in some of the more straightforward applications. The Wein Bridge oscillator in Figure 4 is just such an application.

The HA-2541 is well suited for use as the heart of an oscillator circuit. In spite of the rudimentary diode limiting provided by R_3 - R_7 and D_1 & D_2, a good quality sine wave of 40MHz is readily attainable with an upper limit of 50MHz which exceeds the unity gain bandwidth of the HA-2541.

R_1C_1 and R_2C_2 provide the required regenerative feedback needed for adequate frequency stability. In theory the feedback network requires a gain of three to sustain oscillation. However, the practical gain needed is just over three and is provided for by R_8 and R_9.



*Offset Adjustment Range Is Approximately ± 8mV for RT = 5KΩ

FIGURE 1. SUGGESTED METHOD FOR NULLING V_{OS}

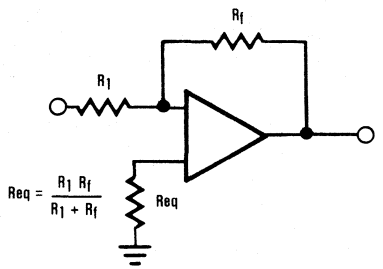
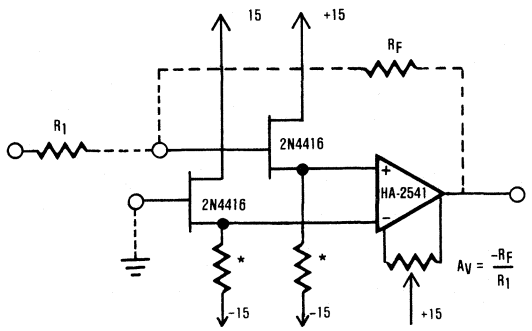


FIGURE 2. MINIMIZING THE EFFECTS OF OFFSET CURRENT



*Value should be determined experimentally for optimum performance.

FIGURE 3. BUFFERING THE HA-2541 INPUTS WITH FETS.

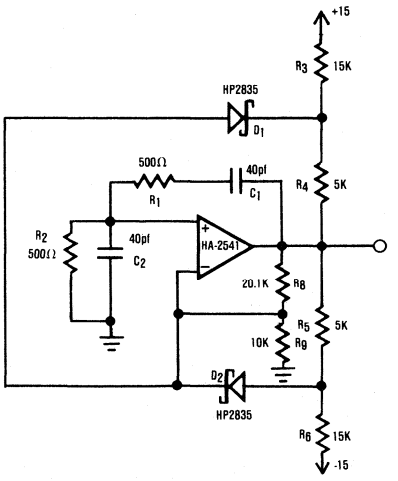


FIGURE 4. 40MHz WEIN BRIDGE OSCILLATOR

High power amplifiers and buffers are in use in a wide variety of applications. Many times the "high power" capability is needed to drive large capacitive loads as well as low value resistive loads. In both cases the final driver stage is usually a power transistor of some type, but because of their inherently low gain, several stages of pre-drivers are often required. The HA-2541, with its 10mA output rating, is powerful enough to drive a power transistor without additional stages of current amplification. This capability is well demonstrated with the high power buffer circuit in Figure 5.

The HA-2541 acts as the pre-driver to the output power transistor. Together, they form a unity gain buffer with the ability to drive three 50 ohm coaxial cables in parallel, each with a capacitance of 2000pF. The total combined load is 16.6 ohms and 6000pF capacitance.

Video

One of the primary uses of the HA-2541 is in the area of video applications. These applications include signal construction, synchronization addition and removal, as well as signal modification. A wide bandwidth device such as the HA-2541 is well suited for use in this class of amplifier. This, however, is a more involved group of applications than ordinary amplifier applications since video signals contain precise DC levels which must be retained.

The addition of a clamping circuit restores DC levels at the output of an amplifier stage. The simple form of the circuit is shown in Figure 6A with a capacitor and analog switch added to the inverting amplifier configuration. The switch closes during a certain portion of the incoming signal. This causes the capacitor to charge to a value which represents the 0V reference of the input waveform. The shorting action of the switch causes the output of the HA-2541 to go to 0V during the 0V reference of the input signal.

This simple amplifier/clamping circuit has several drawbacks. The largest is the drain on the holding capacitor by the input bias currents of the HA-2541, with the resulting change in the reference voltage. This condition is easily addressed with the use of an HA-5320 sample and hold. The low output impedance of the sample and hold can easily provide the required input bias current for the HA-2541 without draining the holding capacitor. The result is a constant DC reference between the scan lines of the video signal.

The second drawback of the simple amplifier/clamp results from the color synchronization information being transmitted along with the 0 Volt DC reference level. By closing the analog switch, the color burst is passed through the low impedance capacitor to ground and consequently lost. This situation is remedied by placing a 3.57MHz trap in series with the analog switch and holding capacitor. This will block the color burst signal and allow it to be passed to the output as an amplified signal. Figure 6B shows both the "trap" and the sample and hold reference additions to the simple amplifier with DC restore.

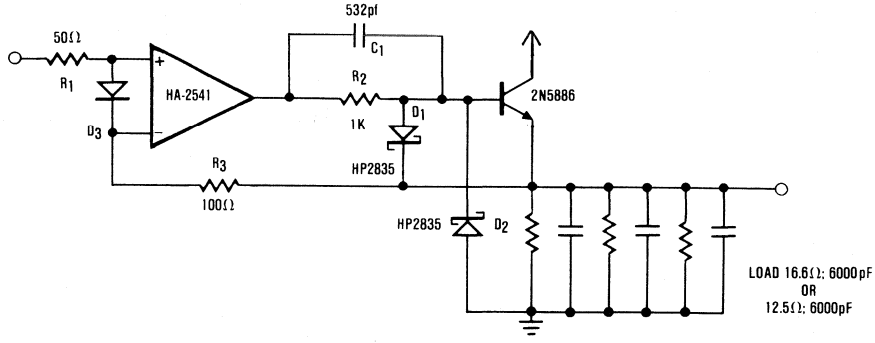


FIGURE 5. DRIVING POWER TRANSISTORS TO GAIN ADDITIONAL CURRENT BOOSTING

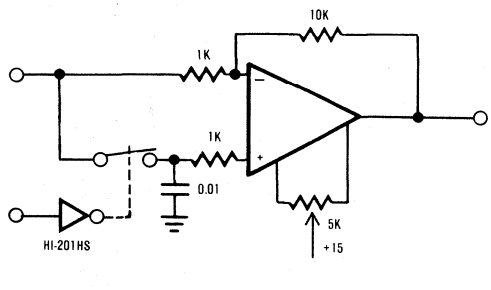


FIGURE 6A. SIMPLE DC RESTORER

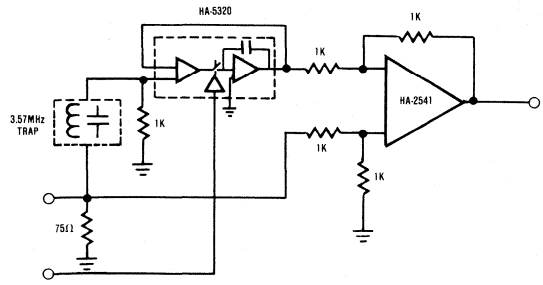


FIGURE 6B. IMPROVED VIDEO DC RESTORER

The amplifier designs to this point work with the full video signal or the "composite" signal. The HA-2541 has several applications one stage back, in the construction of the composite signal itself.

The composite video signal has several components which must be combined to create the final waveform. One that has already been used is the 0 volt reference and the color burst combination. Two others are the horizontal synchronization pulse and the video picture information.

The circuit in Figure 7 is a traditional summing amplifier configuration with the addition of the now familiar DC clamping circuit. The operation is quite simple in that each component (synchronization, color burst, picture information, etc.) of the composite video signal is applied to its own input terminal of the amplifier. These combine algebraically and form the composite signal at the output. The clamping circuit (if used) restores the 0 volt reference of the composite signal.

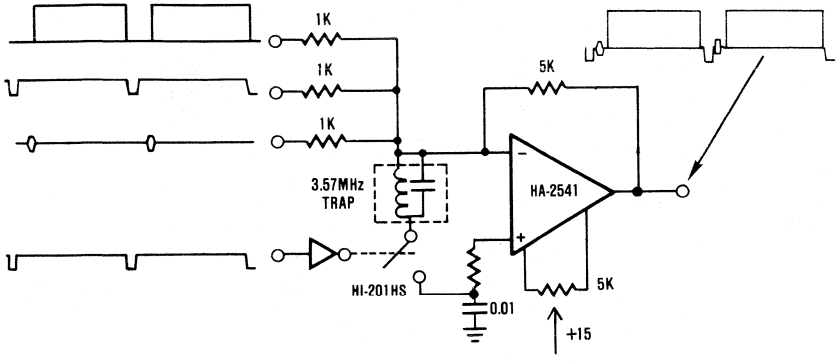


FIGURE 7. SUMMING AMPLIFIER FOR COMPOSITE VIDEO PLUS CLAMPING CIRCUIT

One drawback resulting from the algebraic addition of the input waveforms is the requirement that each input component exist only during the period that it is needed in the composite signal. An example of this is the color burst which can be present at its input terminal only during its portion of the composite signal since no gating circuitry is available.

The multiplexer circuit in Figure 8 can be used for video signal construction by gating each component through to the HA-2541 as it is required. The inherent channel separation of the multiplexer allows each component of the composite signal to be continuously present at the input. This has several important implications. The first is that the duration of each component of the signal is precisely controlled by a digital timing chain (which can be easily reproduced at remote locations with high precision). Second, the only analog signals needed are the color burst and the picture information. All reference signals such as the horizontal synchronization, the 0 volt reference, and the previously unmentioned vertical synchronization signals can be simulated with accurate DC references. These are gated, along with the other components, to form the composite video signal.

An extension of the multiplexed signal construction technique is a type of signal modification. When several cameras are used together without a common synchronization signal, they are not easily combined for special effects and switching. A solution to this problem would be to strip the synchronization pulses off of each of the incoming camera waveforms and apply a new common synchronization pulse. The new pulse will enable switching equipment to combine the separate signals for whatever effect is needed.

It should be noted that widely varying horizontal speeds may necessitate the use of analog delay chains with the synchronization technique. This will produce pictures of compatible quality and proportion (vertical speed is more constant and contains a dead zone for any differences, vertical retrace).

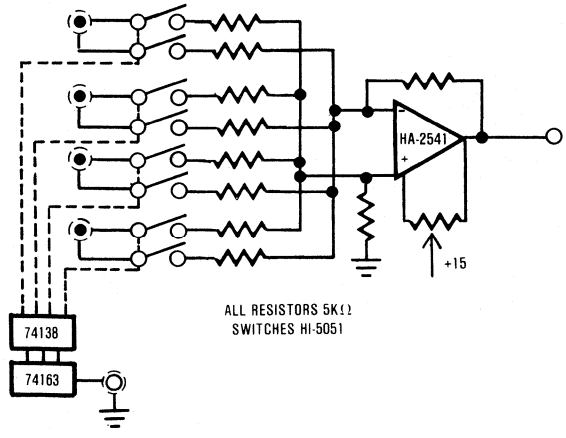


FIGURE 8. MULTIPLEXING WITH HA-2541

The multiplexer system used for video signal construction has other applications of interest. The concept of combining several channels into one can be reversed to form a demultiplexer, where the function is to take several combined channels and separate them into their original form. This type of application can be implemented to solve some well-known industrial problems.

The multiplexer/demultiplexer scheme is readily adapted to the industrial remote controller system where several sensors must communicate over transmission lines to the controller. With the multiplexer/demultiplexer configuration a very large number of sensors are able to communicate with the controller over extended distances through a single coaxial line.

The wide bandwidth of the HA-2541 coupled with its high output rating make it an excellent component of multiplexed data systems. Several schemes of signal switching can be used at the multiplexer end of the system. The HI-5051 switch is well suited for this application especially in the differential configuration shown in Figure 8. The charge injection due to switching channels in and out of the circuit is minimized in this differential mode. A reset pulse aligns the system synchronization and provides the basis for channel separation in the demultiplexer section. As the channels are sequentially placed at the HA-2541 input, they are transmitted to the demultiplexer circuit. In Figure 9 the HA-5320 sample and hold acts as a buffer for each channel and provide a reference source when the other channels are being addressed. Another plus in this demultiplexer circuit is the capability of "de-glitching" the information by simply shifting the clocking rate so as to place all channels in the hold mode during the presence of input spikes.

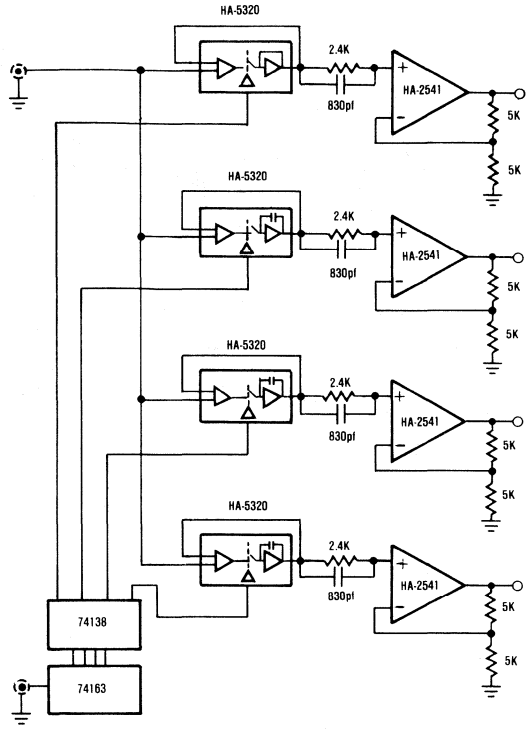


FIGURE 9. DEMULTIPLEXING WITH HA-2541

Write Amplifier

The recent proliferation of industrial and computerized equipment containing programmable memory has increased the need for reliable recording media. The magnetic tape medium is presently one of the most widely used methods. The primary component of any magnetic recording mechanism is the "write" mechanism. In support of this area the circuit of Figure 10 is presented.

The concept of the write generator is very basic. The digital input causes both a change in the output amplitude as well as a change in frequency. This type of operation is accomplished by altering the value of a resistor in the standard twin tee oscillator. An HI-201 analog switch was used to facilitate the switching action. The effect of the external components on the feedback network requires R_{6A} and R_{6B} to be much smaller than would normally have been expected when using the twin tee feedback scheme.

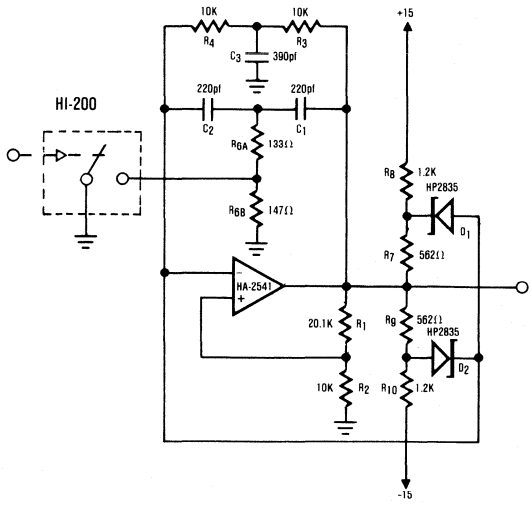


FIGURE 10. USING HA-2541 AS A WRITE AMPLIFIER

The output seen in the photograph of Figure 11 is limited with the aid of D_1, D_2 and R_4-R_7. This is aided by fixing the gain of the amplifier to just over three with R_8 and R_9.

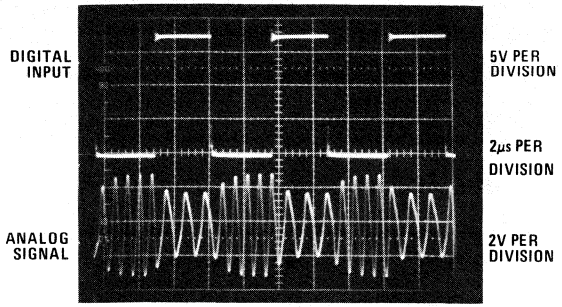


FIGURE 11. DIGITALLY CONTROLLED OUTPUT OF WRITE AMPLIFIERS

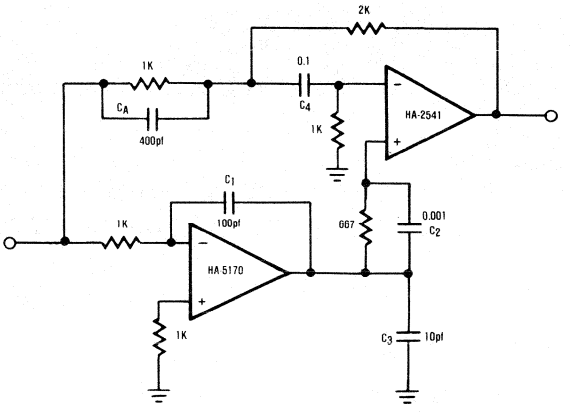


FIGURE 12. COMPOSITE AMPLIFIER

Composite Amplifier

The wide bandwidth of the HA-2541 can be used to extend the dynamic range of other useful but frequency limited amplifiers. The HA-5170 is an excellent example of this adaptation. The precision DC characteristic of the HA-5170 are augmented by the bandwidth of the HA-2541. This produces a composite amplifier which approximates the DC performance of the HA-5170 and the frequency range of the HA-2541.

The circuit in Figure 12 has been optimized for operation in the neighborhood of 15MHz. Optimization is quite simple and is accomplished largely through C_A. If a lower frequency region of operation is desired, an additional capacitor, C_2, will give greater flexibility in the choice of component values.

Programmable Amplifier

Often a circuit will be called upon to perform several functions. In these situations the variable gain configuration of Figure 13 may be quite useful. This programmable gain stage depends on CMOS analog switches to alter the amount of feedback and thereby the gain of the stage. Placement of the switching elements inside relatively low current area of the feedback loop, minimizes the effects of bias currents and switch resistance on the calculated gain of the stage. Voltage spikes may occur during the switching process, resulting in temporarily reduced gain because of the make-before-break operation of the switches. This can be minimized by providing a separate voltage divider network for each switched gain.

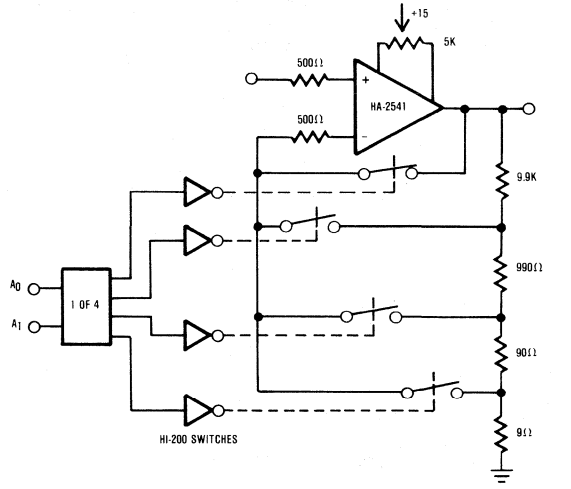


FIGURE 13. A GAIN PROGRAMMABLE HA-2541

References

1. William L. Hughes, "Television Fundamentals and Standards" Electronic Engineers Handbook ed. Bonald G. Fink (McGraw-Hill, 1975) p. 20-3.

2. Thermalloy Semiconductor Accessories Catalog, Thermalloy Inc. Dallas, Texas.

3. Arthur B. Williams, "Designers Handbook of Integrated Circuits." (McGraw-Hill, 1984) pps. 1-10, 1-27.

APP NOTE

FOR YOUR INFORMATION

No. 551

Harris Analog

RECOMMENDED TEST PROCEDURES FOR OPERATIONAL AMPLIFIERS

Authors: Wes Kilgore and Brian Mathews

Introduction

The following text describes the basic test procedures that can be used for most Harris Op-Amps. Note that all measurement conversions have been taken into account in the equations stated.

1) Offset Voltage

The offset voltage V_{IO} of the amplifier under test (AUT) is measured via test circuit 1 as follows:

1. Set +V and -V supplies to values specified in Table 1, Column 1 and V_{DC} to zero volts.
2. Close S_1 and S_2, open S_3.
3. Choose: R_f = 50K for non-precision amplifiers.
   R_f = 5M for precision amplifiers.
4. Measure voltage at E in volts (label as E_1).
   $V_{IO} = E_1$ (mV) for R_f = 50K
   or
   $V_{IO} = E_1$ *10 (μV) for R_f = 5M

The gain of this circuit with R_f = 50K (R_f = 5M) requires the output to be driven to 1000 (100,000) times the offset oltage necessary to maintain the output of the AUT at zero volts. Note that the AUT output is always identical to V_{DC}. Overall circuit stability is maintained by the adjustable feedback capacitor C_A.

2) Input Bias Current

The bias current flowing in or out of the positive terminal of the AUT (I_{B+}) is obtained using test circuit 1 by:

1. Measuring E_1 as in procedure 1 (use R_S = 100K for JFET input devices).
2. Maintain V_{DC} at zero.
3. Close S_2, open S_1 and S_3.
4. Measuring voltage at E in volts (label as E_2).
   $I_{B+} = (E_1 - E_2) \times 100$ (nA) for R_f = 50K, R_S = 10K
   or
   $I_{B+} = (E_1 - E_2) \times 10$ (nA) for R_f = 50K, R_S = 100K

The bias current flowing in or out of the negative terminal (I_{B-}) is found by:

1. Following steps 1 and 2 for I_{B+}.
2. Closing S_1, opening S_2 and S_3.
3. Measuring voltage at E in volts (label as E_3).
   $I_{B-} = (E_1 - E_3) \times 100$ (nA) for R_f = 50K, R_S = 10K
   or
   $I_{B-} = (E_1 - E_3) \times 10$ (nA) for R_f = 50K, R_S = 100K

3) Input Offset Current

Using test circuit 1, the input offset current I_{IO} of the AUT is determined by:

1. Measuring E_1 as in procedure 1.
2. Maintaining V_{DC} at zero.
3. Opening S_1, S_2 and S_3.
4. Measuring voltage at E in volts (label as E_4).
   $I_{IO} = (E_1 - E_4) \times 100$ (nA) for R_f = 50K, R_S = 10K
   or
   $I_{IO} = (E_1 - E_4) \times 10$ (nA) for R_f = 50K, R_S = 100K

4) Power Supply Rejection Ratio

Both positive and negative PSRR's are measured via test circuit 1. For PSRR+:

1. Close S_1 and S_2, open S_3.
2. Choose: R_f = 50K
3. Set V_{DC} = 0, +V = 10V, and -V = -15V.
4. Measure voltage at E in volts (label as E_5).
5. Change +V to +20V.
6. Measure voltage at E in volts (label as E_6).

$$PSRR+ = 20 \log_{10} \left| \frac{10^4}{E_5 - E_6} \right| \text{ (dB) for } R_f = 50K$$

Similarly for PSRR-:

1. Follow steps 1 and 2 for PSRR+ above.
2. Set V_{DC} = 0, +V = +15V, -V = -10.
3. Measure voltage at E in volts (label as E_7).
4. Change -V to -20V.
5. Measure voltage at E in volts (label as E_8).

$$PSRR- = 20 \log_{10} \left| \frac{10^4}{E_7 - E_8} \right| \text{ (dB) for } R_f = 50K$$

5) Common Mode Rejection Ratio

The CMRR is determined by adjusting test circuit 1 as follows:

1. Close S_1 and S_2, open S_3.
2. Chose: R_f = 50K
3. Set +V = +5V, -V = -25V, and V_{DC} = -10V.
4. Measure voltage at E in volts (label as E_9).
5. Set +V = 25V, -V = -5V, and V_{DC} = 10V.
6. Measure voltage at E in volts (label as E_{10}).

$$CMRR = 20 \log_{10} \left| \frac{2 \times 10^4}{E_9 - E_{10}} \right| \text{ (dB) for } R_f = 50K$$

6) Output Voltage Swing

Test circuit 2 is adjusted to measure V_{out+} and V_{out-} the procedure is:

1. Select appropriate +V and -V supply values from Table 1, Column 1.
2. Select specified R_L from Table 1, Column 2.
3. Set V_{in} = 0.5V.
4. Measure voltage at E in volts. V_{out+} = E (volts)

Similarly V_{out-} is found by:

1. Selecting specified R_L from Table 1, Column 1.
2. Setting V_{in} = -0.5V.
3. Measuring voltage at E in volts. V_{out-} = E (volts)

7) Output Current

The output current corresponding to the output voltage of procedure 7 is found by:

1. Measuring V_{out-} and V_{out+} as in procedure 7.

$$I_{out+} = \frac{V_{out+}}{R_L}$$ where R_L is from Table 1, Column 2.

$$I_{out-} = \frac{V_{out-}}{R_L}$$ where R_L is from Table 1, Column 2.

8) Open Loop Gain

Both positive A_{VS+} and negative A_{VS-} open loop gain measurements are determined by adjusting test circuit 1.

For A_{VS+}:

1. Close S_1, S_2 and S_3.
2. Select specified R_L from Table 1, Column 3.
3. Set R_f = 50K.
4. Set V_{DC} = 0V, +V = +15V, and -V = -15V.
5. Measure voltage at E in volts (label as E_{13}).
6. Set V_{DC} = 10V.
7. Measure voltage at E in volts (label as E_{14}).

$$A_{VS+} = \frac{10}{E_{14} - E_{13}}$$ (V/mV) for R_f = 50K

For A_{VS-}:

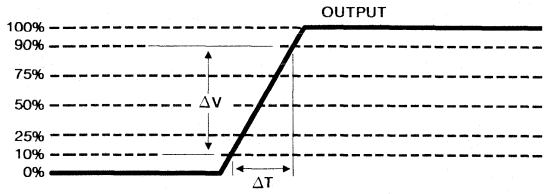
1. Follow steps 1, 2, 3, 4, and 5 above.
2. Set V_{DC} = -10V.
3. Measure voltage at E in volts (label as E_{15}).

$$A_{VS-} = \frac{10}{E_{13} - E_{15}}$$ (V/mV) for R_f = 50K

9) Slew Rate

Test circuit 3 is used for measurement of positive and negative slew rate. For SR+:

1. Select specified R_L, A_{CL}, and C_L from Table 1, Columns 4, 5 and 6.
2. Apply a positive step voltage to V_{AC} (refer to data book for test wave form).
3. Observe ΔV and ΔT at E. A standard approach is to use the 10% and 90% points or else the 25% and 75% points on the wave form.



$$SR = \frac{\Delta V}{\Delta T}$$

For SR- repeat above procedure with negative input pulse.

$$SR- = \frac{\Delta V}{\Delta T}$$

10) Full Power Bandwidth

Full power bandwidth is calculated by:

1. Measuring slew rate as above in procedure 11.
2. Measuring V_{out+} as in procedure 7. (Typically V_{out+} is assumed to be the guaranteed minimum V_{out}, usually 10V.)

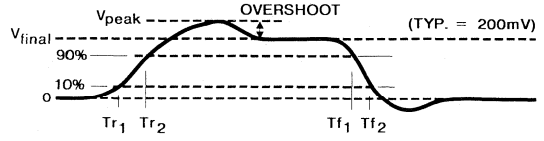
$$FPBW = \frac{SR+}{2\pi V_{out\text{-}peak}}$$

11) Rise Time, Fall Time and Overshoot

The small signal step response of the AUT is determined via test circuit 3. The procedure requires:

1. Selecting the appropriate R_L, A_{CL}, and C_L from Table 1, Columns 4, 5 and 6.
2. Applying a positive input step voltage for rise time T_r and positive overshoot OS+.

   Applying a negative input step voltage for fall time T_f and negative overshoot OS-.
   (Refer to data book for input wave forms.)
3. Observe output of AUT noting the key points as shown.



$T_r = T_{r2} - T_{r1}$
$T_f = T_{f2} - T_{f1}$

$$OS = \frac{V_{peak} - V_{final}}{V_{final}} \times 100\ (\%)$$

12) Settling Time

Test circuit 6 is appropriate for settling time (T_S) measurement, the procedure is:

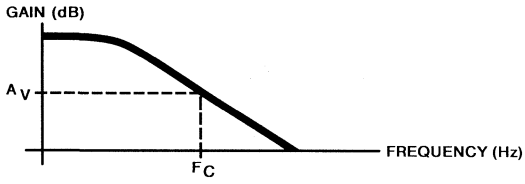
1. Select R_1 and R_2 such that AUT is at the A_{CL} stated in Table 1, Column 5.
2. Select R_3 and R_4 so that $R_3 \geq 2R_1$ and $R_4 \geq 2R_2$ with the condition that the ratio $\frac{R_3}{R_4} = \frac{R_1}{R_2}$ be maintained.
3. Apply step voltage as specified in data book.
4. Measure the time from t_1 (time input step applied) to t_2 (the time E_S settles to within a specified percentage of V_{out} - see data book). $t_S = t_2 - t_1$

NOTE: Clipping diodes of test circuit 6 prevent overdrive of oscilloscope. (Recommend fast Schottky diodes.)

13) Gain Bandwidth Product

Test circuit 4 is used for measuring GBP. The procedure is:

1. Sweep V_{in} thru the required frequency range.
2. With a network analyzer view gain (dB) versus frequency as below.

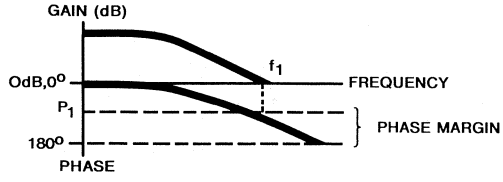


3. At the voltage gain of interest A_V determine the corresponding frequency F_C. Note that chosen A_V must be greater than or equal to that stated to that stated in Table 1. GBP = A_V x FC (Hz) where A_V is in V/V.

14) Phase Margin (Network Analyzer Method)

Test circuit 4 is used to obtain phase margin measurement. The procedure is:

1. Sweep V_{in} thru the required frequency range.
2. Display gain in dB and phase in degrees versus frequency on analyzer as shown.



3. At a gain of 0 dB, record frequency f_1 and corresponding phase P_1. Phase margin = $180^o - P1^o$

15) Input Noise Voltage

Test circuit 5 is designed for measuring input noise voltage. Use of the Quantec Noise Analyzer is recommended to obtain measurements at 1Hz bandwidth around a specific center frequency. The procedure is:

1. Set $R_g = 0$
2. Set circuit card to gain of 10.
3. Select measurement frequency of interest.
4. Record noise voltage (label as En1). Units are $nV/\sqrt{Hz}$

16) Input Noise Current

Using test circuit 5, the input noise current is obtained by:

1. Measuring E_{n1} as above for the desired frequency of interest.
2. Adjust R_g so that $V_O > 2E_{n1}$ (label V_O as E_{n2}).

$$I_n = \frac{\sqrt{E_{n2}^2 - E_{n1}^2 - 4kTR_g}}{R_g^2}$$

Where $K = 1.38 \times 10^{-3}$ (Boltzmann's Constant)
$T = 300^oC$ (27^oC)

17) Channel Separation (Cross Talk)

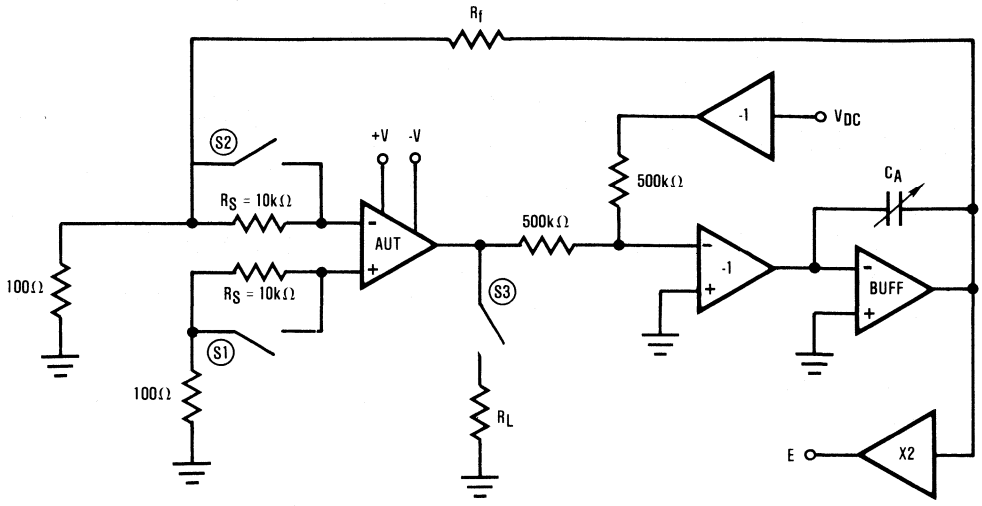
Test circuit 7 is used to measure channel separation (CS). The procedure is as follows:

1. Apply V_{in} at the frequency of interest to input of channel 1.
2. Measure V_{01}.
3. Measure V_{02} of channel 2.

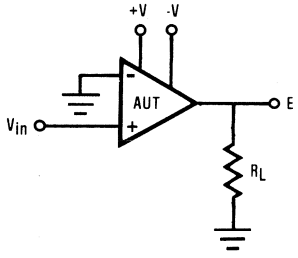
$$CS = 20 \log_{10} \left| \frac{V_{02}}{100\, V_{01}} \right| dB$$

TABLE 1.

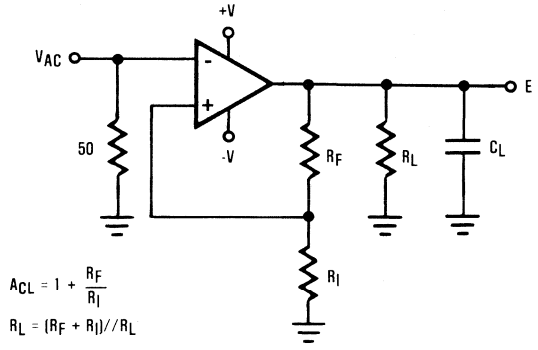
PART NUMBER	(1) SUPPLY VOLTAGE (+V)	PARAMETERS TO MEASURE				
		V_{out}	A_{VS}	SLEW RATE, OS, TR, TF		
		(2) R_L(K)	(3) R_L(K)	(4) R_L(K)	(5) A_{CL}	(6) C_L(pF)
HA-2400/04/05	15	2	2	2	1	50
HA-2500/02/05	15	2	2	2	1	50
HA-2510/12/15	15	2	2	2	1	50
HA-2520/02/05	15	2	2	2	3	50
HA-2539	15	1	1	1	10	10
HA-2540	15	1	1	1	10	10
HA-2541	15	2	2	2	1	10
HA-2542	15	1	1	1	2	10
HA-2600/02/05	15	2	2	2	1	100
HA-2620/02/05	15	2	2	2	5	50
HA-2640/05	40	5	5	5	1	50
HA-4741	15	10	2	2	1	50
HA-5101	15	2	2	2	1	50
HA-5102/04	15	2	2	2	1	50
HA-5111	15	2	2	2	10	50
HA-5112/14	15	2	2	2	10	50
HA-5127	15	0.6	2	2	1	50
HA-5130/05	15	0.6	2	2	1	100
HA-5134	15	2	2	2	1	50
HA-5137	15	0.6	2	2	5	50
HA-5141/12/14	+5/0	50	50	50	1	50
HA-5147	15	0.6	2	2	10	50
HA-5151/12/14	15	10	10	10	1	50
HA-5160/62	15	2	2	2	10	50
HA-5170	15	2	2	2	1	50
HA-5180	15	2	2	2	1	50
HA-5190/95	15	0.2	0.2	2	5	10



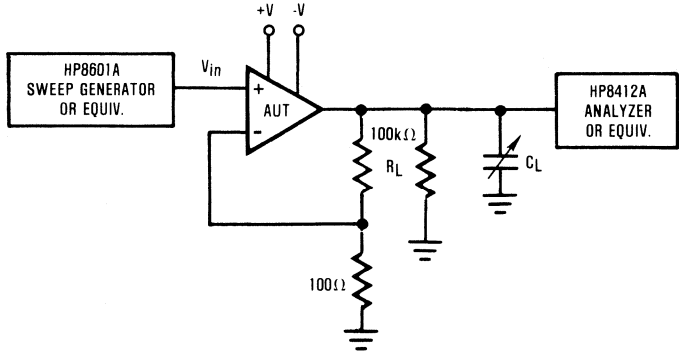
TEST CIRCUIT 1



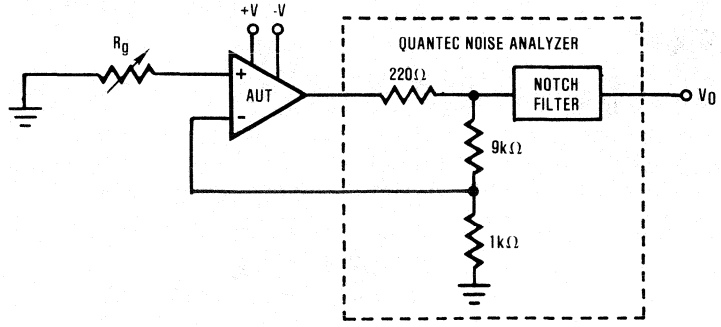
TEST CIRCUIT 2



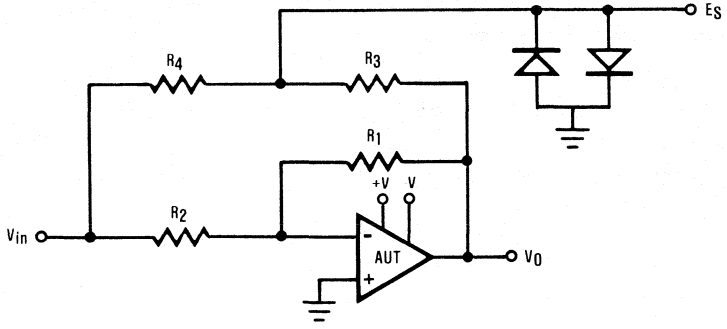
TEST CIRCUIT 3



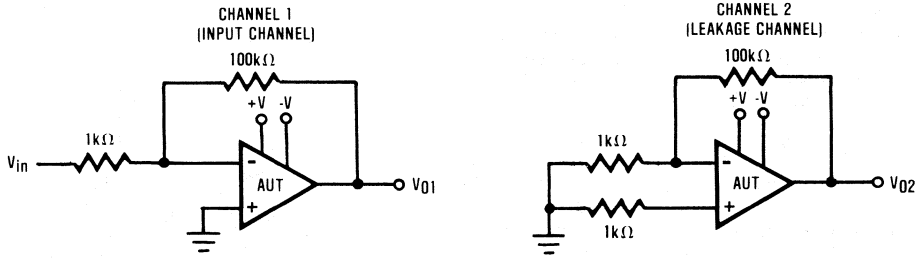
TEST CIRCUIT 4



TEST CIRCUIT 5



TEST CIRCUIT 6



TEST CIRCUIT 7

USING THE HA-2542

Richard A. Whitehead

Introduction

In the multi-faceted electronics industry, there are many circuit applications which require the capabilities of two or more types of operational amplifiers in the same location. To fulfill this need, design engineers are usually challenged with fabricating a discrete amplifier design or selecting an expensive hybrid amplifier which appears to be an "ALL-IN-ONE" type of amplifier.

The Harris HA-2542 is a state of the art monolithic device which also approaches the "ALL-IN-ONE" amplifier concept. This device features an outstanding set of AC parameters augmented by excellent output drive capability providing for suitable application in both high speed and high output drive circuits.

Offset voltage nulling and bandwidth controls add flexibility when the HA-2542 is used in performance-tailored applications.

Primarily intended to be used in balanced 50Ω and 75Ω coaxial cable systems as a driver, the HA-2542 could also be used as a power booster in audio systems as well as a power amp in power supply circuits. This device would also be suitable as a small DC motor driver.

Prototyping Guidelines

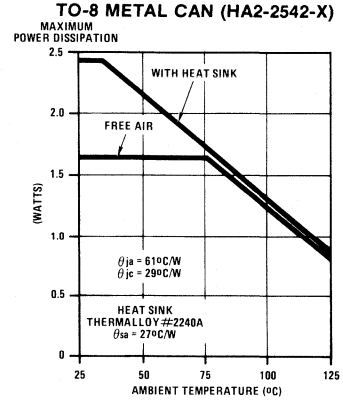
For best overall performance in any application, it is recommended that high frequency layout techniques be used. This should include: 1) mounting the device through a ground plane: 2) connecting unused pins to the ground plane: 3) mounting feedback components on Teflon standoffs and/or locating these components as close to the device as possible; 4) placing power supply decoupling capacitors from device supply pins to ground.

As a result of speed and bandwidth optimization, the HA-2542's case potential, when powered-up is equal to the V- potential. Therefore, contact with other circuitry or ground should be avoided.

Heat Sinking (Also Refer to Application Note 556)

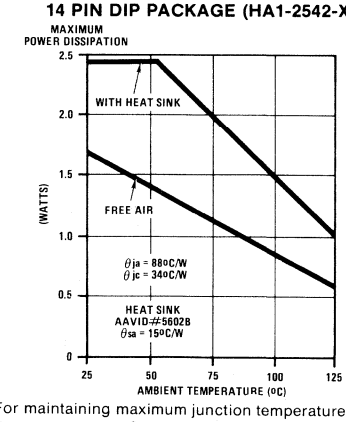
To drive heavy loads found in typical coaxial cable systems, the HA-2542 may require heat sinking to avoid exceeding its maximum junction temperature (+175°C). Figure 1 shows maximum power dissipation curves derived for the HA-2542 with and without the recommended heat sink. Should another type of heat sink be used, then the following expression should be used to determine maximum power dissipation.

TO-8 METAL CAN (HA2-2542-X)



NOTE: For maintaining maximum junction temperatures below +175°C, derate at 16.4mW/°C beyond +75°C ambient

14 PIN DIP PACKAGE (HA1-2542-X)



NOTE: For maintaining maximum junction temperatures below +175°C, derate at 11.4mW/°C beyond +25°C ambient.

FIGURE 1. HA-2542 MAXIMUM POWER DISSIPATION CURVES

$$P_{dmax} = \frac{T_{jmax} - T_A}{\theta_{j\text{-}c} + \theta_{c\text{-}s} + \theta_{s\text{-}a}}$$

Where: T_{jmax} = maximum junction temperature of the device

T_A = Ambient

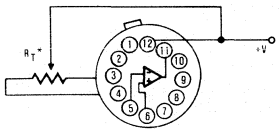
$\theta_{j\text{-}c}$ = Junction to case thermal resistance

$\theta_{c\text{-}s}$ = Case to heat sink thermal resistance

$\theta_{s\text{-}a}$ = Heat sink to ambient thermal resistance

Performance Enhancements

DC errors can be reduced and AC stability increased by recommended adjustments to the control points made available in the HA-2542 device. The suggested method for nulling the offset voltage of HA-2542 is shown in Figure 2, while Figure 3 suggests the method for controlling the bandwidth. Figure 4 shows normalized AC parameters versus compensation capacitance. Experimental results indicated that approximately 17pF was necessary to stabilize the HA-2542 for unity gain operation.



*OFFSET ADJUSTMENT RANGE IS APPROXIMATELY ±15mV FOR R_T = 5KΩ.

FIGURE 2. SUGGESTED OFFSET VOLTAGE ADJUSTMENT

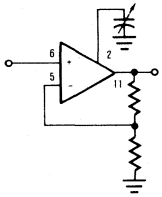


FIGURE 3. SUGGESTED METHOD FOR INCREASING AC STABILITY

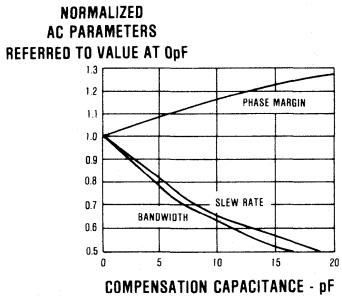
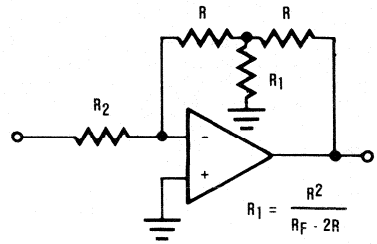


FIGURE 4. NORMALIZED AC PARAMETERS

For best high frequency performance, feedback resistor values should be restricted to minimal values. Values below 5KΩ are recommended to reduce possibilities of introducing unwanted poles into the application's transfer function. Figure 5 indicates how high values for closed loop gain can be implemented, while maintaining feedback element values. This method is called "T network" feedback and values for the resistors can be derived from the following expression.

$$R_1 = \frac{R^2}{R_f - 2R}$$

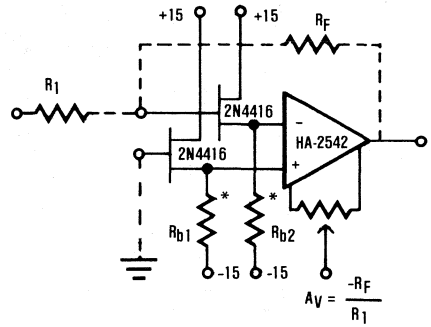
Where: R_f is the value of feedback resistance to be reduced and R is a value preselected by the designer.



WHERE R IS PRESELECTED AND R_F IS DESIRED FEEDBACK RESISTOR VALUE.

FIGURE 5. KEEPING FEEDBACK VALUES LOW

Utilizing some relatively familiar techniques, the input bias currents of the HA-2542 can be sharply reduced. Figure 6 employs discrete FETs to provide input bias currents in the pA range without appreciably diminishing the AC performance.



*R_{b1} AND R_{b2} SHOULD BE DETERMINED EXPERIMENTALLY FOR BEST RESULTS.

FIGURE 6. USING DISCRETE FETs TO REDUCE THE HA-2542's INPUT BIAS CURRENT

Composite amplifiers are hybrid "marriages" between precision and wideband operational amplifiers. Using the HA-2542 as the AC device in the composite amplifier shown in Figure 7 provides an additional dimension to its

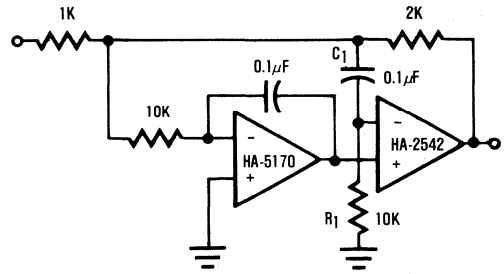


FIGURE 7. COMPOSITE AMPLIFIER CIRCUIT REDUCES DC ERRORS

capabilities. Now, the hybrid represents a precision type, high speed, wideband, power amplifier.

In this circuit, high frequency amplification tasks are performed by the HA-2542 and are set by combination R_1-C_1. The HA-5170 acts as the DC amplifier providing precision type input parameters while cascading its DC gain with that of the HA-2542. This cascade of gains develops very high loop gain for the composite amplifier.

Applications

Most attractive to the video system designer is the HA-2542's combination of speed, bandwidth, and output drive capability. Augmenting these features are much desired differential gain and phase specifications of 0.1% and 0.2 degrees respectively. Previously these parameters could only be provided by hybrid or discrete component circuitry. A primary application which fully utilizes these features is the coaxial cable driver.

The configuration shown in Figure 8 represents a simple multi-channel security system. The HA-2542 is being operated at a closed loop gain of 2 and is driving a balanced coaxial line system which appears as a 50Ω load. The signal throughput from the multiplexer input to the coaxial outputs is 1. Experimental results showed that coaxial line lengths could exceed 100 feet without adversely affecting video signal quality.

HA-2542 is capable of $2V_{p-p}$ signals to 16MHz in this configuration. Resistor R_B is used to trim overall system gain to prevent color saturation if the cameras and monitors are color types. The controller to the multiplexer could be one of several variations including remote, remote wired, or automatically time sequenced.

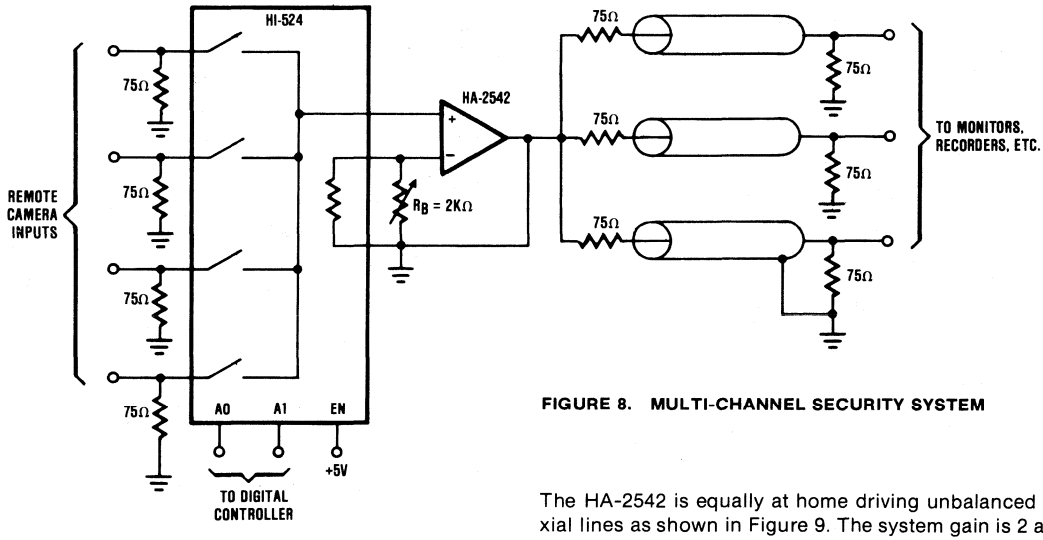


FIGURE 8. MULTI-CHANNEL SECURITY SYSTEM

The HA-2542 is equally at home driving unbalanced coaxial lines as shown in Figure 9. The system gain is 2 and, depending on cable length, compensation capacitance may be necessary to provide additional stability. In this configuration, the HA-2542 can delivery $10V_{p-p}$ signals at frequencies above 8MHz. For this application, power requirements will usually necessitate the use of heat sinking for the HA-2542.

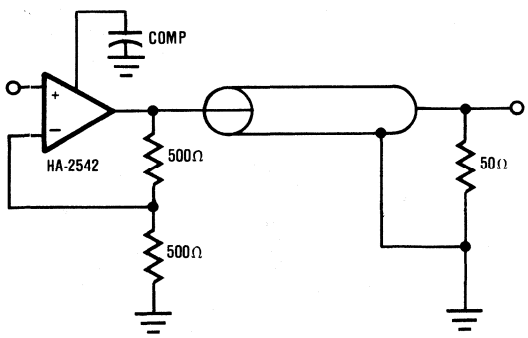


FIGURE 9. DRIVING UNBALANCED COAXIAL CABLES

Another video type application requiring an op amp with excellent speed and output drive is the analog input driver of a flash converter circuit. Figure 10 shows the HA-2542 buffering the input of an 8-bit flash converter. Because of the heavy input capacitance (100pF - 300pF) and high number of individual internal comparator inputs (255), the impedance of the input is non-linear. A typical high speed op amp used in this configuration would exhibit oscillation tendencies regardless of compensation and isolation techniques used. The photograph shown in Figure 10 indicates that the HA-2542 is very stable in this application.

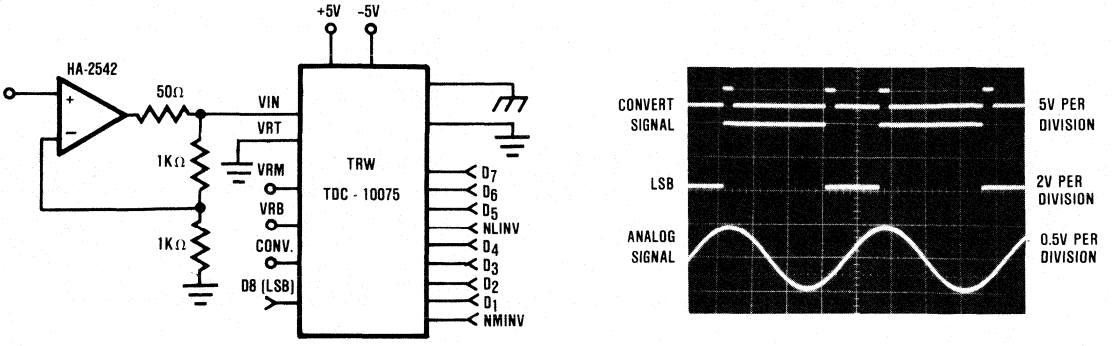


FIGURE 10. DRIVING THE NON-LINEAR INPUT IMPEDANCE OF FLASH CONVERTERS (ONE INPUT SHOWN)

Power Supply

The HA-2542 with its excellent output current could also be used as a power source in DC power supply systems. In Figure 11, a simplified digitally programmable power supply is shown which utilizes the high output current capabilities of the HA-2542. Combination R_1-R_2 sets the gain of the amplifier, while V_{REF} and the "weighted" resistor ladder permit the HI-201 to perform digital selection of the voltage to be used.

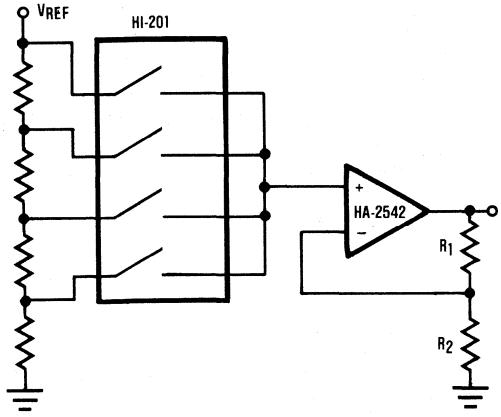


FIGURE 11. DIGITALLY PROGRAMMABLE POWER SUPPLY

Audio

In studio quality audio systems, the HA-2542 could be readily used in driver applications such as a speaker driver. Figure 12 shows a method which increases the power capability of a drive system for audio speakers. In this circuit two HA-2542s are used to operate on half cycles only, which greatly increases their power handling capability. "Bridging" the speaker as shown makes 200mA of output current available to drive the load. The HA-5102 is used as an AC coupled, low noise, preamplifier which drives the bridge circuit.

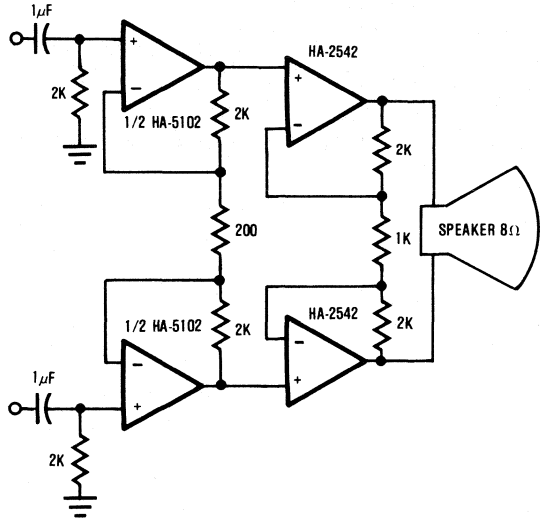


FIGURE 12. BRIDGE LOAD DRIVE FOR AUDIO CIRCUITS

Another variation of the bridged load type circuit is shown in Figure 13a. In this circuit the load voltage is increased by a factor of 4. The HA-2542s are connected in a manner such that the output voltages will be equal in amplitude and opposite in phase. This circuit can also be used to drive long lengths of twisted shielded pair cable.

Boosting Output Current

If the excellent output current of the HA-2542 requires boosting because of extreme loading, then the configuration shown in Figure 13b could be used. In this circuit, the HA-2542 drives the high power transistor stage and provides circuit gain. With the power transistors shown, the output drive is increased to several amps. Speed and power bandwidth have not been appreciably affected. Boosting the output current to these higher levels provides for additional implementation into DC motor drive or bridge transducer drive circuits.

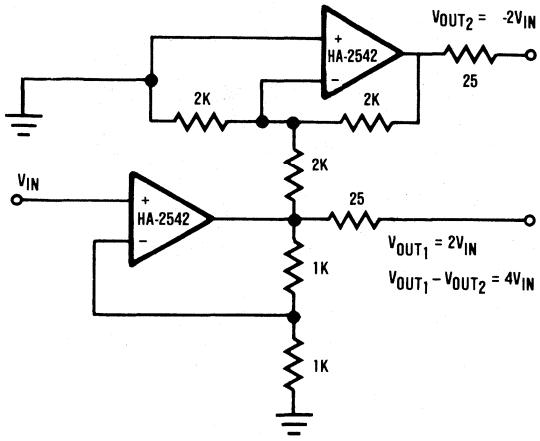


FIGURE 13A. DIFFERENTIAL CIRCUIT FOR LINE DRIVING

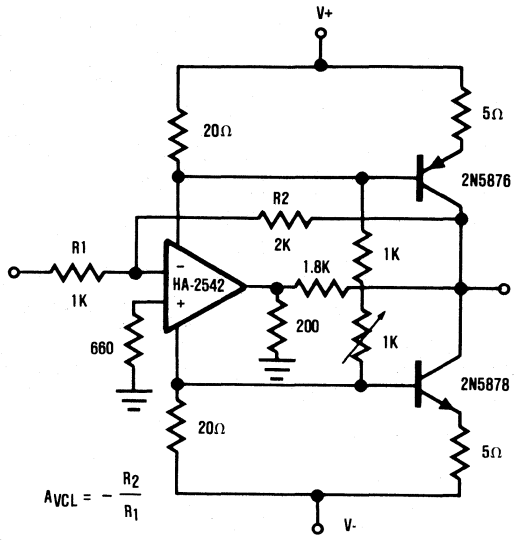


FIGURE 13B. DRIVER STAGE FOR HIGH POWER TRANSISTORS

The output drive capability of the HA-2542 is highly suitable for direct drive applications of small DC motors and, since it is an operational amplifier, it can also perform the function of motor speed control. This type of closed loop system can be found throughout the robotics and media recording industries.

The system shown in Figure 14 consists of the HA-2542, a small 12V DC motor, and a position encoder. During operation, the encoder causes a series of "constant width" pulses to charge C_1. The integrated pulses develop a reference voltage which is proportional to motor speed and is applied to the inverting input of HA-2542. The non-inverting input is held at a constant voltage which represents the desired motor speed. A difference between these two inputs will send a corrected drive signal to the motor which completes the speed control system loop.

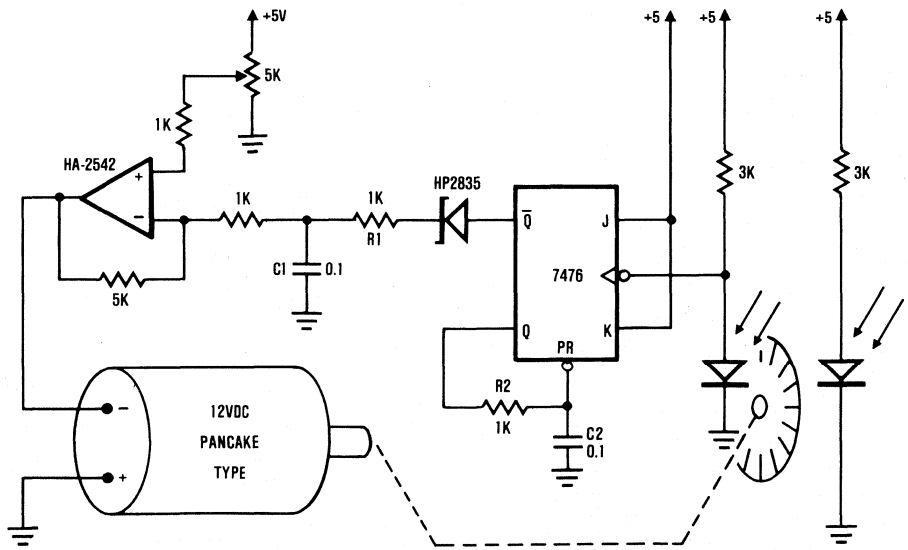


FIGURE 14. CONTROLLING DC MOTOR SPEED WITH HA-2542

HA-5147/37/27, ULTRA LOW NOISE AMPLIFIERS

By Alan Hansford

Introduction

Engineers interested in precision signal processing will find the HA-51X7, with its unique features, very interesting. Utilizing an advanced design with special device geometries, the HA-51X7 has moved the Harris dielectric process into a new arena of both speed and precision. Perhaps one of the most remarkable features of the HA-51X7 is its ultra low noise performance, which makes it the first monolithic amplifier to combine speed, precision, and ultra low noise operation (Figure 1).

To realize this device, intense attention was given to the "total" design from input to output (Figure 2).

The input stage consists of a cross-coupled differential pair which provides a very high CMRR (125dB) through the use of CASCODE circuits. Effective use of the bias current cancellation scheme also keeps the bias currents to a mere 10nA. With laser trimming of the load resistors R1 and R2, the offset voltage is kept below 25μV at 25°C. The entire input stage has been optimized for low noise operation and is largely responsible for the amplifier's ultra low noise voltage of 3.0nV/$\sqrt{Hz}$ @ 1KHz. Low frequency noise, on the other hand, is particularly important in DC applications and the HA-5147's 2.7Hz lower noise corner will prove quite beneficial for many users.

The loading on R1 and R2 is kept to a minimum through the use of emitter followers between the input stage and the second differential pair. C4 provides a feedforward path around the second stage at high frequencies and feeds into the level shifter and current mirror section. This portion of the design provides a differential to single-ended conversion and relies on C2 to tailor the rolloff of the second stage. Two vertically-constructed PNP transistors within the level shifter dramatically increase the frequency response of the amplifier compared to that of other construction techniques.

Emitter followers in the fourth stage reduce the capacitive loading effects of C1 by providing a separate driver for C1 and the output stage. The output stage here is a high speed buffer that employs complementary transistors as well as short circuit protection.

The high performance features of the HA-5147 have quite clearly moved this device closer to the "ideal" than any other amplifier in its class. Yet, with some simple external components, this device can be positioned even closer to the "ideal." An offset nulling potentiometer can reduce V_{OS} (Figure 3a), while the already hefty output stage (I_{out} = 20mAmin) can be boosted without reducing the excellent speed and bandwidth characteristics (Figure 3b).

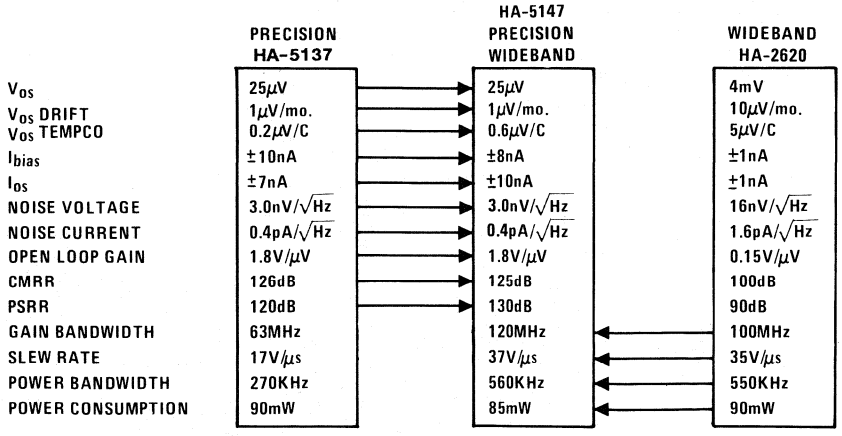


FIGURE 1.
The HA-5147 combines the qualities of precision Op Amps with those of the wideband speed category.

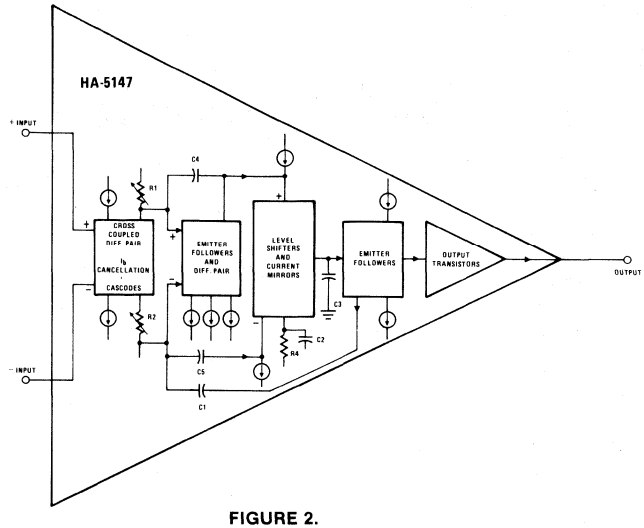


FIGURE 2.

Intense attention was given to the "total" design from inputs to output.

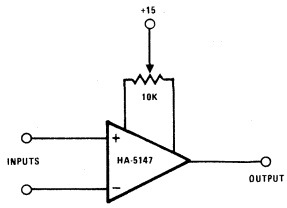


FIGURE 3a.

Nulling the HA-5147's offset voltage to 0 volts brings it closer to "ideal"

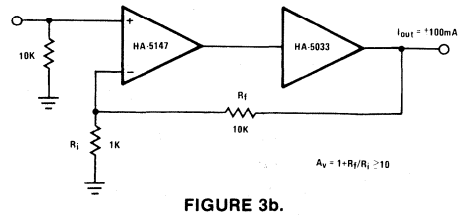


FIGURE 3b.

The HA-5147's output current can be boosted to ±100mA by using the HA-5033. AC performance is not affected.

Low Noise Design

Since the HA-51X7 is a very low noise operational amplifier, low noise design techniques must be used to make the most of this feature. There are two primary means of keeping noise down, one requires the amplifier inputs to look into low source resistances and the other requires bandwidth limiting by filtering. A short outline of noise prediction will be presented here to support these concepts.

Noise can be divided into several categories, which include thermal noise (white noise) and flicker noise (pink noise or 1/f noise). The feedback components are strongly dominated by thermal noise making thermal noise the most important of these from a system design standpoint (an exception to this are high gain DC amplifiers which require low 1/f noise as measured by the noise corner). Flicker noise is more a function of the amplifier construction quality, and system design variations are less effective in reducing this type of noise.

Noise is usually rated in one of two ways. The first is RMS voltage or current (a measure of peak-to-peak noise in a given bandwidth) and the second is by noise density spectrum in $V/\sqrt{Hz}$ and $A/\sqrt{Hz}$ (a measure of the spectral content of the noise in the frequency domain). The two rating schemes are related, with RMS noise levels generated from the integration of the noise density spectrum over a desired frequency bandwidth.

As an illustration of noise prediction, the noise density for the standard inverting amplifier configuration (Figure 4a) will be determined. The total noise is derived from the combination of several noise sources, only three of which are of any significance. These are the amplifier's noise voltage, the thermal noise of the feedback components, and the noise generated by the current noise of the amplifier within the feedback components.

The total noise is defined as the square root of the sum of the squares of the individual noise terms.

$$E_n = G\sqrt{(E_{amp})^2 + (E_{\substack{\text{feedback}\\\text{network}}})^2 + (E_{\substack{\text{current noise in}\\\text{feedback network}}})^2}$$

E_n = total noise

G = gain of stage

E_{amp} = amplifier noise voltage.....3.0nV/$\sqrt{Hz}$ @ f > 1KHz

$$E_{\substack{\text{feedback}\\\text{network}}} = \sqrt{4KTR_{eq}} \quad \text{where...} \quad \begin{array}{l} K = 1.381E\text{-}23 \\ T = 300 \\ R_{eq} = R \,||\, R_f \end{array}$$

$$E_{\substack{\text{current noise in}\\\text{feedback network}}} = I_{noise}\, R_{eq}$$

I_{noise} = 0.4pA/$\sqrt{Hz}$ @ f > 1KHz

or more specifically . . .

$$E_n = G\sqrt{(E_{amp})^2 + R_{eq}4KT + (I_{noise}\, R_{eq})^2}$$

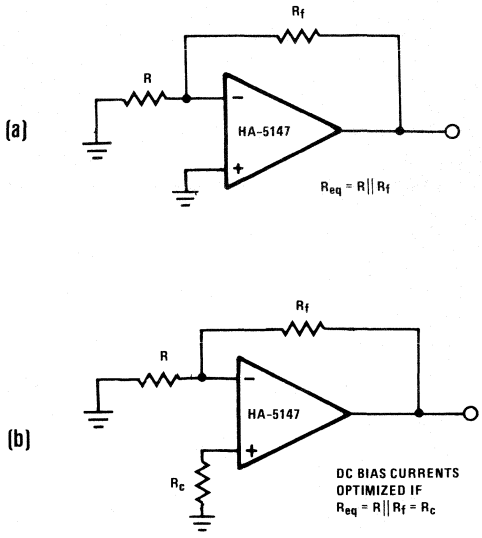


FIGURE 4. NOISE PREDICTION CIRCUITS

A reasonable estimate of noise levels can be generated with these two basic amplifier circuits.

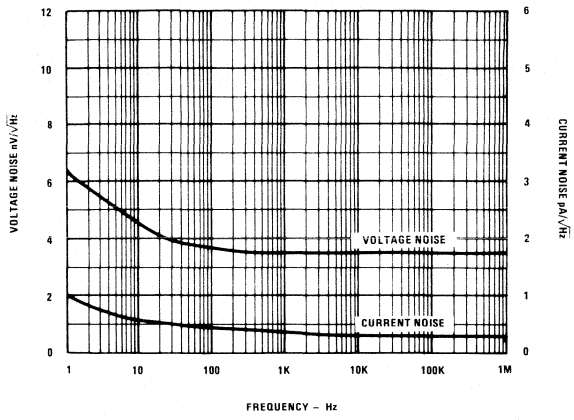


FIGURE 5. HA-5147 NOISE CHARACTERISTICS

The HA-5147's exceptional noise characteristics may be used to improve existing and new high quality audio systems. HA-5127 and HA-5137 have identical noise characteristics.

Both the amplifier noise voltage and noise current are constant above 1KHz and rise slightly for lower frequencies (Figure 5). The resistor thermal noise is derived from the parallel combination of the feedback network (R_{eq}) and several constants (4KT). The third noise term again uses the equivalent resistance of the feedback network (R_{eq}) as well as the current noise generated at the input terminals of the amplifier.

It should be evident from the above formula that extremely large values of R_{eq} (especially over 10Kohm) will dominate the noise density while low values for R_{eq} will yield to the amplifier's own noise characteristics. Note the asyptotic convergence of the noise voltages in Figures 3a-3c at low values of R_{eq}.

A second circuit (Figure 4b) balances the effects of input bias currents by placing a resistor R_C, equal to R_{eq}, between the non-inverting input and ground. While reducing DC errors, this configuration adds two additional terms to the noise formula.

$$E_n = G \sqrt{(E_{amp})^2 + R_{eq}4KT + (I_{noise}\, R_{eq})^2 + R_C\, 4KT + (I_{noise}\, R_C)^2}$$

The original contributors to output noise remain as before and the additional terms represent the thermal contribution by R_C and the associated amplifier current noise seen through that resistor. To optimize DC design, $R_{in} \,||\, R_f = R_{eq} = R_C$, therefore the noise density equation reduces to . . .

$$E_n = G \sqrt{(E_{amp})^2 + 2R_{eq}4KT + 2(I_{noise}\, R_{eq})^2}$$

Again the relationship between large values of R_{eq} and a high noise density spectrum remains.

RMS noise is derived in part as the integral of the noise density spectrum over a given bandwidth. Below is the complete expression . . .

$$E_{rms} \text{ (from } f_0 \text{ to } f_1) = \sqrt{\int_{f_0}^{f_1} E_{\substack{\text{noise} \\ \text{density} \\ \text{spectrum}}}^{\,2}\, df}$$

The strict integration assuming E_n is constant works well for f_0 above $\approx$ 1KHz. Both the amplifier's noise voltage and the noise current increase for frequencies below 1KHz. This makes for difficult integration since complicated expressions for I_{noise} and E_{amp} must be generated. To avoid this problem, graphical integration techniques or sampled methods can be used with great success.

The curves in Figures 6a-6c illustrate the relationship between the RMS noise and R_{eq} for both amplifier designs. It should be apparent from the predicted RMS noise curves that increased bandwidth causes an increase in noise voltage. An interesting effect of this relationship is that only absolute bandwidth (f_1-f_0) is important. The general frequencies of interest (if they are above 1KHz) are irrelevant. More simply, 100Hz of bandwidth near 10KHz contains as much noise as 100Hz of bandwidth near 1MHz. This implies that bandwidth should be restricted with appropriate high and low pass filtering, if the lowest noise voltages are to be attained.

From the previous discussion, it is apparent that low noise designs require low resistor values. This is not to say that high gain should be avoided, just that low input and source resistance values are required for low noise opera-

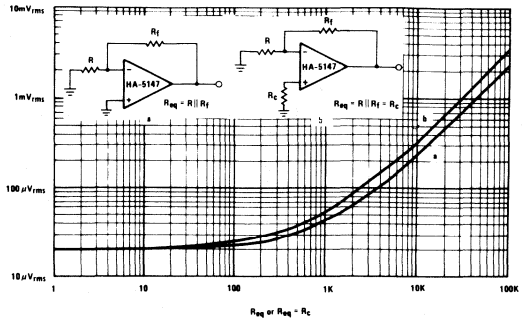


FIGURE 6a. PREDICTED NOISE

Predicted RMS noise at output for bandwidth of 10KHz - 500KHz for HA-5147.

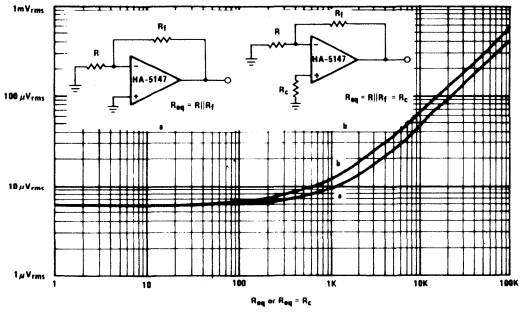


FIGURE 6b. PREDICTED NOISE

Predicted RMS noise at output for bandwidth of 20Hz - 20KHz for HA-5147.

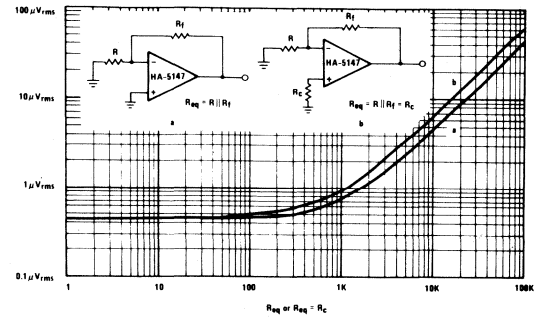


FIGURE 6c. PREDICTED NOISE

Predicted RMS noise at output for bandwidth of 10Hz - 100Hz for HA-5147.

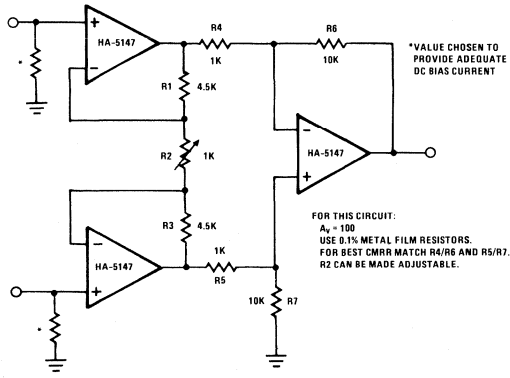


FIGURE 7. INSTRUMENTATION AMPLIFIER

Thanks to higher speed and more bandwidth, this standard three amplifier instrumentation amplifier will have 10MHz bandwidth and 550KHz power bandwidth.

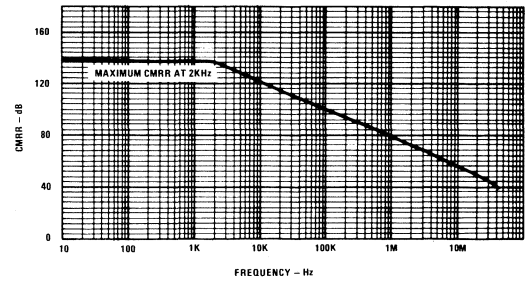


FIGURE 8. HA-5147 CMRR VS. FREQUENCY

The instrumentation amplifier's maximum CMRR can now be moved to much higher frequencies when using the HA-5147.

tion. Closer examination of the RMS noise formula will also show that limiting bandwith, with filtering, will also reduce noise levels. Additionally, metal film and wire-wound resistors have lower excess noise (a component of resistor noise in addition to thermal noise) than carbon resistors and are therefore preferred.

Applications

Heavily used throughout the world of signal processing is the instrumentation amplifier and it is this particular circuit that can best utilize all of the features of the HA-5147. By using the HA-5147, the standard 3 amplifier instrumentation circuit (Figure 7) is now able to extend its bandwidth to 10MHz or its power bandwidth to 500KHz. Additionally, the maximum CMRR (>120dB) is extended to higher frequencies (Figure 8). Other "error producing" input referred parameters of the HA-5147 such as noise, V_{OS}, I_{bias}, V_{OS} drift and temperature coefficients have been minimized, thus maximizing the capabilities of this application.

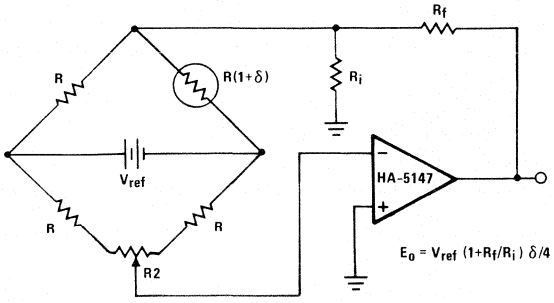


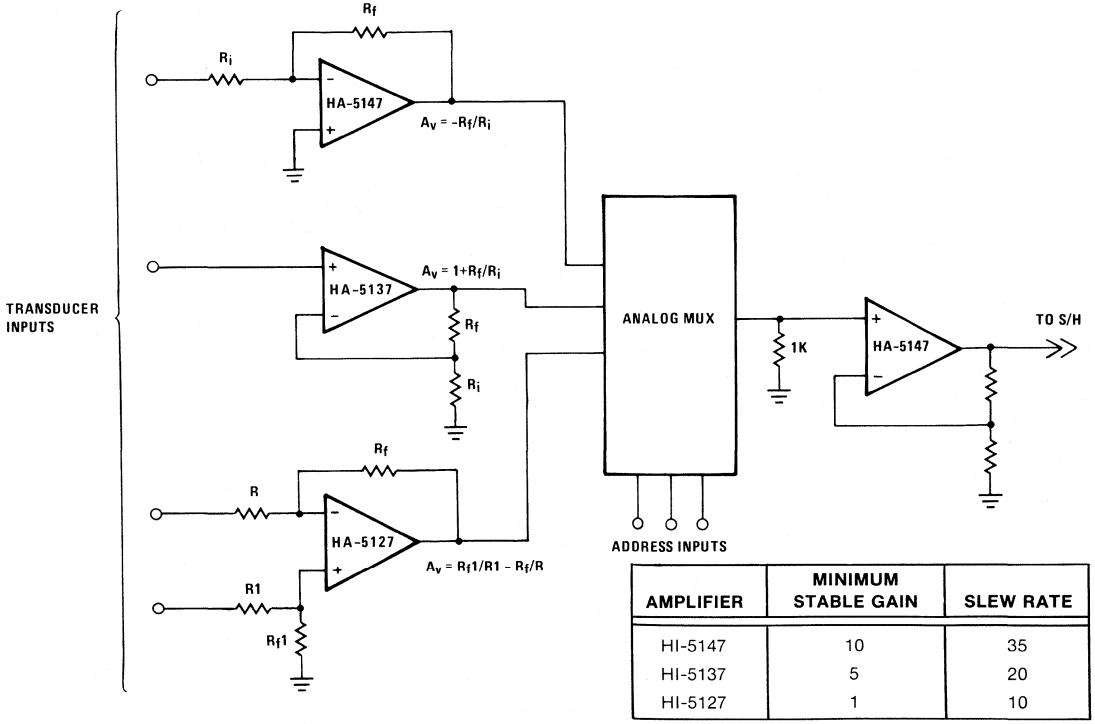
FIGURE 9. LOW LEVEL BRIDGE AMPLIFIER

Very small bridge signals are sensed and amplified accurately when using the precision performance of the HA-5147

Another circuit requiring very accurate amplification of its signal is the transducer bridge amplifier (Figure 9). The HA-5147, shown in an inverting bridge amplifier configuration, is recommended when it is necessary to detect very small bridge level signals. Its high open loop gain (>120dB), low noise, and excellent values for V_{OS}, V_{OS} drift, and bias current provide exceptional sensitivity to the smallest transducer variations. Full scale calibration of this circuit is made possible by placing a small valued potentiometer in series with R_i. Nulling is accomplished with R2.

The high slew rate (37V/μs) and the excellent output current drive ($\pm$20mA min.) make HA-5147 highly suitable as an input output buffer amplifier for analog multiplexers (Figure 10). The precision input characteristics of the HA-5147 help simplify system "error budgets" while its speed and drive capabilities provide fast charging of the multiplexer's output capacitance. This eliminates any increased multiplexer acquisition time, which can be induced by more limited amplifiers. The HA-5147 accurately transfers information to the next stage while effectively reducing any loading effects on the multiplexer's output.

Staying within the realm of signal processing, another standard and much used circuit configuration can be enhanced by the speed and precision of the HA-5147. A precision threshold detector (Figure 11) requires low noise, low and stable offset voltage, high open loop gain, and high speed. These requirements are met by the HA-5147, while adding excellent CMRR and PSRR to the list. The standard variations of this circuit can easily be implemented using the HA-5147. For example, hysteresis can be generated by adding R1 to provide a small amount of positive feedback. The circuit becomes a pulse width modulator if V_{ref} and the input signal are left to vary. Although the output drive capability of this device is excellent, the optional buffering circuit may be used to drive heavier loads while preventing loading effects on the amplifier.



AMPLIFIER	MINIMUM STABLE GAIN	SLEW RATE
HI-5147	10	35
HI-5137	5	20
HI-5127	1	10

FIGURE 10. HIGH SPEED INPUT/OUTPUT ANALOG MULTIPLEXER BUFFERING

Reduced "error" budgets and higher speeds of operation are easily achieved when the combined speed and precision of the HA-51X7 are used in these buffer amplifier applications.

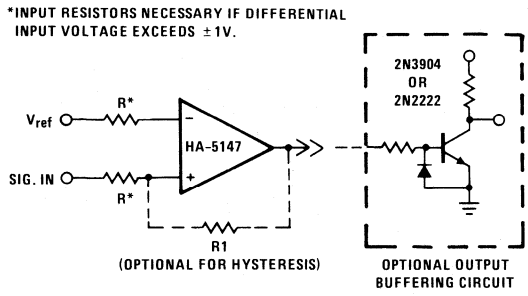


FIGURE 11. PRECISION THRESHOLD DETECTOR

This device can be used to increase response times while maintaining precise detection.

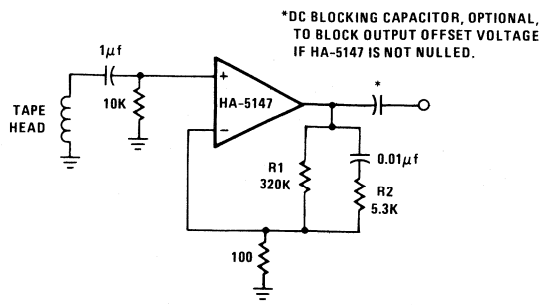


FIGURE 13. PROFESSIONAL AUDIO NAB TAPE PLAYBACK PREAMPLIFIERS

This NAB tape playback preamplifier fully utilizes the speed, bandwidth, and noise features of the HA-5147

Engineers working with professional audio designs will find the HA-5147 highly desirable for many of their applications. With its exceptional noise characteristics (Figure 5), wide power bandwidth (500KHz), and modest power consumption (85mW), this device can be used as a high quality audio preamplifier or as an intermediate stage gain block. A circuit similar to that in Figure 3b can be incorporated into studio or stage monitors.

The audio preamplifier of Figure 3b has a limited output current range. The audio power amplifier in Figure 12 overcomes this limitation and can provide an even greater boost to the HA-5147. Q1 and Q2 are a complementary pair arranged in a push pull manner, with R1 and R2 providing the necessary drive current. The maximum output voltage corresponds to the minimum output current since

$$(15\text{-}V_{be}\text{-}V_o)/R1$$

is the drive current to the transistors. D1 and D2 insure the proper biasing of the transistors as well as a clean crossover from Q1 to Q2.

An audio circuit which can make maximum use of the speed, bandwidth, and low noise of the HA-5147 is the NAB tape playback preamplifier (Figure 13). This circuit is configured to provide low frequency boost to 50Hz, flat response to 3KHz, and high frequency attenuation above 3KHz. Compensation for variations in tape and tape head performance can be achieved by trimming R1 and R2.

Signal generation applications will also find this high precision device useful. As an astable multivibrator (Figure 14) the power bandwidth of the HA-5147 extends the circuit's frequency range to approximately 500KHz. R_t can be made adjustable to vary the frequency if desired. Any timing errors due to V_{OS} or I_{bias} have been minimized by the precision characteristics of the HA-5147. D1 and D2, if used, should be matched to prevent additional timing errors. These clamping diodes may be omitted by tying R_t and the positive feedback resistor Rf directly to the output.

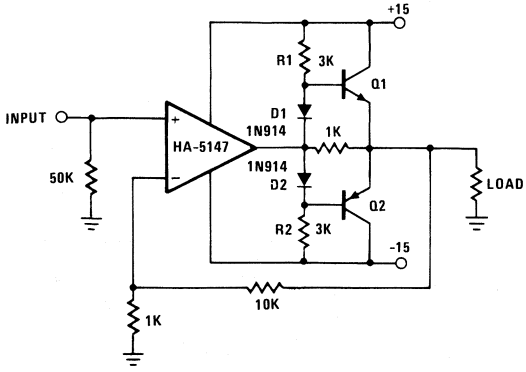


FIGURE 12. HIGH POWER AMPLIFIER

The additional drive capability of the power transistors allows the HA-5147 to drive very heavy loads.

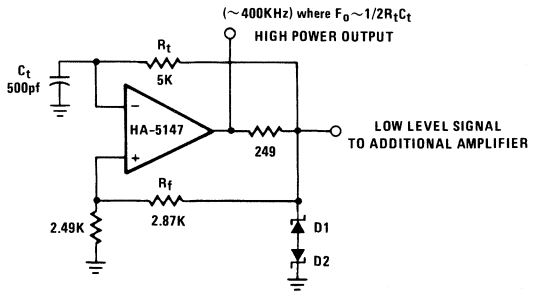


FIGURE 14. ASTABLE MULTIVIBRATOR

Higher frequencies of operation and reduced timing errors make the HA-5147 an attractive building block in signal generation applications.

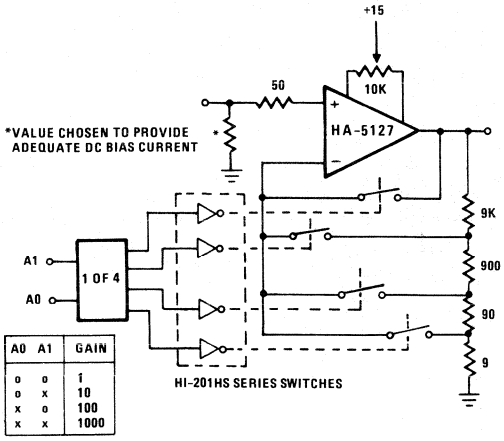


FIGURE 15. PROGRAMMABLE AMPLIFIER

Variable gain of 1, 10, 100, 1000 is achieved by selecting the proper amount of feedback with the use of analog switches.

Often a circuit will be called upon to perform several functions. In these situations the variable gain configuration of Figure 15 may be quite useful. This programmable gain stage depends on CMOS analog switches to alter the amount of feedback and thereby the gain of the stage. Placement of the switching elements inside the relatively low current area of the feedback loop, minimizes the effects of bias currents and switch resistance on the calculated gain of the stage. Voltage spikes may occur during the switching process, resulting in temporarily reduced gain because of the make-before-break operation of the switches. This can be minimized by providing a separate voltage divider network for each level of gain.

Many signal processing applications depend on low noise characteristics for their operation. One such application involves logrithmic amplifiers. The input sensitivity range is governed by the system noise in such a circuit. The HA-5147, with its low noise characteristics, can extend the basic sensitivity of the common logrithmic amplifier (Figure 16). The circuit uses a matched pair of transistors to offset the effects of temperature and quiescent currents. The final expression for V_{out} reduces to ....

$$V_{out} = -0.026(1 + R_5/R_6)\ln[20V_{in}/V_{ref}]$$

or using the schematic values ...

$$V_{out} = -\ln[2V_{in}]$$

R6 should be temperature dependent if the expression for V_{out} is to hold over an extended temperature range. The overall sensitivity is from a few millivolts to about twice V_{ref}.

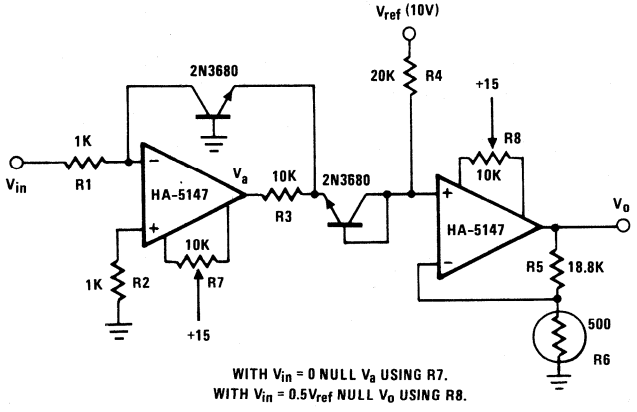


FIGURE 16. LOGRITHMIC AMPLIFIER

The matched pair of transistors makes this a very temperature stable logrithmic amplifier.

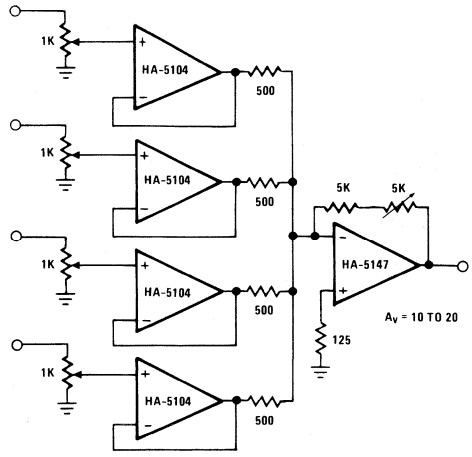


FIGURE 17. INPUT BUFFERED MIXER

Several signals can be combined using this circuit with a minimum of channel cross-talk.

A high signal to noise ratio is important in signal construction and combination. The HA-5147 aids in lowering overall system noise and thereby raises system sensitivity. The signal combination circuit in Figure 17 incorporates input buffering with several other features to form a relatively efficient mixer stage.

The potentiometer used for each channel allows for both variable input levels as well as a constant impedance for the driving source. The buffers serve mainly to prevent reverse cross-talk back through the resistor network. This allows for the combination of varying strength signals without reverse contamination. The gain of the final stage is set at a minimum of 10 and can be adjusted to as much as 20. This allows a great deal of flexibility in combining a vast array of input signals.

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Fitchen, F.C. and Motchenbacker, C.D. Low Noise Electronic Design, New York: John Wiley and Sons, 1973.

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LOW NOISE FAMILY HA-5101/02/04/11/12/14

by Alan Wayne Hansford

The HA-510X/511X series is comprised of six separate products designed to meet a wide range of needs. This is accomplished, in part, by offering the HA-5101, with 10V/μs, the HA-5102/04, each with 3V/μs slew rate, the HA-5111 with 50V/μs, and the HA-5112/14, each with 20V/μs slew rate.

HA-5101	Single Amplifier	10V/μs	Unity Gain Stable
HA-5102	Dual Amplifier	3V/μs	Unity Gain Stable
HA-5104	Quad Amplifier	3V/μs	Unity Gain Stable
HA-5111	Single Amplifier	50V/μs	Gains 10 or more
HA-5112	Dual Amplifier	20V/μs	Gains 10 or more
HA-5114	Quad Amplifier	20V/μs	Gains 10 or more

The entire series shares similar design. The noise voltage and noise current will therefore be the same across the series. With a very low noise input stage at just 4.0nV/$\sqrt{Hz}$ @ 1KHz, the HA-510X/511X is an excellent choice in applications where a high signal-to-noise ratio is critical, as in professional audio circuits and transducer monitors.

In addition to identical noise performance within the series, the HA-510X/511X all share common DC specifications with 0.5mV of offset voltage and 130nA of bias current. The high open loop gain, 250KV/V, together with the choice of compensation levels, will allow the HA-510X/511X series to meet a wide range of requirements.

Low Noise Design

Since the HA-510X/511X is a very low noise operational amplifier, low noise design techniques must be used to make the most of this feature. There are two primary means of keeping noise down, one requires the amplifier inputs to look into low source resistances and the other requires bandwidth limiting by filtering. A short outline of noise prediction will be presented here to support these concepts.

Noise can be divided into several categories, which include thermal noise (white noise) and flicker noise (pink noise or1/f noise). The feedback components are strongly dominated by thermal noise making thermal noise the most important of these from a system design standpoint (an exception to this are high gain DC amplifiers which require low 1/f noise as measured by the "lower 1/f noise corner"). Flicker noise is more a function of the amplifier construction quality, and system design variations are less effective in reducing this type of noise.

Noise is usually rated in one of two ways. The first is RMS voltage or current (a measure of peak-to-peak noise in a given bandwidth) and the second is by noise density spectrum in V/$\sqrt{Hz}$ and A/$\sqrt{Hz}$ (a measure of the spectral content of the noise in the frequency domain). The two rating schemes are related, with RMS noise levels generated from the integration of the noise density spectrum over a desired frequency bandwidth.

As an illustration of noise prediction, the noise density for the standard inverting amplifier configuration (Figure 1a) will be determined. The total noise is derived from the combination of several noise sources, only three of which are of any significance. These are the amplifier's noise voltage, the thermal noise of the feedback components, and the noise generated by the current noise of the amplifier within the feedback components.

The total noise is defined as the square root of the sum of the squares of the individual noise terms.

$$E_n = G\sqrt{(E_{amp})^2 + (E_{\substack{feedback\\network}})^2 + (E_{\substack{current\ noise\ in\\feedback\ network}})^2}$$

E_n = total noise

G = gain of stage

E_{amp} = amplifier noise voltage.....4.0nV/$\sqrt{Hz}$ @ f > 1KHz

$$E_{\substack{feedback\\network}} = \sqrt{4KTR_{eq}}$$ where... K = 1.381E-23, T = 300, $R_{eq} = R \,||\, R_f$

$$E_{\substack{current\ noise\ in\\feedback\ network}} = I_{noise}\, R_{eq}$$

I_{noise} = 0.56pA/$\sqrt{Hz}$ @ f > 1KHz

or more specifically . . .

$$E_n = G\sqrt{(E_{amp})^2 + R_{eq}4KT + (I_{noise}\, R_{eq})^2}$$

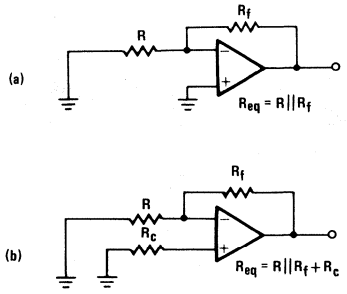


FIGURE 1.

A reasonable estimate of noise levels can be generated with these two basic amplifier circuits.

Both the amplifier noise voltage and noise current are constant above 1KHz and rise slightly for lower frequencies (Figure 2). The resistor thermal noise is derived from the parallel combination of the feedback network (R_{eq}) and several constants (4KT). The third noise term again uses the equivalent resistance of the feedback network (R_{eq}) as well as the current noise generated at the input terminals of the amplifier.

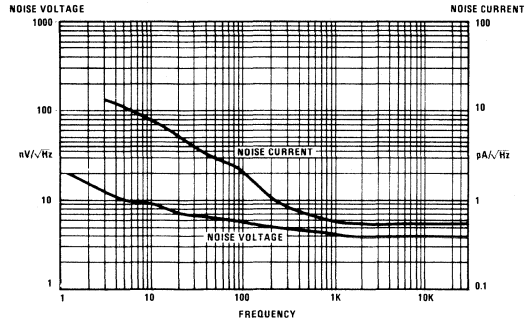


FIGURE 2.

Noise current and voltage for HA-510X/511X.

It should be evident from the above formula that extremely large values of R_{eq} (especially over 10Kohm) will dominate the noise density while low values for R_{eq} will yield to the amplifier's own noise characteristics. Note the asyptotic convergence of the noise voltages in Figures 3a-3c at low values of R_{eq}.

A second circuit (Figure 1b) balances the effects of input bias currents by placing a resistor R_C, equal to R_{eq}, between the non-inverting input and ground. While reducing DC errors, this configuration adds two additional terms to the noise formula.

$$E_n = G\sqrt{(E_{amp})^2 + R_{eq}4KT + (I_{noise}\,R_{eq})^2 + R_C\,4KT + (I_{noise}\,R_C)^2}$$

The original contributors to output noise remain as before and the additional terms represent the thermal contribution by R_C and the associated amplifier current noise seen through that resistor. To optimize DC design, $R_{in} \,||\, R_f = R_{eq} = R_C$, therefore the noise density equation reduces to ...

$$E_n = G\sqrt{(E_{amp})^2 + 2R_{eq}4KT + 2(I_{noise}\,R_{eq})^2}$$

Again the relationship between large values of R_{eq} and a high noise density spectrum remains.

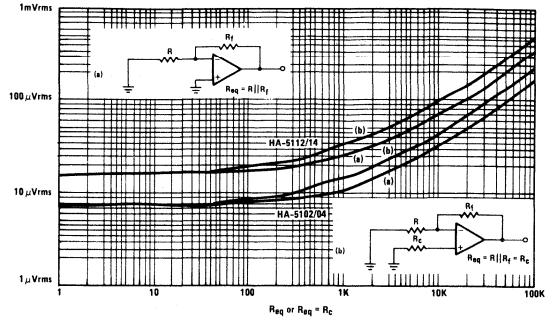


FIGURE 3a. PREDICTED NOISE

Predicted RMS noise at output for bandwidth of 0.1Hz-50KHz for HA-510X and 0.1Hz-250KHz for HA-511X.

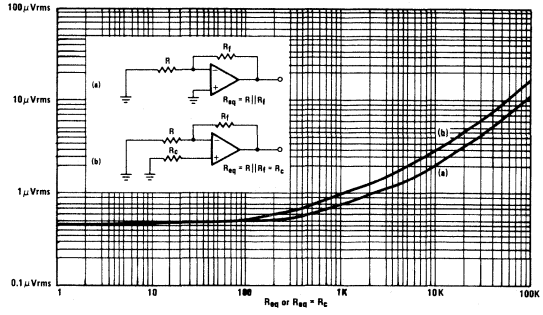


FIGURE 3b. PREDICTED NOISE

Predicted RMS noise at output for bandwidth of 20Hz-20KHz for HA-510X/511X.

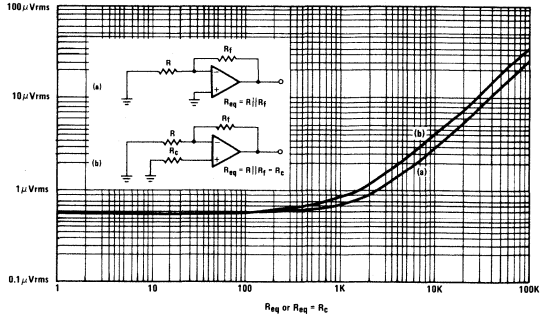


FIGURE 3c. PREDICTED NOISE

Predicted RMS noise at output for bandwidth of 20Hz-100Hz for HA-510X/511X.

RMS noise is derived in part as the integral of the noise density spectrum over a given bandwidth. Below is the complete expression...

$$E_{rms} \text{ (from } f_0 \text{ to } f_1) = \sqrt{\int_{f_0}^{f_1} E_{\substack{\text{noise} \\ \text{density} \\ \text{spectrum}}}^2 \, df}$$

The strict integration assuming E_n is constant works well for f_0 above ≈1KHz. Both the amplifier's noise voltage and the noise current increase for frequencies below 1KHz. This makes for difficult integration since complicated expressions for I_{noise} and E_{amp} must be generated. To avoid this problem, graphical integration techniques or sampled methods can be used with great success.

The curves in Figures 3a-3c illustrate the relationship between the RMS noise and R_{eq} for both amplifier designs. It should be apparent from the predicted RMS noise curves that increased bandwidth causes an increase in noise voltage. An interesting effect of this relationship is that only absolute bandwidth (f_1-f_0) is important. The general frequencies of interest (if they are above 1KHz) are irrelevant. More simply, 100Hz of bandwidth near 10KHz contains as much noise as 100Hz of bandwidth near 1MHz. This implies that bandwidth should be restricted with appropriate high and low pass filtering, if the lowest noise voltages are to be attained.

From the previous discussion, it is apparent that low noise designs require low resistor values. This is not to say that high gain should be avoided, just that low input and source resistance values are required for low noise operation. Closer examination of the RMS noise formula will also show that limiting bandwidth, with filtering, will also reduce noise levels. Additionally, metal film and wirewound resistors have lower excess noise (a component of resistor noise in addition to thermal noise) than carbon resistors and are therefore preferred.

Applications

Electronic scales have come into wide use and the HA-510X, as a very low noise device, can improve such designs. One circuit (Figure 4) uses a strain gauge sensing element as part of a resistive Wien-bridge. An auto-zero circuit is also incorporated into this design by including a sample-and-hold network.

The bridge signal drives the inverting input of a differentially-configured HA-5102. The non-inverting input is driven by the other half of the HA-5102 used as a buffer for the holding capacitor, C_h. This second amplifier and its capacitor C_h form the sampling circuit used for automatic output zeroing. The 20Kohm resistor between the holding capacitor C_h and the input terminal, reduces the drain from the bias currents. A second resistor R_9 is used in the feedback loop to balance the effect of R_8. If R_7 is approximately equal to the resistance of the strain gauge, the input signal from the bridge can be roughly nulled with R_6.

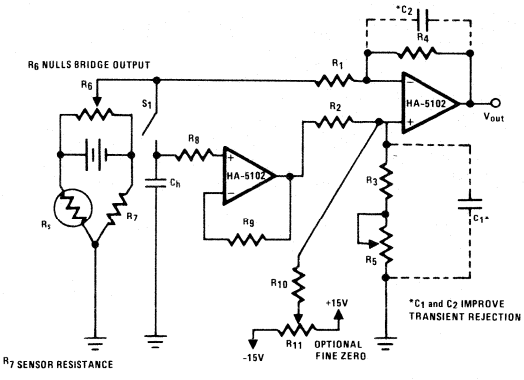


FIGURE 4.

Auto-zeroing scale circuit uses a strain gauge/bridge arrangement to improve sensitivity.

With very close matching of the ratio R_4/R_1 to R_3/R_2, the output offset can be nulled by closing S_1. This will charge C_h and provide a 0 volt difference to the inputs of the second amplifier, which results in a 0 volt output. In this manner, the output of the strain gauge can be indirectly zeroed. R_{10} and potentiometer R_{11} provide an additional mechanism for fine tuning V_{out}, but they may also increase offset voltage away from the zero point. C_1 and C_2 reduce the circuit's susceptibility to noise and transients.

The rise of digital equipment and computers, has created an entire realm of signal processing equipment. In most cases the computer requires elaborate circuitry to bridge over into the analog domain. The digitally programmable attenuator (Figure 5) is a rather simple circuit that still allows a great deal of control of analog signals.

The first stage is a simple buffer used to isolate the signal source from the attenuator stages to follow. Each of the subsequent stages is preceded by a voltage divider formed by two resistors and CMOS switch. Provided that the CMOS switch for each stage is "closed", the drive signal will be attenuated according to the basic voltage divider relationship at each stage. In the event a switch is "open" nearly all of the signal strength will be passed to the next stage through the 1K resistor. The amplifiers act as buffers for the divider networks and reduce interaction between stages. Eight levels of attenuation are possible with the circuit as illustrated in Figure 5, but more stages could be added. Each divider network must be closely matched to the resistor ratios shown or the level of attenuation will not match the levels in the logic chart.

Audio Applications

The HA-510X/511X series lends itself to audio designs. This is due in large part to the low noise characteristics of the series. With 4.0nV/$\sqrt{Hz}$ @ 1KHz, very low noise designs can be realized with little effort. This allows more attention to be placed on the quality of the designs.

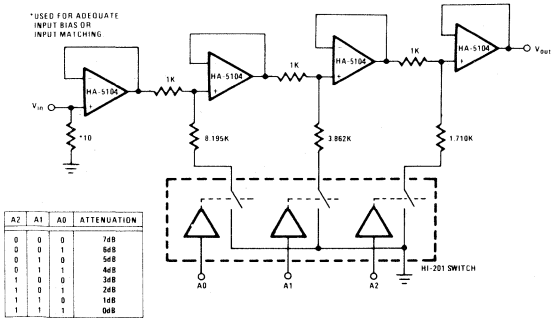


FIGURE 5.

Several resistors may be combined to obtain the precise resistor values used in this precision attenuator or a potentiometer may prove adequate.

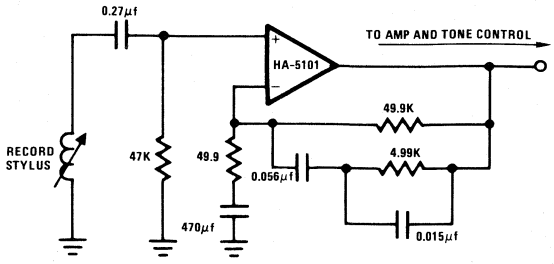


FIGURE 7.

The RIAA amplifier provides industry standard signal correction for vinyl record recordings.

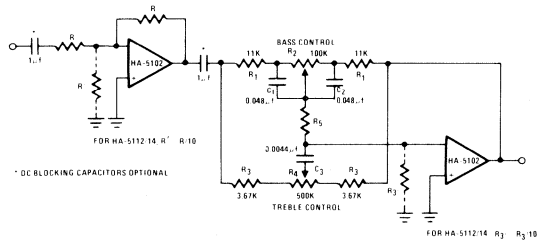


FIGURE 6.

The tone correction circuit requires a low impedance driving source, yet it provides a great deal of control over the output waveform.

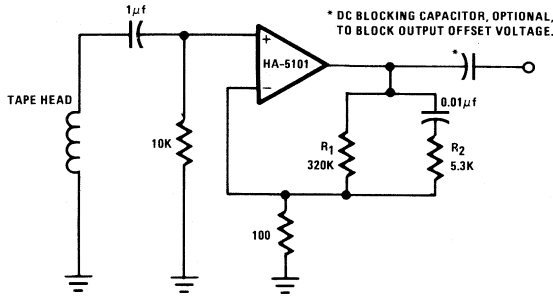


FIGURE 8. PROFESSIONAL AUDIO NAB TAPE PLAYBACK PREAMPLIFIER

This NAB tape playback preamplifier fully utilizes the speed, bandwidth, and noise features of the HA-5101.

The following group of designs point to some of the applications in which the HA-510X/511X series can improve performance without major circuit alterations. They depend, in part, on the $> \pm 20V/\mu s$ slew rate of the HA-511X, which will allow a small signal to be passed without distortion up to 12MHz. The bandwidth of these devices is more than adequate for audio use. The HA-510X will pass a full 10V signal out to 200KHz without distortion and at unity gain. Many other uses for these devices exist. The audio applications simply suggest the more likely uses for the series.

Tone correction of an audio signal is an application that relies on both the low distortion and the low noise of the HA-5102. The Baxandal-type circuit in Figure 6 uses input buffering because of the relatively low input impedance of the RC networks. The output stage is basically a summation amplifier with the high frequency contribution varied by the treble control and the low frequency by the bass control. The component values given in Figure 6 allow ±12dB of gain over the audio range.

One of the more common audio applications is signal correction for recording and playback. Several standard circuits are available and the HA-5101 should prove an excellent centerpiece for these. One such circuit is the RIAA preamplifier used to match the frequency characteristics of vinyl records and phonograph cartridges.

The RIAA circuit essentially provides low frequency boost below 318Hz and high frequency attenuation above 3150Hz. Recent modifications to the response standard include a 31.5Hz peak gain region to reduce DC oriented distortion from external vibration. The circuit in Figure 7 provides the desired response.

The NAB (magnetic tape standard) amplifier circuits are also well suited for use with the HA-5101 (Figure 8). The NAB preamplifier is configured to provide low frequency boost to 50Hz, flat response to 3KHz, and high frequency attenuation above 3KHz. Compensation for variations in tape and tape head performance can be achieved by trimming R_1 and R_2.

The low noise characteristics of the HA-510X family lead to low system noise and improved signal to noise ratios. This has become increasingly more important as the

various recording mediums have progressed to the point of near perfection, at least so far as the ear is concerned.

At the other end of the audio spectrum, opposite the playback arena, is initial sound generation and the microphone. The HA-5104/14 is a very practical choice for a dynamic microphone preamplifier (Figure 9). The relatively simple design allows for DC coupling of both input and output.

The microphone sees an input impedance equal to $R_1 + R_2$ (2Kohm). The input impedance of the amplifier group is not matched to the 600ohm impedance of the microphone. This is because the instrumentation amplifier does not rely on input power, but rather input voltage alone for its driving source. In many cases the frequency range of the microphone will be extended with the reduced loading.

R_5, R_6, and R_7 provide stable DC gain in conjunction with R_3 and R_4, which form the DC feedback network around the first two amplifiers. R_7 also controls the DC offset at the output. R_8, R_9, and C_3 provide the proper AC gain above 0.6Hz. R_{14} is tuned for maximum CMRR by matching the feedback element ratios of the third amplifier [$R_{11}/R_{10} = (R_{13} + R_{14})/ R_{12}$]. With a total gain of 4dB, the 2mV microphone signal is increased to the standard $1V_{rms}$ output.

The optional output stage provides a 600ohm matched output impedance to maximize the power transfer to the next stage. The HA-5104 and the HA-5114 will both function well in this circuit. There will, however, be an extra unused amplifier. To avoid this unused amplifier the tone correction circuit in Figure 6 is recommended for use with the fourth amplifier. If the HA-5114 is used, the DC gain resistors R' and R3' in Figure 6 must be used with the tone correction circuit to insured proper DC stability.

One of the most useful circuits in audio filtering is the Biquad. This universal filter offers low pass, high pass, band pass, band elimination, and all pass functions. The HA-5104 is an excellent choice for the four amplifier Biquad circuit in Figure 10. This is due in large part to the low noise and high slew rate characteristics of the HA-5104, both of which reduce distortion effects.

The Biquad consists of two successive integration stages followed by an inverting stage. The entire group has a feedback loop from the front to the back consisting of R_1 which is chiefly responsible for controlling the center frequency, ω_o. The first stage of integration is termed a "poor" integrator because of R_2 which limits the range of integration. R_2 and C form the time constant of the first stage integrator with R_3 influencing the gain (H) almost directly. The band pass function is taken after the first stage with the low pass function taken after the third stage. The remaining filter operations are generated by various combination of the three stages.

The Biquad is "orthogonally" tuned, meaning that ω_o, Q, and gain (H) can all be independently adjusted. The component values in Figure 10 will allow ω_o to range from 40Hz to 20KHz. The other component values give an adequate range of operation to allow for virtually universal filtering in the audio region. ω_o, Q, and gain (H) can all be independently adjusted by adjusting R_1 - R_3 respectively and in succession.

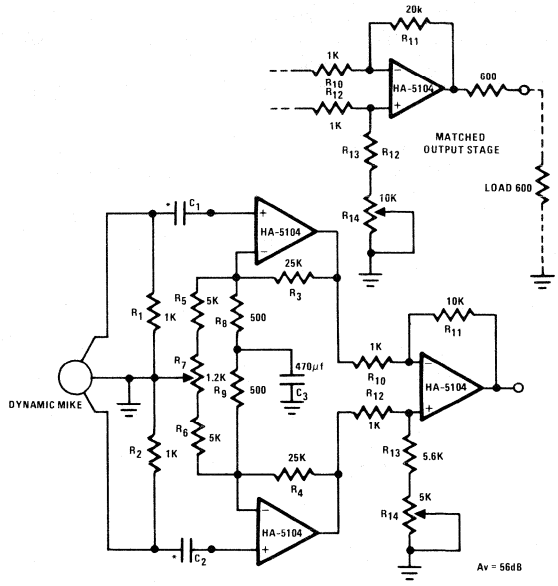
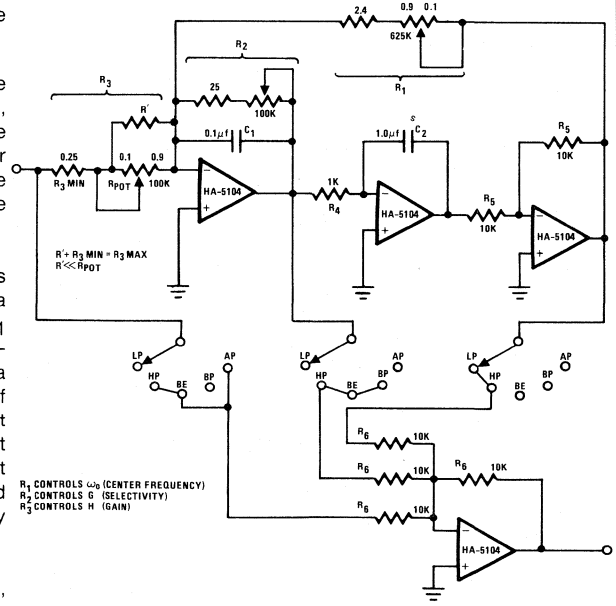


FIGURE 9.

The dynamic microphone preamplifier does not use a transformer which reduces both complexity and cost.



The biquad offers a universal filter with ω_o, Q, and gain "orthogonally" tuned.

The standard Biquad circuit in Figure 10 uses three stages of inverting amplifiers. This produces negative feedback for stability (any odd number of stages would produce the same effect). There, however, is no restriction such that only inverting stages must be used. The standard Biquad of Figure 10 has been altered in Figure 11 by combining the function of the last two stages into one non-inverting integrator. This reduces the number of amplifiers required for the band pass function to just two. The bandpass transfer function is of course altered to reflect the consolidation of the last two stages and is as follows...

$$\frac{V3}{V1} = \frac{-R_1R_2R_3Cs}{(R_1R_2R_3R_4CC)s^2 + (R_1R_2R_3R_4C)s + 2R_2R_3}$$

$$= \frac{-(1/R_3C)s}{s^2 + (1/R_2C)s + 2/R_1R_4CC}$$

$$= \frac{+H\omega_o^2}{s^2 + (\omega_o/Q)s + \omega_o^2}$$

therefore....

$$\omega_o = \sqrt{2/R_1R_4CC}$$

$$Q = \sqrt{2R_2^2/R_1R_4}$$

$$H = -R_1R_4C/2R_3 \qquad \text{if } C_1 = C_2 = C$$

The two amplifier Biquad bandpass filter constructed around the HA-5102 can easily be incorporated into a ten band graphic equalizer. By restricting gain to ±12dB and requiring Q ≈ 1.7, a very usable design can be generated. See Figure 12.

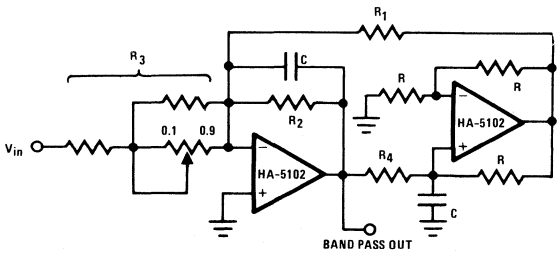


FIGURE 11.

The two amplifier biquad forms an economical band pass filter, which in this case is oriented towards a ten band equalizer.

A high signal to noise ratio is important in signal construction applications. The low noise aspect of the HA-5104 aids in lowering the system noise and thereby raises the system sensitivity. The signal combination circuit in Figure 13 incorporates input buffering with several other features to form a relatively efficient mixer stage.

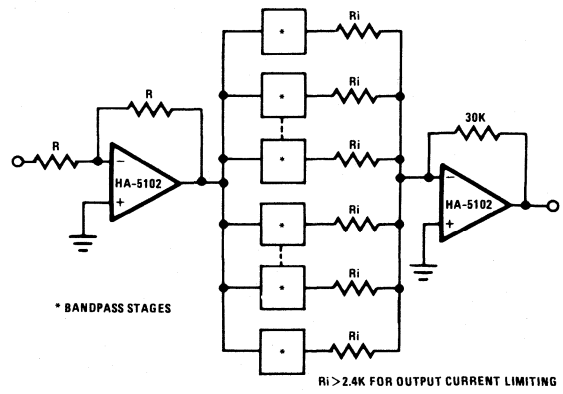


FIGURE 12.

The bandpass stages can be incorporated into a multiple band equalizer.

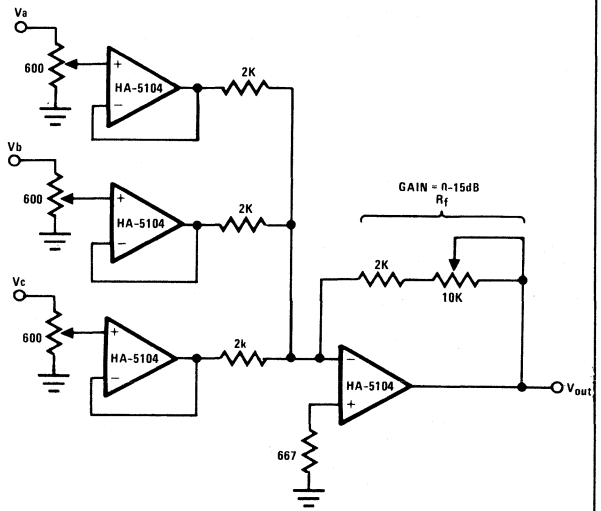


FIGURE 13.

The 600 ohm input impedance provides for proper audio level signal mixing using the HA-5104.

The circuit in Figure 13 uses buffer stages to prevent channel crosstalk back through the mixer resistor network. The potentiometers used for each stage allow for convenient signal strength adjustment while main taining input impedance matching at the 600ohm audio standard. The feedback resistor R_f will permit the output signal gain to be as high as 15dB. The circuit in Figure 14 illustrates some of the other possible buffer combinations. These include a differential input stage, a voltage follower as well as both non-inverting and inverting stages. The allowable resistor ratios and recommended device types are also included. One restriction applies to this type of mixer network which is R_9 >2.4Kohm. This limits the worst case output current for each of the input buffers to less than 10mA.

The bulk of the HA-5102/04/12/14 series applications have involved audio uses. This does not represent the full range of application of the series. In general, most

common amplifier applications, excluding video, could benefit from the group. The goal here was to introduce the designer to some of the more common and well know designs using the series, in hope of triggering interest for more extensive uses.

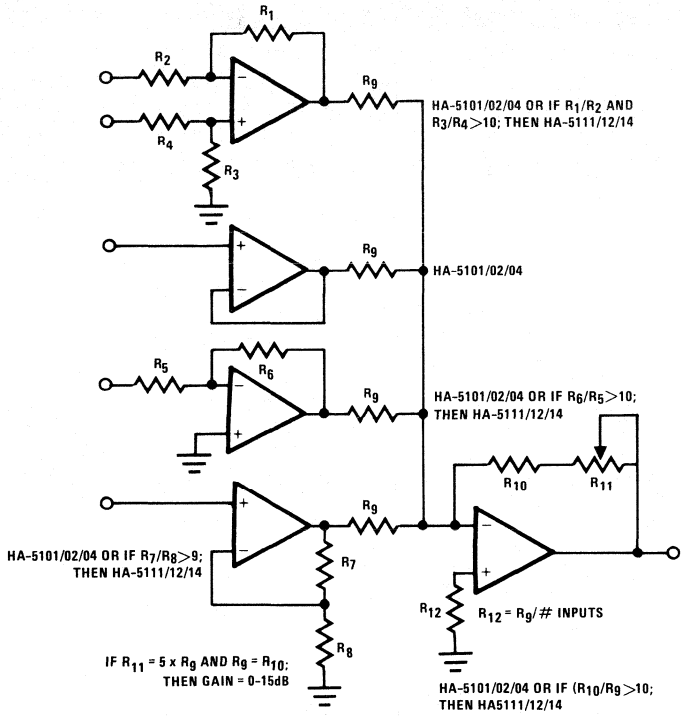


FIGURE 14.

Universal mixer stage combines the more useable configurations of the HA-510X/511X family to meet most signal construction needs.

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ULTRA LOW BIAS AMPLIFIER, HA-5180

by Alan Wayne Hansford

Most amplifiers depend on the voltage at the inputs to determine the output voltage, and require a parasitic input bias current for proper operation. Typically these currents are in the μA range, but they needn't be so large. A very few devices fall into the ultra low bias current group which ranges from fA levels to a few pA. The HA-5180 is one of the few, with only 250fA of Bias current.

DC offset errors are created at the output of most amplifiers from the interaction of input bias currents with circuit resistances. If bias currents are significantly reduced, as with the HA-5180, the DC errors are also significantly reduced. This implies that with very low bias currents, larger resistances can be used without creating a DC error that exceeds normal bias current/resistance combinations. A great many high source impedance applications are only practical with some means of bias reduction, typically FET buffering. The ultra-low bias amplifiers, like the HA-5180, eliminate the need for FET buffering with its FET input stage. This makes the HA-5180 particularly well suited for atomic particle detectors and precision sampling circuits, to name two.

The outstanding features of the HA-5180 do not end simply at input bias current, but combine to form a very usable device. The Common Mode Rejection Ratio (CMRR) and Power Supply Rejection Ratio (PSRR) are both examples of this. The rejection of a common signal appearing at both input terminals of the device is 105dB (CMRR) and the rejection of power supply fluctuations is 110dB (PSRR). The open loop gain is a very respectable 1000KV/V. All of these outstanding features reflect the quality built into the HA-5180.

Given the type of device and the primary emphasis on low input bias currents, the HA-5180 has several other points worthy of praise. The basic speed of the device with a 2MHz bandwidth and a 7V/μSec slew rate, is above average and noteworthy for any amplifier. This becomes even more apparent in light of the low supply current (0.8mA). The relationship between supply current and speed usually implies that a high speed device requires a high supply current. Yet, the design of the HA-5180 has judiciously metered its use of available supply current to optimize speed at gains as low as unity.

Building Tips

The HA-5180 was designed with high performance in mind as indicated by its parameter list. The design enhancements did not stop at the drawing board however, and have been brought into the user's control. The most interesting development is the case connection to pin 8 of the can. By grounding the can through pin 8, a high level of shielding may be easily implemented. The effects of shielding should be further increased by using a grounding plane under the HA-5180. Both of these techniques will also improve the heat transfer away from the chip and package to extend the operational safety margins.

The remarkably low input bias currents are extremely important to many applications. They, in spite of their merit, can not stand alone in every circuit design. For this reason the voltage offset pins were included in the design of the HA-5180. With pins 1 and 5 (Figure 1), the offset voltage can be reduced below the very acceptable value of 100μV, establishing an amplifier with nearly ideal characteristics.

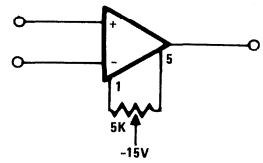


FIGURE 1.
Nulling the HA-5180s offset adjust to 0 volts brings it closer to the "ideal"

Low Noise Design

Since the HA-5180 is a moderately low noise operational amplifier, low noise design techniques must be used to make the most of this feature. There are two primary means of keeping noise down, one requires the amplifier inputs to look into low source resistances and the other requires bandwidth limiting by filtering. A short outline of noise prediction will be presented here to support these concepts.

Noise can be divided into several categories, which include thermal noise (white noise) and flicker noise (pink noise or 1/f noise). The feedback components are strongly dominated by thermal noise making thermal noise the most important of these from a system design standpoint (an exception to this are high gain DC amplifiers which require low 1/f noise as measured by the lower "1/f noise corner"). Flicker noise is more a function of the amplifier construction quality, and system design variations are less effective in reducing this type of noise.

Noise is usually rated in one of two ways. The first is RMS voltage or current (a measure of peak-to-peak noise in a given bandwidth) and the second is by noise density spectrum in $V/\sqrt{Hz}$ and $A/\sqrt{Hz}$ (a measure of the spectral content of the noise in the frequency domain). The two rating schemes are related, with RMS noise levels generated from the integration of the noise density spectrum over a desired frequency bandwidth.

As an illustration of noise prediction, the noise density for the standard inverting amplifier configuration (Figure 2a) will be determined. The total noise is derived from the combination of several noise sources, only three of which are of any significance. These are the amplifier's noise voltage, the thermal noise of the feedback components, and the noise generated by the current noise of the amplifier within the feedback components.

The total noise is defined as the square root of the sum of the squares of the individual noise terms.

$$E_n = G\sqrt{(E_{amp})^2 + (E_{\substack{feedback\\network}})^2 + (E_{\substack{current\ noise\ in\\feedback\ network}})^2}$$

E_n = total noise

G = gain of stage

E_{amp} = amplifier noise voltage.....$70nV/\sqrt{Hz}$ @ f > 1KHz

$$E_{\substack{feedback\\network}} = \sqrt{4KTR_{eq}} \quad \text{where...} \quad \begin{array}{l} K = 1.381E\text{-}23 \\ T = 300 \\ R_{eq} = R \,||\, R_f \end{array}$$

$$E_{\substack{current\ noise\ in\\feedback\ network}} = I_{noise}\, R_{eq}$$

$I_{noise} = 0.01pA/\sqrt{Hz}$ @ f > 1KHz

or more specifically . . .

$$E_n = G\sqrt{(E_{amp})^2 + R_{eq}4KT + (I_{noise}\, R_{eq})^2}$$

Both the amplifier noise voltage and noise current are constant above 1KHz and rise slightly for lower frequencies (Figure 3). The resistor thermal noise is derived from the parallel combination of the feedback network (R_{eq}) and several constants (4KT). The third noise term again uses the equivalent resistance of the feedback network (R_{eq}) as well as the current noise generated at the input terminals of the amplifier.

It should be evident from the above formula that extremely large values of R_{eq} (usually over 10Kohm, but

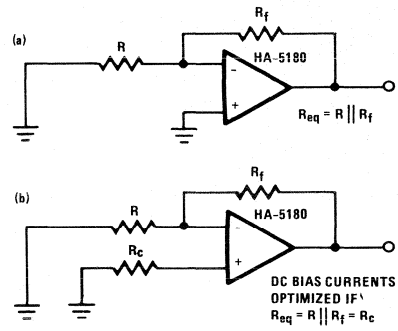


FIGURE 2. NOISE PREDICTION CIRCUITS

A reasonable estimate of noise levels can be generated with these two basic amplifier circuits.

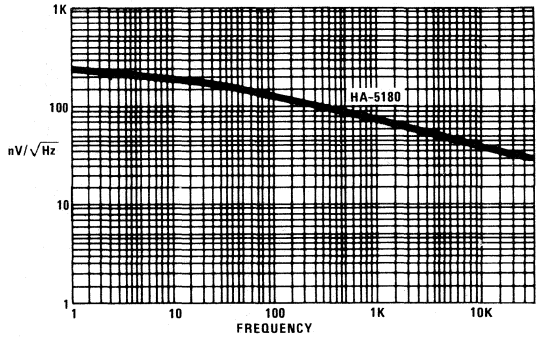


FIGURE 3. NOISE VOLTAGE

Due to the extremely low noise currents, only the voltage noise generates a significant contribution.

1Megohm for the HA-5180) will dominate the noise density while low values for R_{eq} will yield to the amplifier's own noise characteristics. Note the asyptotic convergence of the noise voltages in Figures 4a-4c at low values of R_{eq}.

A second circuit (Figure 2b) balances the effects of input bias currents by placing a resistor R_C, equal to R_{eq}, between the non-inverting input and ground. While reducing DC errors, this configuration adds two additional terms to the noise formula.

$$E_n = G\sqrt{(E_{amp})^2 + R_{eq}4KT + (I_{noise}\, R_{eq})^2 + R_C\, 4KT + (I_{noise}\, R_C)^2}$$

The original contributors to output noise remain as before and the additional terms represent the thermal contribution by R_C and the associated amplifier current noise seen through that resistor. To optimize DC design, $R_{in} \,||\, R_f = R_{eq} = R_C$, therefore the noise density equation reduces to ...

$$E_n = G\sqrt{(E_{amp})^2 + 2R_{eq}4KT + 2(I_{noise}\, R_{eq})^2}$$

Again the relationship between large values of R_{eq} and a high noise density spectrum remains.

RMS noise is derived in part as the integral of the noise density spectrum over a given bandwidth. Below is the complete expression...

$$E_{rms} \text{ (from } f_0 \text{ to } f_1) = \sqrt{\int_{f_0}^{f_1} E_{\substack{\text{noise} \\ \text{density} \\ \text{spectrum}}}^2 \, df}$$

The strict integration assuming E_n is constant works well for f_0 above ≈1KHz. Both the amplifier's noise voltage and the noise current increase for frequencies below 1KHz. This makes for difficult integration since complicated expressions for I_{noise} and E_{amp} must be generated. To avoid this problem, graphical integration techniques or sampled methods can be used with great success.

The curves in Figures 4a-4c illustrate the relationship between the RMS noise and R_{eq} for both amplifier designs. It should be apparent from the predicted RMS noise curves that increased bandwidth causes an increase in noise voltage. An interesting effect of this relationship is that only absolute bandwidth (f_1-f_0) is important. The general frequencies of interest (if they are above 1KHz) are irrelevant. More simply, 100Hz of bandwidth near 10KHz contains as much noise as 100Hz of bandwidth near 1MHz. This implies that bandwidth should be restricted with appropriate high and low pass filtering, if the lowest noise voltages are to be attained.

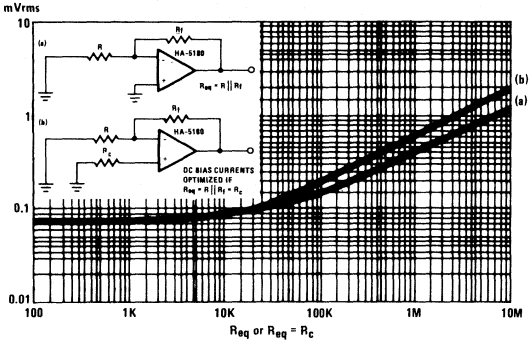


FIGURE 4a. PREDICTED NOISE

Predicted RMS noise at output of HA-5180 for a bandwidth of 0.1Hz-110KHz.

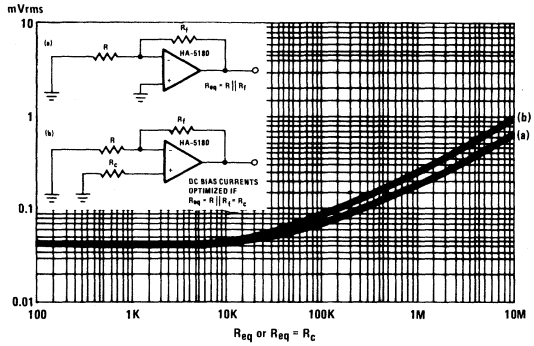


FIGURE 4b. PREDICTED NOISE

Predicted RMS noise at output of HA-5180 for a bandwidth of 20Hz-20KHz.

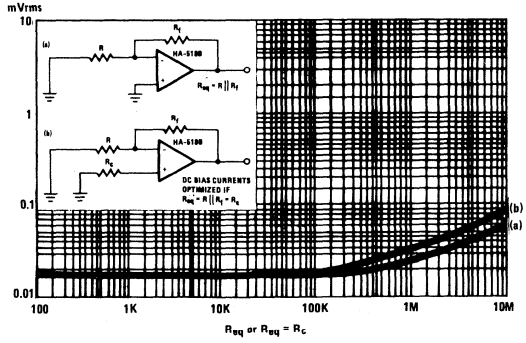
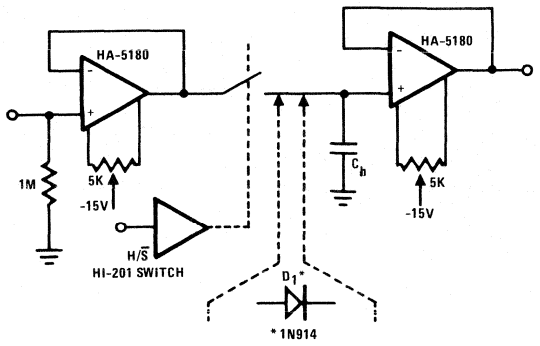


FIGURE 4c. PREDICTED NOISE

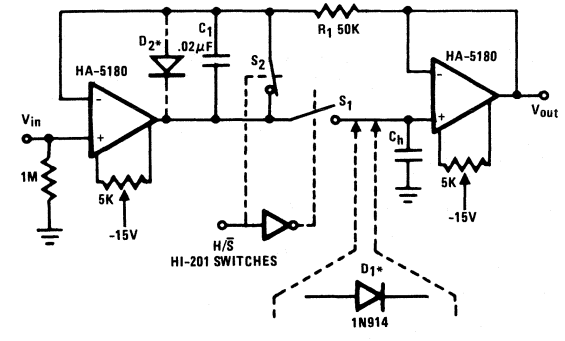
Predicted RMS noise at output of HA-5180 for a bandwidth of 20Hz-100Hz.



*Diode used for S/H peak detector

FIGURE 5a.

"Fast" sample-and-hold must be nulled using the offset potentiometers but offers very short aquisition times.



*Diodes used for S/H peak detector

FIGURE 5b.

"Precision" sample-and-hold is an excellent use of the HA-5180, but, because of the extended feedback, has greater overshoot.

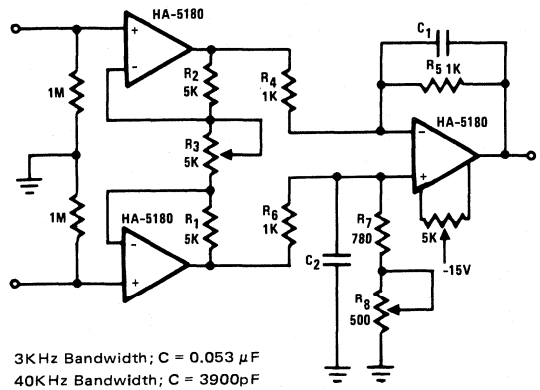


FIGURE 6.

The standard three amplifier instrumentation configuration gives a multimeter preamplifier extremely high input impedance.

From the previous discussion, it is apparent that low noise designs require low resistor values. This is not to say that high gain should be avoided, just that low input and source resistance values are required for low noise operation. Closer examination of the RMS noise formula will also show that limiting bandwith, with filtering, will also reduce noise levels. Additionally, metal film and wirewound resistors have lower excess noise (a component of resistor noise in addition to thermal noise) than carbon resistors and are therefore preferred.

Applications

One of the most critical applications, relative to input bias currents, is the sample-and-hold. The HA-5180 requires such a low input bias current (250fA) that the drain on holding capacitors is all but eliminated. Figure 5 illustrates both a "precision" sample-and-hold as well as a "fast" sample-and-hold. Both circuits buffer the input voltage and the sampled voltage on C_h.

The "precision" circuit achieves a lower error voltage by closing the feedback loop around both amplifiers. This adds a delay to the feedback signal and increases the overshoot. The DC error voltages are reduced in this configuration and can be reduced further with the V_{OS} offset nulling potentiometers, hence the term "precision". C_1 improves transient response while R_1 provides isolation of the input and the output during the hold cycle. S_1 determines whether the holding capacitor C_h follows the input voltage or holds a previous value. The necessary feedback to the input buffer is provided by S_2 during the hold operation. D_1 converts the sample-and-hold into a peak voltage sample-and-hold. D_2 reduces the reverse saturation of the input buffer when used in the peak mode.

The "fast" sample-and-hold incorporates feedback around each amplifier separately. This makes for a much faster response, but does tend to increase DC error voltages. The effects of DC offset can be minimized with the V_{OS} offset nulling potentiometers. As with the precision sample-and-hold, S_1 controls the charging and holding operation of the holding capacitor C_h. D_1, as before, converts the circuit into a peak voltage sample-and-hold.

Like the sample-and-hold, the differential instrumentation amplifier relies on extremely high input impedance for effective operation. The HA-5180 with its JFET input stage, performs well as a multimeter preamplifier (Figure 6). The standard three amplifier configuration is used with very close matching of the resistor ratios R_5/R_4 and $(R_7 + R_8)/R6$, to insure high common mode rejection (CMRR). The gain is controlled through R_3 and is equal to $2R_1/R_3$. Additional gain can be had by increasing the ratios R_5/R_4 and $(R_7 + R_8)/R_6$.

The capacitors C_1 and C_2 improve the AC response by limiting the effects of transients and noise. Two suggested values are given for maximum transient suppression at frequencies of interest. Some of the faster

DVM's are operating at a peak sampling frequency of 3KHz, hence the 4KHz low pass time constant. The 40KHz low pass time constant for AC voltage ranges is an arbitrary choice, but should be chosen to match the bandwidth of the other components in the system. C_1 and C_2 may however, reduce CMRR for AC signals if not closely matched. Input impedances have also been added to provide adequate DC bias currents for the HA-5180 when open circuited.

Sensors And Transducers

Most passive transducers and sensors vary in resistance relative to light, sound, pressure, etc. Often the average resistance of the transducer is quite large. This presents a problem in the choice of an amplifier, since bias currents are typically high enough to create a significant error voltage ($V_{error} = I_{bias}$ R). Extremely low input bias currents of the HA-5180 minimize this effect for the most part and allow for more conventional transducer and sensor circuits.

The circuit in Figure 7 uses a light sensitive cadmium sulfide cell to form a crude light level detecton module. If R, the sensor matching resistor, is equal to the "dark" resistance of the cadimum sulfide cell, the amplifier output will range from 0 volts to ≈12 volts as the light level ranges from "dark" to "bright". The circuit in Figure 8 operates in a similar manner but use the standard non-inverting configuration instead of the voltage follower configuration. This allows for variable gain. Although the "dark" resistance of the cadmium sulfide cell is only ≈7Kohms, the principles of operation apply to other types of detectors which require the high input impedance of the HA-5180 for reasonable linearity and useability.

An example of a high resistive value sensor that depends heavily on high amplifier input impedance is the pH probe and Detector, with the average probe resistance on the order of 100Megohms. The circuits in Figures 7 and 8 may still be used with this type of transducer, but a bridge circuit may prove more appropriate (Figure 9). The greatest sensitivity is achieved if R_1 is approximately equal to the probe resistance. The circuit can be "zeroed" with R_2 while the full scale voltage is controlled by R_5. The correlation between pH and output voltage may not be linear, which would necessitate a shaping circuit. A calibration scheme, using solutions of known pH, may prove adequate and more reliabile over a period of time due to probe variance.

The general schematic could be applied to strain gauges or any other type of resistive sensor. The key is the extremely low input bias current required by the HA-5180, which allows higher value resistances to be used without producing significant error voltages. This leads to more conventional designs with less exotic circuitry.

Along the same lines as the pH meter and light level detector, is the photo-diode current to voltage converter (Figure 10). One common use of this type of device is as a light to voltage converter for densitometers. This circuit depends on the light level/current relationship of a photo-

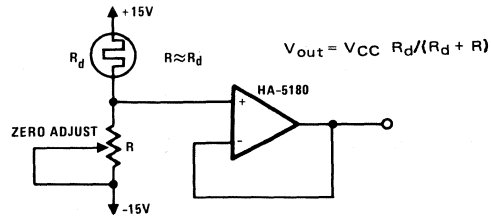


FIGURE 7.
Cadmium Sulfide cells control two light detection circuits.

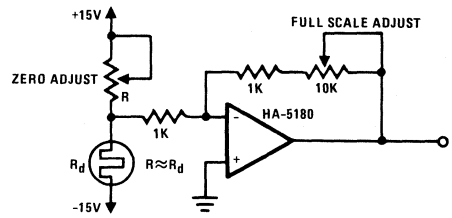


FIGURE 8.
Cadmium Sulfide cells control two light detection circuits.

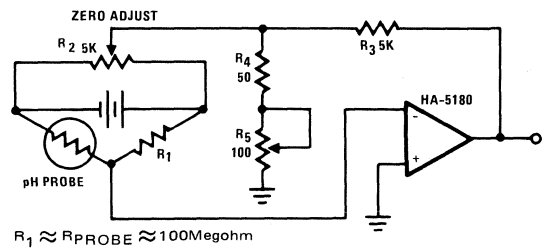


FIGURE 9.
Another popular sensor circuit is the bridge network. The pH probe can be replaced with nearly any resistive sensor.

diode. Since the diode will only pass as much current as the light level will allow, the diode becomes a light controlled current sink. A current source is summed along with the photo-diode current, and a difference current appears at the input of the HA-5180. Relying on ideal amplifier input impedance, which is nearly the case with the HA-5180, all of the difference current is applied to R_f. The output is then defined as . . .

$$V_{out} = (I_{ref} - I_d)R_f$$

Several current sources may be used. The simplest is a resistor with $I = (V_{CC} - V_{be})R$. A more accurate current source is the two transistor current mirror, where $I = (V_{CC} - V_{be})/R_{ref}$ (Figure 10). Since the controlling component, R_{ref}, is not in the current path for I, a more accurate summation at the amplifier input terminal can take place. The stage can be zeroed with R or R_{ref} as the case may be. The nulling potentiometer will provide the fine zero.

The precision integrator is a classic circuit which can also benefit from the JFET inputs of the HA-5180. The traditional relationship between C and R holds very well in one

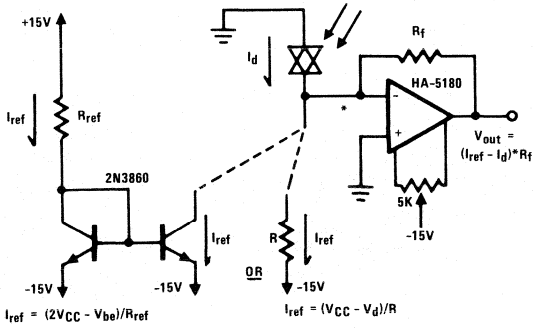


FIGURE 10.

The low bias currents of the HA-5180 provide a nearly ideal summing point (*) for the circuit currents in this photo-diode current to voltage converter.

design (Figure 11), since the drain on C by the amplifier is so small. A second HA-5180 has been incorporated into this design to allow a threshold voltage to be adjusted. The threshold voltage is set while present at the input with S_1 and S_2 closed. S_1 is opened before S_2, then S_3 is closed momentarily to reset the output voltage. The stage will then take the time integral of the input signal relative to the threshold voltage. R_2 provides stable gain during the threshold setting procedure. The nulling potentiometer reduces the effects of V_{OS}.

The precision integrator can be converted into a precision timer with a few modifications. The reset switch used to discharge the capacitor C is used as the timer on reset switch. The output will be proportional to the elapse time as long as the input voltage is constant and not equal to the threshold voltage. If the timer needs a hold function, a switch must be inserted to isolate the capacitor C from the resistor R.

Many signal processing applications depend on low amplifier bias currents for their operation. One such design involves logarithmic amplifiers (Figure 12). The input sensitivity is governed by the system bias currents in such a circuit. The HA-5180, with its low input bias currents, can extend the sensitivity of the logarithmic current to voltage converter. The specific application may well be an atomic particle counter in which the current from the detector is converted into a voltage. For the design in Figure 12 the output voltage is defined as ...

$$V_O = -V_t(R_3 + R_4)/R_3 \ln[I_{in}/I_{ref}]; \text{ where } V_t = 0.0259V.$$

Using the schematic values, the expression reduces to .....

$$V_O = -\ln[2000 I_{in}]$$

This is a typical matched transistor pair logarithmic amplifier. The matching removes a constant from the output expression and improves temperature stability. The temperature stability will be even greater if R_t varies inversely with temperature.

The input range of this circuit can be extended by using another HA-5180 as a current preamplifier to the logarithmic converter, as shown in Figure 12.

The HA-5180 is an extremely powerful building block. The sample-and-hold and the precision integrator are examples of the low drain placed on circuit capacitors by the bias currents. The bias currents themselves are nearly low enough to class the HA-5180 as an "ideal amplifier" in that respect. The transducer applications illustrate the HA-5180's merit in this area. The list of applications and uses could continue on, but the material presented should allude to the general applications and uses of the HA-5180.

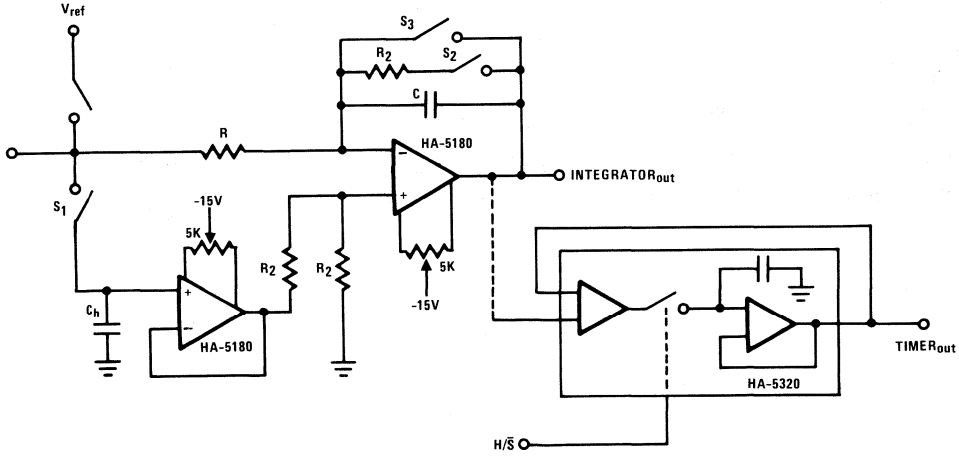


FIGURE 11.

S_1 and S_2 when closed, provide a threshold settling for this precision integrator while S_3 allows the output to be reset.

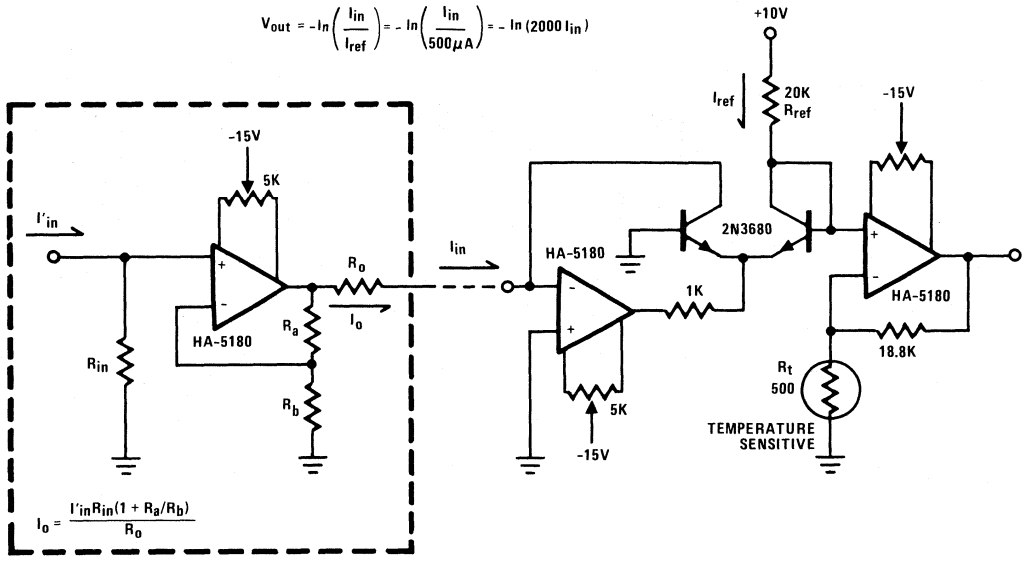


FIGURE 12

Logarithmic current to voltage converter depends on the low bias currents of the HA-5180 for accuracy.

References

"D-C Amplifier Noise Revisited", Al Ryan & Tim Scranton Analog Dialog, 1969.

Fitchen, F.C. and Motchenbacker, C.D. Low Noise Electronic Design, New York: John Wiley and sons, 1973.

Instruction Manual, model 2173C Transistor Noise Analyzer Control Unit. Quan-Tech, Division of KMS Industries. Whippany, New York.

THERMAL SAFE-OPERATING-AREAS FOR HIGH CURRENT OP AMPS

By: Brian Mathews

Many new Harris op amps can supply large amounts of output sink or source current. While this is a useful feature, it must be used carefully to avoid damaging or degrading the reliability of the device.

Output current contributes to the total amount of power dissipated within the amplifier according to the following formula:

TOTAL POWER = SUPPLY POWER + OUTPUT POWER

$P_{TOTAL} = [I_{CC} \times (V^+ - V^-)] + [|I_{OUT}| \times |(V_{CC} - V_{OUT})|]$

I_{CC} is the quiescent supply current and $(V^+ - V^-)$ is the total supply voltage. I_{OUT} is the amount of current flowing into or out of the output terminal and $(V_{CC} - V_{OUT})$ is the voltage across the op amp's output device.

Power dissipation generates heat and is related to temperature in the following way:

$$\text{POWER DISSIPATION} = \frac{\text{TEMPERATURE DIFFERENCE}}{\text{THERMAL RESISTANCE}}$$

The temperature difference we are interested in is the difference between the junction temperature of the circuit (T_J) and the ambient temperature (T_A). Thermal resistance is a measure of the heat conductivity of the integrated circuit, the mounting medium and the package. Different packages and die mounts have different thermal resistances measured in degrees Centigrade of temperature rise per watt of power dissipated ($^oC/W$). Typically, integrated circuits will have two thermal resistances, θ_{ja} and θ_{jc}. θ_{ja} is the thermal resistance from the semiconductor junction to ambient air. θ_{jc} is from junction to case only. This is useful if a heat sink is used. If so, then the total thermal resistance is the sum of junction-to-case, case-to-sink and sink-to-air. Thus, for no sink, the equation is:

$$P = \frac{T_J - T_A}{\theta_{ja}}$$

Harris maintains an absolute maximum rating on junction temperature or power dissipation on all op amps. The maximum junction temperature for most Harris op amps is $+175^oC$ although some have been designed for and specified at a T_J maximum of $+200^oC$.

We can now see that maximum allowable power dissipation depends on the ambient temperature and the thermal resistance of the package. For example, given that ambient temperature and maximum junction temperature are $+25^oC$ and $+175^oC$ respectively, assuming a thermal resistance of $+100^oC/W$, the maximum allowable power dissipation would be:

$$P_{MAX} = \frac{175 - 25}{100} = 1.5W$$

Applying this to our output power equation we can determine the maximum allowable output current.

Assuming: $V^+ = +15V$, $V^- = -15V$, $I_{CC} = 10mA$, $V_{OUT} = \pm 5V$

recall that

$P_{TOTAL} = [I_{CC} \times (V^+ - V^-)] + [|I_{OUT}| \times (|V_{CC} - V_{OUT}|)]$

$1.5W = [(10 \times 10^{-3}) \times (30)] + [I_{OUT} \times (10)]$

I_{OUT} MAX = 0.120 = 120mA

Thus, although this device might have a rated maximum output current of 200mA, that amount of current would cause the junction temperature to exceed the absolute maximum, with the given conditions, $T_A = +25^oC$, $V_{OUT} = 5V$, etc.

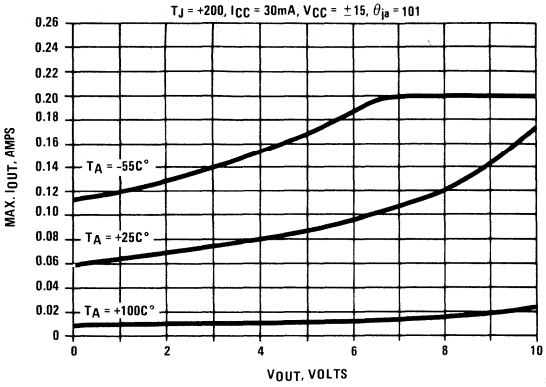
A collection of curves is included which represent graphically the maximum allowable output current over a range of output voltages. Only one quadrant is shown since it is symmetrical with respect to both axes. The graphs are entitled SOA for Safe-Operating-Area since the device can safely be operated within these boundaries. Each graph shows maximum output current for three different temperatures. The title lines indicate part type, package type, maximum T_J, assumed I_{CC} and V_{CC} levels and the package thermal resistance from junction to ambient temperature.

As long as voltage and current Maximum Limits are observed, then second breakdown effects will not be a factor in this analysis. Second breakdown must be considered for transient conditions exceeding the normal limits. This type of operation will be covered in a future report.

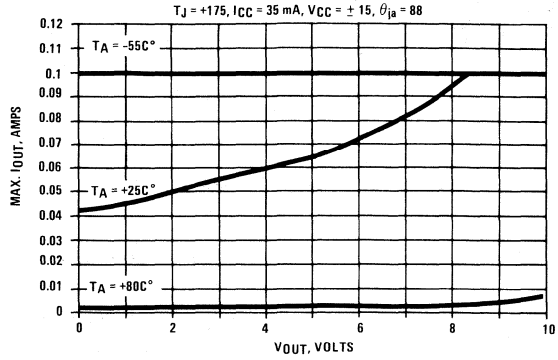
The graphs show how the output current capability is severely limited at elevated ambient temperatures. Several things can be done to help regain some of the output drive. Package choice can make a great deal of difference, be sure that the thermal implications of the package chosen are understood. Voltage supply levels are sometimes variable. Some devices, like the HA-5002, are specified at lower supply voltages. Other amplifiers may not meet all specifications but will operate with acceptable performance at reduced supply levels which will reduce quiescent power dissipation allowing greater output current levels.

DC SOA Graphs

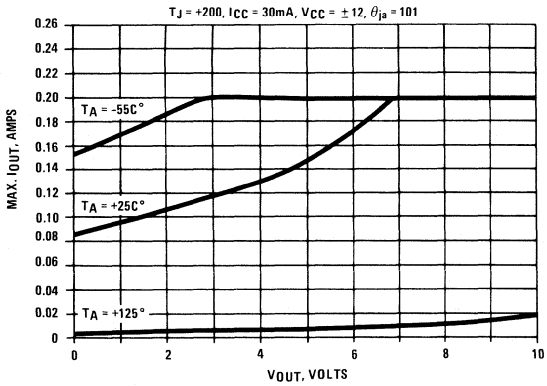
HA-5033 SOA, TO-8, NO SINK



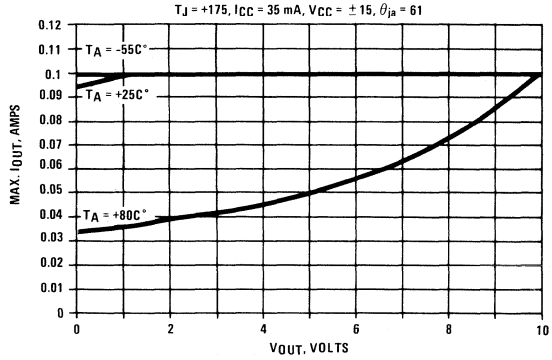
HA-2542 SOA, CERDIP, NO SINK



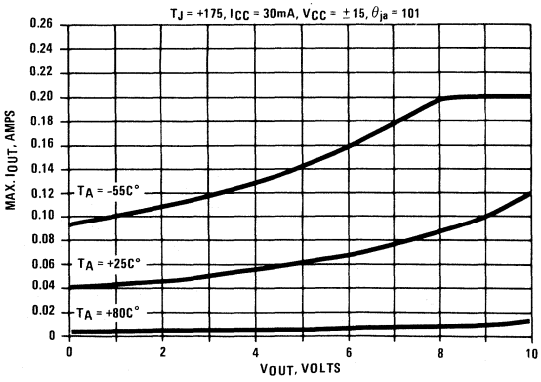
HA-5033 SOA, TO-8, NO SINK



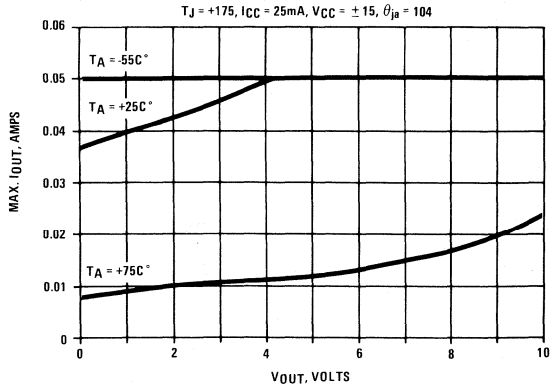
HA-2542 SOA, TO-8, NO SINK



HA-5033 SOA, TO-8, NO SINK

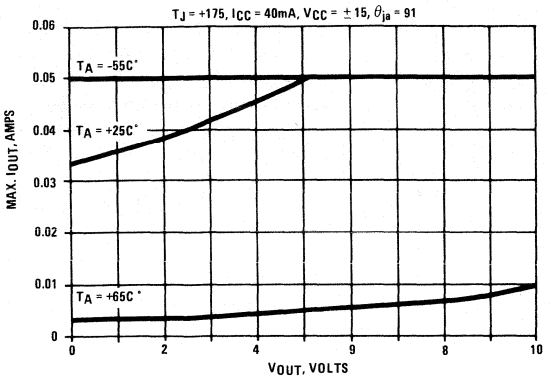


HA-2539/40 SOA, CERDIP, NO SINK

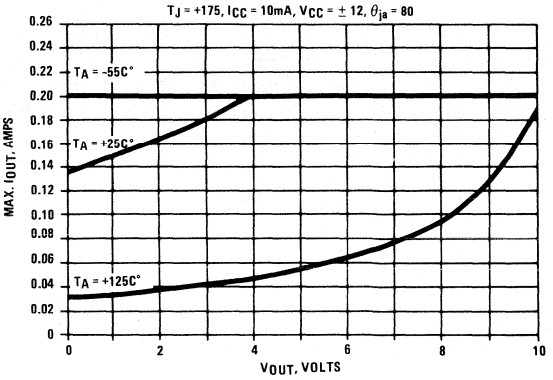


DC SOA Graphs

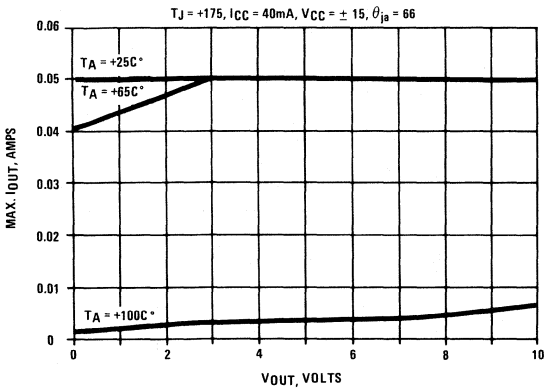
HA-2541 SOA, CERDIP, NO SINK



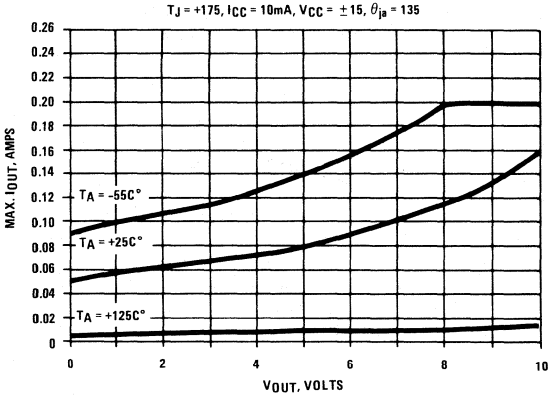
HA-5002 SOA, PLASTIC DIP, NO SINK



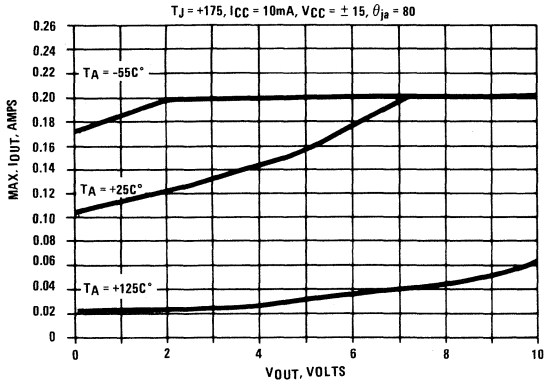
HA-2541 SOA, TO-8, NO SINK



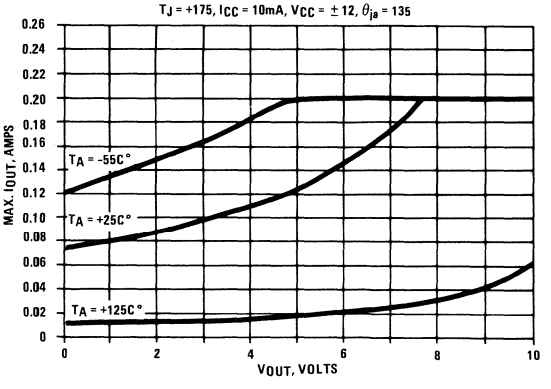
HA-5002 SOA, TO-99, NO SINK



HA-5002 SOA, PLASTIC DIP, NO SINK

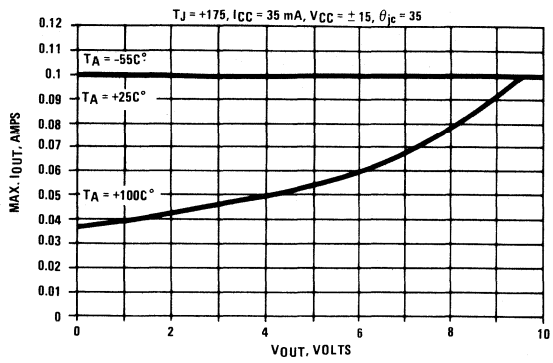


HA-5002 SOA, TO-99, NO SINK

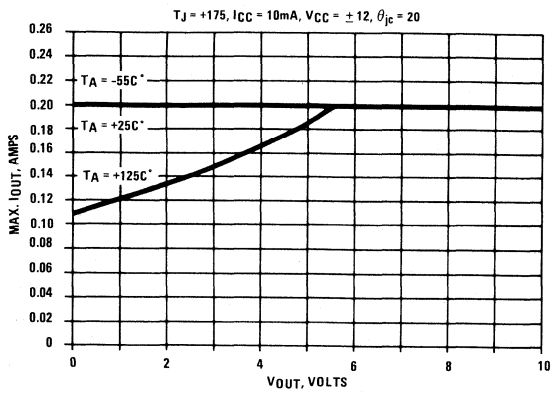


SOA Graphs With Heat Sink

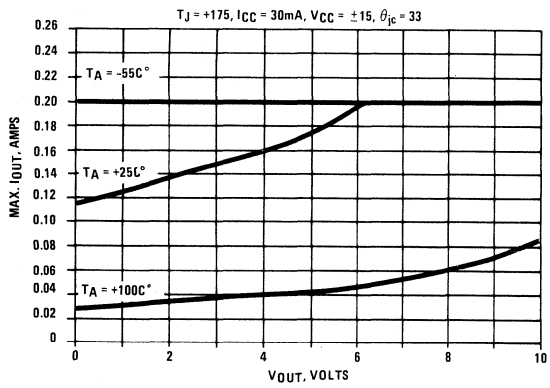
HA-2542, DIP, AAVID 5802 θ_{sa} = 15



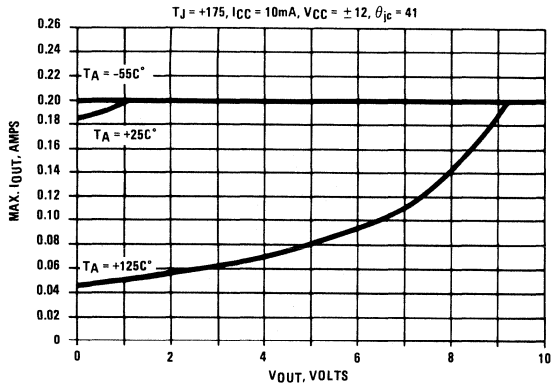
HA-5002, PLASTIC DIP, AAVID 5801 θ_{sa} = 12



HA-5003, TO-8, AAVID 5792 θ_{sa} = 25



HA-5002, TO-99, THERMALLOY 2227 θ_{sa} = 21



If package and supply voltage selection still do not allow enough current then a heat sink will be necessary. The thermal equation when a sink is used is:

$$P = \frac{T_J - T_A}{\theta_{jc} + \theta_{cs} + \theta_{sa}}$$

θ_{jc} is given in the device data sheet, θ_{cs} is from case to sink and is usually very small (one or less), and θ_{sa} is from sink to ambient and is given by the heat sink manufacturer.

Some representative curves are shown for some different types of heat sinks with different Harris part types.

Only DC steady-state conditions have been examined. AC and transient situations are not as straight forward.

The simplest way to handle the AC case is to utilize conservation of power. Thus, the output stage power drawn from the supplies is equal to the power in the load plus the power dissipated in the amplifier's output:

$$P_{SUPPLY} = P_{DISS} + P_{LOAD}$$

This discussion will assume a sine-wave output with peak voltage and current; V_P and I_P, and a resistive load, R_L.

The average power drawn from the supplies is:

$$P_{SUPPLY} = 2V_{CC}\, I_{CAVG}$$

Where I_{CAVG} is the average collector current in the output device. After calculating this current the following is obtained [1]:

$$P_{SUPPLY} = 2V_{CC}\,\frac{V_P}{\pi R_L}$$

The average power in the load is half the product of peak voltage and current, referred to voltage alone:

$$P_{LOAD} = \frac{V_P^2}{2R_L}$$

Thus the average power dissipated in the device's output is:

$$P_{DISS} = P_{SUPPLY} - P_{LOAD}$$

$$P_{DISS} = \frac{2V_{CC}V_P}{\pi R_L} - \frac{V_P^2}{2R_L}$$

This figure, added to the quiescent device dissipation, should be used to determine the thermal operating conditions when the output is a sine-wave and the load is resistive. For complex waveforms or reactive loads a thorough analysis should be performed on the particular application. This obviously cannot be done in this article.

For transient conditions, thermal capacitance and second breakdown must be considered. When power is supplied by an amplifier, the junction temperature does not rise instantaneously. The different elements in the thermal path all have thermal capacitance in addition to thermal resistance. Thus, the thermal transient response is determined by a time constant which is the product of thermal resistance and capacitance. Thermal capacitance is a material dependent value and will be covered thoroughly in a follow-up article along with second breakdown. Suffice to say that most packages have thermal time constants on the order of hundreds of milliseconds so that power pulses of short duration should not raise the junction temperature appreciably. Again, transient thermal characteristics will be covered in another article.

The graphs shown here are only general guidelines. The equations are included so that specific applications can be analyzed and thermal requirements can be determined. Methods have been shown for calculating total power dissipation, maximum allowable power dissipation, and average AC power dissipation with respect to output current and voltage, ambient temperature, junction temperature and thermal resistance. Thus, Harris high output devices can be used with confidence if these techniques are used.

Bibliography:

1. Antognetti, (Ed.): "Power Integrated Circuits," New York: McGraw-Hill, 1986.

2. Gray, P. and Meyer, R.: "Analysis and Design of Analog Integrated Circuits," New York: Wiley, 1977.

Heat Sink Manufacturers:

AAVID Engineering, Inc.
One Kool Path
Box 400
Laconia, NH 03247
(603) 524-4443

Thermalloy, Inc.
P.O. Box 810839
2021 West Valley View Lane
Dallas, TX 75381-0839
(214) 243-4321

APP NOTE

FOR YOUR INFORMATION

No. 557

Harris Analog

RECOMMENDED TEST PROCEDURES FOR ANALOG SWITCHES

By: Brian Mathews

Introduction

The following text describes the basic test procedures that can be used for most Harris CMOS switches. Various test conditions are used with the various switches. Table 1 has been included to help define the specific test setups to be used with each variety of switch. One additional note, all schematics assume an open switch for high logic inputs.

DC Switch Parameters

Analog Signal Range ($+V_S$) and ($-V_S$)

The analog signal range is the maximum input signal level which can be switched to the output with minimal distortion. For supply voltages lower than nominal, the analog signal range should be restricted to the voltage span between the supplies. Note that other parameters, such as "ON" resistance and leakage currents, are guaranteed over a smaller input range and tend to degrade toward the analog limits ($+V_S$ and $-V_S$). Harris switches can tolerate the positive analog signal limit ($+V_S$) applied to one side of a switch cell while the negative analog signal limit ($-V_S$) is applied to the other side (the switch must be open to avoid excessive currents).

The analog signal range is measured (Figure 1) by increasing an input waveform until the output shows evidence of distortion or the maximum analog level is reached (as stated in the maximum ratings section of the data sheet).

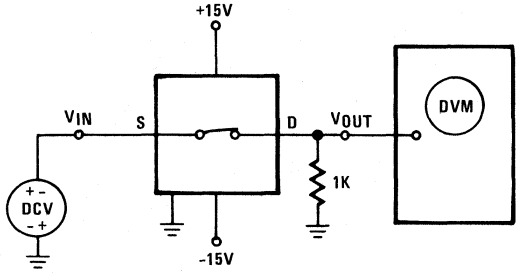
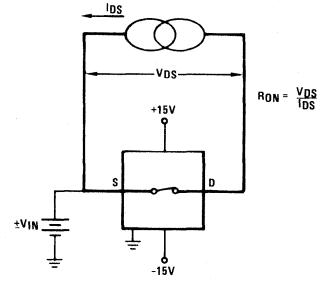


FIGURE 1. SUGGESTED CIRCUIT TO DETERMINE ANALOG SIGNAL RANGE

R_{ON}, ON Resistance (R_{DS})

"ON" resistance is the effective series on-switch resistance measured from input to output under specified conditions. Note that R_{ON} typically changes with temperature (highest at high temperature), and to a lesser degree with signal voltage and current.

R_{ON} is calculated from the voltage drop across a switch with a known current flow as in Figure 2.



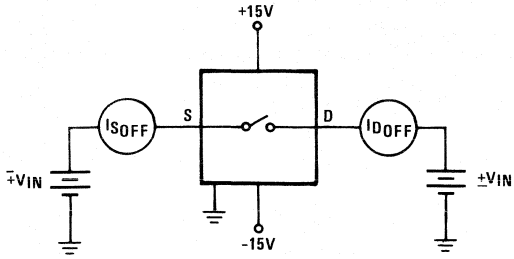
See Table 1 for Specific Test Conditions

FIGURE 2. "ON" RESISTANCE TEST CIRCUIT

$I_{S(OFF)}$, $I_{D(OFF)}$, $I_{D(ON)}$: Leakage Currents

Harris prefers to guarantee only worst case high temperature leakage currents because the room temperature picoampere levels are virtually impossible to measure repeatedly on currently available automated test equipment. Even under laboratory conditions, fixture and test equipment leakage currents may frequently exceed the device leakage currents. Since the leakage currents tend to double for every 10°C increase in temperature, it is reasonable to assume that the +25°C value is about 1/1000 the +125°C value; however, in some cases there may be ohmic leakage paths, such as across the package, which would tend to make the +25°C reading slightly higher than expected.

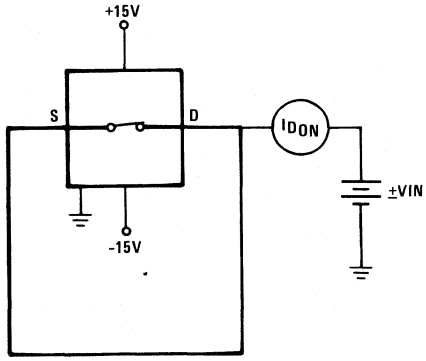
$I_{S(OFF)}$, measured directly with the circuit in Figure 3, consist largely of the diode leakage current from the source-body junction. $I_{D(OFF)}$, also measured directly with the circuit in Figure 3, is largely due to the diode leakage current in the drain-body junction.



See Table 1 for Specific Test Conditions

FIGURE 3. OFF LEAKAGE CURRENT TEST CIRCUIT

"ON" leakage current ($I_{D(ON)}$) is the current flowing through both the source-body and drain-body junctions of a closed switch. $I_{D(ON)}$ tends to have the most noticeable effect since it creates an offset voltage across the switch equal to $I_{D(ON)} * R_{ON}$. $I_{D(ON)}$ is measured directly with the circuit in Figure 4.



See Table 1 for Specific Test Conditions

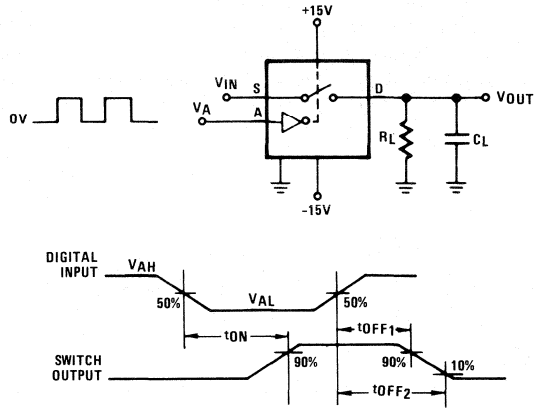
FIGURE 4. "ON" LEAKAGE CURRENT TEST CIRCUIT

Dynamic Switch Parameters

T_{ON}, T_{OFF}: Access Time

Switch "Turn On" time T_{ON} is the time required to activate an "OFF" switch to an "ON" state. T_{ON} is measured from the 50% point of the logic transition to the 90% point of the output transition (Figure 5).

Switch "Turn Off" time T_{OFF} is the time required to deactivate an "ON" switch to an "OFF" state. T_{OFF} is measured from the 50% point of the logic transition to the 10% point of the output transition (Figure 5).



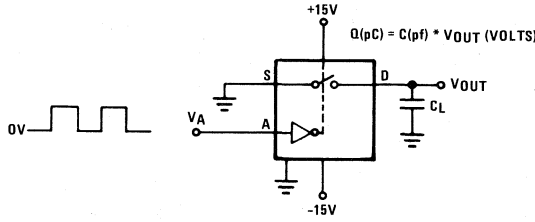
See Table 1 for Specific Test Conditions

FIGURE 5. "TURN ON" AND "TURN OFF" DELAY TEST CIRCUIT AND WAVEFORMS

Charge Injection

Cycling a switch "ON" or "OFF" results in a small amount of charge being injected into the analog signal path. This charge injection is generated through the capacitive coupling between the digital control lines and the analog outputs. The ensuing voltage spikes create an acquisition interval during which the output level is invalid even when little or no steady state level change is involved. The total net energy (charge injection) coupled onto the analog lines is especially critical when switching voltage to a capacitor since the injection charge will change the capacitor voltage at the instant of switching.

Charge injection, measured in pico-coulombs, is measured with the aid of the circuit in Figure 6.

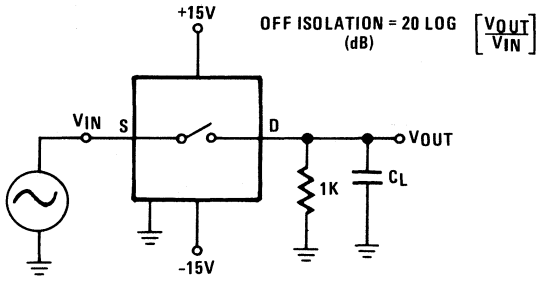


See Table 1 for Specific Test Conditions

FIGURE 6. CHARGE INJECTION TEST CIRCUIT

Off Isolation

Off Isolation is the degree of attenuation seen at the output of an "Open" switch when a high frequency signal is applied to the input. This feedthrough occurs through the source-body and drain-body capacitances and has a greater effect at higher frequencies. Off isolation is usually specified in decibels where Off Isolation = 20Log (V_{OUT}/V_{IN}), see Figure 7. The isolation generally decreases by 10dB/decade with increasing frequency.

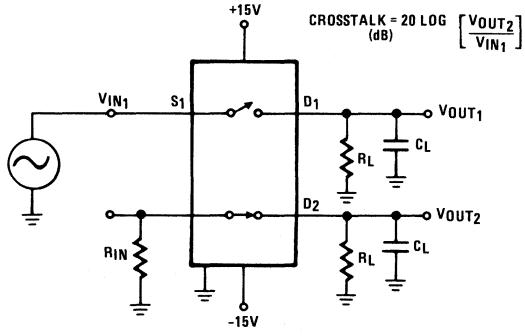


See Table 1 for Specific Test Conditions

FIGURE 7. OFF ISOLATION TEST CIRCUIT

Crosstalk

Crosstalk is the amount of signal cross coupling from an "OFF" analog input to the output of another "ON" channel output. Crosstalk is usually measured in decibles where: Crosstalk = 20Log(V_{OUT2}/V_{OUT1}), see Figure 8.

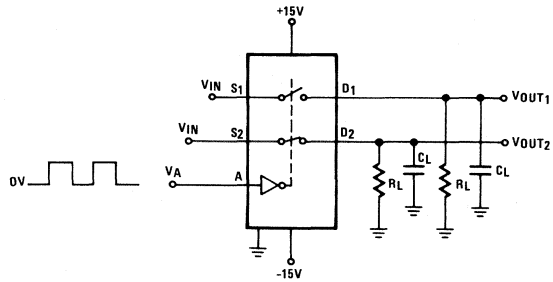


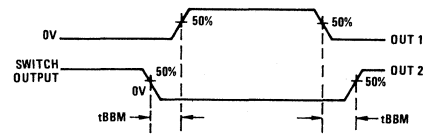
See Table 1 for Specific Test Conditions

FIGURE 8. GENERAL CROSSTALK TEST CIRCUIT

Break-Before-Make-Delay $T_{(OPEN)}$

The break-before-make-delay $T_{(OPEN)}$ is the elapsed time between the "Turn Off" of one switch and the corresponding "Turn On" of another for a common change in logic states (Figure 9). The delay measurement is taken at the 50% levels of the output transitions. The $T_{(OPEN)}$ delay prevents the switches from being simultaneously close during switching transitions.





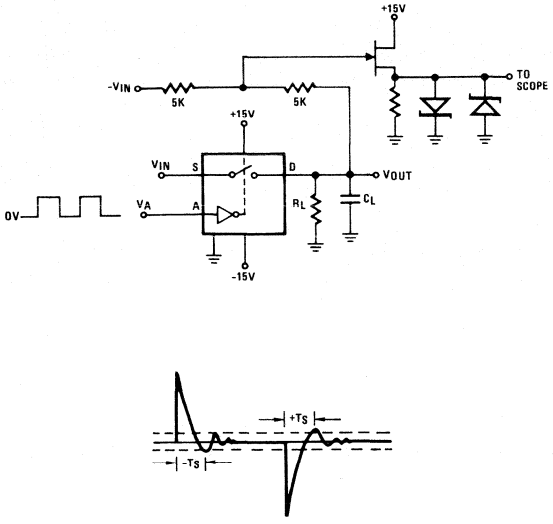
See Table 1 for Specific Test Conditions

FIGURE 9. BREAK-BEFORE-MAKE-DELAY TEST CIRCUIT AND WAVEFORMS

Settling Time

Settling time is the time required for the switch output to settle within a given percentage of the final value following a change in the digital input level. Usually the worst-case settling time occurs when the switch is required to slew across its full dynamic range (generally a 0V to +10V transition). This is known as full-scale settling time.

The settling time circuit is Figure 10, employs two resistors to generate an error voltage equal to the output error. A FET is used to buffer the summing junction from the oscilloscope probe capacitance.



Settling Time (T_S) is measured using a high speed recovery oscilloscope to display the error voltage V_E.

See Table 1 for Specific Test Conditions

FIGURE 10. SETTLING TIME TEST CIRCUIT AND WAVEFORM

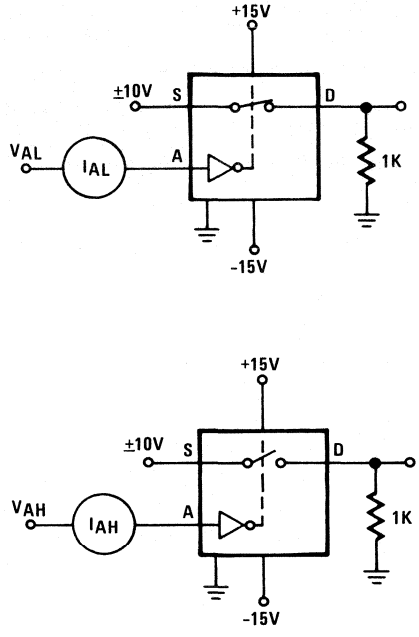
Switch Logic Parameters

Input Thresholds V_{AL} and V_{AH}

The input thresholds are the digital input upper and lower limits at which proper switching action is guaranteed to take place. The input low threshold V_{AL} is the maximum allowable voltage that can be applied to the digital input and still be recognized as a logic low ("0") input. The input high threshold V_{AH} is the minimum allowable voltage that can be applied to the digital input and still be recognized as a logic high ("1") input. All other parameters will be valid if the logic inputs are either below V_{AL} or above V_{AH}.

Input Leakage Current (I_{AL}, I_{AH})

Input leakage current is the bias current flowing either into or out of the digital input terminal. Input leakage current high (I_{AH}) is the current flowing while the digital input is in the high state ($\geq V_{AH}$), while input leakage current low (I_{AL}) is the current flowing when the digital input is in the low state ($\leq V_{AL}$). Input leakage currents are measured directly using the circuits in Figure 11.



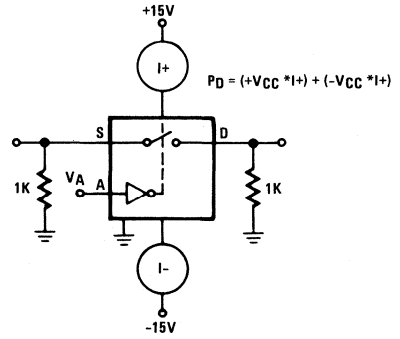
See Table 1 for Specific Test Conditions

FIGURE 11. INPUT LEAKAGE CURRENT TEST CIRCUITS

Static and Package Related Switch Parameters

P_D Power Dissipation: I+, I-

Quiesent power dissipation $P_D = (+V_{CC}{}^*I+) + (-V_{CC}{}^*I-)$ (Figure 12). P_D may be specified with the switch in either a cycling or a steady state condition. Note that, as with all CMOS devices, power dissipation increases with switching frequency.



See Table 1 for Specific Test Conditions

FIGURE 12. SUPPLY CURRENT TEST CIRCUIT

Switch Capacitance $C_{S(OFF)}$, $C_{D(OFF)}$, $C_{D(ON)}$, C_A

The various switch capacitances are stated as typical values. These values are given by design and are not subject to production testing (Figure 13).

Capacitance Source-Off $C_{S(OFF)}$ is the capacitance with respect to ground seen at the analog input with the switch open. This capacitance is the sum of the source capacitance of the N-channel and P-channel switching devices.

$$C_{S(OFF)} = C_{SGP1} + C_{SBP1} + C_{SGN} + C_{SBN}$$

Capacitance Drain-Off $C_{D(OFF)}$ is the capacitance with respect to ground seen at the output terminal with the switch open. This capacitance is the sum of the drain capacitance of the N-channel and P-channel switching devices.

$$C_{D(OFF)} = C_{DGP1} + C_{DBP1} + C_{DGN} + C_{DBN}$$

Capacitance Drain-On $C_{D(ON)}$ is the capacitance with respect to ground at the drain with the switch closed. Generally $C_{D(ON)}$ is the total of the source-off and drain-off capacitances.

$$C_{D(ON)} = C_{D(OFF)} + C_{S(OFF)}$$

Input to output capacitance $C_{DS(OFF)}$ is the capacitance between the analog input and output with the switch open.

Digital input capacitance C_A is the capacitance with respect to ground at the digital input. C_A chiefly affects propagation delays when the switch is driven by CMOS logic.

Switch Test Fixture Design Rules

The high performance characteristics of Harris switches require high quality test fixtures for accurate characterization. The following design rules should eliminate most sources of error and provide highly accurate results.

- Decoupling capacitors should be placed as close to the supply pins as possible.
- A ground plane should be used to minimize distributed capacitance.
- All grounds should terminate at a single point ground.
- All sensitive analog lines should be routed between ground traces and kept away from digital lines.
- Analog and digital lines should cross at right angles.
- All unused logic pins should be connected to either V_{AL} or V_{AH}.
- All unused analog pins should be connected to ground through a 1K resistor.
- Teflon sockets should be used to minimize socket capacitance.

Acknowledgement

This Application Note is the combined result of the work of various laboratory technical staff, most notably Robert C. Junkins.

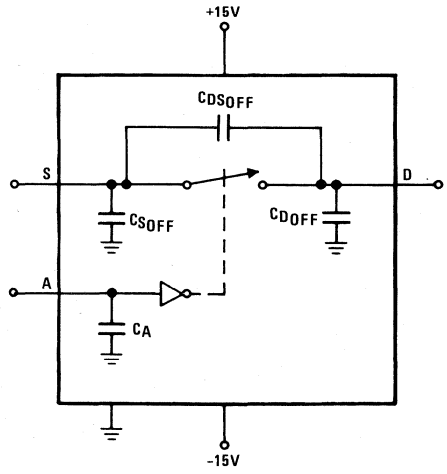


FIGURE 13. EQUIVALENT SWITCH CIRCUIT INCLUDING CAPACITANCES

TABLE 1.

	LOGIC LEVELS	LOGIC REFERENCE	R_{ON}	I_S, I_D	T_{ON}, T_{OFF}	CHARGE INJECTION	CROSSTALK	OFF ISOLATION	SETTLING TIME	BREAK-BEFORE-MAKE	I_{AL}, I_{AH}	POWER DISSIPATION
HI-200	V_{AL} = 0.8V V_{AH} = 2.4V	V_{REF} OPEN	V_{IN} = +10V I_{DS} = 1mA	V_{IN} = +14V	V_{IN} = +10V R_L = 1K C_L = 35pF V_A = 0V, 4V			V_{IN} = 3Vrms f = 100KHz R_L = 1K C_L = 10pF V_A = 5V, 0V		V_{AL} = 0V V_{AH} = 4V	V_{AL}min = 0V V_{AH}max = 5V	V_A = 0V or V_A = 3V
HI-201	V_{AL} = 0.8V V_{AH} = 2.4V	V_{REF} OPEN	V_{IN} = +10V I_{DS} = 1mA	V_{IN} = +14V	V_{IN} = +10V V_A = 0V, 4V			V_{IN} = 3Vrms f = 100KHz R_L = 1K C_L = 10pF V_A = 5V, 0V		V_{AL} = 0V V_{AH} = 4V	V_{AL}min = 0V V_{AH}max = 5V	V_A = 0V or V_A = 3V
HI-201HS	V_{AL} = 0.8V V_{AH} = 3.0V		V_{IN} = +10V I_{DS} = 1mA	V_{IN} = +14V	V_{IN} = +10V R_L = 1K C_L = 35pF V_A = 3V, 0V	C = 1000pF	V_{IN} = 3Vrms f = 100KHz R_L = 1K V_A = 3V, 0V R_{IN} = 1K	V_{IN} = 3Vrms f = 100KHz R_L = 1K C_L = 10pF V_A = 3V, 0V	V_{IN} = +10V R_L = 1K C_L = 35pF V_A = 3V, 0V		V_{AL}min = 0V V_{AH}max = 5V	V_A = 0V or V_A = 3V
HI-300 Thru HI-303	V_{AL} = 0.8V V_{AH} = 4.0V		V_{IN} = +10V I_{DS} = 10mA	V_{IN} = +14V	V_{IN} = +3V R_L = 300 C_L = 33pF V_A = 4V, 0V	C = 10000pF V_A = 5.0V		V_{IN} = 1Vrms f = 500KHz R_L = 1K C_L = 15pF		V_{AL} = 0V V_{AH} = 5V R_L = 300 C_L = 33pF V_{IN} = +3V	V_{AL}min = 0V V_{AH}max = 5V	V_A = 0.8V or V_A = 4.0V
HI-304 Thru HI-307	V_{AL} = 3.5V V_{AH} = 11.0V		V_{IN} = +10V I_{DS} = 10mA	V_{IN} = +14V	V_{IN} = +3V R_L = 300 C_L = 33pF V_A = 15V, 0V	C = 10000pF V_A = 15V		V_{IN} = 1Vrms f = 500KHz R_L = 1K C_L = 15pF		V_{AL} = 0V V_{AH} = 15V R_L = 300 C_L = 33pF V_{IN} = +3V	V_{AL}min = 0V V_{AH}max = 15V	V_A = 0V or V_A = 15V
HI-381 Thru HI-390	V_{AL} = 0.8V V_{AH} = 4.0V		V_{IN} = +10V I_{DS} = 10mA	V_{IN} = +14V	V_{IN} = +3V R_L = 300 C_L = 33pF V_A = 5V, 0V	C = 10000pF V_A = 5.0V		V_{IN} = 1Vrms f = 500KHz R_L = 1K C_L = 15pF		V_{AL} = 0V V_{AH} = 5V R_L = 300 C_L = 33pF V_{IN} = +3V	V_{AL}min = 0V V_{AH}max = 5V	V_A = 0.8V or V_A = 4.0V
HI-5040 Thru HI-5051	V_{AL} = 0.8V V_{AH} = 3.0V	V_L = 5V V_R = 0V	V_{IN} = +10V I_{DS} = 1mA	V_{IN} = +10V	V_{IN} = +10V R_L = 1K	C = 10000pF	V_{IN} = 2Vp-p f = 100KHz R_L = 100 C_L = 5pF R_{IN} = 0	V_{IN} = 2Vp-p f = 100KHz R_L = 100 C_L = 15pF			V_{AL}min = 0V V_{AH}max = 5V	V_A = 0V or V_A = 3.0V

APP NOTE

FOR YOUR INFORMATION

No. 571

Harris Analog

USING RING SYNC WITH HC-5502A AND HC-5504 SLICs

Dave Donovan

Introduction

The ring synchronization (sync) input pin is a TTL compatible clock input in both the HC-5502A and HC-5504 SLICs. It's purpose is to insure that the ring relay is activated or deactivated only when the instantaneous AC ring voltage, which may be as high as 150V peak, is at or near AC zero crossing.

If ring sync is not used, it must be tied high to insure proper ring trip. When used, it is important to consider at which zero crossing of the AC ring voltage, positive or negative, the ring sync signal must be synchronized with. Subsequent illustrations and equations highlight this consideration.

For detailed description of the ring trip sequence of events, refer to Application Note 549 by P. G. Phillips. Excerpts from the pertinent section are included below.

Ring Trip Sequence

The Ring Command (RC) input is taken low during ringing. This activates the ring relay driver (RR) output providing the telephone is not off-hook or the line is not in a power denial state. The ring relay connects the ring generator to the subscriber loop. The ring generator output is usually an $80V_{RMS}$, 20Hz signal. For use with the Harris SLIC, the ring signal should not exceed 150V peak. Since the telephone ringer is AC coupled, only ring current will flow. For the HC-5502A SLIC, the ring current is sunk by the ring feed amplifier output stage whereas for the HC-5504 the ring path flows directly into V_{B}- via a set of relay contacts. The high impedance terminal RFS exists on the HC-5504 so that the low impedance RF node can be isolated from the hot end of the ring path in the battery referenced ring scheme.

The AC ring current flowing in the subscriber circuit will be sensed across RB4, and will give rise to an AC voltage at the output of the longitudinal amplifier. R19 and C4 attenuate this signal before it reaches the ring trip detector to prevent false ring trip. C4 is nominally set at 0.47μF but can be increased towards 1μF for short lines or if several telephones are connected in parallel across the line in order to prevent false or intermittent ring trip.

When the subscriber goes off-hook, a DC path is established between the output winding of the ring generator and the battery ground or V_{B}- terminal. A DC longitudinal imbalance is established since no tip feed current is flowing through the tip feed resistors. The longitudinal amplifier output is driven negative. Once it exceeds the ring trip threshold of the ring trip detector, the logic circuitry is driven by GK to trip the ring relay establishing an off-hook condition such that SHD will become active as loop metallic current starts to flow.

Figure 1 illustrates the sequence of events during ring trip with ring synchronization. Note, that owing to the 90° phase shift introduced by the low pass filter (R19, C4) the RS pulse will occur at the most negative point of the attenuated ring signal that is fed into the ring trip detector. Hence, when DC conditions are established for RTD, the AC component actually assists ring trip taking place. If ring synchronization is not used, then the RS pin should be held permanently to a logic high of 5V nominally: ring trip will occur asynchronously with respect to the ring voltage. Ring trip is guaranteed to take place within three ring cycles after the telephone going off-hook.

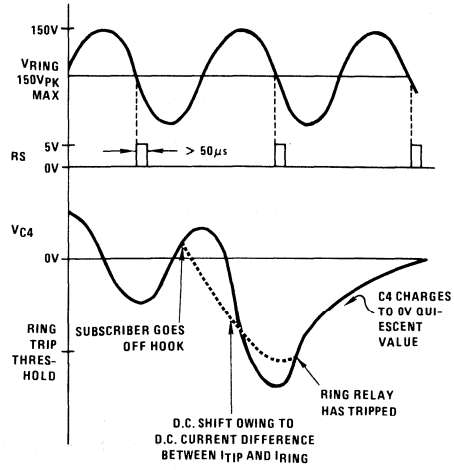


FIGURE 1. RING TRIP SEQUENCE.

Case I: HC-5502A Tip Injected Ringing

$V_{LA} = (I_{RING} - I_{TIP})(RB4)(K)$
(During Ringing $I_{TIP} = 0$)
$V_{LA} = (I_{RING})(RB4)(K)$
$I_{RING} = (V_{RF} - V_{RING})/RB4$
$\therefore V_{LA} = (V_{RF} - V_{RING})K$

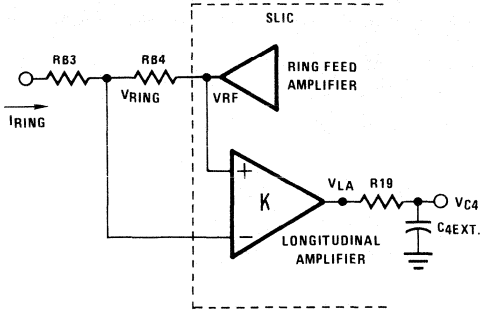


FIGURE 2.

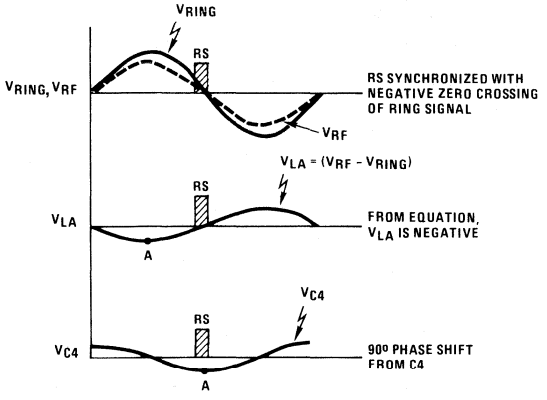


FIGURE 3.

For Case I, refer to Figures 2 and 3. In this situation the desired result is obtained, namely, that ring sync occurs during the negative peak of V_{C4}. This helps achieve ring trip faster because, once a subscriber goes off-hook, a negative DC shift is observed at V_{C4}. This shift approaches a comparator threshold in the ring trip detection circuit. If the negative peak of V_{C4}(AC) precedes the negative going DC shift at V_{C4}, one can achieve ring trip in a shorter time frame. Also this configuration allows ring trip to occur for long lines, in the order of 3000 ohms. At these line lengths, the DC negative shift will never reach the threshold because there is not enough DC current through the sense resistor, RB4. However, the negative peak of V_{C4} (AC) will cross the ring trip detector comparator threshold and ring trip will occur.

Conclusion 1: For this case make sure ring sync is synchronized with the negative zero crossing of V_{RING} as it appears on the line.

Case II: HC-5504 Ring Injected Ringing

$V_{LA} = (I_{RING} - I_{TIP})(RB4)(K)$
(During Ringing $I_{TIP} = 0$)
$V_{LA} = (I_{RING})(RB4)(K)$
$I_{RING} = (V_{RFS} - V_{RING})/RB4$
$\therefore V_{LA} = (V_{RFS} - V_{RING})K$

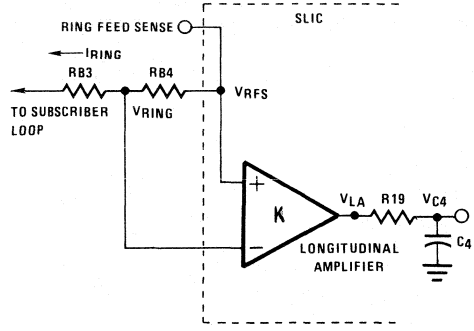


FIGURE 4.

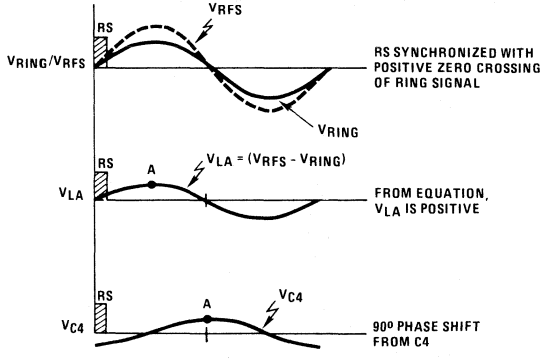


FIGURE 5.

For Case II refer to Figures 4 and 5. Here ring sync must be synchronized with the positive zero crossing of V_{RING} (AC) as it appears on the line so as to coincide with the negative peak of V_{C4} (AC), as in the previous case. One can see from Figure 5 that ring sync on the negative zero crossing would coincide with the positive peak of V_{C4}, inhibiting ring trip for loops greater than approximately 800 ohms.

Conclusion 2: For this case make sure ring sync is synchronized with the positive zero crossing of V_{RING} (AC.).

For all other ring configurations, namely, tip injected and balanced ringing for the 5504, if ring sync is used, it must be synchronized with the negative zero crossing of V_{RING}(AC).

Acknowledgement

The author wishes to thank Geoff Phillips for his contribution to this paper.

APP NOTE

FOR YOUR INFORMATION

No. 573

Harris Analog

THE HC-5560 DIGITAL LINE TRANSCODER

David J. Donovan

1.0 Introduction

The Harris HC-5560 digital line transcoder provides mode selectable, psuedo ternary line coding and decoding schemes for North American and European transmission lines. Coding schemes include Alternate Mark Inversion (AMI), Bipolar with N Zero Substitution (BNZS), and High Density Bipolar 3 (HDB3), used for transmission lines as follows:

AMI: North American T1(1.544MHz) and T1C(3.152MHz) lines
B6ZS: North American T2(6.3212MHz) lines
B8ZS: North American T1(1.544MHz) lines
HDB3: European PCM30(2.048 & 8.448MHz) CEPT lines. Recommended by CCITT

The transcoder is a single chip, single supply device fabricated with standard cell CMOS. Features include simultaneous coding and decoding, asynchronous operation, loop back mode, transmission error detection, an alarm indication signal, and a full chip reset.

This application note will describe why coding for digital transmission is necessary, the types of coding, which is best, and why, and the functionality and applications of the HC-5560 digital line transcoder.

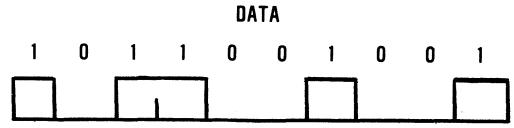
2.0 Why Line Coding?

Transmission of serial data over any distance, be it a twisted pair, fiber optic link, coaxial cable, etc., requires "maintenance" of the data as it is transmitted (through repeaters, echo cancellors etc.). The data integrity must be maintained through data reconstruction, with proper timing, and retransmitted. Line codes were created to facilitate this "maintenance".

In selecting a particular line coding scheme some considerations must be made, as not all line codes adequately provide the all important synchronization between transmitter and receiver. Other considerations for line code selection are noise and interference levels, error detection/checking, implementation requirements, and the available bandwidth.

2.1 Unipolar Coding

The most basic transmission code is unipolar or unbalanced coding whereby each discrete variable to be transmitted is assigned a different level, 0V and +3V, for example:



UNIPOLAR (UNBALANCED) SIGNAL

There are, however, a number of disadvantages:

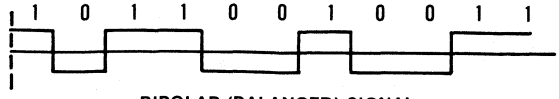
- The average power (Ao/2) is two times other codes
- The coded signal contains DC and low frequency components. When long strings of zeros are present, a DC or baseline wander occurs. This results in loss of timing and data because a receiver/repeater cannot optimally discriminate ones and zeros.

DC WANDER

- Repeaters/receivers require a minimum pulse density for proper timing extraction. Long strings of ones or zeros contain no timing information and lead to timing jitter and possible loss of synchronization.
- There is no provision for line error rate monitoring.

2.2 Bipolar Coding is Better

With bipolar, or balanced, coding, the same data may be transmitted more efficiently achieving the same error distance with half the power (Ao/4). This coding is often referred to as Non-Return to Zero (NRZ) coding as the signal level is maintained for the duration of the signal interval.



BIPOLAR (BALANCED) SIGNAL

Although bipolar coding is more efficient than unipolar, it still lacks provisions for line error monitoring, and is susceptible to DC wander and timing jitter.

The HC-5560 digital line transcoder provides a number of augmented bipolar coding schemes which:

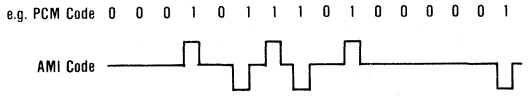
- Eliminate DC Wander
- Minimize Timing Jitter
- Provide for Line Error Monitoring

This is accomplished by introducing controlled redundancy in the code through extra coding levels.

3.0 Line Code Descriptions

The HC-5560 transcoder allows a user to implement any of the four line coding schemes described below.

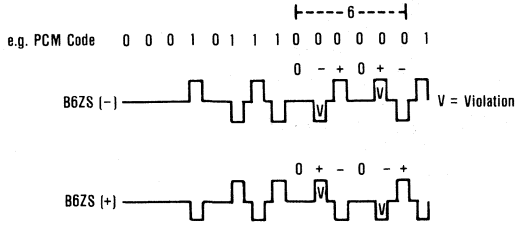
AMI, Alternate Mark Inversion, is used primarily in North American T1 (1.544MHz) and T1C (3.152MHz) carriers. Zeros are coded as the absence of a pulse and one's are coded alternately as positive or negative pulses. This type of coding reduces the average voltage level to zero to eliminate DC spectral components, thereby eliminating DC wander.



To facilitate timing maintenance at regenerative repeaters along a transmission path, a minimum pulse density of logic 1's is required. Using AMI, there is a possibility of long strings of zeros and the required density may not always exist, leading to timing jitter and therefore higher error rates.

A method for insuring a minimum logic 1 density by substituting bipolar code in place of strings of 0's is called BNZS or Bipolar with N Zero Substitution. B6ZS is used commonly in North American T2 (6.3212MHz) carriers. For every string of 6 zeros, bipolar code is substituted according to the following rule:

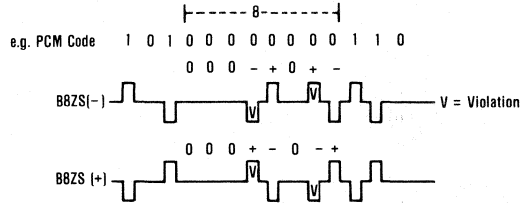
If the immediate preceding pulse is of (-) polarity, then code each group of 6 zeros as 0-+0+-, and if the immediate preceding pulse is of (+) polarity, code each group of 6 zeros as 0+-0-+. One can see the consecutive logic 1 pulses of the same polarity violate the AMI coding scheme.



B8ZS is used commonly in North American T1(1.544MHz) and T1C(3.152MHz) carriers. For every string of 8 zeros, bipolar code is substituted according to the following rules:

1) If the immediate preceding pulse is of (-) polarity, then code each group of 8 zeros as 000-+0+-.

2) If the immediate preceding pulse is of (+) polarity, then code each group of 8 zeros as 000+-0-+.

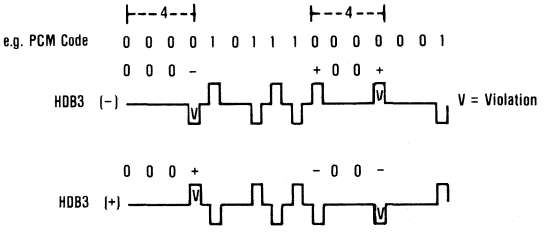


The BNZS coding schemes, in addition to eliminating DC wander, minimize timing jitter and allow a line error monitoring capability.

Another coding scheme is HDB3, high density bipolar 3, used primarily in Europe for 2.048MHz carriers. This code is similar to BNZS in that it substitutes bipolar code for 4 consecutive zeros according to the following rules:

1) If the polarity of the immediate preceding pulse is (-) and there have been an odd (even) number of logic 1 pulses since the last substitution, each group of 4 consecutive zeros is coded as 000-(+00+).

2) If the polarity of the immediate preceding pulse is (+) then the substitution is 000+(-00-) for odd (even) number of logic 1 pulses since the last substitution.



The 3 in HDB3 refers to the coding format that precludes strings of zeros greater than 3. Note that violations are produced only in the fourth bit location of the substitution code and that successive substitutions produce alternate polarity violations.

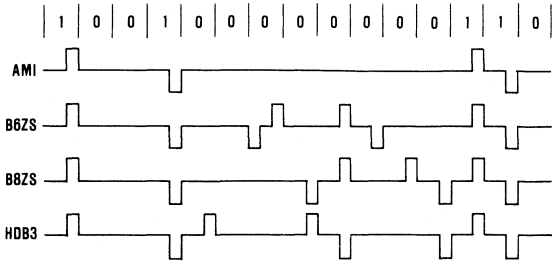


FIGURE 1. SUMMARY OF CODING SCHEMES PROVIDED BY THE HC-5560 TRANSCODER.

A summary graph of all four substitution coding schemes is illustrated in Figure 1. To simplify timing recovery, logic 1's are encoded with 50% duty cycle pulses.

4.0 Functional Description

The HC-5560 transcoder can be divided into six sections: transmitter(coder), receiver(decoder), error detector, all ones detector, testing functions, and output controls. A block diagram is shown in Figure 2.

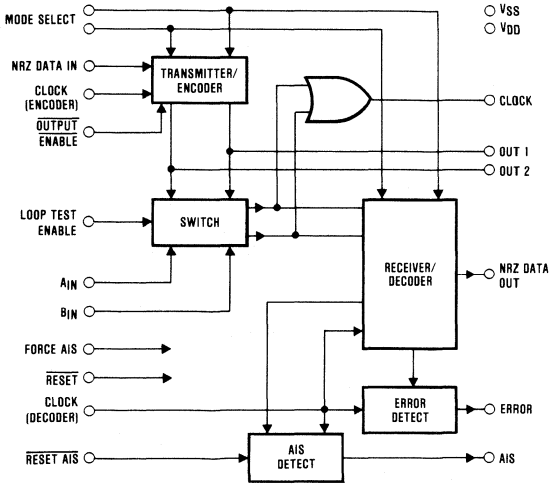


FIGURE 2. HC-5560 TRANSCODER FUNCTIONAL BLOCK DIAGRAM.

4.1 Transmitter (Coder)

The transmitter codes a non-return to zero (NRZ) binary unipolar input signal (NRZ IN) into two binary unipolar return to zero (RZ) output signals (OUT1, OUT2). These output signals represent the NRZ data stream modified according to the selected encoding scheme (i.e., AMI, B8ZS, B6ZS, HDB3) and are externally mixed together (usually via a transistor or transformer network) to create a ternary bipolar signal for driving transmission lines.

4.2 Receiver (Decoder)

The receiver accepts as its input the ternary data from the transmission line that has been externally split into two binary unipolar return to zero signals (A_{IN} and B_{IN}). These signals are decoded, according to the rules of the selected line code into one binary unipolar NRZ output signal (NRZ OUT).

The encoder and decoder sections of the chip perform independently (excluding loopback condition) and may operate simultaneously.

4.3 Error Detector

The Error output signal is active high for one cycle of CLK DEC upon the detection of any bipolar violation in the received A_{IN} and B_{IN} signals that is not part of the selected line coding scheme. The bipolar violation is not removed, however, and shows up as a pulse in the NRZ DATA OUT signal. In addition, the Error output signal monitors the received A_{IN} and B_{IN} signals for a string of zeros that violates the maximum consecutive zeros allowed for the selected line coding scheme (i.e., 8 for B8ZS, 6 for B6ZS, and 4 for HDB3). In the event that an excessive amount of zeros is detected, the Error output signal will be active high for one cylce of CLK DEC during the zero that exceeds the maximum number. In the case that a high level should simultaneously appear on both received input signals A_{IN} and B_{IN} a logical one is assumed and appears on the NRZ data out stream with the error signal active.

4.4 All Ones Detector

An input signal received at inputs A_{IN} and B_{IN} that consists of all ones (or marks) is detected and signalled by a high level at the alarm indication signal (AIS) output is set to a high level when less than three zeros are received during one period of Reset AIS immediately followed by another period of Reset AIS containing less than three zeros. The AIS output is reset to a low level upon the first period of Reset AIS containing 3 or more zeros.

4.5 Testing Functions

A logic high level on LTE enables a loopback condition where OUT1 is internally connected to input A_{IN} and OUT2 is internally connected to B_{IN} (this disables inputs A_{IN} and B_{IN} to external signals). In this condition, the input signal NRZ DATA IN appears at output NRZ DATA OUT (delayed by the amount of clock cycles it takes to encode and decode the selected line code). A decode clock must be supplied for this operation. The Reset input can be used to initialize this process.

4.6 Output Controls

The output controls are Output Enable and Force AIS. These pins allow normal operation, force OUT1 and OUT2 to zero, or force OUT1 and OUT2 to output all ones (AIS condition).

5.0 Applications

The HC-5560 transcoder is designed for use in North American and European PCM transmission lines where psuedo ternary line code substitution schemes are desired. Any equipment that interfaces to T1, T1C, T2 or PCM30 transmission lines may incorporate transcoders. Such equipment includes multiplexers, channel service units, echo cancellors, repeaters, etc. This section will illustrate and describe a basic circuit application, and various system level applications examples.

5.1 Basic Applications Circuit

The basic applications circuit is shown in Figure 3. The encoder accepts serially clocked unipolar non-return to zero (NRZ/PCM) data at the NRZ IN pin and codes it into two unipolar return to zero (RZ) signals at pins Out1 and Out2. A coding scheme is chosen via mode select pins MS1 and MS2. Data is clocked in on the negative edge of ECLK and clocked out on the positive edge of ECLK.

The outputs must be mixed externally, via a transistor/transformer network, to produce the ternary 'bipolar' code selected and to drive the transmission line. The length of Out1 and Out2 are set by the length of the positive ECLK pulse.

To decode ternary coded data, the signal must first be split into two unipolar signals and presented to the A_{IN} and B_{IN} pins. This may be accomplished by an amplifier with a differential output, and two comparators. Both inputs are sampled by the positive edge of DCLK. Decoded data is clocked out in NRZ form to the NRZ OUT pin on the positive edge of DCLK.

All the logic inputs and outputs are TTL compatible.

5.2 System Level Examples

Examples of system level transcoder applications are illustrated in Figure 4 through 8.

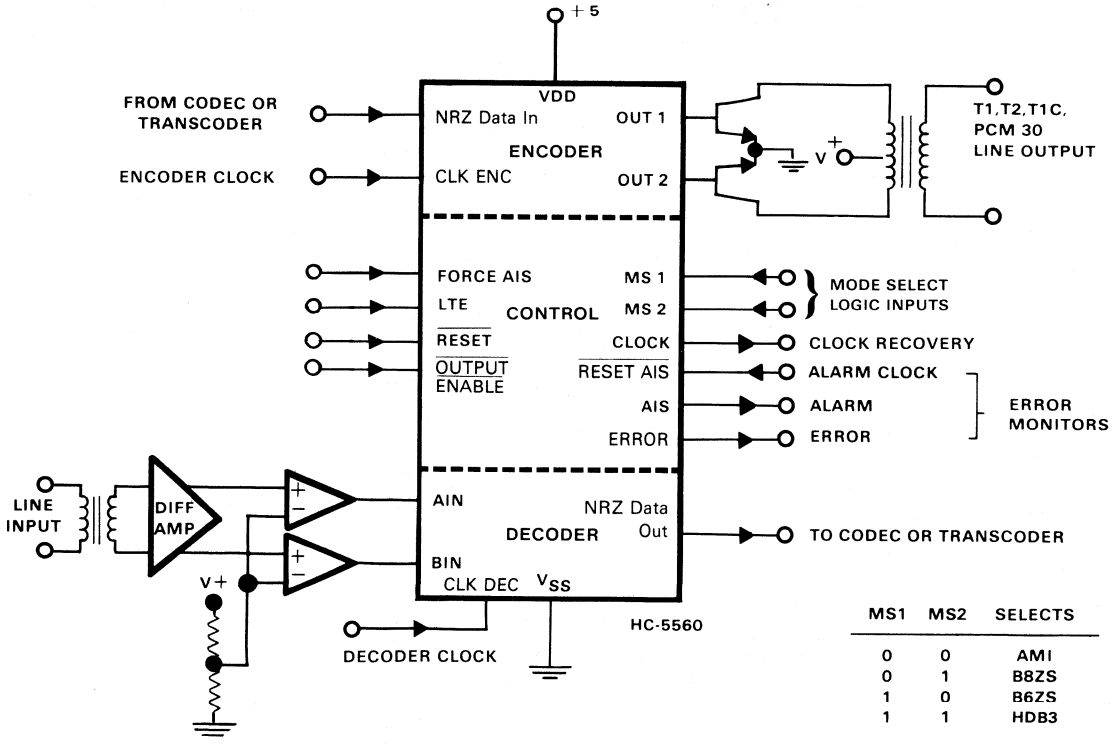


FIGURE 3. BASIC TRANSCODER APPLICATIONS CIRCUIT.

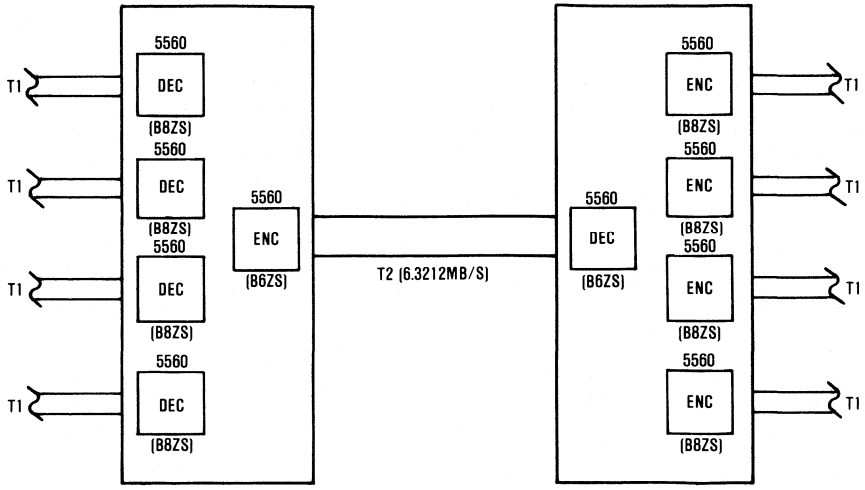


FIGURE 4. M12 MULTIPLEXER

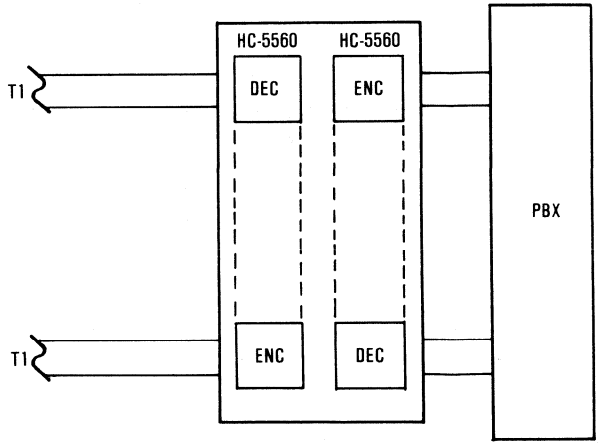


FIGURE 5. CHANNEL SERVICE UNIT (CSU)

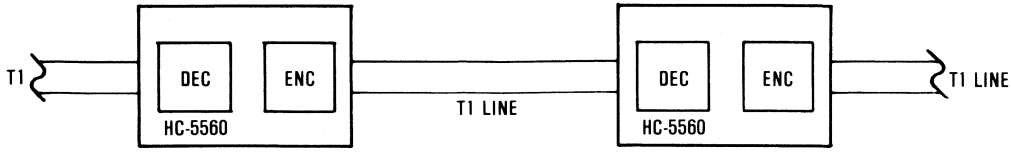


FIGURE 6. ECHO CANCELLOR

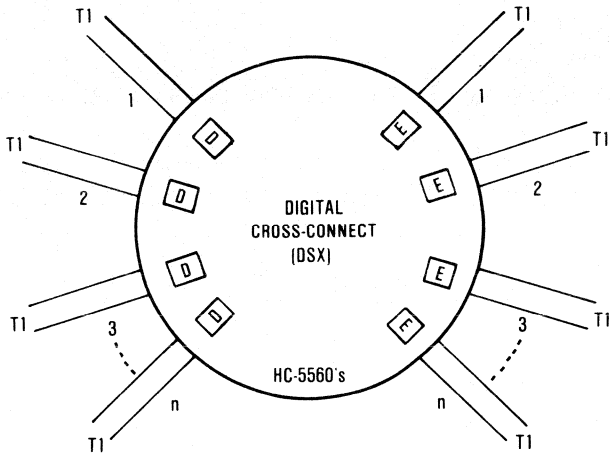


FIGURE 8. T1 COMPRESSION BY ADPCM

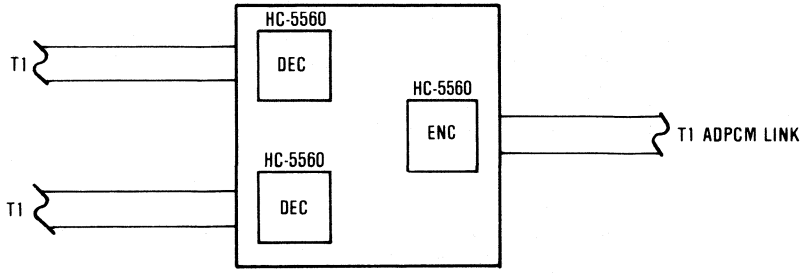


FIGURE 7. DIGITAL CROSS CONNECT (DCS)

APP NOTE

FOR YOUR INFORMATION

No. 574

Harris Analog

UNDERSTANDING PCM CODING

David J. Donovan

1.0 Introduction

The process of converting analog voice signals into Time Division Multiplexed (TDM) Pulse Code Modulated (PCM) format is described and illustrated herein. Application Note No. 570, "Understanding CODEC Timing", by D.J. Donovan is recommended reading as accompanyment to this application note.

Analog time varying voice input information is transmitted over two-wire (2w) pairs (channels) from subscribers. The PCM filter band-limits voice signals to 4kHz, one per channel, and removes power line and ringing frequencies. Research has shown that voice transmission band-limited to 4kHz has enough fidelity for telephony purposes.

2.0 Sampling

The process of converting filtered voice information into a digitized pulse train format begins with sampling the voice signal at uniform intervals. These intervals are determined by the Nyquist Sampling Theorem, which simply states that any signal may be completely re-constructed from its representative sampling if it is sampled at least twice the maximum frequency of interest. The telephone system, being a worldwide standard 8kHz sampling system, satisfies Nyquist, as all voice signals are band-limited to 4kHz. When the voice waveform is sampled, a train of short pulses is produced, each representing the amplitude of the waveform at the specific instant of sampling. This process is called Pulse Amplitude Modulation (PAM). The envelope of the PAM samples replicate the original waveform. Figures 1A thru 1D illustrate representative PAM samples for up to 24(30) individual voice channels in a μ-Law (A-Law) telephone system.

There are relatively large intervals between each PAM sample that may be used for transmitting PAM samples from other voice channels. Interleaving several voice channels on a common bus is the fundamental principle of Time Division Multiplexing (TDM). As the number of voice channels on the TDM bus increases, the time alloted to each sample is reduced, and bandwidth requirements increase (See Figure 1E).

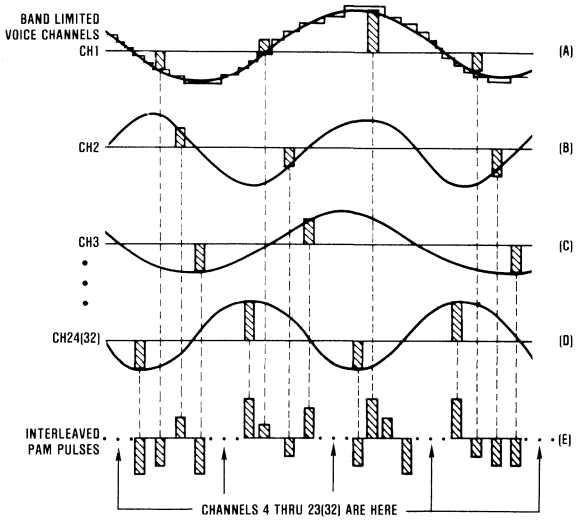


FIGURE 1 (A THROUGH E).

3.0 Quantizing

The PAM samples still represent the voice signal in analog form. For digital transmission, further processing is required. Pulse Code Modulation (PCM) is a technique used to convert the PAM samples to a binary weighted code for digital transmission. PCM coding is a two step process performed by the CODEC. The first step is quantization, where each sample is assigned a specific quantizing interval. The second step is PCM coding of the quantizing interval into an 8 bit PCM code word. Each is discussed in the text that follows.

Converting PAM samples to a digital signal involves assigning the amplitude of a PAM sample one of a whole range of possible amplitude values, which are divided into quantizing intervals. There are 256 possible quantizing intervals, 128 positive and 128 negative. The boundaries between adjacent quantizing intervals are called decision values.

If PAM samples are uniformly quantized, there will be situations where several different amplitude values will be assigned the same quantizing interval during encoding. Then, during decoding, one signal amplitude value is recovered for each quantizing interval which corresponds to the midpoint of the quantizing interval. This results in small discrepencies that occur between the original waveform and the quantized approximation; i.e., infinite analog levels in the original waveform being assigned finite quantizing intervals. These discrepancies result in a quantizing noise or quantizing distortion, the magnitude of which is inversely proportional to the number of discrete quantizing intervals. These noise signals may be of the same order of magnitude as the input signal, thereby reducing the signal to quantizing noise ratio to an intolerable level. For this reason non-uniform quantization is used. Large signals need a smaller number of quantizing intervals, while small signals require a larger number of quantizing intervals. Such a non-uniform quantization process is defined as companding characteristics by both Bell and CCITT.

The PCM CODEC performs this non-uniform or non-linear quantization through μ-Law or A-law companding characteristics shown in Figure 2. This process enhances lower amplitude signals, to allow them to compete with system noise, and attenuates higher amplitude signals, preventing them from saturating the system. This form of signal compression results in a relatively uniform signal to quantization noise ratio, approaching 40dB for a wide range of input amplitudes. Also, the dynamic range approaches that of a 13(11) bit A/D or 80(66)dB for μ-Law (A-Law) companding. The digital realization of this companding process is obtained by a segment and chord piecewise linear approximation to a semi-logarithmic function.

Both the μ-Law and A-law companding characteristics are composed of 8 linear segments or chords in each quadrant. Within each chord are 16 uniform quantization intervals, or steps. With μ-Law, moving away from the origin, each chord is twice the width of the preceding chord, and each group of 16 uniform steps is twice the width of the preceding group. It is also referred to as the 15 segment characteristic . The first chord about the origin in the positive and the negative quadrant are of the same slope and are therefore considered one chord (chord 0). With A-law, the first two chords and step groups in each quadrant are uniform. Successive chords and steps follow the same pattern as μ-Law. A-Law is referred to as the 13 segment characteristic. The first two chords about the origin in the positive quadrant, and the first two chords about the origin in the negative quadrant are all of the same slope and therefore are considered one chord (chord 1). There are 64 uniform steps in chord 1, 32 positive and 32 negative. However, for purposes of encoding and decoding samples that fall into the quantization intervals in chord 1, a different 3 bit chord code (refer to Figure 3) is assigned for the first segment of 16 uniform steps closest to the origin and the next segment moving away from the origin. Chord 1 in A-Law is twice that of chord 0 in μ-Law.

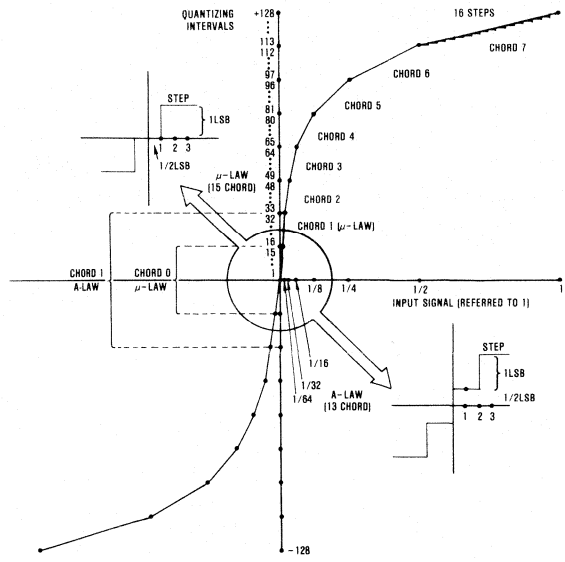


FIGURE 2.

The μ-Law companding characteristic is used primarily in North America and Japan, while A-Law is used primarily in Europe. The differences are minimal and are summarized below:

μ-Law

- Step sizes double for each successive chord
- Virtual edge = +/-8159 units
- Input level = 3.172dBm0
- 2 codes for 0 input

A-Law

- Step sizes double for each successive chord after the second chord
- Virtual edge = +/-4096 units
- Input level = 3.14dbm0
- No code for 0 input

The input level is determined with reference to the power level at the central office or 'switch'. That point is referred to as the zero transmission level point (0TLP). All CODEC measurements must be translated to the 0TLP. The unit of translated level is the dBm0 (dB relative to 1mW referred to a transmission level of 0TLP).

There is no absolute voltage standard for the CODEC, however, a standard exists relative to full scale. The point at which the CODEC begins to clip is called the virtual edge. It is measured in normalized voltage units or steps, +/-8159 steps for μ-Law and +/-4096 steps for A-Law. If a PAM sample representing the peak of a voice input signal hits the virtual edge of a μ-Law system, it has a relative power of +3.172dBm0. The corresponding A-Law relative power is +3.14dBm0. These numbers are chosen to minimize intrinsic gain error at 0dBm0 and 1000Hz.

4.0 Encoding

The second stage of conversion to binary PCM data for transmission involves the coding of the 256 quantizing intervals assigned to the individual PAM samples into 8 bit binary words (7 data bits plus 1 sign bit). The MSB in each word is a polarity bit indicating a 1 for positive quadrant quantizing intervals, and a 0 for negative quadrant quantizing intervals. The next three bits represent the chord, and the last four bits identify the step within the chord. The 8 bit PCM word partitioning is illustrated in Figure 3.

BIT NUMBER	1	2	3	4	5	6	7	8	
BIT WEIGHT-MSB	+/-	2^6	2^5	2^4	2^3	2^2	2^1	2^0	LSB
	SIGN	CHORD			STEP				

FIGURE 3.

A-Law and μ-Law coding about the origin differ. μ-Law defines two codes for 0V input while A-Law defines no code for 0V input (see Figure 4). The two μ-Law zero codes represent a normal quantization step that is divided into halves by the y-axis of the companding curve (refer to Figure 2). These half steps represent the lowest resolvable signal of the μ-Law characteristic.

INPUT	BINARY EQUIV.	μ-LAW	A-LAW
+FULL SCALE	1111 1111	1000 0000	1010 1010
+CENTER	1000 0000	1111 1111	1101 0101
-CENTER	0000 0000	0111 1111	0101 0101
-FULL SCALE	0111 1111	0000 0000	0010 1010

FIGURE 4.

5.0 Multiplexing and Transmission

Each 8 bit PCM word is transmitted in its respective time slot, which is assigned to each CODEC by the system controller (See App. Note 570). A number of PCM words may be transmitted consecutively from different channels, creating a PCM TDM signal for transmission. Each CODEC channel has an average data rate of 8K samples/sec x 8 bits = 64kbits/s. This means that within a 1/8kHz = 125μs period, 24(30) PCM words of 8 bits each are transmitted consecutively in a μ-Law (A-Law) system.

5.1 μ-Law Systems

For μ-Law systems, the bus format allows 24 groups, or timeslots, of 8 bit PCM words, plus one synchronization (sync) bit for a total of 193 bits per frame (see Figure 5). This sync bit partitions the boundary between timeslots 24 and 1, and allows the time slot counter at the receive end to maintain sync with the transmit end. All signalling information is contained in bit 8 (LSB) of the PCM word. These multiplexed frames of 24, 193 bit channels constitute the 1.544MHz T1 transmission channel.

5.2 A-Law Systems

For A-Law systems, the bus format groups data into 32 timeslots of 8 bit PCM words each, giving 30 voice channels plus one 8 bit sync and alarm channel, and one 8 bit signalling channel. The sync and alarm, and signalling information are contained in channels 0 and 16, respectively (see Figure 5). Bits 2, 4, 6, and 8 are inverted for transmission per CCITT recomendation. These multiplexed frames of 32, 256 bit channels constitute the 2.048MHz PCM30-CEPT (Committee of European Postal and Telegraph) transmission channel.

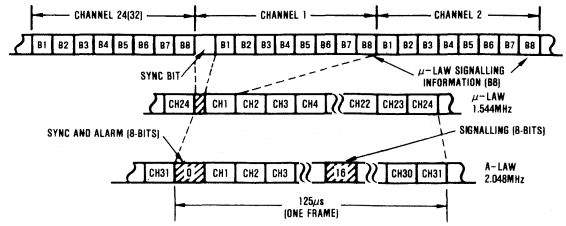


FIGURE 5.

6.0 Line Coding

PCM code generated by the CODEC function is in Non-Return to Zero (NRZ) format. It cannot effectively be transmitted directly on a transmission line because the signal contains a DC component and lacks timing information.

An additional coding step is necessary which converts NRZ code to a pseudo ternary code suitable for transmission. Practical coding schemes include Alternate Mark Inversion (AMI), Bipolar with N Zero Substitution (BNZS), and High Density Bipolar 3 (HDB3) coding. These schemes eliminate the dc component of NRZ code, thereby eliminating the troublesome dc wander phenomenon. They also provide a means for detecting line coding errors, and enhance synchronization between transmitter and receiver through reduction of timing jitter. For additional information, refer to Application Note 573, "The HC-5560 Transcoder", by D. J. Donovan.

7.0 Demultiplexing

After transmission, the CODEC must recover the 8 bit PCM words from the TDM signal, sort out, decode, and distribute the PCM information appropriately. The demultiplexing process is fully controlled electronically.

8.0 Decoding

The CODEC receive function allocates a signal amplitude to each 8 bit PCM word which corresponds to the midpoint of the particular quantizing interval. The expanding characteristic is the same as that for non-linear companding on the transmit side. If the LSB of a μ-Law PCM word contains signalling information, it is extracted by the CODEC, latched into a flip-flop, and distributed to the CODEC signalling output (Sig_R). This means that there is a lost bit (LSB) in the incoming PCM data stream during a signalling frame. The decoder interprets the missing LSB as a 1/2 (i.e. halfway between a 0 and a 1) to minimize noise and distortion. The PCM words are decoded in the order in which they are received and then converted to PAM pulses. The PAM pulses are summed, then low pass filtered, which smoothes the PAM envelope and reproduces the original voice signal.

HC-5512 PCM FILTER CLEANS UP CVSD CODEC SIGNALS

P. G. Phillips and D. J. Donovan

The HC-5512 is a CMOS switched capacitor PCM Filter originally designed for use with the PCM CODEC to filter transmit and receive audio signals. It can also be used as an input/output filter for the HC-55564 CVSD. This offers the designer extremely high quality filter characteristics for a minimum componet count and system cost.

The HC-5512 Filter is manufactured using double-poly silicon gate CMOS technology. Switched capacitor integrators are used to simulate LC ladder filters with low component sensitivity. The IC contains two switched capacitor filters. The transmit filter is a fifth order elliptic low pass filter cascaded with a fourth order Chebyshev high pass filter. It has a flat band pass response and rejects signals of frequencies less than 200Hz and greater than 3.4kHz. The receive filter is a fifth order elliptic low pass filter with SINX/X compensation. The response of this filter can be tailored for CVSD use with an external RC network to flatten the SINX/X correction characteristic.

The HC-55564 is a half duplex modulator/demodulator CMOS integrated circuit used to convert voice signals into serial NRZ digital data and reconvert that data into voice. Continuously Variable Slope Deltamodulation (CVSD) is the method of conversion. As in any sampling system, the reconstituted signal contains noise due to switching. In addition, to prevent alias distortion, the input signal must be filtered to remove frequencies above one-half the sampling frequency. In order to minimize these unwanted noise frequencies, and to pre-condition the input signal, it is necessary to filter the input and the decoded output of the CVSD.

The transmit and receive filter responses are shown in Figures 1A and 1B. The transfer characteristic of the CVSD is illustrated in Figure 2. A suggested circuit configuration is shown in Figure 3.

The HC-5512 filter is configured such that it utilizes a 2.048MHz clock for the switched capacitors. A 16kHz or 32kHz sampling clock for the CVSD is easily derived as shown in Figure 3. A 32kHz sampling clock is recommended to enhance noise performance, frequency response, and dynamic range of the CVSD. For the circuit as shown the audio signal into the CVSD should be 1Vp-p over the 3.2kHz band to obtain a flat response. As can be seen from Figure 2, for lower frequency signals, higher signal levels can be used. However, an external compensation network is required to flatten the inherent SINX/X output response of the receive filter stage (see Figure 1B). R_A, R_B and C_A form a simple lead lag filter at the output of the receive filter in the HC-5512 . This introduces a pole at 1kHz and a zero at 3.3kHz in order to give some degree of compensation against the filter's SINX/X characteristics.

Transmit Filter Stage

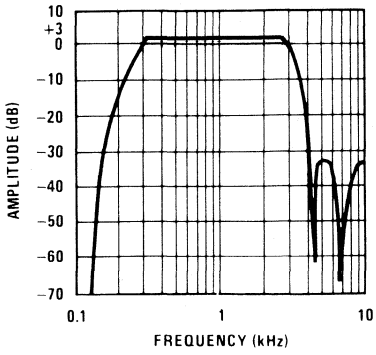


FIGURE 1A. TRANSMIT FILTER STAGE

Receive Filter Stage

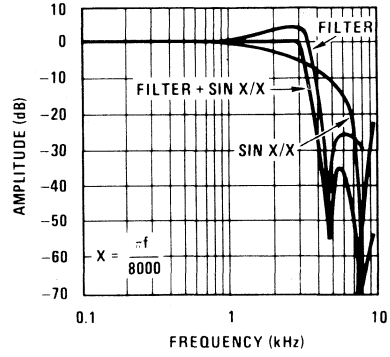


FIGURE 1B. RECEIVE FILTER STAGE

The CVSD is AC coupled to the filter since the audio in/out ports of the CVSD are DC biased at $V_{DD}/2$. (In fact, audio can be directly coupled to V_{FRI} if desired.) It is often necessary to provide a side tone back to the user headset so the speaker may hear his own voice, thus preventing a dead feeling in the instrument. The side tone is provided at the audio out pin of the CVSD during the encode operation and is of the same amplitude as the input signal, transfer gain excepted.

The CVSD has an Automatic Gain Control (AGC) output. The signal present is a digital output whose duty cycle is proportional to the average input audio level. The signal may be integrated to provide feedback information to an AGC amplifier or a voice level indicator.

The Force Zero (FZ) input to the CVSD is used to reset all the internal counters at the start of an encode or decode cycle to prevent momentary overload. It will also recover the part from a latch-up condition. Cycling FZ during power-up sequencing is recommended. A suggested power-up reset circuit is shown in Figure 3 on the FZ control line. During the time FZ is active (low), an alternating 1,0 quieting pattern appears at the NRZ output which is at half the sampling clock rate, and is decoded inaudible. The quieting pattern may also be generated by activating the Alternate Plain Text (APT) input (low), or by removing the signal from the audio input pin.

Additional information on CVSD is contained in Application Note 607.

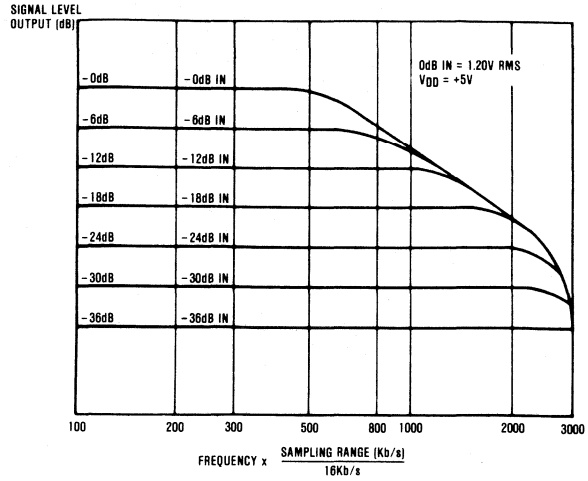


FIGURE 2. TRANSFER FUNCTION FOR CVSD AT 16KB

Illustrates the frequency response of the HC-55564 for varying input levels. To prevent slope overload (slew rate limiting) do not exceed the 0dB boundary. The frequency response is directly proportional to the sampling rate. The output levels were measured after filtering.

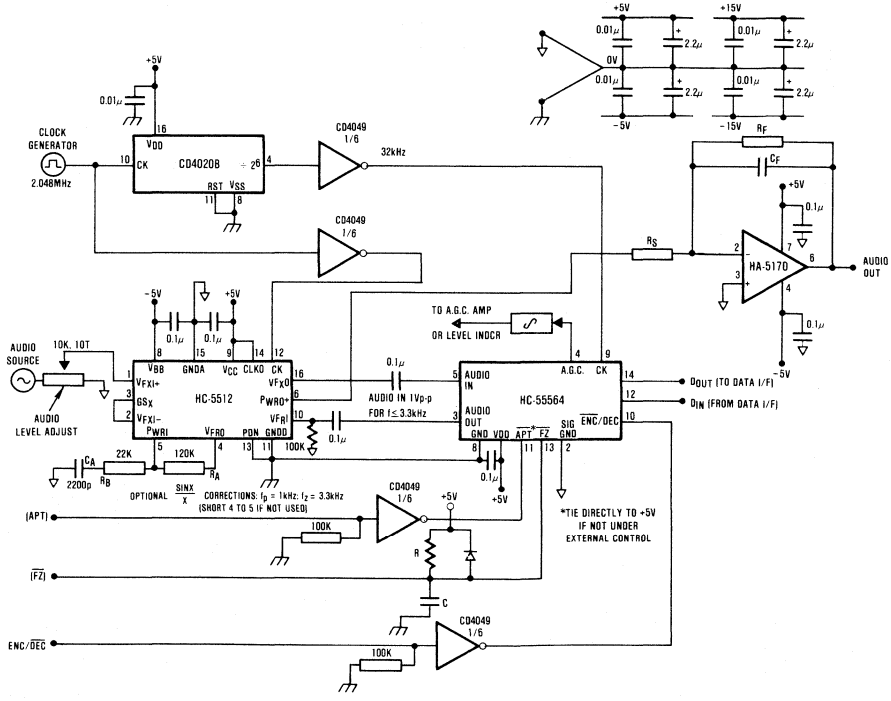


FIGURE 3. SUGGESTED CVSD-PCM FILTER INTERFACE

DELTA MODULATION FOR VOICE TRANSMISSION

By Don Jones

Introduction To Deltamod

Delta modulation has evolved into a simple, efficient method of digitizing voice for secure, reliable communications and for voice I/O in data processing.

To illustrate basic principles, a very simple delta modulator and demodulator are illustrated in Figure 1. The modulator is a sampled data system employing a negative feedback loop. A comparator senses whether or not the instantaneous level of the analog voice input is greater or less than the feedback signal. The comparator output is clocked by a flip-flop to form a continuous NRZ digital data stream. This digital data is also integrated and fed back to the comparator. The feedback system is such that the integrator ramps up and down to produce a rough approximation of the input waveform. An identical integrator in the demodulator produces the same waveform, which when filtered, reproduces the voice.

One can see that the digital data 0's and 1's are commands to the integrators to "go up" or "go down" respectively. Another way of looking at it is that the digital data stream also has analog significance; it approximates the differential of the voice, since analog integration of the data reproduces the voice.

Note that the integrator output never stands still; it always travels either up or down by a fixed amount in any clock period. Because of its fixed integrator output slope, the simple delta modulator is less than ideal for encoding human voice which may have a wide dynamic amplitude range.

The integrator cannot track large, high frequency signals with its fixed slope. Fortunately, human speech has statistically smaller amplitudes at higher frequencies, therefore an integrator time constant of about 1 millisecond will satisfactorily reproduce voice in a 3kHz bandwidth.

A more serious limitation is that voice amplitude changes which are less than the height of the integrator ramp during one clock period cannot be resolved. So dynamic range is proportional to clock frequency, and satisfactory range cannot be obtained at desirable low clock rates.

A means of effectively increasing dynamic range is called "companding" (compressing-expanding); where at the modulator, small signals are given higher relative gain, and an inverse characteristic is produced at the demodulator.

The CVSD: A popular effective scheme for companded delta modulation is known as CVSD (continuously variable slope deltamod) shown in Figure 2. Additional digital logic, a second integrator, and an analog multiplier are added to the simple modulator.

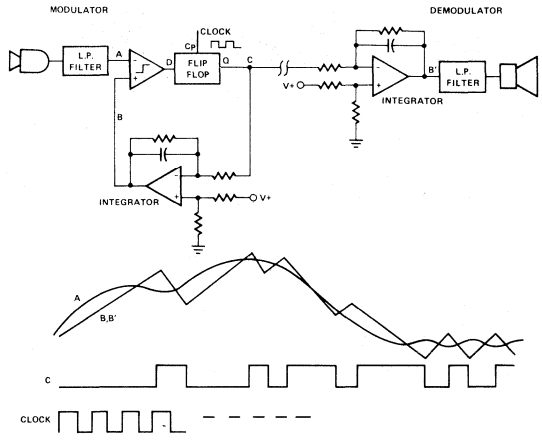
Under small input signal conditions, the second integrator (known as the syllabic filter) has no input, and circuit function is identical to the simple modulator, except that the multiplier is biased to output quite small ramp amplitudes giving good resolution to the small signals.

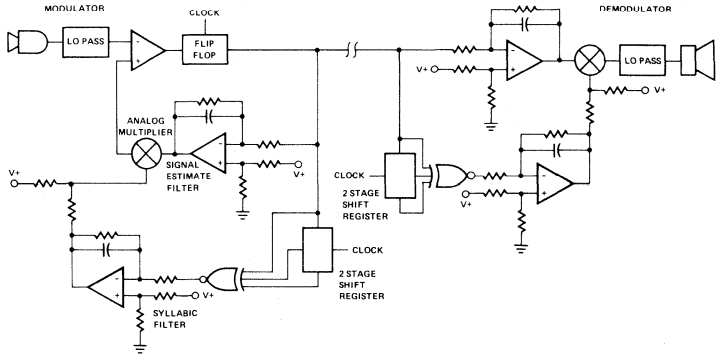
A larger signal input is characterized by consecutive strings of 1's or 0's in the data as the integrator attempts to track the input. The logic input to the syllabic filter actuates whenever 3 or more consecutive 0's or 1's are present in the data. When this happens, the syllabic filter output starts to build up, increasing the multiplier gain, passing larger amplitude ramps to the comparator, enabling the system to track the larger signal. Up to a limit, the more consecutive 1's or 0's generated, the larger the ramp amplitude. Since the larger signals increase the negative feedback of the modulator and the forward gain of the demodulator, companding takes place. By listening tests, the syllabic filter time constant of 4 to 10 milliseconds is generally considered optimum.

An outstanding characteristic of CVSD is its ability, with fairly simple circuitry, to transmit intelligible voice at relatively low data rates. Companded PCM, for telephone quality transmission, requires about 64K bits/sec data rate per channel. CVSD produces equal quality at 32K bits/sec. (However, at this rate it does not handle tone signals or phase encoded modern transmissions as well.)

CVSD is useful at even lower data rates. At 16K bits/sec the reconstructed voice is remarkably natural, but has a slightly "Fuzzy Edge". At 9.6K bits/sec intelligibility is still excellent, although the sound

is reminiscent of a damaged loudspeaker. Of course, very sophisticated speech compression techniques have been used to transmit speech at even lower data rates; but CVSD is an excellent compromise between circuit simplicity and bandwidth economy.





The Digital CVSD

Delta modulated data is in a form which can be digitally filtered with fairly simple circuitry. A compatible CVSD can be made using digital integrators and multipliers driving a digital-to-analog converter. The block diagram of the Harris HC-55564 monolithic CVSD is shown in Figure 3.

The CMOS digital circuit functions of Figure 3 closely parallel the equivalent analog function in Figure 2. The filters are single pole recursive types using shift registers with feedback. A digital multiplier feeds a 10 bit R-2R DAC which reconstructs the voice waveform. The DAC output is in steps, rather than ramps.

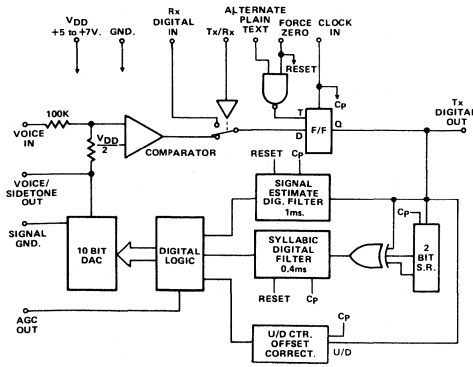


Figure 3 – HC-55564 CVSD Functional Diagram

The digital CVSD has a number of advantages over its analog counterpart, and has desirable features which would otherwise require additional circuitry:

1) The all CMOS device requires only 1mA current from a single +4.5V to +7V supply.

2) No bulky external precision resistors or capacitors are required for the integrators; time constants of the digital filters are set by the clock frequency and do not drift with time or temperature.

3) For best intelligibility and freedom from listener fatigue, it is important that the recovered audio is quiet during the pauses between spoken words. During quiet periods, an alternate "1", "0" pattern should be encoded, which when decoded and filtered will be inaudible. Achieving this in the analog CVSD requires that up and down ramp slopes are precisely equal and that offsets in the comparator and amplifiers are adjusted to zero. Improper adjustment or excessive component drift can result in noisy oscillations. In the digital design, comparator offset and drift are adjusted by a long up-down counter summed to the DAC to insure that over a period of time equal numbers of 1's and 0's are generated.

   An added feature is automatic quieting, where if the DAC input would be less than 2 LSB's the quieting pattern is generated instead. This has proven to aid intelligibility.

4) To prevent momentary overload when beginning to encode or decode, it is desirable to initialize the integrators. In the analog CVSD, external analog switches would be required to discharge the capacitors.

   In the digital CVSD, the filters are reset by momentarily putting the "Force Zero" pin low. At the same time, a quieting pattern is generated without affecting internal encoding by putting the "Alternate Plain Text" pin low.

5) In some analog CVSD designs, transient noise will be generated during recovery from a low frequency overdriven input condition. The digital CVSD has a clipped output with instant recovery, when overdriven.

6) Half-duplex operation (using the same device, switching between the encode and decode functions) requires external circuits with the analog CVSD, while the digital type is switched internally by a logic input.

Applications Of Delta Modulation

1) **Telecommunications:** Digitized signals are easily routed and multiplexed with low cost digital gates. Voice channels may be easily added to existing multiplexed digital data transmission systems. The digital signals are much more immune to crosstalk and noise when transmitted over long distances by wire, R.F., or optical paths. CVSD has better intelligibility than PCM when random bit errors are introduced during transmission.

2) **Secure Communications:** Digital data can be quite securely encrypted using fairly simple standard hardware (Figure 4a). Scrambled speech for audio channels may also be accomplished by encoding into a shift register, then selecting different segments of the shifted data in pseudo-random fashion and decoding it (Figure 4b).

3) **Audio Delay Lines:** Although charge-coupled deviced (CCD) will perform this function, they are still expensive and choice of configurations is quite limited. Also, there is a practical limit to the number of CCD stages, since each introduces a slight degradation to the signal.

   As shown in Figure 5, the delay line consists of a CVSD modulator, a shift register and a demodulator. Delay is proportional to the number of register stages divided by the clock frequency. This can be used in speech scrambling, as explained above, echo supression in PA systems; special echo effects; music enhancement or synthesis; and recursive or nonrecursive filtering.

4) **Voice I/O:** Digitized speech can be entered into a computer for storage, voice identification, or word recognition. Words stored in ROM's, disc memory, etc. can be used for voice output. CVSD, since it can operate at low data rates, is more efficient in storage requirements than PCM or other A to D conversions. Also, the data is in a useful form for filtering or other processing.

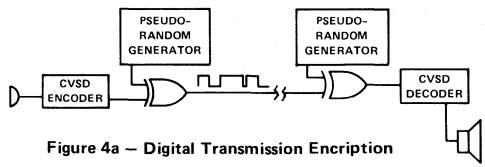


Figure 4a – Digital Transmission Encription

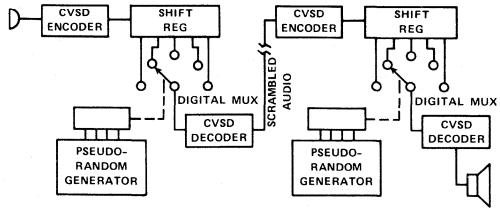


Figure 4b – Voice Transmission Scrambling

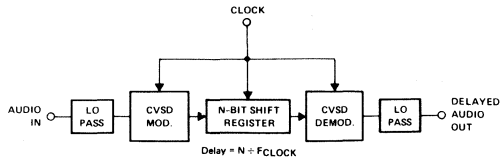


Figure 5 – Audio Delay Line

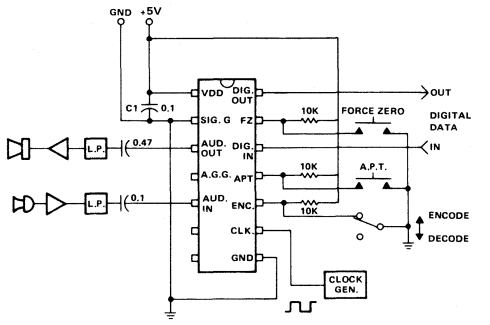


Figure 6 – CVSD Hookup for Evaluation

Figure 6 illustrates a simple evaluation breadboard circuit for the HC-55564. A single device is sufficient to evaluate sound quality, etc. since, when encoding, the feedback signal at pin 3 is identical to the decoded signal from a receiver. The following are some pointers for using the devices:

1) Power supply decoupling is essential with the capacitor (C1 in Figure 6) located close to the I.C.

2) Power to the I.C. must be present before the audio input, the clock, or other digital inputs are applied. Failure to observe this may result in a latchup condition, which is usually not destructive and may be removed by cycling the supply off, then on.

3) Signal ground (pin 2) should be externally connected to pin 8 and power ground. It is recommended for noise-free operation that the audio input and output ground returns connect directly to pin 2 and to no other grounds in the system. Pins 6 and 7 must be open circuited.

4) Digital inputs and outputs are similar to and compatible with standard CMOS logic circuits using the same supply voltage. The illustrated 10K pullup resistors are necessary only with mechanical switches, and are not necessary when driving these pins with CMOS. Unused digital inputs should be tied to the appropriate supply rail for the desired operation. TTL output, however, will require pullup resistors (about 1K) to obtain the required CMOS input levels. Pins 4 and 14 will drive CMOS logic, or each can drive one low power TTL input.

5) Capacitor coupling is recommended for the audio in and out (pins 3 and 5) as each pin is internally biased to about 1/2 the supply voltage.

6) The AGC output (pin 4) is a digital output, whose duty cycle is dependent on the average audio level. This may be externally integrated to drive an AGC preamplifier; or it could be used (through a buffer gate) to drive an LED indicator to indicate proper speaking volume.

7) To prevent generation of alias frequencies, the input filter should reduce the audio amplitude at frequencies greater than half the clock rate to less than 12 millivolts peak-to-peak.

8) The PCM Filter shown in the data sheet lends itself well as a cost-effective input/output filter to the CVSD.

9) A suggested receiver clock circuit is a free running multivibrator, synchronized at each transition of the incoming data. Any synch errors occurring during reception of long strings of zeros or ones will have negligible effect on the decoded voice.

Figures 7 though 11 illustrate some typical audio output (before filtering) and digital output waveforms. To make the scope picture stationary, the audio input generator was synchronized with a submultiple of the clock frequency.

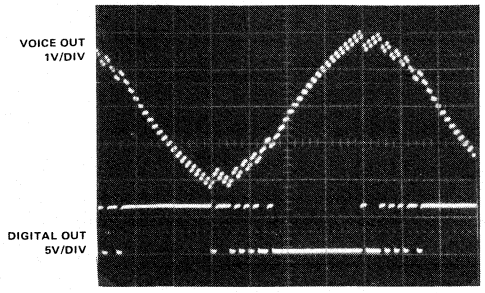
Figure 7 shows the results of a large low frequency sine wave. The somewhat jagged peaks are typical of all CVSD systems. Note that the digital output is continuous "ones" while the waveform is slewing down and continuous "zeros" while slewing up.

Figure 8 shows the excellent recovery from overdriven conditions at low frequency. Some analog type CVSD's have trouble recovering from this condition.

As mentioned previously, CVSD's cannot handle large signals at high frequencies (but these are not generally present in the human voice). Figure 9 shows this limitation where the voice output is slewing at its maximum rate, but cannot catch up with the input. At reduced amplitudes, however, the same signal can be reproduced, as shown in Figure 10.

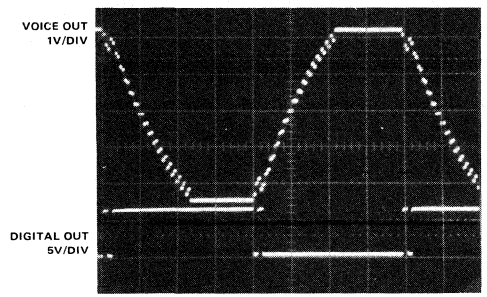
The transfer function curve on the data sheet shows that at 16kHz clock rate, a 1.2V RMS signal can be tracked up to 500Hz. With a 32kHz clock, the same curves may be used, but with each of the indicated frequencies doubled. Likewise, each of the SNR figures shown on the data sheet will be 6dB better with a 32kHz clock.

Figure 11 shows the 10 millivolt voice output waveform at 1/2 the clock rate, when there is no audio input. After filtering, this signal is inaudible.



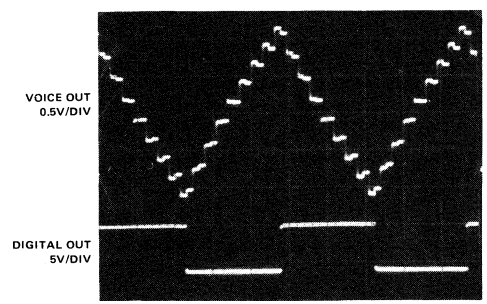
0.5ms/DIV.
VOICE IN = 250Hz, 4V P-P SINE WAVE
CLOCK = 16kHz

Figure 7 – CVSD Large Signal Sine Wave Reconstruction



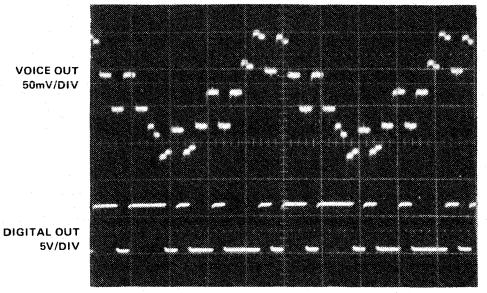
0.5ms/DIV.
VOICE IN = 250Hz, 6V P-P SINE WAVE
CLOCK = 16kHz

Figure 8 – CVSD Large Signal, Low Frequency Clipped Waveform



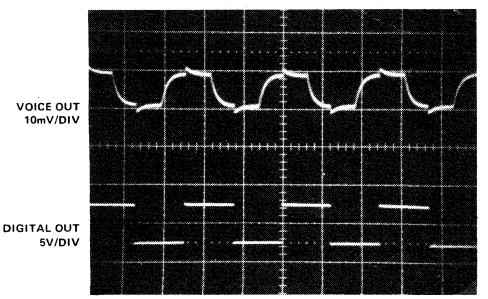
0.2ms/DIV.
VOICE IN = 1kHz, 6V P-P SINE WAVE
CLOCK = 16kHz

Figure 9 – CVSD Large Signal, High Frequency Slew Limiting



VOICE IN = 1kHz, 0.15V P-P SINE WAVE
CLOCK = 16kHz

Figure 10 – CVSD Small Signal Sine Wave Reconstruction



50 μs/DIV.
VOICE IN = 0
CLOCK = 16kHz

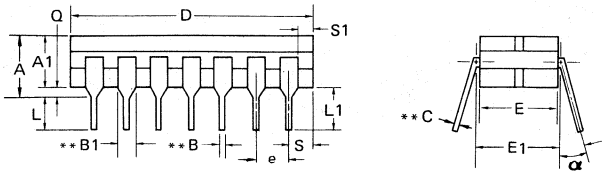
Figure 11 – CVSD Zero Signal Idle Pattern

ANALOG

Packaging 11

Package Configuration

A B C D E .300 CERAMIC DUAL-IN-LINE



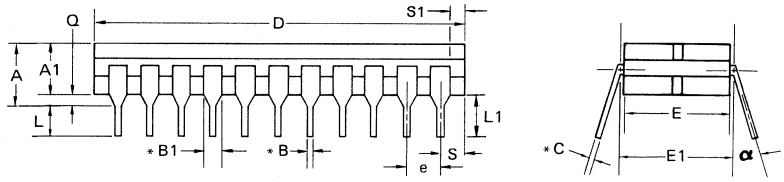
PKG. CODE	LEAD COUNT	DIM. A	DIM. A1	DIM. B	DIM. B1	DIM. C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. L1	DIM. S	DIM. S1	DIM. Q	DIM. α
A	8 / SSI	— / .200	.140 / .160	.016 / .023	.050 / .065	.008 / .015	.375 / .395	.245 / .265	.290 / .310	.100 / BSC	.125 / .150	.150 / —	— / .055	.005 / —	.015 / .060	0° / 15°
B1	14 / MSI	— / .200	.140 / .170	.016 / .023	.050 / .065	.008 / .015	.753 / .785	.265 / .285	.290 / .310	.100 / BSC	.125 / .180	.150 / —	— / .098	.005 / —	.015 / .060	0° / 15°
B2	14 / LSI	— / .200	.140 / .170	.016 / .023	.050 / .065	.008 / .015	.753 / .785	.285 / .305	.300 / .320	.100 / BSC	.125 / .180	.150 / —	— / .098	.005 / —	.015 / .060	0° / 15°
C1	16* / MSI	— / .200	.140 / .170	.016 / .023	.050* / .065*	.008 / .015	.753 / .785	.265 / .285	.290 / .310	.100 / BSC	.125 / .180	.150 / —	— / .080	.005 / —	.015 / .060	0° / 15°
C2	16* / LSI	— / .200	.140 / .170	.016 / .023	.050* / .065*	.008 / .015	.753 / .785	.285 / .305	.300 / .320	.100 / BSC	.125 / .180	.150 / —	— / .080	.005 / —	.015 / .060	0° / 15°
D	18 / LSI	— / .200	.140 / .170	.016 / .023	.050* / .065*	.008 / .015	.882 / .915	.285 / .305	.300 / .320	.100 / BSC	.125 / .180	.150 / —	— / .098	.005 / —	.015 / .060	0° / 15°
E	20 / LSI	— / .200	.140 / .170	.016 / .023	.050* / .065*	.008 / .015	.940 / .970	.285 / .305	.300 / .320	.100 / BSC	.125 / .180	.150 / —	— / .080	.005 / —	.015 / .060	0° / 15°

* End leads are half leads where B remains the same and B1 is $\frac{0.035}{0.045}$

** Solder dip finish add +0.003 inches

F .400 CERAMIC DUAL-IN-LINE

G H .600 CERAMIC DUAL-IN-LINE



PKG. CODE	LEAD COUNT	DIM. A	DIM. A1	DIM. B	DIM. B1	DIM. C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. L1	DIM. S	DIM. S1	DIM. Q	DIM. α
F .400	22 / LSI	— / .225	.150 / .180	.016 / .023	.050 / .065	.008 / .015	1.055 / 1.085	.375 / .395	.395 / .415	.100 / BSC	.125 / .180	.150 / —	— / .080	.005 / —	.015 / .060	0° / 15°
G .600	24 / LSI	— / .225	.150 / .180	.016 / .023	.050 / .065	.008 / .015	1.24 / 1.27	.515 / .535	.595 / .615	.100 / BSC	.125 / .180	.150 / —	— / .098	.005 / —	.015 / .060	0° / 15°
H .600	28 / LSI	— / .225	.160 / .190	.016 / .023	.050 / .065	.008 / .015	1.44 / 1.47	.515 / .535	.595 / .615	.100 / BSC	.125 / .180	.150 / —	— / .098	.005 / —	.015 / .060	0° / 15°

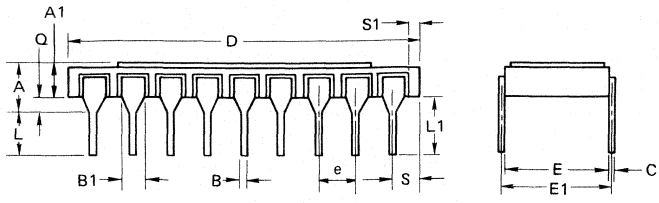
* Solder dip finish add +0.003 inches.

NOTE: Dimensions are $\frac{\text{Min}}{\text{Max}}$. Dimensions are in inches.

BSC means basic spacing between centerlines.

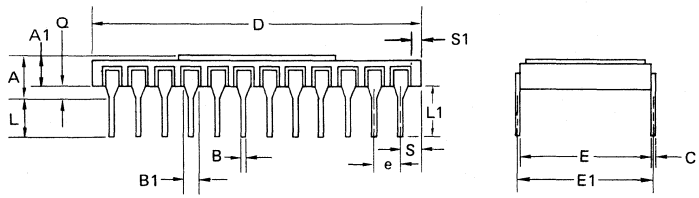
Package Configuration

I .300 SIDEBRAZE DUAL-IN-LINE



PKG. CODE	LEAD COUNT	DIM. A	DIM. A1	DIM. B	DIM. B1	DIM. C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. L1	DIM. S	DIM. S1	DIM. Q
I	18	— .200	.080 .110	.016 .023	.045 .060	.008 .015	.890 .910	.280 .300	.290 .310	.100 BSC	.125 .180	.150 —	— .098	.005 —	.025 .045

J K L .600 SIDEBRAZE DUAL-IN-LINE

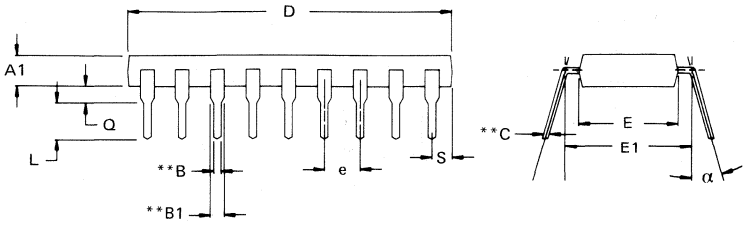


PKG. CODE	LEAD COUNT	DIM. A	DIM. A1	DIM. B	DIM. B1	DIM. C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. L1	DIM. S	DIM. S1	DIM. Q
J	24	— .225	.080 .110	.016 .023	.040 .054	.008 .015	1.185 1.215	.587 .603	.598 .612	.100 BSC	.125 .180	.150 —	— .080	.005 —	.040 .060
K	28	— .225	.080 .110	.016 .023	.040 .054	.008 .015	1.385 1.415	.587 .603	.598 .612	.100 BSC	.125 .180	.150 —	— .080	.005 —	.030 .060
L	40	— .225	.080 .110	.016 .023	.040 .054	.008 .015	1.980 2.020	.587 .603	.598 .612	.100 BSC	.125 .180	.150 —	— .080	.005 —	.040 .060

NOTE: Dimensions are $\frac{\text{Min}}{\text{Max}}$. Dimensions are in inches. BSC means basic spacing between centerlines.

Package Configuration

M N O P Q .300 PLASTIC DUAL-IN-LINE

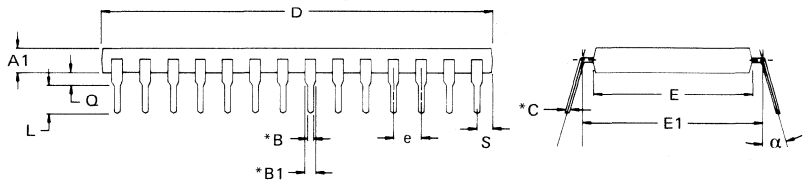


PKG. CODE	LEAD COUNT	DIM. A1	DIM. B	DIM. B1	DIM. C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. S	DIM. Q	DIM. α
M	8	.125/.140	.016/.023	.050/.070	.008/.015	.370/.390	.245/.265	.290/.310	.090/.110	.110/.150	.030/.050	.020/.040	0°/15°
N	14	.125/.140	.016/.023	.050/.070	.008/.015	.750/.770	.245/.265	.290/.310	.090/.110	.110/.150	.030/.050	.020/.040	0°/15°
O	16*	.125/.140	.016/.023	.050/.070	.008/.015	.750/.770	.245/.265	.290/.310	.090/.110	.110/.150	.025/.035	.020/.040	0°/15°
P	18	.125/.140	.016/.023	.050/.070	.008/.015	.900/.920	.245/.265	.290/.310	.090/.110	.110/.150	.040/.060	.020/.040	0°/15°
Q	20	.130/.145	.016/.023	.050/.070	.008/.015	1.030/1.050	.250/.270	.290/.310	.090/.110	.110/.150	.060/.080	.020/.040	0°/15°

* End leads are half leads where B remains the same and B1 is $\frac{0.035}{0.045}$

** Solder dip finish add 0.003 inches.

R S .600 PLASTIC DUAL-IN-LINE



PKG. CODE	LEAD COUNT	DIM. A1	DIM. B	DIM. B1	DIM. C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. S	DIM. Q	DIM. α
R	24	.145/.155	.016/.023	.050/.070	.008/.015	1.24/1.26	.540/.560	.590/.610	.090/.110	.110/.150	.045/.095	.020/.040	0°/15°
S	28	.145/.155	.016/.023	.050/.070	.008/.015	1.54/1.57	.540/.560	.590/.610	.090/.110	.110/.150	.110/.160	.020/.040	0°/15°

* Solder dip finish add 0.003 inches.

NOTE: Dimensions are $\frac{\text{Min}}{\text{Max}}$. Dimensions are in inches.

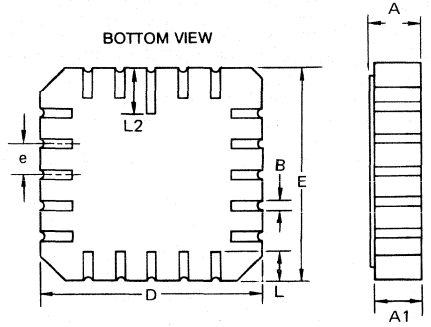
BSC means basic spacing between centerlines.

Package Configuration

T .350 CERAMIC LEADLESS CHIP CARRIER*

U .450 CERAMIC LEADLESS CHIP CARRIER*

V .650 CERAMIC LEADLESS CHIP CARRIER*

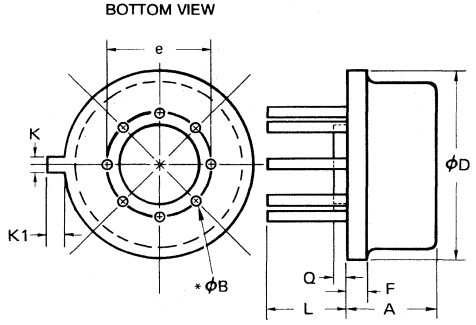


PKG. CODE	LEAD COUNT	DIM. A	DIM. A1	DIM. B	DIM. D	DIM. E	DIM. e	DIM. L	DIM. L2
T	20 .350 SQ	.073 .089	.063 .077	.022 .028	.342 .358	.342 .358	.050 BSC	.045 .055	.075 .095
U	28 .450 SQ	.074 .088	.064 .076	.022 .028	.442 .458	.442 .458	.050 BSC	.045 .055	.075 .095
V	44 .650 SQ	.073 .089	.063 .077	.022 .028	.643 .662	.643 .662	.050 BSC	.045 .055	.075 .095

* Solder dip finish for military parts conform to MIL-M-38510, Type A.

W TO-99 METAL CAN

X TO-100 METAL CAN



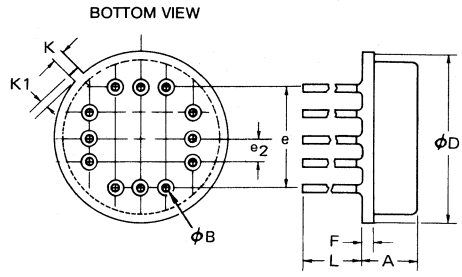
PKG. CODE	LEAD COUNT	DIM. A	DIM. ϕB	DIM. ϕD	DIM. e	DIM. F	DIM. K	DIM. K1	DIM. L	DIM. Q
W	8 TO-99	.165 .185	.016 .018	.345 .365	.190 .210	.020 .040	.028 .034	.028 .040	.505 .550	.015 .040
X	10 TO-100	.165 .185	.016 .018	.345 .365	.220 .240	.020 .040	.028 .034	.028 .040	.505 .550	.015 .040

* Solder dip finish add +0.003 inches.

NOTE: Dimensions are $\frac{\text{Min}}{\text{Max}}$. Dimensions are in inches. BSC means basic spacing between centerlines.

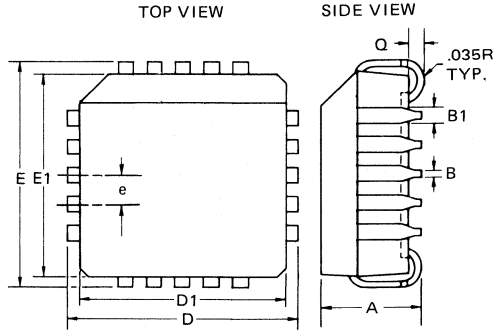
Package Configuration

Y TO-8 METAL CAN



PKG. CODE	LEAD COUNT	DIM. A	DIM. ϕB	DIM. ϕD	DIM. e	DIM. e2	DIM. F	DIM. K	DIM. K1	DIM. L
Y	12 TO-8	.130 / .150	.016 / .021	.585 / .615	.400 BSC	.100 BSC	.020 / .040	.027 / .034	.027 / .045	.500 / .550

AA AB AC PLASTIC LEADED CHIP CARRIER



PKG. CODE	LEAD COUNT	DIM. A	DIM. B	DIM. B1	DIM. D/E	DIM. D1/E1	DIM. e	DIM. Q
AA	20	.165 / .180	.013 / .021	.026 / .032	.385 / .395	.350 / .356	.050 BSC	.020 / —
AB	28	.165 / .180	.013 / .021	.026 / .032	.485 / .495	.450 / .456	.050 BSC	.020 / —
AC	44	.165 / .180	.013 / .021	.026 / .032	.685 / .695	.650 / .656	.050 BSC	.020 / —

NOTE: Dimensions are $\frac{\text{Min}}{\text{Max}}$. Dimensions are in inches. BSC means basic spacing between centerlines.

ANALOG

Appendices

12

CMOS Digital Products

CMOS Microprocessors

80C286	Static 16-Bit Microprocessor
80C86	Static 16-Bit Microprocessor
80C88	Static 8/16-Bit Microprocessor

CMOS Peripherals

82C37A	High Performance Programmable DMA Controller
82C54	Programmable Interval Timer
82C55A	Programmable Peripheral Interface
82C59A	Priority Interrupt Controller
82C82	Octal Latching Bus Driver
82C83H	Octal Latching Inverting Bus Driver
82C84A	Clock Generator Driver
82C85	Static Clock Controller/Generator
82C86H	Octal Bus Transceiver
82C87H	Octal Bus Transceiver (Inverting)
82C88	Bus Controller
82C89	Bus Arbiter

Data Communications

HD-15530	Manchester Encoder-Decoder
HD-15531	Manchester Encoder-Decoder
HD-4702	Programmable Bit Rate Generator
HD-6402	Universal Asynchronous Receiver Transmitter
HD-6406	Programmable Asynchronous Communication Interface
82C50A	Asynchronous Communications Element
82C52	Serial Controller Interval Timer
HD-6408	Asynchronous Serial Manchester Adapter
HD-6409	Manchester Encoder-Decoder

CMOS Memory

HM-6504	4K x 1 Synchronous RAM
HM-6508	1K x 1 Sychronous RAM
HM-6514	1K x 4 Synchronous RAM
HM-6516	2K x 8 Synchronous RAM
HM-65162	2K x 8 Asynchronous RAM
HM-6518	1K x 1 Synchronous RAM
HM-65262	16K x 1 Asynchronous RAM
HM-6551	256 x 4 Synchronous RAM
HM-6561	256 x 4 Synchronous RAM
HM-6564	64K Synchronous RAM Module
HM-65642	8K x 8 Asynchronous RAM
HM-6617	2K x 8 Fuse Link PROM
HM-6642	512 x 8 Fuse Link PROM
HM-8808/08A	8K x 8 Asynchronous RAM Module
HM-8816H	16K 8 Asynchronous RAM Module
HM-8832	32K x 8 Asynchronous RAM Module
HM-92560	256K Synchronous RAM Module
HM-92570	256K Buffered Synchronous RAM Module
HM-91M2	1M-Bit Asynchronous RAM Module

CMOS Programmable Logic

HPL-16LC8	Programmable Logic
HPL-16RC4	Programmable Logic
HPL-16RC6	Programmable Logic
HPL-16RC8	Programmable Logic
HPL-82C339	Programmable Chip Select Decoder (PCSD)
HPL-82C338	Programmable Chip Select Decoder (PCSD)
HPL-82C139	Programmable Chip Select Decoder (PCSD)
HPL-82C138	Programmable Chip Select Decoder (PCSD)

CICD Radiation Hardened Products

Memories

HS-6508RH	1K x 1 CMOS Static RAM (Synchronous)	Rad Hard
HS-6551RH	256 x 4 CMOS Static RAM (Synchronous)	Rad Hard
HS-6504RH	4K x 1 CMOS Static RAM (Synchronous)	Rad Hard
HS-6514RH	1K x 4 CMOS Static RAM (Synchronous)	Rad Hard
HS-65142RH	1K x 4 CMOS Static RAM (Asynchronous)	Rad Hard
HS-65C162RH HS-65T162RH	2K x 8 CMOS Static RAM (Asynchronous)	Rad Hard
HS-65C262RH HS-65T262RH	16K x 1 CMOS Static RAM (Asynchronous)	Rad Hard
HS-6564RH	8K x 8 or 16K x 4 CMOS RAM Module (Synchronous)	Rad Hard
HS-6617RH	2K x 8 CMOS PROM (Synchronous)	Rad Hard
HS-76161RH	2K x 8 Bipolar PROM (Synchronous)	Rad Hard

Quad Power Strobe

HS-6600RH	Quad Power Strobe	Rad Hard

Microprocessor and Peripherals

80C85 8-BIT MICROPROCESSOR FAMILY

HS-80C85RH	8-Bit CMOS Microprocessor	Rad Hard
HS-3374RH	CMOS/TTL Bidirectional Level Shifter	Rad Hard
HS-54C138RH	3-Line to 8-Line CMOS Decoder/Demultiplexer	Rad Hard
HS-81C55/56RH	256 x 8 CMOS RAM with I/O Ports and Timer	Rad Hard
HS-82C08RH	8-Bit CMOS Bus Transceiver	Rad Hard
HS-82C12RH	8-Bit CMOS I/O Port	Rad Hard
HS-83C55RH	2K x 8 CMOS ROM with I/O Ports	Rad Hard

80C86 16-BIT MICROPROCESSOR FAMILY

HS-80C86RH	16-Bit CMOS Microprocessor	Rad Hard
HS-82C37ARH	CMOS Programmable DMA Controller	Rad Hard
HS-85C52RH	CMOS Serial Controller Interface	Rad Hard
HS-82C54RH	CMOS Programmable Interval Timer	Rad Hard
HS-82C55ARH	CMOS Programmable Peripheral Interface	Rad Hard
HS-82C59ARH	CMOS Programmable Interrupt Controller	Rad Hard
HS-82C85RH	CMOS Static Clock Controller/Generator	Rad Hard

Operational Amplifiers, Comparator & Regulator

HS-3516RH	High Slew Rate Wide Band Operational Amplifier	Rad Hard
HS-3530RH	Low Power Programmable Operational Amplifier	Rad Hard
HS-3569RH	Wide Range Dual Programmable Operational Amplifier	Rad Hard
HS-5104RH	Quad Low Noise Operational Amplifier	Rad Hard
HS-3560RH	High Speed Latching Comparator	Rad Hard
HS-3761RH	Regulating Pulse Width Modulator	Rad Hard

Multiplexers and Switches

HS-508ARH	8 Channel CMOS Analog Multiplexer	Rad Hard
HS-1840RH	16 Channel CMOS Analog Multiplexer	Rad Hard
HS-302/303/306/ 307/384/390RH	CMOS Analog Switches	Rad Hard

CICD Radiation Hardened Products

Semicustom

HS-CXXXXRH	CMOS Standard Cell Multiple Technologies	Rad Hard
HS-DXXXXRH	CMOS Standard Cell 2.5 Micron CMOS/Analog/Digital Cell Library	Rad Hard

Special Products

HS-2420RH	Sample and Hold	Rad Hard
HS-3112RH	Dual 4 Gate	Rad Hard
HS-3113RH	Flip Flop	Rad Hard
HS-3114RH	Quad 2 Gate	Rad Hard
HS-3315RH	Multiplexer	Rad Hard
HS-3116RH	Demultiplexer	Rad Hard
HS-3117RH	Register File	Rad Hard
HS-3118RH	Arithmetic Logic Unit (ALU)	Rad Hard
HS-3120RH	Counter	Rad Hard
HS-3121RH	Shift Register	Rad Hard
HS-3128RH	High Drive Multiplexer	Rad Hard
HS-3148RH	PROM	Rad Hard
HS-3504RH	12-Bit Digital to Analog Converter	Rad Hard
HS-3506RH	10V Precision Reference	Rad Hard
HS-3508RH	Line Receiver/Driver	Rad Hard
HS-3509RH	Voltage Regulator	Rad Hard
HS-3510RH	Comparator	Rad Hard
HS-3511RH	Operational Amplifier	Rad Hard
HS-3525RH	8 Channel Multiplexer	Rad Hard
HS-3535RH	Dual Analog Switch	Rad Hard
HS-3536RH	Quad Analog Switch	Rad Hard
HS-3565RH	J-FET Driver	Rad Hard
HS-3580RH	Sense Amplifier	Rad Hard
In Development	Dual MOS Driver	Rad Hard
In Development	Switching Regulator	Rad Hard

Communications Interface Devices

HS-15530RH	CMOS Manchester Encoder/Decoder	Rad Hard
HS-245/246/248/249	Triple Line Transmitter/Receiver	
HS-3182	ARINC 429 Bus Interface Line Driver	
HS-3273	MIL-STD-1553 Bus Interface Circuit	
HS-3282	ARINC 429 Bus Interface Circuit	
HS-3447	CMOS Data Encryption/Decryption Device Cypher I™	

Cypher I™ is a trademark of Harris Corporation

Harris Microwave/Gallium Arsenide Products

GaAs FETs

HMF-0300	125mW Power GaAs FET-Chip
HMF-0301	125mW Power GaAs FET-Packaged
HMF-0302	125mW Power GaAs FET-Flange
HMF-0310	High Gain GaAs FET-Chip
HMF-0314	High Gain Low Noise GaAs FET-Package
HMF-0330	High Gain Low Current GaAs FET
HMF-0600	250mW Power GaAs FET-Chip
HMF-0602	250mW Power GaAs FET-Flange
HMF-0610	High Gain Power GaAs FET-Chip
HMF-0620	High Gain Power GaAs FET-Chip
HMF-1200	500mW Power GaAs FET-Chip
HMF-1202	500mW Power GaAs FET-Flange
HMF-1210	High Gain Power GaAs FET
HMF-2400	1W Power GaAs FET-Chip
HMF-2402	1W Power GaAs FET-Flange

GaAs Digital Integrated Circuits

HMD-11011	Divide by 10/11 Variable Modulus Divider
HMD-11016	Divide by 2/4/8 Binary Counter
HMD-11101	5-Input NOR/OR Gate
HMD-11104	5-Input NAND/AND Gate
HMD-11131	Master/Slave D Flip-Flop
HMD-11301	Divide by Two Prescaler
HMD-12141	Four-Bit Universal Shift Register
HMD-11113	Dual 2-Input Exclusive OR Gate
HMD-11685	Ultra-High Speed Comparator
HMD-11188	Dual Clock Driver/Fanout Buffer
HMD-11502	Programmable Pulse Driver/Formatter

MMICs

HMM-10610	2-6GHz MMIC Amplifier
HMM-10620	Low Current 2-6 GHz MMIC Amplifier
HMM-11810	6-18GHz MMIC Amplifier
HMR-10502	0.5-5.0GHz MMIC Amplifier
HMR-10503	1.0-5.0GHz MMIC Amplifier

IC Evaluation Kits

HMK-11MSI-1	MSI Evaluation Kit
HMK-11SSI-2	SSI Evaluation Kit

GaAs Programs and Services

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Custom Digital Integrated Circuits
Semicustom Digital Integrated Circuits
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High Reliability Screening

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April 1988

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